HP 2100 ALTER-SKIP INSTRUCTION TEST

HP Product No. HP 24208

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HP 2100 ALTER-SKIP INSTRUCTION TEST

This program checks all instruction code combinations of the Alter-Skip Instruction group as defined in the Consolidated Coding Table.

HARDWARE CONFIGURATION

The program runs on an HP 2100 computer with any memory core size and does not use a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program should be run only after the Memry Ref. Instruction Test (HP 24209) as instructions from the Memory Reference group are used to test the Alter-Skip group.

To start the program the user loads the program with the Basic Binary Loader, sets Starting Address 100_8, and presses RUN.

The program begins by executing a string of basic tests that check the ability to clear, set, and test the E-Register. A basic test failure results in a unique MEMORY DATA halt. (See Table ALT-2.) This error should be corrected before proceeding further with testing. No provisions are available for repeating Basic Tests.

Next the program executes the extended tests that test the full set of alter-skip instruction code combination using simple E-register instructions (CLE -- CCE -- CME -- SEZ and SEZ,RSS) and the memory reference instructions.

Each valid instruction combination is checked 18 times. First nine different data patterns are checked in the A- or B-register (depending on the instruction), with the E-register clear. Then the nine different data patterns are checked in the A- or B-register (depending on the instruction) with the E-register set.

After the execution of the instruction, the program checks the contents of the A- or B-, and the E-register and checks if the instruction did or did not skip as expected. A detected failure results in a halt and an information display. MEMORY DATA contains $10200x_8$ where x is an octal digit with bit meanings as follows:

bit 0 = 1,A- or B-register error
bit 1 = 1,E-register error.
bit 2 = 1,Instruction skipped or did not skip as expected.

This information should also be displayed after the halt:

A-register -- Actual A- or B-register result.
B-register -- Expected A- or B-register result.
E-register -- Actual E-register result.

After RUN is pressed another halt occurs and this information should be displayed:

MEMORY DATA - Second display halt (102000_8) identification
A-Register - Octal code of failing alter-skip instruction; bit 11 of the instruction identifies the register:
0 = A-register,
1 = B-register,
B-register - Original data pattern in the A- or B-register.
E-register - Original contents of the E-register.

Following the second display halt, the program continues if switch register bit 0 is clear. If switch register bit 0 is set, the original values are restored in the E- and A- or B-registers, and another halt (102076_8) occurs. The next instruction executed is the failing instruction. The result can be observed by single stepping.

After all instructions have been tested, the program normally loops back and repeats the basic and extended tests until an error is detected. If switch register bit 15 is set, the program halts with 102077_8 displayed in MEMORY DATA. A 32 bit pass count is contained in the A- and B-registers, with the most significant bits in the B-register.

Unexpected Changes In A- or B-Registers

If a change occurs in the B-register after executing an alter-skip instruction involving the A-register or vice versa, the computer halts with 103000_8 displayed in MEMORY DATA if the A-register changed unexpectedly, or with 103001_8 displayed in MEMORY DATA if the B-register changes unexpectedly. The unexpected change is left in the register, and the other register contains the octal code of the alter-skip instruction. When the operator presses RUN the program bypasses the other results normally checked. However, if switch rigister bit 0 is set, the computer halts with 102076_8 displayed in MEMORY DATA and the failing instruction is repeated.

A fixed non-symmetrical data pattern of 043210_8 is placed in the register (A- or B-) not expected to change before each alter-skip instruction is executed. (This procedure does not apply to the basic tests.)

OPERATING INSTRUCTIONS

a. Load the HP 2100 Alter-Skip Instruction Test with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. Press RUN.
   The program executes according to the switch register options selected.

Table ALT-1
Switch Register Options

Switch If Set	Meaning
0	Repeat a failing alter-skip instruction but halt 102076_8 before its execution. (Does not apply to the basic tests.)
15	Halt 102077_8 at the end-of-pass (diagnostic cycle). A pass count is contained in the B- and A-registers (most significant bits in B-register).

Table ALT-2.

Summary Of Program Halts

MEMORY DATA	Comments
10200*X*	Alter-skip instruction error halt.
102000	Display halt following error halt.
102076	Halt before repeating failing Alter-Skip instruction.
102077	End-of-pass halt. The A- and B-registers contain the number of passes completed.
102040	RSS instruction failed.
102041	CLE SEZ sequence failed.
102042	CLE SEZ,RSS sequence failed.
102043	CCE SEZ,RSS sequence failed.
102044	CCE SEZ sequence failed.
102045	CLE CME SEZ,RSS sequence failed.
102046	CCE CME SEZ sequence failed.
103000	Unexpected change in A-register after executing an alter-skip instruction.
103001	Unexpected change in B-register after executing an alter-skip instruction.

Figure ALT-1
Consolidated Coding Table

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEMORY REFERENCE INSTRUCTIONS															
D/I	AND		001	0	Z/C	← Memory Address →									
D/I	XOR		010	0	Z/C										
D/I	IOR		011	0	Z/C										
D/I	JSB		001	1	Z/C										
D/I	JMP		010	1	Z/C										
D/I	ISZ		011	1	Z/C										
D/I	AD*		100	A/B	Z/C										
D/I	CP*		101	A/B	Z/C										
D/I	LD*		110	A/B	Z/C										
D/I	ST*		111	A/B	Z/C										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHIFT-ROTATE GROUP INSTRUCTIONS															
0	SRG		000	A/B	0	D/E	*LS		000	†CLE	D/E	‡SL*	*LS		000
				A/B	0	D/E	*RS		001		D/E		*RS		001
				A/B	0	D/E	R*L		010		D/E		R*L		010
				A/B	0	D/E	R*R		011		D/E		R*R		011
				A/B	0	D/E	*LR		100		D/E		*LR		100
				A/B	0	D/E	ER*		101		D/E		ER*		101
				A/B	0	D/E	EL*		110		D/E		EL*		110
				A/B	0	D/E	*LF		111		D/E		*LF		111
				NOP	000				000		000				000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALTER-SKIP GROUP INSTRUCTIONS															
0	ASG		000	A/B	1	CL*	01	CLE	01	SEZ	SS*	SL*	IN*	SZ*	RSS
				A/B	1	CM*	10	CME	10						
				A/B	1	CC*	11	CCE	11						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAC AND INPUT/OUTPUT INSTRUCTIONS															
1	MAC		000	A/B	0										
1	IOG		000	A/B	1	H/C	HLT		000	← Select Code →					
					1	0	STF		001						
					1	1	CLF		001						
					1	0	SFC		010						
					1	0	SFS		011						
				A/B	1	H/C	MI*		100						
				A/B	1	H/C	LI*		101						
				A/B	1	H/C	OT*		110						
				0	1	H/C	STC		111						
				1	1	H/C	CLC		111						
					1	0	STO		001		000			001	
					1	1	CLO		001		000			001	
					1	H/C	SOC		010		000			001	
					1	H/C	SOS		011		000			001	

Notes: 1) * = A or B. Use with bit 11 as Ø (A-Register) or 1 (B-Register).

2) D/I, A/B, Z/C, D/E, H/C coded: 0/1.

3) †CLE: Only this bit is required.

4) ‡SL*: Only this bit and bit 11 (A/B as applicable) are required.