HP 2100A TIME BASE GENERATOR TEST

HP Product No. HP 24213

11000 Wolfe Road
Cupertino, California 95014

Manual of Diagnostics
Diagnostic Program Procedure
HP 12539-90005

October 1971

HP 2100A TIME BASE GENERATOR TEST

This diagnostic program confirms proper operation of the HP 12539 Time Base Generator (TBG) interface cards.

HARDWARE CONFIGURATION

The diagnostic program requires a 2100A computer with at least 2K of core (or 4K if a teleprinter is included), a HP 12539 Time Base Generator interface card, and optionally a teleprinter.

FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

This program is controlled by program options set into an *internal switch register* at configuration time, or by overriding that internal switch register during a run of the program. During any program run, the computer's S button is lit to indicate that the DISPLAY REGISTER is functioning as a switch register. If the DISPLAY REGISTER bit 0 is on, the *internal switch register* is overridden and the other bits are interpreted for program options, as listed in Table GEN-1.

This diagnostic performs the following tests:

Tests 1 through 4

Check the ability to clear, set, and test the interrupt system:

Test 1 checks the CLF Ø, SFC Ø combination.
Test 2 checks the CLF Ø, SFS Ø combination.
Test 3 checks the STF Ø, SFC Ø combination.
Test 4 checks the STF Ø, SFS Ø combination.

HP Computer Museum
www.hpmuseum.net

For research and education purposes only.

Test 5

Checks the absence of an interrupt when the TBG flag flip-flop is set, the TBG control flip-flop set, and the interrupt system is off. A failure here results in an irrecoverable halt 102005_8.

Test 6 through 11

Check the ability to clear, set, and test the TBG flag:

Test 6 checks the CLF TBG, SFC TBG combination.
Test 7 checks the CLF TBG, SFS TBG combination.
Test 10 checks the STF TBG, SFC TBG combination.
Test 11 checks the STF TBG, SFS TBG combination.

Test 12

The select code screen test sets the flag of every select code (10 through 77) except the TBG select code and checks that the TBG flag is not set in the process.

Test 13

Checks the ability of the TBG to interrupt by setting the flag and control flip-flops and turning on the interrupt system. The interrupt in Test 13 should not occur before a string of instructions affecting priority are executed.

Test 14

Checks that the interrupt occurred where expected.

Test 15

Checks that the contents of the Central Interrupt Register is the TBG select code.

Test 16

Checks that another interrupt does not occur when the interrupt system is turned back on. A failure here results in an irrecoverable halt 102016_8.

Test 17

Checks that the TBG flag is still set following the interrupt.

Test 20

Checks that, with the TBG control and flag flip-flops set and the interrupt system on, there is no interrupt following a CLC TBG instruction. A CLC TBG instruction should reset the TBG control flip-flop.

Test 21

Indirectly checks that a CLC Ø instruction resets the TBG control flip-flop.

Test 25

Checks that EXTERNAL PRESET switch on the 2100A sets the TBG flag (POPIO signal line).

NOTE: Test 25 requires a response from the operator and has an initializing halt. It is bypassed if switch 2 is set.

Test 30

Checks that a STC TBG instruction resets the error flip-flop.

Test 31

This is the 1 ms relative timing test.

Test 32

Checks that the error flip-flop is still reset following the interrupt in Test 31.

Test 33

Checks that the TBG flag flip-flop is still set following the interrupt in Test 31.

Test 34

Checks that, with the TBG control and flag flip-flops left unchanged from Test 31, another interrupt does not occur when the interrupt system is turned back on. The set flag flip-flop should inhibit the resetting of the flag buffer flip-flop. This test waits a minimum of 1.2 ms for the unexpected interrupt.

TEST 35

Checks that the error flip-flop is not set.

NOTE: With the TBG control and flag flip-flops left on from Test 31, at least 1.2 ms have elapsed since the interrupt in Test 31.

Test 36

Checks that a STC TBG instruction now resets a set error flip-flop.

Test 37

Indirectly checks that the OTB TBG instruction resets the TBG control flip-flop. This should prevent an interrupt if the TBG flag, TBG control flip-flop, and the interrupt system were on.

Test 40

This is the 0.1 ms relative timing test and is bypassed if switch 4 is set.

Test 42

This is the 10 ms relative timing test.

Test 43

This is the 100 ms relative timing test.

Test 44

This is the 1 sec relative timing test.

Test 45

This is the 10 sec relative timing test and is run only if switch 8 is set and switch 4 is reset.

Test 46

This is the 100 sec relative timing test and is run only if switch 7 is set and switch 4 is reset.

Test 47

This is the 1000 sec relative timing test and is run only if switch 6 is set and switch 4 is reset.

Relative Timing Tests

The relative timing tests check that an interrupt occurs in the 2100A within 1% of the time obtained by counting while waiting for the interrupt. An interrupt is assumed not to occur if it does take place within an interval 20% greater than the expected interval. If an interrupt does occur, but the actual count is not within 1% of the expected count, the error indications give the actual and expected count. The expected counts, tolerances, and count representations are:

TEST	INTERVAL	EXPECTED COUNT	1% TOLERANCE IN COUNTS	EACH COUNT REPRESENTS
31	1 ms	255	5*	3.92 us
40	0.1 ms	25	1*	3.92 us
42	10 ms	2551	25	3.92 us
43	100 ms	25510	255	3.92 us
44	1 sec	1000	10	1 ms
45	10 sec	10000	100	1 ms
46	100 sec	10000	100	10 ms
47	1000 sec	10000	100	100 ms

**NOTE: The first pulse which the decade dividers sees could come anytime from 0 to 0.01 ms after the control flip-flop sets. This represents an error of 10% on the 0.1 ms interval and 1% on the 1 ms interval. Thus, the test tolerance for Test 31 is 2% or 5 counts and Test 40 is timed between 2 interrupts.*

LIMITATIONS

The program does not check the SRQ signal to the DMA or the priority lines PRH and PRL. PRH and PRL may be tested with the 2100A Interrupt Test, HP 24215.

MESSAGE ANALYSIS

Error and program messages are indicated by printed messages on the teleprinter and/or by coded computer halts. (See Table GEN-2.) All teleprinter message data is in octal except for the end-of-pass count and the actual and expected counts in the error messages for the relative timing tests.

Program messages occur only if switches 1 and 10 are reset and include an introductory message, a message to the operator before test 25, and an end of pass message.

Error messages are printed only if switch 1 and 11 are reset.

OPERATING INSTRUCTIONS

NOTE: The program can be run with the optional jumper on the interface card in the W2 position. This reduces the time required to check the four upper decade dividers. If jumper W2 on the interface card is used, set switch 4 to indicate to the program that the jumper is in that position. At the completion of testing, the W2 jumper must be removed if the card is to function properly.

To Configure the Diagnostic

a. Optionally load the SIO Teleprinter driver with the Basic Binary Loader and configure the driver.

b. Load the 2100A Time Base Generator Test Tape with the Basic Binary Loader.

c. Set Starting Address 2_8 or 111_8.

d. Press RUN. The computer halts and 107000_8 is displayed in MEMORY DATA.

e. Set the switch register to the Time Base Generator Select Code.

f. Press RUN.

1. If the computer halts with 107000_8 displayed in MEMORY DATA, the select code was not in the range 10_8-77_8. Go to step e.

2. If the computer halts with 107001_8 displayed in MEMORY DATA, enter the contents of the internal switch register into the external switch register and press RUN.

3. When the computer halts with 107077_8 displayed, configuration is complete. To start the program, press RUN and go to step c of the procedure, *To Load And Execute The Diagnostic.*

NOTE: The program can be configured from location 111_8 at any time. It can be configured from location 2_8 only after loading and before the diagnostic has been run since running destroys the link in location 2_8.

To Make A Tape Of The Configured Diagnostic

a. If a High Speed Tape Punch is available, load the SIO Tape Punch driver with the Basic Binary Loader and configure the driver.

b. If a High Speed Tape Punch is not available, turn on the teleprinter tape punch.

c. Load the SIO System Dump.

d. Set Starting Address 2_8.

e. Set switch register bit 15.

f. Press RUN.

g. A configured 2100A Time Base Generator Test tape is punched. The computer halts with 102077_8 displayed in MEMORY DATA. To make additional copies of the configured 2100A Time Base Generator Test Tape, press RUN.

To Load And Execute The Diagnostic

a. Load the configured 2100A Time Base Generator Test Tape with the Basic Binary Loader.

b. Set Starting Address 100_8.

c. If program options other than those set into the internal switch register during the procedure *To Configure The Diagnostic* are to be used, perform these steps:

   1. Press S.
   2. Set the program option bits of the DISPLAY REGISTER according to Table GEN-1.

d. Press RUN.

NOTE: To access and loop on a specific test, set switch register bit 15. The computer halts and 102076_8 is displayed in MEMORY DATA at the end of each test, with the test number contained in the A-register. Once the desired test is reached, reset switch register bit 15 and set bit 13. The program now loops on this test until bit 13 is reset. If necessary, set switch register bits 14 and 11 to suppress all error indications until the desired test is reached.

This information does not apply to tests 14, 15, 16, 17, 32, 33, 34, and 35. (See Table GEN-1, Note under Switch 13.)

Table GEN-1

Program Options--Switch Register Settings

SWITCH	MEANING IF SET
15	HALT 102076_8 AT END OF TEST (test number contained in A-register after halt.)
14	SUPPRESS ERROR HALTS
13	REPEAT LAST TEST
	NOTE: Tests 13, 14, 15, 16 and 17 all loop back to Test 13 if switch 13 is set. Tests 31, 32, 33, 34, and 35 all loop back to Test 31 if switch 13 is set.
12	HALT 102077_8 AT END OF PASS (pass count contained in the A- and B-registers after halt.)
11	SUPPRESS ERROR MESSAGES
10	SUPPRESS NON-ERROR MESSAGES
9	
8	INCLUDE 10 SECOND RELATIVE TIMING TEST
7	INCLUDE 100 SECOND RELATIVE TIMING TEST
6	INCLUDE 1000 SECOND RELATIVE TIMING TEST
5	
4	INDICATES OPTIONAL JUMPER IS IN W2 POSITION
3	
2	SKIP TEST 25 (requires operator response)
1	INDICATES THAT NO TELETYPE IS AVAILABLE
0	OVERRIDE THE INTERNAL SWITCH REGISTER

Table GEN 2

Diagnostic Messages

NOTE: If a program halt occurs (see Table GEN-1 bit 14), and data is associated, the data is contained in the A- and/or B-registers. If a message is printed (see Table GEN-1 bits 10 and 11), any data associated is included in the message.

MEMORY DATA	Message	Comment
	21ØØA TBG DIAGNOSTIC	Header message.
102000	PRESS EXT. PRESET, PRESS RUN	Initializing halt for Test 25. To skip Test 25 for subsequent passes, set switch register bit 2. (See Table GEN-1.)
102001	E-1 CLF Ø - SFC Ø	Cannot clear, set, or test interrupt system.
102002	E-2 CLF Ø - SFS Ø	(Same as 102001)
102003	E-3 STF Ø - SFC Ø	(Same as 102001)
102004	E-4 STF Ø - SFS Ø	(Same as 102001)
102005	E-5 INTP.! IEN?	Irrecoverable halt - program interrupted with TBG flag and control flip-flops set but with interrupt system off. Check IEN signal line.
102006	E-6 CLF *x* - SFC *x*	Cannot clear, set, or test TBG flag. *x* = TBG select code.
102007	E-7 CLF *x* - SFS *x*	(Same as 102006)
102010	E-1Ø STF *x* - SFC *x*	(Same as 102006)
102011	E-11 STF *x* - SFS *x*	(Same as 102006)
102012	E-12 FLG *x* set by STF *y*	Select code screening test: *x* = TBG select code. *y* (in A-register at halt) = select code causing the TBG flag to set.

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102030	E-3Ø STATUS NOT Ø, IS *x*	STC TBG instruction did not reset error flip-flop or input lines other than bit 4 not 0. *x* (in A-Register at halt) = actual status (input line contents); Ø (in B-Register at halt) = expected status.
102031	E-31 {W1 / W2} 1 MS TEST {NO INTP / *x/y*}	1 ms relative timing test error (Test 31). *x* (in A-Register at halt) = actual count; *y* (in B-Register at halt) = expected count. (One or the other of the items in brackets { }, but not both, are printed.) At the halt, if the E-Register = 0, there was no interrupt; if the E-Register = 1, there was an interrupt.
102032	E-32 STATUS AFTER 1ST INTP. NOT Ø IS *x*	Error flip-flop should not be set immediately after the interrupt in Test 31. *x* (in A-Register at halt) = actual status (input line contents); Ø (in B-Register at halt) = expected status.
102033	E-33 FLAG NOT SET	TBG flag not set following interrupt in Test 31.
102034	E-34 2ND 1 MS INTP.	Another interrupt occurred following the interrupt in Test 31. Possibly, the TBG flag buffer flip-flop was not inhibited.

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102035	E-35 STATUS NOT 2Ø, IS *x*	Error flip-flop (bit 4) not set and/or other input lines not 0. *x* (in A-Register at halt) = actual status (input line contents); $2Ø_8$ (in B-Register at halt) = expected status.
102036	E-36 STATUS NOT Ø, IS *x*	A set error flip-flop not reset by a STC TBG instruction and/or other input lines not 0. *x* (in A-Register at halt) = actual status (input line contents); expected status in B-Register at halt.
102037	E-37 INTP. FOLLOWING OTB *x*	OTB TBG instruction did not reset TBG control flip-flop. *x* = TBG select code.
102040	E-4Ø W1 Ø.1 MS TEST {NO INTP. / *x/y*}	Halts 102040 through 102047 and messages E-4Ø through E-47 are
102042	E-42 {W1 / W2} 1Ø MS TEST {NO INTP. / *x/y*}	Relative Timing Test errors: *x* (in A-Register at halt) =
102043	E-43 {W1 / W2} 1ØØ MS TEST {NO INTP. / *x/y*}	actual count; *y* (in B-Register
102044	E-44 {W1 / W2} 1 SEC TEST {NO INTP. / *x/y*}	at halt) = expected count. At the halt, if E-Register = 0,
102045	E-45 W1 1Ø SEC TEST {NO INTP. / *x/y*}	there was no interrupt; if E-
102046	E-46 W1 1ØØ SEC TEST {NO INTP. / *x/y*}	Register = 1, there was an interrupt. (One or the other
102047	E-47 W1 1ØØØ SEC TEST {NO INTP. / *x/y*}	of the items in brackets { }, but not both, are printed.)

Table GEN-2 (cont.)

MEMORY DATA	Message	Comment
102076		End of test halt. A-Register contains the test number.
102077		End of pass halt. The pass count is contained in the A- and B-Register with the B-Register containing the most significant bits.
1060*xx*		Unexpected trap cell halt. *xx* = select code.
107000		Start of configuration halt. Enter select code of TBG *NOTE: Also occurs if entered select code is not in range 10_8-77_8.*
107001		Configuration halt. Enter contents of internal switch register.
107077		End of configuration halt. To start the program press RUN.