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CUSTOMER SUPPORT HANDBOOK

HP 2000 HARDWARE SUPPORT DATA

DATA SYSTEMS DIVISION
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CONTENTS

The information contained in this handbook has been compiled in quick-reference form to aid Customer Engineers in maintaining Hewlett-Packard equipment. The contents herein is in no way intended to reflect Hewlett-Packard policies, procedures, or specifications.

COMMON DATA

CONTENTS PAGE

WORD FORMATS

Memory Reference Instructions

15	14 13 12	11	10	9 8 7 6 5 4 3 2 1 0
D/I	OP CODE	A/B	Z/C	Address Within Page

Shift Rotate Group

15	14 13 12	11	10	9 8 7 6 5 4 3 2 1 0
0	0	A/B	0	MICRO OP

ALTER Skip Group

15	14 13 12	11	10	9 8 7 6 5 4 3 2 1 0
0	0	A/B	1	MICRO OP

Input/Output Group

15	14 13 12	11	10	9 8 7 6 5 4 3	2 1 0
1	0	A/B	1	MICRO OP	Select Code

MACRO (EAU)

15	14 13 12	11	10	9 8 7 6 5 4 3 2 1 0
1	0		0	MACRO OP

Full Address

15	14 13 12 11 10	9 8 7 6 5 4 3 2 1 0
D/I	Page Address	Address Within Page

Data (Single precision fixed point)

15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
s	integer

Data (Double precision fixed point)

15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	inte	ger
	B REG	A REG

***Data (Floating point)**

15	14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1	0
s	mantissa		exponent	s
	A REG	B REG		

*Floating point data word format does not apply to 2114, 2115, and 2116.

DATA REPRESENTATION

Positive and Negative Integers

Single Precision Fixed Point
1 sign bit, 15 data bits
range $-32{,}768 \leqslant x \leqslant 32{,}767$

Double Precision Fixed Point
1 sign bit, 31 data bits
range $-2{,}147{,}483{,}648 \leqslant x \leqslant 2{,}147{,}483{,}647$

***Floating Point (2 words)**

23 digits for mantissa, 7 for exponent
1 sign bit for mantissa, 1 for exponent
range $\pm 1.701411 \times 10^{-38} \leqslant X \leqslant 1.701411 \times 10^{+38}$
accuracy 6 to 7 digits depending on value

ROUND OFF ERROR

Number	Exponent	Maximum Error
8,388,607.0	+23	1.0
1,048,474.87	+20	.125
32,767.996	+15	.0039
1,023.99988	+10	.000122
31.9999952	+ 5	.0000038
.999998881	0	.00000012

SYMBOLOGY

Y	any register
(Y)	contents of Y
S.A.	starting address
Reg	register
SC	select code
(A/B)	either A-reg or B-reg

FLOATING POINT OPERATORS

(X)	+ (Y)	addition
(X)	- (Y)	subtraction
(X)	$\wedge$ (Y)	logical AND
(X)	$\vee$ (Y)	logical IOR
(X)	$\oplus$ (Y)	logical EOR
(X)	$\leftarrow$ (Y)	replaced by
(X)	= (Y)	equals

*Floating point data representation does not apply to 2114, 2115, and 2116.

CODING TABLE

MEMORY REFERENCE INSTRUCTIONS

15	14 13 12	11	10	9	8 7 6	5 4 3	2 1 0
D/I	AND 001	0	Z/C	← Memory Address →			
D/I	XOR 010	0	Z/C				
D/I	IOR 011	0	Z/C				
D/I	JSB 001	1	Z/C				
D/I	JMP 010	1	Z/C				
D/I	ISZ 011	1	Z/C				
D/I	AD* 100	A/B	Z/C	Local page address (Bits 0-9) OR'd with M-reg (Bits 10-14) for complete address			
D/I	CP* 101	A/B	Z/C				
D/I	LD* 110	A/B	Z/C				
D/I	ST* 111	A/B	Z/C				

SHIFT ROTATE INSTRUCTIONS

15	14 13 12	11	10	9	8 7 6	5 4 3	2 1 0
0	000	A/B	0	D/E	*LS 000	CLE D/E SL*	*LS 000
0	000	A/B	0		*RS 001		*RS 001
0	000	A/B	0	Enables bits (6-8)	R*L 010	Enables bits (0-2)	R*L 010
0	000	A/B	0		R*R 011		R*R 011
0	000	A/B	0		*LR 100		*LR 100
0	000	A/B	0		ER* 101		ER* 101
0	000	A/B	0		EL* 110		EL* 110
0	000	A/B	0		*LF 111		*LF 111
0	NOP 000	000			000	000	000

ALTER-SKIP INSTRUCTIONS

15	14 13 12	11	10	9	8 7 6	5 4 3	2 1 0
0	000	A/B	1	0 CL* 1	CLE 01	SEZ SS* SL*	IN* SZ* RSS
0	000	A/B	1	1 CM* 0	CME 10		
0	000	A/B	1	1 CC* 1	CCE 11		

INPUT/OUTPUT INSTRUCTIONS

15	14 13 12	11	10	9	8 7 6	5 4 3	2 1 0
1	000	A/B	1	H/C	HLT 000	← Select Code →	
1	000		1	0	STF 001		
1	000		1	1	CLF 001		
1	000		1	0	SFC 010		
1	000		1	0	SFS 011		
1	000	A/B	1	H/C	MI* 100		
1	000	A/B	1	H/C	LI* 101		
1	000	A/B	1	H/C	OT* 110		
1	000	0	1	H/C	STC 111		
1	000	1	1	H/C	CLC 111		
1	000		1	0	STO 001	000	001
1	000		1	1	CLO 001	000	001
1	000		1	H/C	SOC 010	000	001
1	000		1	H/C	SOS 011	000	001

Notes: * = A-register or B-Register (A/B)
Code: D/I Direct or Indirect Address
Z/C Zero or Current Page
D/E Disable or Enable the following 3 bit group
H/C Hold or Clear the Flag

MACRO INSTRUCTIONS (EAU)

MACRO INSTRUCTIONS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	MPY	000		000			010			000			000		
1	DIV	000		000			100			000			000		
1	DLD	000		100			010			000			000		
1	DST	000		100			100			000			000		
1	ASR	000		001			000			01	bits 0-3				
1	ASL	000		000			000			01	No. of Shifts/				
1	LSR	000		001			000			10	Rotates				
1	LSL	000		000			000			10	1B=1, 2B=2, etc.				
1	RRR	000		001			001			00	17B=15				
1	RRL	000		000			001			00	0B=16				

Bits 10, 12-14=0
Bit 15=1
These instructions take control of the CPU and retain control until the operation is completed (variable # cycles).

Mnemonic	Name	Function
MPY Y P+1 addr of Multiplier	Multiply	(A)=Multiplicand Result: [B][A] ,double prec. integer. (P), (M)← (P)+2
DIV Y P+1 addr of Divisor	Divide	[B][A] = Dividend Result: A=Quotient, B=Remainder Overflow: set for ÷ 0, or numerical overflow where quotient would exceed 15 bits. (P),(M)← (P)+2
DLD Y P+1 addr 1st word	Double Load	(A)← (1st word), (B)← (2nd word) (P),(M)← (P)+2
DST Y P+1 addr 1st word	Double Store	(1st word)← (A), (2nd word)← (B) (P),(M)← (P)+2

DLD,DST require 5 cycles, MPY 12 cycles, DIV 13 cycles.
Y is a label. The 15 bit address is placed in location P+1.

ASR X	Arithmetic Shift Right	[B][A] (B15) unchanged, (B14)← (B15),... (A0)← (A1), (A0) lost
	Right	
ASL X	Arith Shift Left	[B][A] (A0)← 0, (A1)← (A0), (B14) lost, if (15)≠(14) and shift → set Overflow
LSR X	Logical Shift Right	[B][A] ignore sign. (B15)← 0 (B14)← (B15),...(A0)← (A1), (A0) lost
LSL X	Logical Shift Left	[B][A] ignore sign. (A0)← 0, (A1)← (A0),..., (B15) lost
RRR X	Rotate Right	[B][A] wrap around. (A0)← (A1)... (B14)← (B15), (B15)← (A0)
RRL X	Rotate Left	[B][A] wrap around. (B15)← (B14) (A0)← (B15)

ASR, ASL, LSR, LSL, RRR, and RRL require 2 to 5 cycles depending on number of shifts/rotates. Bits 0-3 specify # of shifts (X). Octal 0 provides 16 shifts/rotates. The value of X ranges from 0B to 17B.

MACHINE LANGUAGE

MEMORY REFERENCE GROUP

Bit 15: 0=Direct, 1=indirect addressing.
Bit 11: 0=A reg, 1=B Reg, except as noted
Bit 10: 0 ➔clear M Reg (10-14), 1 ➔hold M Reg (10-14)
All Memory Reference Instructions (except JMP)require both Fetch and Execute phases. All may use one or more Indirect phases. Y represents the operand address and must be on the current or zero page.

Mnemonic	Name	Function
AD(A/B) Y	Add to A or B	(A/B)◄- (A/B)+(Y) includes Carry
	if overflow,	(V)◄- 1 (indicates numerical error)
	if carry,	(E)◄- 1
CP(A/B) Y	Compare with A or B	if (A/B)=(Y), (P)◄- (P)+1
		if (A/B)≠(Y), (P)◄- (P)+2
LD(A/B) Y	Load A or B	(A/B)◄- (Y)
ST(A/B) Y	Store A or B	(Y)◄- (A/B)
next three Bit 11=1		
JSB Y	Jump Subroutine	(Y)◄- (P)+1
		(P),(M)◄- (Y)+1
JMP Y	Jump	(P),(M)◄- (Y)
ISZ Y	Increment, Skip if Zero	(Y)◄- (Y)+1; (P),(M)◄- (P)+1
		if (Y) becomes 0, (P),(M)◄- (P)+2
next three Bit 11=0		
AND Y	And	(A)◄- (A) Λ (Y)
XOR Y	Exclusive Or	(A)◄- (A)⊕(Y)
IOR Y	Inclusive Or	(A)◄- (A) V (Y)

SHIFT ROTATE GROUP

Bits 10, 12-15=0
Bit 11 indicates A or B Reg
Requires Fetch Phase only

Mnemonic	Name	Function
(A/B)LS	Left Shift	(15) unchanged, (14) lost,...,(0)◄- 0
		set V if (15)≠(14) prior to shift
(A/B)RS	Right Shift	(15)unchanged,(14)◄- (15),...,(0) lost
R(A/B)L	Rotate Left	wrap around. (15)◄- (14),...,(1)◄-(0)
		(0)◄- (15)
R(A/B)R	Rotate Right	wrap around. (0)◄- (1),...,(15)◄- (0)
(A/B)LR	Left Shift	(15)◄- 0, (14)◄- (13),...,(0)◄- 0
ER(A/B)	Rotate E Right	(0)◄- (1),...,(15)◄- (E), (E)◄- (0)
EL(A/B)	Rotate E Left	(15)◄- (14),...,(0)◄- (E), (E)◄- (15)
(A/B)LF	Rorate Left 4	(15)◄- (11), (14)◄- (10),...,(0)◄- (12)

For instructions above Bit 9 enables (6-8) and Bit 4 enables (0-3). This allows one or two instructions per cycle.

SL(A/B)	Skip if LSB is Zero	if (0)=0, (P),(M)◄- (P)+2
		if (0)=1, (P),(M)◄- (P)+1
CLE	Clear E reg	(E)◄- 0
NOP	No Operation	(P),(M)◄- (P)+1

MACHINE LANGUAGE (CONT)

SHIFT ROTATE GROUP (CONT)

Combine Instructions with Inclusive Or bit by bit

15	14 13 12	11 10 9			8 7 6	5 4 3			2 1 0
0	0	A/B	0	D/E		CLE	D/E	SL*	

Bit 9 enables bits 8,7,6
Bit 4 enables bits 2,1,0

*LS 0	*LS 0
*RS 1	R*S 1
R*L 2	R*L 2
R*R 3	R*R 3
*LR 4	*LR 4
ER* 5	ER* 5
EL* 6	EL* 6
*LF 7	*LF 7

SHIFT-ROTATE GROUP (SRG) SUMMARY				
A Reg Operations	**1**	**2**	**3**	**4**
	ALS (1000)	CLE (40)	SLA (10)	ALS (20)
	ARS (1100)			ARS (21)
	RAL (1200)			RAL (22)
	RAR (1300)			RAR (23)
	ALR (1400)			ALR (24)
	ERA (1500)			ERA (25)
	ELA (1600)			ELA (26)
	ALF (1700)			ALF (27)
B Reg Operations	**1**	**2**	**3**	**4**
	BLS (5000)	CLE (4040)	SLB (4010)	BLS (4020)
	BRS (5100)			BRS (4021)
	RBL (5200)			RBL (4022)
	RBR (5300)			RBR (4023)
	BLR (5400)			BLR (4024)
	ERB (5500)			ERB (4025)
	ELB (5600)			ELB (4026)
	BLF (5700)			BLF (4027)

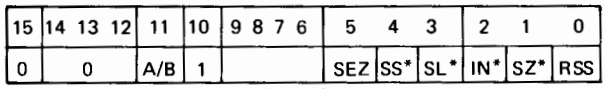
MACHINE LANGUAGE (CONT)

ALTER SKIP GROUP

Bits 12-15=0, bit 10=1
Bit 11 indicates A or B
Requires Fetch Phase only

Mnemonic	Name	Function
CL(A/B)	Clear Reg	(A/B)← 0
CM(A/B)	Complement Reg	(0) ← $\overline{(0)}$, (1)← $\overline{(1)}$,. . .,
CC(A/B)	Clear, Comp Reg	(A/B)← 177777
CLE	Clear E	(E)← 0
CME	Complement E	(E)← $\overline{(E)}$
CCE	Clear, Comp E	(E)← 1
SEZ	Skip if E Zero	if (E)=0, (P),(M)← (P)+2 if (E)=1, (P),(M)← (P)+1
SS(A/B)	Skip if Sign Bit is Zero	if (15)=0, (P),(M)← (P)+2 if (15)=1, (P),(M)← (P)+1
SL(A/B)	Skip if LSB is Zero	if (0)=0, (P),(M)← (P)+2 if (0)=1, (P),(M)← (P)+1
IN(A/B)	Increment Reg	(A/B)← (A/B)+1 if overflow, (V)← 1, if carry (E)← 1
SZ(A/B)	Skip if Entire Reg is Zero	if (A/B)=0, (P),(M)← (P)+2 if (A/B)≠ 0,(P),(M)← (P)+1
RSS *	Reverse Skip Sense	when used alone (P),(M)← (P)+2 when used with skip, skip condition is non-zero

Combine Instructions with Inclusive Or bit by bit



15	14 13 12	11	10	9 8 7 6	5	4	3	2	1	0
0	0	A/B	1		SEZ	SS*	SL*	IN*	SZ*	RSS

CL* 0 1 0 1 CLE
CM* 1 0 1 0 CME
CC* 1 1 1 1 CCE

*For the combination "SS(A/B), SL(A/B), RSS" both conditions required for skip.

ALTER-SKIP GROUP SUMMARY

A Reg Operations	**1**	**2**	**3**	**4**
	CLA (2400)	SEZ (2040)	CLE (2100)	SSA (2020)
	CMA (3000)		CME (2200)	
	CCA (3400)		CCE (2300)	
	5	**6**	**7**	**8**
	SLA (2010)	INA (2004)	SZA (2002)	RSS (2001)
B Reg Operations	**1**	**2**	**3**	**4**
	CLB (6400)	SEZ (6040)	CLE (6100)	SSB (6020)
	CMB (7000)		CME (6200)	
	CCB (7400)		CCE (6300)	
	5	**6**	**7**	**8**
	SLB (6010)	INB (6004)	SZB (6002)	RSS (6001)

MACHINE LANGUAGE (CONT)

INPUT/OUTPUT GROUP

Bits 10,15=1, 12-14=0
Bit 11 indicates A or B Reg (may be "don't care")
Bit 9 allows hold flag, or clear flag condition

Mnemonic	Name	Function
HLT	Halt	(P),(M)← (P)+1, clear Run FF's
STF	Set Flag	(Flag)← 1
CLF	Clear Flag	(Flag)← 0
SFC	Skip if Flag Clear	if (Flag)=0, (P),(M)← (P)+2 if (Flag)=1, (P),(M)← (P)+1
SFS	Skip Flag Set	if (Flag)=0, (P),(M)← (P)+1 if (Flag)=1, (P),(M)← (P)+2
MI(A/B)	Merge into Reg	(0)← (0) V IOBI0, (1)← (1) V IOBI1,...
LI(A/B)	Load into Reg	(0)← IOBI0, (1)← IOBI1, etc
OT(A/B)	Output Reg	(buf 0)← IOBO0, (buf 1)← IOBO1,...
STC	Set Control	(Control FF)← 1
CLC	Clear Control	(Control FF)← 0

STF1, CLF1, SFS1, and SFC1 all refer to Overflow Reg.
LI(A/B)1, and MI(A/B)1 both refer to the Switch Reg.
OT(A/B)1 (in 2114 only) sets Switch Reg and illuminates lamps.

INPUT/OUTPUT GROUP (IOG) SUMMARY

Octal codes for all 28 IOG variations are listed. Overflow instructions H/C the overflow bit after skip test; all others H/C the flag bit as the final function. (XX is select code.)

MIA H SC	1024XX	STF SC	1021XX
MIA C SC	1034XX	CLF SC	1031XX
MIB H SC	1064XX	SFC SC	1022XX
MIB C SC	1074XX	SFS SC	1023XX
LIA H SC	1025XX	STC H SC	1027XX
LIA C SC	1035XX	STC C SC	1037XX
LIB H SC	1065XX	CLC H SC	1067XX
LIB C SC	1075XX	CLC C SC	1077XX
OTA H SC	1026XX	STO	102101
OTA C SC	1036XX	CLO	103101
OTB H SC	1066XX	SOC H	102201
OTB C SC	1076XX	SOC C	103201
HLT H SC	1020XX	SOS H	102301
HLT C SC	1030XX	SOS C	103301

INPUT/OUTPUT

Select Code. Each I/O device is associated with the Select Code of the slot into which the Interface is inserted. The various signals (IRQ, FLG, SRQ, PRH and PRL) explicitly contain the Select Code information by virtue of the back plane wiring. The signals (STC, CLC, STF, CLF, OTA, etc.) are sent to all I/O slots, but the Select Code information allows servicing with the proper device.

Data. Data is sent to the I/O peripheral with an OT(A/B) instruction. Data is input to the computer from the I/O device with a LI(A/B) or MI(A/B) instruction. Typically a data storage register is provided on the interface for data output. The I/O device usually provides its own data storage for input to the computer. The MI(A/B) is used primarily with byte oriented devices to allow packing.

Device Initiation. The STC SC,C initiates the device cycle. The Set Control provides the device command signal (read, punch, etc.) and also sets the Control FF which is required for interrupt operation. The CLF assures proper Flag and IRQ condition. When the device has completed its cycle it generates a Device Flag signal. This clears the command and initiates the Flag and IRQ circuitry.

PRIORITY STRING JUMPERS

2116B/C Jumpers on I/O control board: DMI - W1; DMA - W2; Mem Prot or Parity Error - W3.

2115A Jumper W1 on Front Panel Coupler for DMA.

INTERRUPT SERVICING

The Interrupt operation is called by different names in the various 2100 Series computers

PH4 in 2116/15/14
PH1B in 2100
Interrupt in 21MX

but all perform a common function.

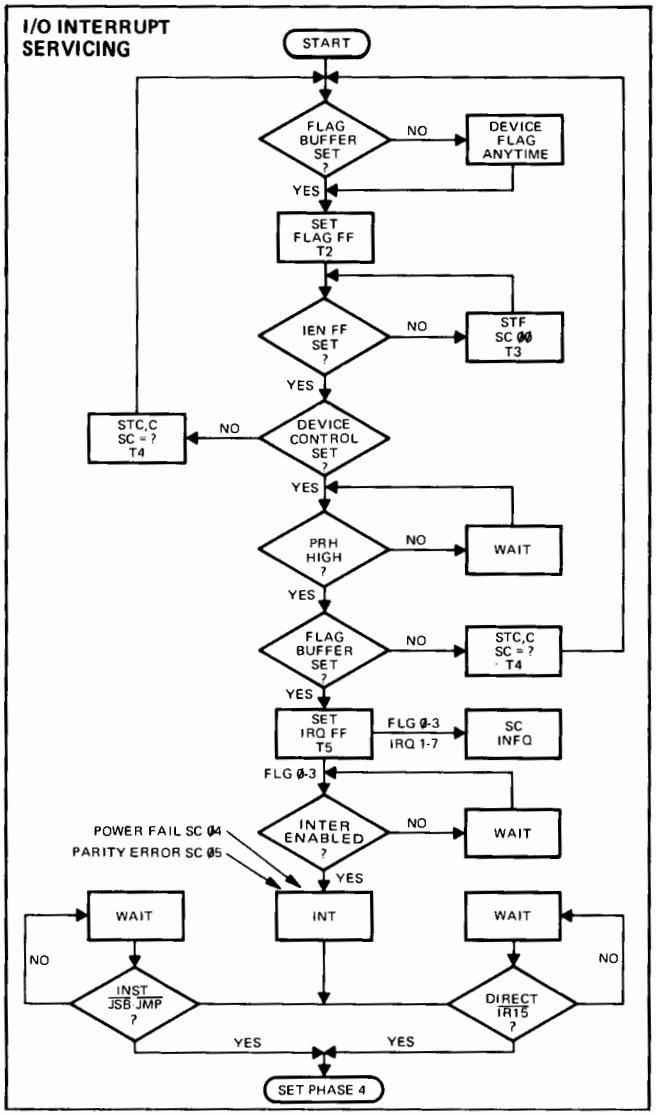
INPUT/OUTPUT (CONT)

IEN. Interrupt Enable indicates the condition of the computer interrupt system (Flag Ø), plus some housekeeping details. PRH Priority High to the device indicates that no higher interrupts are being serviced. PRL Priority Low is a hold off to lower priority devices. IRQ and FLG are the Interrupt Request signals that request the Phase 4. IAK Interrupt Acknowledge indicates a Phase 4 has taken place.

The device completion provides a Flag, setting the Flag Buf. At T2 Flag FF sets. At T5 (if Interrupt is enabled, no higher Priority device is being serviced, and Control is set) the IRQ is set. It toggles at T5 and T2 until serviced. Upon Phase 4 service the IAK clears the Flag Buf. Flag FF is cleared at end of the servicing subroutine.

SIO. In this environment the device is initiated and the program waits with SFS SC, Jmp*-1 until the completion Flag. A SKF signal then skips over the Jmp*-1 and the program continues.

DMA. The SRQ is trapped and compared by DMA to allow DMA processing. The DMA provides the STC,SC and data input or output to achieve the transfer. The STF allows the initial DMA servicing for some devices.


I/O INTERRUPT SERVICING
START
FLAG BUFFER SET ?
NO
DEVICE FLAG ANYTIME
YES
SET FLAG FF T2
IEN FF SET ?
NO
STF SC Ø4 T3
YES
STC,C SC = ? T4
NO
DEVICE CONTROL SET ?
YES
PRH HIGH ?
NO
WAIT
YES
FLAG BUFFER SET ?
NO
STC,C SC = ? T4
YES
SET IRQ FF T5
FLG Ø-3
IRQ 1-7
SC INFO
FLG Ø-3
INTER ENABLED ?
NO
WAIT
POWER FAIL SC Ø4
PARITY ERROR SC Ø5
YES
WAIT
INT
WAIT
NO
NO
INST JSB JMP ?
DIRECT IR15 ?
YES
YES
SET PHASE 4

INPUT/OUTPUT (CONT)

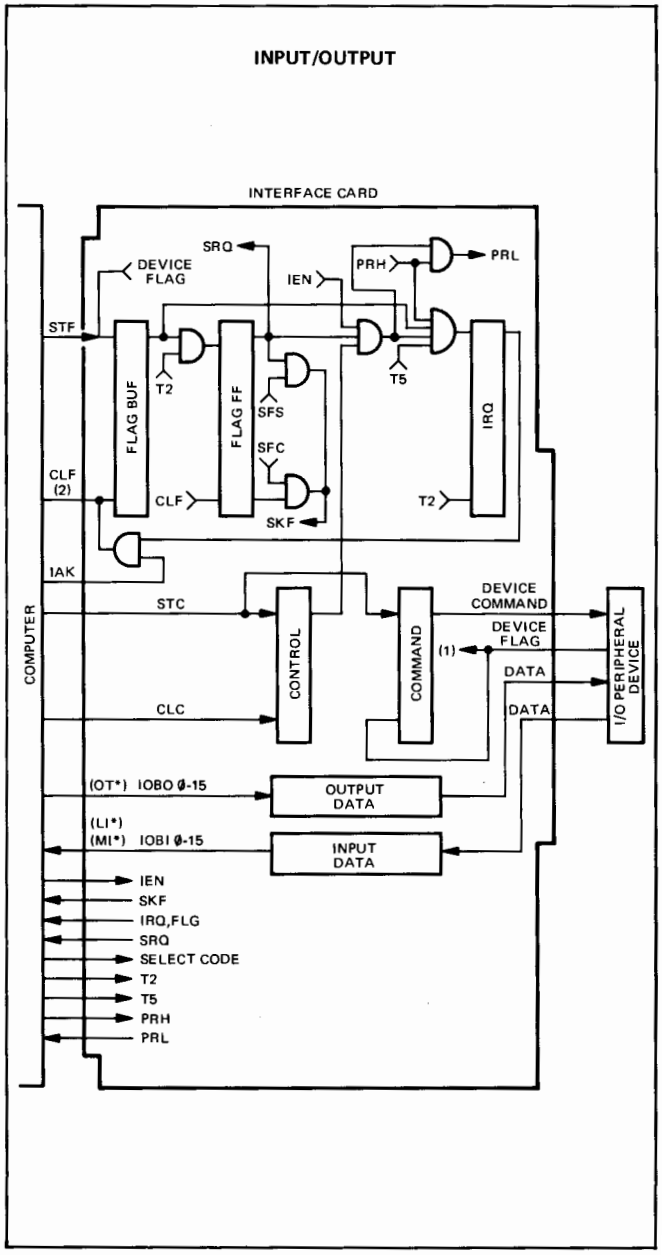
I/O-Instruction Table

	SC0	SC1	SC2/3	SC4	SC5	SC6/7	SC10-70
STC	NOP	NOP	Prepare DMA channel 1/2 to receive & store the block length in 2's complement form.	Reenable power fail logic	Turn on mem. protect	Sets contr. FF on DMA channel 1/2 (activates DMA)	Sets control FF & turn on device on channel specified by S.C.
CLC	Reset all control and command FF's on all I/O channels.	NOP	Prepare DMA channel 1/2 to receive & store the direction of data flow & core mem. starting address.	Reenable power fail logic	NOP	Clear contr. FF on DMA channel 1/2 (reestablishes priority with STF, does not turn off DMA.)	Clears control FF & turns off device (aborts data transfer if programmed.)
STF	Interrupt on	STO Set Overflow	NOP	Flag FF will be set when power comes up. (No program control possible)	Turn on parity error interrupt.	Hardware controlled: Sets when word count is reached (turns off DMA). Program controlled: Aborts data transfer.	Sets when data transfer finished.
CLF	Interrupt off (except for power fail, SC4 and Parity Error SC5)	CLO Clear Overflow	NOP	Flag FF will be clear when power fail occurs. (No program control)	Turn off parity error interrupt	Clears flag FF on DMA channel 1/2	Clear flag FF on interface card.

INPUT/OUTPUT (CONT)

	SC0	SC1	SC2/3	SC4	SC5	SC6/7	SC10-77
SFS	Skip if interrupt is on	SOS	NOP	NOP	Skip if parity error interrupt is on.	Tests if DMA transfer is completed	Test if data transfer is completed
SFC	Skip if interrupt is off	SOC	NOP	Skip if power fail occurred	Skip if parity error interrupt is off	Test if DMA transfer is still in progress.	Test if data transfer still in progress.
LIA/B	NOP	Read S-reg into A/B reg.	Read present contents of DMA word count reg. channel 1/2 into A/B-reg.	Load central interrupt register into least signif. bits of A/B reg. (SC of last interrupting peripheral.)	Violation Reg to A/B bit 15=1, PE bit 15=0, MPV	2100 CLA/B 21MX CCA/B	Transfer data from I/O interface buffer to A/B reg.
MIA/B	NOP	Merge S-reg into A/B reg.	Merge present contents of DMA word count reg channel 1/2 into A/B reg.	Merge central interrupt register into least signif. bits of A/B reg.	Merge contents of violation reg. into A/B reg.	NOP	Merge data from I/O interface buffer to A/B reg.
OTA/B	NOP	Transfer data from A/B reg. to display reg.(2114 & 2100 only)	Output to DMA channel 1/2 the block length in 2's complement form(previously prepared by STC 2/3 or the direction of data flow & core mem. starting address (previously prepared by CLC 2/3	NOP	Sets fence reg. for mem. protect (first addressable mem. loc.)	Output to DMA 1,2 S.C. of device. Specify STC after each word CLC after block; byte mode if 2116.	Transfer data from A/B reg. to specified interface card

I/O BLOCK DIAGRAM



MEMORY PROTECT RULES

OT*	05	Output A/B to the fence register
LI*	05	Load violation register into A/B
STC	05	Turn on memory protect

Turn off memory protect? – Press Internal Preset in Halt mode or a HLT or any Non-I/O instruction executed in a trap cell (PH3B).

Memory Protect Violations

1. ISZ, JSB, ST*, or DST attempts to execute at a location in the range $2 \leqslant$ violation $\leqslant F\text{-}1$

2. JMP attempts execution below the fence.
   $0 \leqslant$ violation $\leqslant F\text{-}1$

3. Any I/O instruction except
   (a) those with S.C.=1 (not including HLT 01)
   (b) those in trap cells fetched by PH1B

The violating instruction is inhibited, an interrupt to location 5 is generated, the address of the violating instruction is in the violation register (Bit 15=0).

Any instruction may go indirect through the protected area.

HLT in the trap cell is executed and turns off memory protect.

DMA cannot cause a violation.

After the third level of indirect for JMP or JSB an interrupt is allowed if one is waiting. (This is not considered a violation and no interrupt to 5 is generated).

Memory protect inhibits the violating instruction whether the interrupt system is on or not. Always do a STF 00 and set up the fence before doing a STC 5.

GENERAL APPROACH TO TROUBLESHOOTING

Although the computer is a complex device, it can usually be repaired with little difficulty if the right approach is taken. The computer can be divided into four basic sections: CPU (Central Processor Unit), I/O (Input/Output), Memory, and Power Supply. Generally, it is best to be certain that the power supply is functioning properly before going on to any other troubles. The CPU section which is next on the list, provides timing and controls for the other sections. It is good practice to remove CPU options such as DMA, EAU, and memory protect when approaching a problem, since they can affect normal CPU operation. Memory problems are typically dropping or picking bits or loss of access to certain areas of core. When trying to locate the cause of a dropped or picked bit failure, remember that the sense lines from all sections of core are "OR" tied. The same is true for the inhibit lines. The section remaining is I/O; failures in this area are usually limited to a malfunction with a particular I/O device. The problem is to determine where the actual trouble is. It could be the interface, the device itself, or control signals from the CPU. Many I/O devices can be "checked out" off line. In many cases, it is required to actually look at signals with an oscilloscope to determine the exact source of the problem.

SIMPLE PROGRAM TO CHECK COMPUTER

If the computer runs, halt it manually. Get the contents of the "M" Register (on 2100A, Press "M"). If 77 < M < 122 then O.K. - Press RUN and let it run (especially if looking for intermittent).

```
PAGE 0002 #01

0001                ASMB,A,B,L
0002*
0003*  THIS PROGRAM MAY BE USED TO CHECK CERTAIN
0004*  INSTRUCTIONS USED BY THE BBL.  IT ASSUMES
0005*  THAT THE LOADER IS INTACT (I.E. CHECKED
0006*  AGAINST LISTING OR BOOTED). THIS PROGRAM
0007*  DOES NOT CHECK THOSE INSTRUCTIONS USED
0008*  BY THE BOOT WHICH ARE:
0009*   STC,C  SFS  JMP  LIA  MIA  STA B,I
0010*
0011*  THIS PROGRAM CHECKS THE FOLLOWING:
0012*   A REGISTER - SET AND CLEAR ALL BITS
0013*   B REGISTER - SET AND CLEAR ALL BITS
0014*   E REGISTER - SET BY CARRY AND CLEAR BY
0015*                  INSTRUCTION
0016*   ARITHMETIC - ALL ADDERS & CARRIER &
0017*                  COMPARE
0018*   MEM REFERENCE - A CRUDE TEST OF LOAD,
0019*                   STORE & JSB.
0020*
0021*  IT IS EQUALLY USEFUL IN THE FIELD OR
0022*   CAN BE TOGGLED BY A CUSTOMER OVER
0023*   THE TELEPHONE.
0024*
0025  00100               ORG 100B
0026  00100 003500  START CCA,CLE       DONT'T START HERE AGAIN
0027  00101 007400        CCB
0028  00102 054000        CPB 0         A=B=177777?
0029  00103 002040        SEZ           E=0 AFTER CLE?
0030  00104 102001        HLT 1B
0031  00105 002004        INA           BUMP "A"
0032  00106 002040        SEZ           DID "E" SET?
0033  00107 002002        SZA           DID "A" ROLL OVER
0034  00110 102003        HLT 2B
0035  00111 006004        INB           BUMP "B"
0036  00112 006002        SZB           DID "B" ROLL OVER
0037  00113 102003        HLT 3B
0038  00114 060122        LDA B377      GET 8 LOW BITS
0039  00115 070001        STA 1B        ALSO IN "B"
0040  00116 001727        ALF,ALF       NOW HIGH 8 BITS
0041  00117 030001        IOR 1B        A=177777
0042  00120 000040        CLE
0043  00121 014100        JSB START     THAT'S RIGHT, JSB!
0044  00122 000377  B377  OCT 377
0045                      END
**  NO ERRORS*
```

SHORT CPU-MEMORY TEST PROGRAM

This test program is useful if absolute programs cannot be loaded with the ABL due to hardware failures. It first tests a selection of ASG and SRG instructions followed by some MRG instructions. With the help of this program a certain bit pattern is stored in the first available memory location, read back and compared. A constant is added and the sum is stored in the same memory location repetitively. When a positive overflow is reached the next sequential memory location is loaded with the same variable bit patterns. Whenever the ABL is reached or one memory location does not compare a HLT 33 occurs with memory location 20 displaying the failing address or starting address of the ABL, the A-Reg. displaying the proper and the B-Reg. the faulty data pattern. Run time is a function of memory size and computer.

ADDR	CONTENTS		
2	103101	CLO	
3	003534	CCA,CLE,SSA,SLA,INA	A-Reg:000000,E=1
4	000135	SLA,ERA	A-Reg:100000,E=0
5	102011	HLT 11	
6	170020	STA I,20	
7	164020	LDB I,20	
10	054000	CPB A	Go to HLT 33 if not equal
11	002003	SZA,RSS	JMP to 13
12	102033	HLT 33	
13	040004	ADA 4	ADD 135_8 to A-Reg
14	103301	SOS,C	0VFF set if A-Reg 07777,CLO
15	024006	JMP 6	
16	034020	ISZ 20	Go to next mem. loc.
17	024003	JMP 3	
20	000021	DEF 21	Starting Address

NOTE: If location 20 contains the address of the ABL at HLT 33, the test ran correctly. To restart, location 000020 must be changed to 000021.

MEMORY CHECKERBOARD TEST

Address	Mnemonic	Contents
2 Start	LDB First	064022
3	INB	006004
4	LDA CT	060021
5	STA CTR	070020
6	CLA	002400
7 Loop	STA B, I	170001
10	CPA B,I	150001
11	CMA, RSS	003001
12	HLT	102001
13	ISZ CTR	034020
14	JMP Loop	024007
15	CPB Last	054023
16	JMP Start	024002
17	JMP Start + 1	024003
20 CTR	BSS 1	
21 CT	OCT *	
22 First	OCT **	
23 Last	OCT **	

Start at address two. Alternately stores all ones and zeros in a given location. Will continue this on that location for a number of times determined by contents of memory location *21. **Starting and ending locations to be tested are determined by the contents of locations 22 and 23. Error halts with correct pattern in A Register and failing location in B Register.

CPU BIT AND MEMORY CHECKER

ADDRESS	MNEMONIC	CONTENTS
02	OCT	177777
03	OCT	017677
04	OCT	000026
05	OCT	000026
06	NOP	000000
07	LDA 4	060004
10	INA	002004
11	STA 4	070004
12	CPA 3	050003
13	JMP 25	026025
14	LIA 1	102501
15	STA 4,I	170004
16	LDB 4,I	164004
17	CPB 2	054002
20	JMP 22	026022
21	HLT 22	102022
22	CLA	002400
23	STA 4,I	170004
24	JMP 6	026006
25	LDA 5	060005
26	JMP 10	026010

02 (Changed for bit pattern)
03 (Stop address)
04 (Start address and error)
05 (Auto restart address)
06 (Program starting address)
07 (SW reg = address 02)

SUPER JUMP SELF MEMORY TEST

```
          ASMB,A,B,L,T
    OPERATING PROCEDURE
    STARTING ADDRESS 100
    SWITCH REGISTER (BITS 0-5) SELECT CODE OF OUTPUT DEVICE
    SET BIT 15 TO A 1 TO LOOP
    OUTPUT DEVICE-BUF'D TTY CARD(MOST EFFECTIVE)OR GND TRUE I/O
    TTY CARD MUST HAVE HOOD REMOVED,GRD TRUE I/O MUST HAVE
    SPECIAL HOOD CONNECTOR (SAME AS DMA TEST)
    "RUN"
    HALT 0B
    SET SWITCH REGISTER FOR LAST AVAILABLE WORD OF MEMORY
    "RUN"
    THIS PROGRAM MUST BE RELOADED TO RESTART.
00004               ORG 4B
00004 102004        HLT 4B
00005 102005        HLT 5B
00100               ORG 100B
00100 064137        LDB WRD1        GET "JMP GO" INSTRUCTION.
00101 102501        LIA 1           GET DEVICE SELECT CODE.
00102 001021        ELA,ARS         PUT LOOPING FLAG IN E REG.
00103 174000        STB 0,I         PUT "JMP GO" IN TRAP CELL.
00104 073121        IOR S1          CONFIGURE
00105 073121        STA S1           I/O
00106 073126        IOR S2            INSTRUCTIONS.
00107 073126        STA S2
00110 002440        CLA,SEZ         LOOPING FLAG SET?
00111 070116        STA END         YES.
00112 102000        HLT 0
00113 102501        LIA 1           GET MAXIMUM MEMORY
00114 070143        STA MAXAD        ADDRESS AND SAVE IT.
00115 002001        RSS
00116 102077  END   HLT 77B         DONE. "RUN" TO RESTART.
00117 102100        STF 0           ENABLE INTERRUPTS.
00120 060140        LDA OUT         CONFIGURE INTERFACE
00121 102600  S1    OTA 0            FOR OUTPUT.
00122 060141        LDA BEGIN       STARTING ADDRESS FOR
00123 064142  R1    LDB INSTR        JUMP SELF INSTRUCTION.
00124 174000  R2    STB 0,I
00125 102001        OTA 1
00126 001100  S2    OCT 1100        THIS BECOMES A STC CHAN,C.
00127 124000        JMP 0,I         EXECUTE JUMP SELF.
00130 050143  GO    CPA MAXAD       END OF MEMORY?
00131 024116        JMP END         YES.
00132 002004        INA             BUMP MEMORY ADDRESS OF
00133 002004        INB              JUMP SELF INSTRUCTION.
00134 054144        CPB PAGE        END OF MEMORY PAGE?
00135 024123        JMP R1          YES.
00136 024124        JMP R2          NO.
00137 024130  WRD1  JMP GO
00140 110000  OUT   OCT 110000
00141 002000  BEGIN OCT 2000
00142 026000  INSTR OCT 26000
00143 000000  MAXAD BSS 1
00144 030000  PAGE  OCT 30000
                    END
```

CLEARING CORE

Address	Mnemonic	Octal
2	STA 1, I	170001
3	INB	006004
4	JMP *-2	024002

Initialize: B Register 5 B Will destroy loader if left enabled
A Register contains bit pattern stored in core

MEMORY ADDRESS TEST

Address	Mnemonic	Contents
2 Start	LDA First	060012
3	STA ,I	170000
4	CPA ,I	150000
5	INA, RSS	002005
6	HLT	102005
7	CPA Last	050013
10	JMP Start	024002
11	JMP Start + 1	024003
12 First	OCT 14	000014
13 Last	OCT *	

*Set to last location to be tested @ 1 location 12 may also be changed to test a different starting location.

Start at address 2. Stores memory address in the address. If an error occurs, the program halts with failing address in the A register.

COMMON DATA SECTION

SYSTEM TO I/O PROCESSOR DIAGNOSTIC LOADING

```
ASMB,A,B,L

         HED DIAGNOSTIC BOOTSTRAP
SW       ORG 2          EQU 01B
RC       EQU 10B        I/O TO MAIN CHANNEL
SC       EQU 11B        MAIN TO I/O CHANNEL
TU       EQU 12B        TELETYPE CHANNEL
PR       EQU 13B        PHOTOREADER CHANNEL

*THIS PROGRAM WILL LOAD ABSOLUTE PROGRAMS
*INTO THE I/O PROCESSOR WHEN THE SWITCH REGISTER IS
*CLEAR WHEN BIT 15 IS SET THE PROGRAM WILL GO
*INTO A MODE WHICH WILL RECEIVE MESSAGES
*FROM THE I/O PROCESSOR PROGRAM AND PRINT
*THESE MESSAGES ON THE CONSOLE.

START    EQU *
         LIB  SR        GET SWITCH REGISTER
         SSB            TEST FOR MODE OF OPERATION
         JMP  RITE      GO TO PRINT MODE
READ     STC  PR,C      START PHOTO READER
         LIB  SW        ARE WE SWITCHING MODES?
         SSB            TESTING
         JMP  START     YES
         SFS  PR        WAIT FOR CHARACTER
         JMP  *-4       NONE YET
         LIA  PR        GET CHARACTER FROM PHOTOREADER
         SFS  SC        WAIT FOR IOP TO ACKNOWLEDGE
         JMP  *-1       PREVIOUS CHARACTER
         OTA  SC        OUTPUT TO IOP
         STC  SC,C      SET FLAG
         JMP  READ      GET NEXT CHARACTER OR MODE
RITE     SFS  RC        READY FOR MESSAGE?
         JMP  CHK
         LIA  RC        GET CHARACTER FROM IOP
         OTA  TY        SEND CHARACTER TO TTY
         STC,TY,C       WAKE UP TTY
         SFS            CHECKING
         JMP  *-1       NOT YET
         STC  RC,C      SET FLAG
         JMP  RITE      GET NEXT CHARACTER OR MODE
CAK      LIB  SW        SWITCHING MODES?
         SSB            TESTING
         JMP  RITE      STAY IN MESSAGE MODE
         END  FINI
```

DIAGNOSTIC HISTORICAL SUMMARY

	BINARY	MOD	2105/8/12	2100A/S	2116C	2116B	2116A	2115A	2114B	2114A
Alter Skip	20400-60001	02116-91761			0	0	0	0	0	0
Alter Skip	24208-60001	02100-90019	0	0	0	0	0	0	0	0
Alter Skip	24316-16001	02100-90211	*	*	*	*	*	*	*	*
Long Diag.	24390-16001	02100-90001	*	*	¢	¢	¢	¢	¢	¢
Memory Ref	20401-60001	02116-91762			0	0	0	0	0	0
Memory Ref	24209-60001	02100-90018	0	0	0	0	0	0	0	0
Memory Ref	24315-16001	02100-90218	*	*	*	*	*	*	*	*
Long Diag.	24390-16001	02100-90001	*	*	¢	¢	¢	¢	¢	¢
Shift Rotate	20402-60001	02116-91763			0	0	0	0	0	0
Shift Rotate	24210-60001	02100-90017	0	0	0	0	0	0	0	0
Shift Rotate	24317-16001	02100-90212	*	*	*	*	*	*	*	*
Long Diag.	24390-16001	02100-90001	*	*	¢	¢	¢	¢	¢	¢
Low Memory Addr.	20403-60001	02116-91792			0	0	0	0	0	0
Low Memory Addr.	24211-60001	02100-90008	0	0	*	*	*	*	*	*
Low Memory Addr.	24323-16001	02100-90219	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
High Memory Addr.	20404-60001	02116-91792			0	0	0	0	0	0
High Memory Addr.	24212-60001	02109-90008	0	0	*	*	*	*	*	*
High Memory Addr.	24323-16001	02100-90219	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
Low Memory Checker Bd.	20513-60001	02114-90406						0	0	0
Low Memory CheckerBd.	20405-60001	02116-9011					0			
Low Memory Checker Bd.	20426-60001	02116-91793				0				
High Memory Checker Bd.	20512-60001	02114-90406						0	0	0
High Memory Checker Bd.	20406-60001	02116-9011					0			
High Memory Checker Bd.	20426-60001	02116-91793				0				
Low Memory Pattern	24161-60001	02116-91782			0					
Low Memory Pattern	24193-60001	02100-90023	0	0						
Low Memory Pattern	24323-16001	02100-90219	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
High Memory Pattern	24162-60001	02116-91782			0					
High Memory Pattern	24194-60001	02100-90023	0	0						
High Memory Pattern	24323-16001	02100-90219	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
Memory Parity Check	20345-60001	05951-01320					0	0	0	
Memory Parity Check	24144-60001	12591-90011			0	0				
Memory Parity Check	24198-60001	02100-90021	0	0						
Memory Parity Check	24325-16001	02100-90221	*	*						
Long Diag.	24390-16001	21000-90001	*	*	¢	¢	¢	¢	¢	¢
Interrupt Diagnostic	20415-60001	02116-91768			0	0	0	0	0	0
Interrupt Diagnostic	24215-60001	02100-90025	0	0	0	0	0	0	0	0
Interrupt Diagnostic	24318-16001	02100-90213	*	*	*	*	*	*	*	*
Long Diag.	24390-16001	02100-90001	*	*						
Power Fail/Auto Restart	20428-60001	02116-91769			0	0	0	0	0	0
Power Fail/Auto Restart	24206-6001	02100-90020	0	0	0	0	0	0	0	0
Power Fail/Auto Restart	24321-16001	02100-90216	*	*	*	*	*	*	*	*
Long Diag.	24390-16001	02100-90001	*	*						

NOTE: An entry into a field of a * or 0 designates that diagnostic as operational on that CPU.
* Current
0 Old Version
¢ Stand alone version in Long Diagnostic only, used with configurator.

DIAGNOSTIC HISTORICAL SUMMARY (CONT.)

	BINARY	MOD	2105/8/12	2100A/S	2116C	2116B	2116A	2115A	2114B	2114A
Power Fail Interrupt	20434-60001	02116-91759			0	0				
DMA/DCPC	20524-60001								0	
DMA/DCPC	24185-60001	12578-90013			0	0	0	0		
DMA/DCPC	24195-60001	12578-90014	0	0	0	0	0	0		
DMA/DCPC	24322-16001	12578-90217	*	*	*	*	*	*		
Long Diag.	24390-16001	12578-90001	*	*						
Extended Arith. Unit	24186-60001	12579-90013			0	0	0	0		
Extended Arith. Unit	24214-60001	02100-90007	0	0	0	0	0	0		
Extended Arith. Unit	24319-16001	02100-90214	*	*	*	*	*	*		
Long Diag.	24390-16001	02100-90001	*	*						
Floating Point	24251-60001	02100-90064	0	0						
Floating Point	24320-16001	02100-90215	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
Memory Protect	24222-60001	02100-90006	0	0						
Memory Protect	24324-16001	02100-90220	*	*						
Long Diag.	24390-16001	02100-90001	*	*						
WCS	24284-60001	12908-90005		0						
WCS 129088 & 12978A	24390-16001	12908-90001	*	*						

COMMON DATA SECTION

HP 2000 DIAGNOSTIC CONFIGURATION 24296-60001

1. LOAD CONFIGURATOR USING BBL, BBDL, OR BMDL

2. P=100,PRESET,RUN,HALT=102000.

3. S=XXXXXX(USE TABLE1),RUN,HALT=102001.

TABLE 1

BASIC OCTAL ASSIGNMENTS

2100A =070073
2100S =070077
2105/2108 =100032
2114A =050010
2114B =060010
2115A =010010
2116A =010010
2116B =020010
2116C =030010

VARIABLES ACCORDING TO OPTIONS

S.W.REG	2108	2105	2100S	2100A	2116C	2116B	2116A	2115A	2114A	2114B	
7										*	DMA SINGLE CHAN.
6	*	*		*							FLOATING PT.
5	*				*	*	*	*	*	*	MEM PROT.
4					*	*	*				MEM PARITY
3							*	*			CIR
2	*	*		*	*	*	*	*		*	DMA, DCPC
1					*	*	*	*			EAU
0	*	*			*	*	*	*	*	*	P.F. AUTO REST.

4. S=XXXXXX(USE TABLE 2),RUN,RUN,RUN,RUN,HALT=102005.

TABLE 2

2752/2754 =1000SC
2762 =0100SC
2600/2615 =0400SC

MOST COMMON DEVICES

****NOTE THERE IS AN OPTIONAL PROCEDURE FOR THIS STEP****
****SEE MANUAL NO. 02100-90157****

5. S-XXXXXX(USE TABLE3),RUN,HALT=102077.

TABLE 3

4K=000001 20K=040001
8K=010001 24K=050001
12K=020001 28K=060001
16K=030001 32K=070001

6. CONFIGURATION COMPLETE.

7. TO DUMP CONFIGURED COPY.

P=XXXXXX(USE TABLE 4),S=SELECT CODE OF PUNCH OR TTY, PRESET, RUN,HALT=102077.

TABLE 4

4K=007677 20K=047677
8K=017677 24K=057677
12K=027677 28K=067677
16K=037677 32K=077677

COMMDN DATA SECTION

LONG DIAGNOSTIC - 24390-16001,2&3

1. Load tape #1, record #1 using the ABL.

2. Set P=100

   S Reg = Bits 0-5 Tape Reader S.C.
   Bits 6-11 Console Device
   Bit 12 Skip Tape #1
   Bits 14-15 Number of Passes
   00 1
   10 10
   01 100
   11 65K

3. PRESET, RUN

4. Error Halts defined in M.O.D.. Test being run is identified by one of the following Diagnostic Serial Numbers in loc. 126:

   041000 Initial Check
   042000 Long Diagnostic Control Module
   101000 MRG
   101001 ASG
   101002 SRG
   102100 Memory
   043000 Long Diagnostic Control Program

5. Halt 107077 = Successful completion

6. Place tape #2 in reader (skip to step 11 to run tape #3)

7. S Reg = Bit 0 Delete EAU
   1 Delete Mem Protect
   2 Delete Floating Point
   3 Delete EIG (Index)
   4 Delete EIG1 (Bit, Byte, Word)
   14-15 Number of Passes

8. PRESET; RUN

9. Error halts or messages defined in M.O.D.. DSN in loc 126:

   044000 Parameter set up
   101004 EAU
   102001 Memory Protect
   101107 Floating Point
   101011 EIG (Index)
   101012 EIG1 (Bit, Byte, Word)
   045000 End Message

10. Halt 107077 = Successful completion.

11. Place Tape #3 in reader

COMMON DATA SECTION

LONG DIAGNOSTIC-24390-16001, 2 & 3 (Continued)

12. S Reg = Bit 0 Delete IOG
    1 Delete DMA
    2 Delete Pwr Fail/Auto Restart
    3 Delete Memory Parity
    4 Delete WCS
    14-15 Number of passes

13. PRESET; RUN

14. Each test is preceeded by HLT 106000. DSM in loc 126:

    101103 IOG
    101105 DMA
    101106 Pwr Fail/Auto Restart
    102002 Memory Parity
    103105 WCS

15. IOG (otherwise skip to step 16)

    a. PRESET; RUN
    b. HLT 107000
    c. Set S Reg bit 0-5 to S.C. to be tested
    d. Run
    e. HLT 107001
    f. Repeat steps c and d for each I/O slot to be tested.
    g. Set S Reg = 0 to terminate S.C. input
    h. RUN; HLT 102074
    i. PRESET; RUN

16. DMA (otherwise skip to step 17)

    a. A microcircuit, 16 bit duplex or 8 bit duplex card with a 1251-0332 test hood (24 pin shorting connector with pins 22 and 23 connected) is required for this test. The legal jumper configurations are:

    12566A/B (Pos or Neg True) Microcircuit

W1	W2	W3	W4	W9
B	A	A	B	A
B	C	A	A	A
B	C	A	B	A

COMMON DATA SECTION

LONG DIAGNOSTIC 24390-16001, 2 & 3 (Continued)

12554A +16 Bit Duplex

W4	W5	W6	W7
B	B	A/B	A
B	A	A	A
A/B	B	C	A
B	A	C	B
A	A	A/B	B

12554A-01 -16 Bit Duplex

W4	W5	W6	W7
A/B	A	B	B
A	A	A	B
B	A	C	B
A/B	B	C	A
A/B	B	B	A

12597A + 8 Bit Duplex

Standard tape reader or punch configuration

b. Set S Reg = S.C. of test card
c. PRESET; RUN
d. HLT 102074
e. Set S Reg bit 8 (also bit 5 if 8-bit duplex is used)
f. PRESET; RUN

17. Pwr Fail/Auto Restart (otherwise skip to step 18)

a. Set ARS/$\overline{\text{ARS}}$ switch to ARS (2100 = A7 card; 21MX = CPU card)
b. PRESET; RUN
c. S Reg Bits 0-7 will increment
d. Power off (standby only for 21MX w/o battery)
e. Power back on.

18. Memory Parity (otherwise skip to step 19)

a. ARS/$\overline{\text{ARS}}$ switch to ARS; P.E. switch to INTERRUPT
b. If tape #2 was not run, set loc 115 = 100173
c. S Reg = S.C. of standard I/O card
d. PRESET; RUN
e. HLT 102074
f. PRESET; RUN
g. HLT 102002
h. Power Off (standby on 21MX w/o battery)

COMMON DATA SECTION

LONG DIAGNOSTIC 24390-16001, 2 & 3 (Continued)

i. Force bad parity as follows:

2114, 15, 16 - Remove Parity Card
2100 - Short E1 to E2 and E3 to E4 on Data Control Card
21MX - Short PAR to ground on Memory Controller

j. Power On
k. Set P Reg = 130; Set S Reg = 0
l. PRESET; RUN
m. HLT 102003
n. Power Off (Standby on 21MX w/o battery)
o. Restore parity ckt. to original configuration for good parity
p. Power On
q. Set Parity switch to HALT
r. Set P Reg = 131; Set S Reg = 0
s. PRESET; RUN
t. Computer halts with PARITY indicator on, T Reg displayed and B Reg = 1
u. Set Parity switch to INTERRUPT; S Reg = 0
v. PRESET; RUN
w. The PARITY indicator lites and the next tape record is read.

19. WCS (otherwise End of Tape)

a. Set S Reg bits 0-5 = S.C. of lowest WCS card
12-15 = Control Store Module #

Note: If 21MX - Modules 0, 1, 2, 16_8 and 17_8 are illegal
If 2100 - Module 0 is illegal

b. PRESET; RUN
c. HLT 102074
d. Set S Reg = 0
e. PRESET; RUN

20. HLT 107077 = Successful completion

LONG DIAGNOSTIC (FIELD SERVICE VERSION)

1. Load 1st segment using ABL
2. S.A. 10_8
3. RUN; Halt 107000_8
4. SW Reg. =0-5 Photoreader or buffered TTY select code
   6-11 TTY Select Code
   14 Delete central interrupt test
   15 Serial TTY
5. RUN; Halt 107001_8
6. SW Reg. =0 Test 2 channels if DMA present
   1-14 Delete test # that corresponds to switch #
   15 Short version (one pass per test)
7. RUN; Halt 107002_8
8. SW Reg. = Upper memory limit (normally ABL-1)
9. RUN; Halt 107003_8
10. SW Reg. =0
11. RUN
12. Normal halt 102077_8

DIAGNOSTICS INCLUDED IN TAPE

#1 Hi Memory Address – Error Halt 102001_8
A Reg. = Address Expected
B Reg. = Address Read

#2 Hi Memory Crusher – Error Halt 102001_8
A Reg. = Data Read
B Reg. = Data Expected
RUN; Halt 102002_8
A Reg. = Data Read
B Reg. = Address of failure

#3 MRG Test 24209 Rev A
#4 ASG Test 24208 Rev A
#5 SRG Test 24210 Rev A
#6 EAU Test 24214 Rev A
#7 Memory Protect 24222 Rev A
#8 Reserved for Floating Point
#9 Basic I/O W/Interrupt 24215 Rev A
#10 Super Duper DMA

Error Halts		
102011 Ch. #1	102021 #2	–CLF failure
102012 Ch. #1	102022 Ch. #2	–STF failure
102013 Ch. #1	102023 Ch. #2	–Wd.-Cntr bit failure
102014 Ch. #1	102024 Ch. #2	–Data Output Failure
102015 Ch. #1	102025 Ch. #2	–Data Input Failure
102016 Ch. #1	102026 Ch. #2	–Interrupt failure
102017 Ch. #1	102027 Ch. #2	–Wd.-Cntr Counting

#11 Lo Memory Address – Same as #1
#12 Lo Memory Crusher – Same as #2
#77 End-of-Tapes

LONG DIAGNOSTIC (FIELD SERVICE VERSION) (CONT)

CONTROL PROGRAM HALTS

107000 – Set SW Reg. for I/O devices
107001 – Set SW Reg. for program options
107002 – Set SW Reg. for Upper Memory Limit
107003 – Set SW Reg. for diagnostic parameters
102051 – No reader select code specified (restart)
102055 – Checksum on control program (Restart)
102065 – Reader time out (RUN to continue)

RESTART (TO READ NEXT TEST)

In Hi Control =7070_8
In Lo Control =145_8 (Last two tests)

MEMORY ADDRESS TEST

MEM ADDR	CONTENTS	LABEL	INSTRUCTION
00002	006204		INB, CME
00003	060023		LDA FRST
00004	150000	CMPAR	CPA Ø, I
00005	002001		RSS
00006	102000		HLT
00007	052022		CPA LAST
00010	024014		JMP START
00011	002004		INA
00012	024004		JMP CMPAR
00013	000000		NOP
00014	060023	START	LDA FRST
00015	170000	STORE	STA Ø, I
00016	050022		CPA LAST
00017	024002		JMP CMPAR-2
00020	002004		INA
00021	024015		JMP STORE
00022*	007777	LAST	OCT 7777
00023	000024	FRST	OCT 00024

*For 8K machines (22) 017777
Use 007677 or 017677 if you do not desire to test protected area.
Starting address 14.
Depress PRESET and RUN. The computer shall run. If it halts, there is an address error.
Extend bit shall blink on and off, B-reg increments each pass.
Locations 00022 and 00023 may be changed to test any core area.
(requires ≈ 1 sec)

CPU DIAGNOSTIC

MEMORY PATTERN TESTS (24161,2)
(any computer)

Load Diagnostic,

STK #	PROG AREA	TEST AREA	SA
24161	2-620	621-upper limit	2
24162	17000-17574	6-16777*	17000

If both Parity and Memory Protect installed bit 11 = 0 and Parity Switch down (interrupt)

If Memory protect not installed, bit 11 = 1, and Parity Switch up (HALT) if installed.

Sw reg = 0, PRESET, RUN (default test area = 8K memory)

To Test Selected Area

(24161): SA = 2, raise bit 15, RUN, Hlt 1 @ P = 30;
Sw reg ≥ 621, RUN, Hlt 2 @ P = 34;
Sw reg ≤ X7677 (or desired limit), RUN;
HLT 4 @ P = 47. Select options (Recommend 000200),
RUN, Hlt 77 on completion.

(24162): S.A. = 17000, raise bit 15, RUN, Hlt 1 @ P = 17030;
Sw reg ≥ 2, RUN, Hlt 2 @ P = 17034;
Sw reg ≤ 16777, RUN; Hlt 4 @ P = 17047; Select opticns
(Recommend 000200). RUN, Hlt 77 on completion.

Bit	Function
0	hold current checkerboard pattern (use with 12 + 13)
1	store in table of errors.
2	Display current error momentarily.
3	Reset table of errors (with 6).
4	Suppress error halts.
5	Return to start HLT 5 @ P = 23
6	Return to start & halt A = next available address, B = # of errors.
7	Halt at end at diagnostic. Hlt 77 @ P = 114
11	ON - if no memory protect installed.
12	Loop on test 3 (overrides 13 +14) bit 0 checkerboard
13	Loop on test 2 (overrides 14) bit 1 checkerboard
14	Loop on test 1 word checkerboard
15	Test specified area.

*will test 2-16777 but parity error or power fail may cause problems. (due to interrupt at Select Code 4 or 5)

BOOTSTRAP LOADER

```
20   103713      STC  RDR,C   }
21   102313      SFS  RDR      }  Read 1st char.
22   024021      JMP  *-1      }
23   102513      LIA  RDR
24   001727      ALF, ALF        Pack
25   103713      STC  RDR,C   }
26   102313      SFS  RDR     }  Read 2nd char.
27   024026      JMP  *-1     }
30   102413      MIA  RDR     }
31   170001      STA  1,I
32   006004      INB
33   024020      JMP  20B
          RDR EQU  13B
```

Toggle in program, B-reg = *77700, S.A. = 20, load special bootstrap tape in reader, enable protected loader area. RUN. Press HALT.

*Loader Starting Addresses

MEMORY SIZE	STARTING ADDRESS OF LOADER		
	For Paper Tape	For FH Disc	For MH Disc
4K	07700		
8K	17700	17760	17750
12K	27700	27760	27750
16K	37700	37760	37750
24K	57700	57760	57750
32K	77700	77760	77750

BOOTSTRAP LOADER GENERATOR (A008-22009)
Load tape, S.A. = 2, Sw reg = SC of TTY, RUN. Follow directions printed on TTY.

LOADER LOADER

A. STARTUP FROM SCRATCH

1. Enter instructions shown in table 1-1 via switch register.
2. Place paper tape in reader (be it photoreader or teletype); set P to 3000_8.
3. Set switch register to indicate desired loader and select codes per table 1-2.
4. Press PRESET (External and Internal, if applicable), LOADER ENABLE, and RUN. Tape will be read in and new loader placed into top locations of memory.

B. IF PAPER TAPE LOADER EXISTS

Unwind paper tape to first section of blank tape and place paper tape into reader at this blank area. Load tape using existing paper tape loader. Set P to 100_8 and proceed as in steps 3 and 4 above.

C. PROGRAM HALTS

Memory Data	Meaning
102077	Program completed successfully.
102001	Select code is less than 10_8 (bad select code displayed in A-reg).
102002	Loader number not implemented yet.
102003	An instruction was not stored correctly – possibly caused by not enabling the loader.

After any program halt, the program may be restarted by resetting the switch register (if necessary) and pressing PRESET (External and Internal, if applicable), LOADER ENABLE, and RUN.

LOADER LOADER (CONT)

Table 1-1. Instructions Entered Via Switch Register

Memory Location	Contents		Source Code	
2765	. . .	READ	BSS	1
2766	002500		CLA,CLE	
2767	1037XX		STC	RDR,C
2770	1023XX		SFS	RDR
2771	026770		JMP	*-1
2772	001626		ELA,ELA	
2773	001626		ELA,ELA	
2774	1024XX		MIA	RDR
2775	002040		SEZ	
2776	126765		JMP	READ,I
2777	026767		JMP	READ+2
3000	016765	START	JSB	READ
3001	073003		STA	*+2
3002	016765		JSB	READ

XX = paper tape reader select code

Table 1-2. Switch Register Options

Loader	Bits 15-12	Bits 11-6	Bits 5-0
BBL	0000	Not used	Reader SC
BBDL	0001	Fixed-head disc SC	Reader SC
BMDL (7900/7901)	0010	Moving-head disc SC	Reader SC
BMDL (2883)	0011	Moving-head disc SC	Reader SC
BMDL (2870)	0100	Moving-head disc SC	Reader SC
MTRS	0101	Magnetic tape SC	Not used

(For two-channel interfaces, use lower select code)

BINARY LOADER

```
                ASMB,A,B,L,T
17700                ORG 17700B   DEPENDS ON CORE SIZE
17700 107700 LOAD    CLC 0,C      TURN OFF ALL DEVICES
17701 063770         LDA STAI
17702 106501         LIB 1        CHECK FOR OPTIONS
17703 004010         SLB          S-REG(0)=1?    .
17704 002400         CLA          YES: CHECKSUM OPTION
17705 006020         SSB          S-REG(15)=1?
17706 063771         LDA CPAI     YES: VERIFY CORE OPT.
17707 073736         STA OPTI     STORE OPTIONAL INST.
17710 006401         CLB,RSS      BYPASS EOT CHECK
17711 067773 CONT    LDB CM11     B=-11 FOR EOT CHECK
17712 006006 EOTCH   INB,SZB      END OF TAPE?
17713 027717         JMP LD1      NO: GET NEXT CHAR
17714 107700         CLC 0,C      TURN OFF ALL DEVICES
17715 102077         HLT 77B      END OF TAPE
17716 027700         JMP LOAD     START NEXT TAPE
17717 017762 LD1     JSB CHAR     GET A CHARACTER
17720 002003         SZA,RSS      IS IT THE WORD COUNT?
17721 027712         JMP EOTCH    NO: CHECK FOR EOT
17722 003104         CMA,CLE,INA  (2'S COMP WORD COUNT)
17723 073774         STA COUNT    SAVE WORD COUNT
17724 017762         JSB CHAR     SKIP NEXT CHAR
17725 017753         JSB WORD     GET STARTING ADDRESS
17726 070001         STA 1        INITIALIZE CHECKSUM IN B
17727 073775         STA ADDRS    ALSO IN ADDRESS
17730 063775 LD2     LDA ADDRS    CHECK FOR ADDR>=LOADER
17731 043772         ADA MAXAD
17732 002040         SEZ          E-REG=0  OK
17733 027751         JMP ADERR    BAD ADDRESS
17734 017753         JSB WORD     NEXT WORD IN A-REG
17735 044000         ADB 0        CONTINUE CHECKSUM
17736 000000 OPTI    NOP          STA, CPA, OR NOP
17737 002101         CLE,RSS      NORMALLY BYPASS HALT
17740 102000         HLT 0B       DID NOT COMPARE
17741 037775         ISZ ADDRS    INCREMENT ADDRESS
17742 037774         ISZ COUNT    UPDATE WORD COUNT
17743 027730         JMP LD2      NEXT WORD
17744 017753         JSB WORD     END OF RECORD
17745 054000         CPB 0        COMPARE CHECKSUMS
17746 027711         JMP CONT     LOOK FOR END OF TAPE
17747 102011         HLT 11B      CHECKSUM ERROR
17750 027700         JMP LOAD     START OVER
17751 102055 ADERR   HLT 55B      ILLEGAL ADDRESS
17752 027700         JMP LOAD     START OVER
17753 000000 WORD    NOP          READ ONE BYTE
17754 017762         JSB CHAR     FIRST BYTE
17755 001727         ALF,ALF      POSITION BYTE
17756 073776         STA TEMP     SAVE IT
17757 017762         JSB CHAR     SECOND BYTE
17760 033776         IOR TEMP     MERGE BYTES
17761 127753         JMP WORD,I   RETURN WITH WORD
17762 000000 CHAR    NOP          READ BYTE FROM READER
17763 103713         STC RDR,C    INITIATE READ
17764 102313         SFS RDR      ** CHECK THESE IF  **
17765 027764         JMP *-1      ** LOADER BOMBED   **
17766 102513         LIA RDR      GET BYTE
17767 127762         JMP CHAR,I   HAVE BYTE A-REG(0-7)
17770 173775 STAI    STA ADDRS,I  HAVE OPT1 FOR NORMAL LOAD
17771 153775 CPAI    CPA ADDRS,I  OPT1 FOR VERIFY OPTION
17772 160100 MAXAD   ABS -LDR     LOADER ADDRESS (2'S COMP)
17773 177765 CM11    DEC -11      EOT CHAR COUNT
17774 000000 COUNT   BSS 1        WORD COUNT
17775 000000 ADDRS   BSS 1        ADDRESS LOCATION
```

BINARY LOADER (CONT)

```
  17776 000000  TEMP  BSS 1       HOLDS FIRST BYTE
  00013         RDR   EQU 13B     READER SELECT CODE
  17700         LDR   EQU 17700B  LOADER ADDRESS
*CHECK 17764,17765 IF LOADER IS BOMBED
*17763,17764,17766 DEPEND ON READER SELECT CODE
*17772 DEPENDS ON CORE SIZE
                    END
```

DISC LOADER

```
            ASMB,A,B,L,T
17700               ORG 17700B  DEPENDS ON CORE SIZE
17700 107700 START  CLC 0,C
17701 002401        CLA,RSS
17702 063726 CONT   LDA M.17  FEED FRAME COUNTER
17703 006700        CLB,CCE   SET E TO READ BYTE
17704 017742        JSB READ  GET # OF CHAR
17705 007306        CMB,CCE,INB,SZB   (2'S COMP)
17706 027713        JMP *+5   NON-ZERO BYTE
17707 002006        INA,SZA   FEED FRAME COUNTER
17710 027703        JMP *-5
17711 102077        HLT 77B   END OF TAPE
17712 027700        JMP START
17713 077754        STB WD.CT # WORDS IN RECORD
17714 017742        JSB READ  GET FEED FRAME
17715 017742        JSB READ  GET ADDRESS
17716 074000        STB 0     INITIATE CHECKSUM
17717 077757        STB ADDR
17720 067757 CHECK  LDB ADDR
17721 047755        ADB MAXAD CHECK ADDR BELOW LOADER
17722 002040        SEZ       E-1 OK
17723 027740        JMP HLT55 ADDR>=LOADER
17724 017742        JSB READ  GET NEXT WORD
17725 040001        ADA 1     CONTINUE CHECKSUM
17726 177757 M.17   STB ADDR,I ALSO USED AS CONSTANT
17727 037757        ISZ ADDR
17730 000040        CLE
17731 037754        ISZ WD.CT
17732 027720        JMP CHECK
17733 017742        JSB READ
17734 054000        CPB 0
17735 027702        JMP CONT
17736 102011        HLT 11B   CHECKSUM ERROR
17737 027700        JMP START
17740 102055 HLT55  HLT 55B   ADDRESS >= LOADER
17741 027700        JMP START
17742 000000 READ   NOP       E=0 READ WORD, =1 BYTE
17743 006600        CLB,CME   E-REG BYTE POINTER
17744 103713        STC RDR,C  START READER
17745 102313        SFS RDR    ** CHECK THESE IF  **
17746 027745        JMP *-1    ** LOADER BOMBED   **
17747 107413        MIB RDR,C  GOT BYTE
17750 002041        SEZ,RSS
17751 127742        JMP READ,I
17752 005767        BLF,CLE,BLF
17753 027744        JMP *-7
17754 000000 WD.CT  NOP       WORD COUNT
*17755 1X0100 MAXAD ABS -LDR  LOADER ADDR (2'S COMP)
 17756 0200XX DMA.C OCT 0200XX DISC SC (DATA CHANNEL)
17757 000000 ADDR   NOP
17760 107700        CLC 0,C
17761 063756        LDA DMA.C
17762 102606        OTA DMA.6 PROG WORD
```

DISC LOADER (CONT)

```
17763 002700          CLA,CCE
17764 102615          OTA DISC+1 DISC TRACK 0,SECTOR 0
17765 001500          ERA
17766 102602          OTA DMA.2  CORE ADDRESS
17767 063777          LDA M.64
17770 102702          STC DMA.2
17771 102602          OTA DMA.2  WORD COUNT, BYTE
17772 103706          STC DMA.6,C
17773 102714          STC DISC
17774 067776          LDB JMP.
17775 074077          STB BP.77  FOR JUMP SELF
17776 024077  JMP.    JMP BP.77
17777 177700  M.64    DEC -64    TRANSFER ONE SECTOR
00013         RDR     EQU 13B    READER SELECT CODE
17700         LDR     EQU 17700B LOADER ADDRESS
00014         DISC    EQU 14B    DISC SELECT CODE
00006         DMA.6   EQU 6B     USE CHANNEL ONE
00002         DMA.2   EQU 2B
00077         BP.77   EQU 77B    BASE PAGE (JMP SELF)
 CHECK 17745,17746 IF LOADER IS BOMBED
                      END
```

* 8K = 160100
12K = 150100
16K = 140100
24K = 120100
32K = 100100

Address	Contents	Address	Contents
x7700	002701	x7740	1023kk
x7701	063722	x7741	027740
x7702	002307	x7742	1064kk
x7703	102077	x7743	002041
x7704	017735	x7744	127735
x7705	007307	x7745	005767
x7706	027702	x7746	027737
x7707	077733	x7747	030000
x7710	017735	x7750	1026dd
x7711	017735	x7751	1037dd
x7712	074000	x7752	067747
x7713	077734	x7753	1066cc
x7714	067734	x7754	1037cc
x7715	047777	x7755	1066dd
x7716	002040	x7756	063776
x7717	102055	x7757	102606
x7720	017735	x7760	067732
x7721	040001	x7761	106602
x7722	177734	x7762	1037dd
x7723	037734	x7763	102702
x7724	000040	x7764	106602
x7725	037733	x7765	013741
x7726	027714	x7766	1067cc
x7727	017735	x7767	1026cc
x7730	054000	x7770	1037dd
x7731	027701	x7771	103706
x7732	102011	x7772	1037cc
x7733	000000	x7773	1023cc
x7734	000000	x7774	027773
x7735	000000	x7775	127717
x7736	006600	x7776	1200dd
x7737	1037kk	x7777	1n0100

x = 2 for 12k, 3 for 16k, 4 for 20k, 5 for 24k, 6 for 28k, 7 for 32k

kk = tape input device select code

cc = low priority (higher numbered) disc select code

dd = high priority (lower numbered) disc select code

n = 5 for 12k, 4 for 16k, 3 for 20k, 2 for 24k, 1 for 28k, 0 for 32k

Address	Contents	Address	Contents		
x7700	002701	x7740	1023kk		
x7701	063722	x7741	027740		
x7702	002307	x7742	1064kk		
x7703	102077	x7743	002041		
x7704	017735	x7744	127735		
x7705	007307	x7745	005767		
x7706	027702	x7746	027737		
x7707	077733	x7747	177600	x	= 2 for 12k, 3 for 16k,
x7710	017735	x7750	063775		4 for 20k, 5 for 24k,
x7711	017735	x7751	1026cc		6 for 28k, 7 for 32k
x7712	074000	x7752	1037cc		
x7713	077734	x7753	1023cc		
x7714	067734	x7754	027753	kk	= tape input device
x7715	047777	x7755	067776		select code
x7716	002040	x7756	106606		
x7717	102055	x7757	067732	cc	= low priority (higher
x7720	017735	x7760	106602		numbered) disc
x7721	040001	x7761	102702		select code
x7722	177734	x7762	067747		
x7723	037734	x7763	106602	dd	= high priority (lower
x7724	000040	x7764	001000		numbered) disc
x7725	037733	x7765	1067cc		select code
x7726	027714	x7766	1026cc		
x7727	017735	x7767	1037dd	n	= 5 for 12k, 4 for 16k,
x7730	054000	x7770	103706		3 for 20k, 2 for 24k,
x7731	027701	x7771	1037cc		1 for 28k, 0 for 32k
x7732	102011	x7772	1023cc		
x7733	000000	x7773	027772		
x7734	000000	x7774	127717		
x7735	000000	x7775	020000		
x7736	006600	x7776	1200dd		
x7737	1037kk	x7777	1n0100		

Address	Contents	Address	Contents			
x7700	002701	x7740	1023kk			
x7701	063722	x7741	027740			
x7702	002307	x7742	1064kk			
x7703	102077	x7743	002041			
x7704	017735	x7744	127735	y	=	0 select Boot from head 0
x7705	007307	x7745	005767	y	=	1 select Boot from head 2
x7706	027702	x7746	027737			
x7707	077733	x7747	03y000	x	=	2 for 12k, 3 for 16k,
x7710	017735	x7750	002400			4 for 20k, 5 for 24k,
x7711	017735	x7751	1026dd			6 for 28k, 7 for 32k
x7712	074000	x7752	1037dd			
x7713	077734	x7753	067747			
x7714	067734	x7754	1066cc	kk	=	tape input device
x7715	047777	x7755	1037cc			select code
x7716	002040	x7756	1066dd			
x7717	102055	x7757	063776	cc	=	low priority (higher
x7720	017735	x7760	102606			numbered) disc
x7721	040001	x7761	067732			select code
x7722	177734	x7762	106602			
x7723	037734	x7763	1037dd	dd	=	high priority (lower
x7724	000040	x7764	102702			numbered) disc
x7725	037733	x7765	106602			select code
x7726	027714	x7766	013741			
x7727	017735	x7767	1026cc	n	=	5 for 12k, 4 for 16k,
x7730	054000	x7770	1037dd			3 for 20k, 2 for 24k,
x7731	027701	x7771	103706			1 for 28k, 0 for 32k
x7732	102011	x7772	1037cc			
x7733	000000	x7773	1023cc			
x7734	000000	x7774	027773			
x7735	000000	x7775	127717			
x7736	006600	x7776	1200dd			
x7737	1037kk	x7777	1n0100			

MTRS LOADER

```
                ASMB,A,B,L,T,C      MTRS ABSOLUTE PROTECTED LOADER
17700 063775            LDA SLORW       SELECT UNIT 0
17701 102611            OTA CMND         AND
17702 103711            STC CMND,C        REWIND TAPE.
17703 106501            LIR SSW         GET ORDINAL NUMBER OF PROGRAM.
17704 007307            CMB,CCE,INB,SZB,RSS    MAKE < 0, PRESET -E-.
17705 067767            LDB DFALT       USE DEFAULT IF SWREG = 0.
17706 077773            STB PROG#       SAVE FOR COUNTER.
17707 063774 READ       LDA RRF         OUTPUT
17710 102611            OTA CMND         READ COMMAND
17711 102511            LIA CMND          AND
17712 001323            RAR,RAR            TEST
17713 001310            RAR,SLA             FOR REJECT.
17714 027707            JMP READ        REJECTED, KEEP TRYING UNTIL O.K.
17715 103711            STC CMND,C      START TAPE.
17716 103710            STC DATA,C      INITIALIZE DATA CHANNEL.
17717 063773            LDA PROG#       GET PROG ORDNL CNTR - 0 IF LOAD.
17720 006645            CLB,SEZ,CME,INB,RSS    -B- _ DATA RECORD MASK.
17721 027725            JMP DATAR       DATA RECORD, SKIP NEXT.
17722 067766            LDB ADRSA       POST RECORD,
17723 077777            STB PTR           INITIALIZE ADDRESS POINTER.
17724 067771            LDB MASK1       -B- _ POST REC MASK (S.A. ONLY).
17725 002042 DATAR      SEZ,SZA         IF DATA RECORD AND NOT LOADING,
17726 027707            JMP READ          IGNORE THE RECORD.
17727 102211            SFC CMND        POST RECORD OR (DATA RECORD AND
17730 027741            JMP DONE         LOADING), WAIT FOR DATA OR
17731 102310 LOOP       SFS DATA          FOR TAPE TO STOP.
17732 027727            JMP *-3
17733 103510            LIA DATA,C      GET WORD FROM TAPE
17734 173777            STA PTR,I         AND STORE IT.
17735 006011            SLB,RSS         IF WORD IS TO BE SAVED,
17736 037777            ISZ PTR           BUMP ADDRESS POINTER.
17737 004065            CLE,ERB         SHIFT STORE/NO STORE MASK.
17740 027731            JMP LOOP        RETURN FOR NEXT WORD.
17741 005500 DONE       ERB             FINAL SHIFT, -E- _ 1 IF WE JUST
                                          READ POST RECORD, 0 IF DATA.
17742 073777            STA PTR         SAVE DATA LOAD ADDR IF POST.
17743 067773            LDB PROG#       GET PROGRAM ORDINAL COUNTER.
17744 063776            LDA S.A.        GET PROGRAM STARTING ADDRESS.
17745 002240            SEZ,CME         IF THIS WAS DATA RECORD
17746 002003            SZA,RSS          OR CONTINUATION POST RECORD,
17747 027754            JMP ZTEST          SKIP INITIAL POST REC STEPS.
17750 033765            IOR JMP         INITIAL POST REC, INCLUDE JUMP
17751 006007            INB,SZB,RSS      TO STARTING ADDRESS.  IF THIS
17752 070002            STA 2              IS OUR PROG, STORE THE JUMP.
17753 000040            CLE             WIPE OUT -E- CAUSED BY INB,SZB.
17754 006020 ZTEST      SSB             IF WE HAVEN'T FOUND OUR PROG YET
17755 027706            JMP READ-1        UPDATE PROG#, READ NEXT REC.
17756 102511            LIA CMND        OUR PROG OR POST RECORD OF NEXT
17757 013772            AND MASK2        ONE, CHECK FOR PARITY ERROR
17760 002002            SZA                OR END-OF-FILE.
17761 102001            HLT 1           ERROR HALT.  **NOT PROTECTED**
17762 006003            SZB,RSS         1ST POST REC OF NEXT PROGRAM?
17763 027706            JMP READ-1      NO, UPDATE PROG#, CONTINUE.
17764 063770            LDA HLT70       YES, STORE FINAL HALT.
17765 024000 JMP        JMP A           GO TO IT.
```

MTRS LOADER (CONT)

```
   CONSTANTS AND STORAGE.

00000          A      EQU 0          -A- REGISTER ADDRESS DEFINITION.
17766 017776   ADRSA  DEF CORSZ-2    POINTER TO 2-WORD BUFFER.
00011          CMND   EQU DATA+1     MAG TAPE COMMAND CHANNEL S.C.
17767 177774   DFALT  ABS -DEFLT     - (PROGRAM ORDINAL DEFAULT).
17770 102070   HLT70  HLT 708        FINAL HALT (GOOD HALT).
17771 001677   MASK1  OCT 1677       POST RECORD READ MASK.
17772 000202   MASK2  OCT 202*       MAG TAPE STATUS MASK.
17773 000000   PROG#  NOP            PROGRAM ORDINAL COUNTER.
17774 000023   RWF    OCT 23         MT READ ONE RECORD COMMAND CODE.
17775 001501   SLORW  OCT 1501       MT SELECT 0/REWIND COMMAND CODE.
00001          SSW    EQU 1          SWITCH REG ADDRESS DEFINITION.

   THE FOLLOWING TWO WORDS MUST BE CONTIGUOUS, AND THEIR ORDER
 MUST NOT BE CHANGED.

17776 000000   S.A.   BSS 1          PROG START ADDR (IN POST REC).
17777 000000   PTR    BSS 1          MOVING PTR/DATA REC LOAD ADDR.

                      END
```

*OCT 200 TO INHIBIT PARITY CHECK

HARDWARE CONFIGURATION

SC	2000A		2116B/C		2000B	2114A/B	
10	MPX	12584-6001	PROC INT	12566-6001	A	MPX (DATA)	12584-6001
11	TTY	12531-6001	PROC INT	12566-6001	B	MPX (DATA)	12584-6001
12	TBG	02116-6119	TTY	12531-6001	A	PROC INT	12566-6001
13	RDR	12597-6001	RDR	12597-6001	B	PROC INT	12566-6001
14	DISC	12610-6001	DISC	12610-6001		MPX (PHO CONT)	12584-6001
15	DISC	12610-6002	DISC	12610-6002		MPX (PHO CONT)	12584-6001
16	optional		TBG	02116-6119		unused	
17	optional		optional			unused	

Power Fail switch up
Parity Check switch up
Disc/Drum switch down

Numerical representation

$-999 \leqslant \eta \leqslant 999$	Small integer	ΛXXXΛΛ
$-32768 \leqslant -1000$ or $1000 \leqslant 32767$	Large integer	ΛXXXXXΛΛ
$.1 \leqslant \eta \leqslant 999999.5$	Large integer or real	ΛXXXXXXXΛΛΛΛ
$\eta \leqslant .1$ or $999999.5 \leqslant \eta$	Large integer or real	ΛX.XXXXXE±eeΛΛΛ

TIMESHARE (CONT)

2000C HARDWARE CONFIGURATION

MAIN CPU 2100A/S OR 2116B/C			I/O CPU 2100A/S, 2114A/B OR 2116B/C	
SC				
10	PROC INT A	12566-6001	MPX (DATA)	12584-6001
11	PROC INT B	12566-6001	MPX (DATA)	12584-6001
12	TTY	12531-6001	PROC INT A	12566-6001
13	RDR	12597-6001	PROC INT B	12566-6001
14	FH DISC 1	12610-6001	MPX (PHO CONT)	12584-6001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12584-6001
16	TBG	12539-60001		
17	*MH DISC 1	12565/13210		
20	*MH DISC 2	12565/13210		

HIGH-SPEED 2000C HARDWARE CONFIGURATION

MAIN CPU 2100A/S OR 2116B/C			I/O CPU 2100A/S, **2114B, OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	CONSOLE	12531-6001	TBG	12539-60001
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	FH DISC 1	12610-6001	1st MPX (DATA)	12921-60001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12922-60001
16	TBG	12539-60001	2nd MPX (DATA)	12921-60002
17	*MH DISC 1	12565/13210	2nd MPX (DATA)	12921-60001
20	*MH DISC 2	12565/13210	MPX (PHO CONT)	12922-60001
21	MAG TAPE 1	13181-60070	Optional	
22	MAG TAPE 2	13181-60010		

*MH Discs can be either two 2883A's or two 7900A's, but not both.
**I/O Extender must be used with 2114B if two multiplexers are to be used in system.

2000E HARDWARE CONFIGURATION (REV. C OR LATER SOFTWARE)

SC	DEVICE	P/N
10	TTY CONSOLE	12531-6001
11	DISC 1	13210-60004
12	DISC 2	13210-60001
13	RDR	12597-6001
14	MPX (DATA)	12921-60002
15	MPX (DATA)	12921-60001
16	MPX (PHO CONT)	12922-60001
17	TBG	12539-60001
20	MAG TAPE 1 (Optional)	13181
21	MAG TAPE 2 (Optional)	13181

TIMESHARE (CONT)

2000F OPT 200/205 HARDWARE CONFIGURATION

	MAIN CPU 2100A/S ONLY		I/O CPU 2100A/S, **2114B, OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	TTY CONSOLE	12531-6001	TBG	12539-60003
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	TBG	12539-60003	1st MPX (DATA)	12921-60001
15	*MH DISC 1	13210/12565	MPX (PHO CONT)	12922-60001
16	*MH DISC 2	13210/12565	2nd MPX (DATA)	12921-60002
17	MAG TAPE 1	13181-60070	2nd MPX (DATA)	12921-60001
20	MAG TAPE 2	13181-60010	MPX (PHO CONT)	12922-60001

2000F OPT 210/215 HARDWARE CONFIGURATION

	MAIN CPU 2100A/S ONLY		I/O CPU 2100A/S, **2114B, OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	CONSOLE	12531-6001	TBG	12539-60001
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	FH DISC 1	12610-6001	1st MPX (DATA)	12921-60001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12922-60001
16	TBG	12539-60001	2nd MPX (DATA)	12921-60002
17	*MH DISC 1	12565/13210	2nd MPX (DATA)	12921-60001
20	*MH DISC 2	12565/13210	MPX (PHO CONT)	12922-60001
21	MAG TAPE 1	13181-60070	Optional	
22	MAG TAPE 2	13181-60010		

*MH Discs can be either two 2883A's or two 7900A's, but not both.
**I/O Extender must be used with 2114B if two multiplexers are to be used in system.

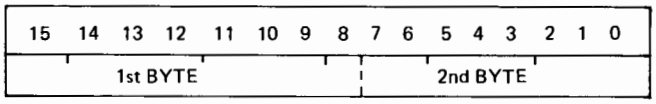
ASCII CHARACTER CODES

87 654 * 321

TELEPRINTER

	0	1	2	3	4	5	6	7
00	NULL	SOM	EOA	EOM	EOT	WRU	RU	BELL
01	FE	H.TAB	LF	V.TAB	FORM	CR	SO	SI
02	DC	X-ON	TAPE ON	X-OFF	TAPE OFF	ERROR	SYNC	LEM
03	S0	S1	S2	S3	S4	S5	S6	S7
04	SPACE	!	"	#	$	%	&	'
05	(	)	*	+	,	–	.	/
06	0	1	2	3	4	5	6	7
07	8	9	:	;	<	=	>	?
10	@	A	B	C	D	E	F	G
11	H	I	J	K	L	M	N	O
12	P	Q	R	S	T	U	V	W
13	X	Y	Z	[	\	]	↑	←
14								
15								
16								
17					ACK	ALT MODE	ESC	RO

BYTE PACKING



CNTL inhibits bit 7
SHIFT complements bit 5
Keyboard Print requires bit 6 or bit 7
Parity – even, bit 8 (ignored by HP Software)

} Teleprinter

PACKED ASCII

CHAR	OCTAL CODE 1st BYTE	OCTAL CODE 2nd BYTE	CHAR	OCTAL CODE 1st BYTE	OCTAL CODE 2nd BYTE
A	040400	000101	:	035000	000072
B	041000	000102	;	035400	000073
C	041400	000103	<	036000	000074
D	042000	000104	=	036400	000075
E	042400	000105	>	037000	000076
F	043000	000106	?	037400	000077
G	043400	000107	@	040000	000100
H	044000	000110	[	055400	000133
I	044400	000111	\	056000	000134
J	045000	000112	]	056400	000135
K	045400	000113	↑	057000	000136
L	046000	000114	←	057400	000137
M	046400	000115	ACK	036000	000174
N	047000	000116	①	036400	000175
O	047400	000117	ESC	037000	000176
P	050000	000120	DEL	037400	000177
Q	050400	000121	NULL	000000	000000
R	051000	000122	SUM	000400	000001
S	051400	000123	EOA	001000	000002
T	052000	000124	EOM	001400	000003
U	052400	000125	EOT	002000	000004
V	053000	000126	WRU	002400	000005
W	053400	000127	RU	003000	000006
X	054000	000130	BELL	003400	000007
Y	054400	000131	RE_0	004000	000010
Z	055000	000132	HT/SK	004400	000011
			LF	005000	000012
0	030000	000060	VTAB	005400	000013
1	030400	000061	FF	006000	000014
2	031000	000062	CR	006400	000015
3	031400	000063	SO	007000	000016
4	032000	000064	SI	074000	000017
5	032400	000065	DC_0	010000	000020
6	033000	000066	DC_1	010400	000021
7	033400	000067	DC_2	011000	000022
8	034000	000070	DC_3	011400	000023
9	034400	000071	DC_4	012000	000024
			ERR	012400	000025
space	020000	000040	SYNC	013000	000026
!	020400	000041	LEM	013400	000027
"	021000	000042	S_0	014000	000030
#	021400	000043	S_1	014400	000031
$	022000	000044	S_2	015000	000032
%	022400	000045	S_3	015400	000033
&	023000	000046	S_4	016000	000034
'	023400	000047	S_5	016400	000035
(	024000	000050	S_6	017000	000036
)	024400	000051	S_7	017400	000037
*	025000	000052			
+	025400	000053			
,	026000	000054			
−	026400	000055			
.	027000	000056			
/	027400	000057			

MATHEMATICAL EQUIVALENTS

$2^{\pm n}$ IN DECIMAL

2^n	n	2^{-n}		n	
1	0	1.0	65536	16	0.00001 52587 89062 5
2	1	0.5	1 31072	17	0.00000 76293 94531 25
4	2	0.25	2 62144	18	0.00000 38146 97265 625
			5 24288	19	0.00000 19073 48632 8125
8	3	0.125	10 48576	20	0.00000 09536 74316 40625
16	4	0.0625			
32	5	0.03125	20 97152	21	0.00000 04768 37158 20312 5
			41 94304	22	0.00000 02384 18579 10156 25
64	6	0.01562 5	83 88608	23	0.00000 01192 09289 55078 125
128	7	0.00781 25			
256	8	0.00390 625	167 77216	24	0.00000 00596 04644 77539 0625
			335 54432	25	0.00000 00298 02322 38769 53125
512	9	0.00195 3125	671 08864	26	0.00000 00149 01161 19384 76562 5
1024	10	0.00097 65625			
2048	11	0.00048 82812 5	1342 17728	27	0.00000 00074 50580 59692 38281 25
			2684 35456	28	0.00000 00037 25290 29846 19140 625
4096	12	0.00024 41406 25	5368 70912	29	0.00000 00018 62645 14923 09570 3125
8192	13	0.00012 20703 125			
16384	14	0.00006 10351 5625	10737 41824	30	0.00000 00009 31322 57461 54785 15625
			21474 83648	31	0.00000 00004 65661 28730 77392 57812 5
32768	15	0.00003 05175 78125	42949 67296	32	0.00000 00002 32830 64365 38696 28906 25

NUMERICAL CONVERSION

OCTAL	DECIMAL	DECIMAL	OCTAL	2's COMP
0- 7	0- 7	1	1	177777
10-17	8-15	10	12	177766
20-27	16-23	20	24	177754
30-37	24-31	40	50	177730
40-47	32-39	100	144	177634
50-57	40-47	200	310	177470
60-67	48-55	500	764	177014
70-77	56-63	1000	1750	176030
100	64	2000	3720	174040
200	128	5000	11610	166170
400	256	10000	23420	154360
1000	512	20000	47040	130740
2000	1024	32768		100000
4000	2048			
10000	4096			
20000	8192			
40000	16384			
77777	32767			

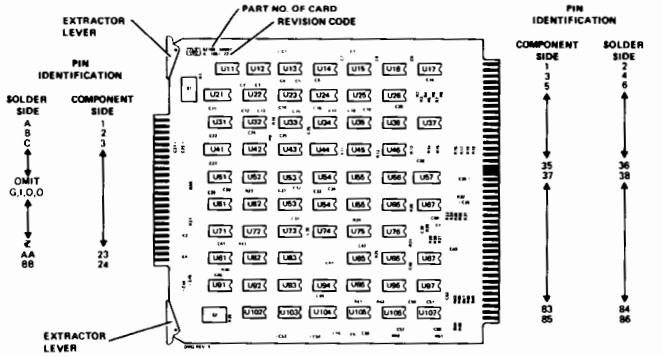
OCTAL ADDITION

0	01	02	03	04	05	06	07
1	02	03	04	05	06	07	10
2	03	04	05	06	07	10	11
3	04	05	06	07	10	11	12
4	05	06	07	10	11	12	13
5	06	07	10	11	12	13	14
6	07	10	11	12	13	14	15
7	10	11	12	13	14	15	16

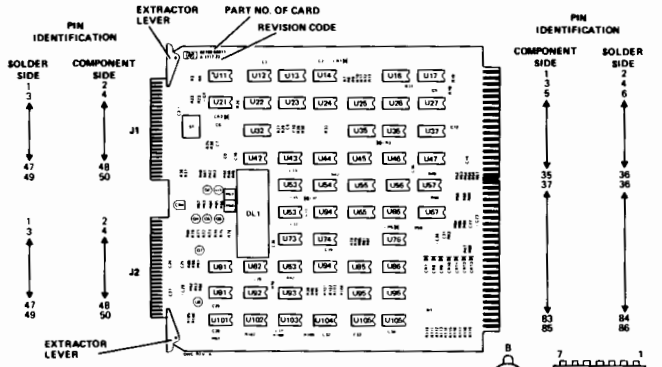
OCTAL MULTIPLICATION

1	02	03	04	05	06	07
2	04	06	10	12	14	16
3	06	11	14	17	22	25
4	10	14	20	24	30	34
5	12	17	24	31	36	43
6	14	44	30	36	44	52
7	16	35	34	43	52	61

PRINTED-CIRCUIT CARD DETAILS

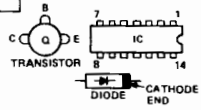


A. ONE 48-PIN EDGE-CONNECTOR



B. TWO 50-PIN EDGE CONNECTORS

NOTE: INTEGRATED CIRCUITS ARE NUMBERED IN ROW AND COLUMN ORDER.



TOP VIEWS

NOTE: ALL BOARDS ARE MARKED WITH A DATE STAMP; THIS STAMP IS UPDATED AT EACH REWORK. IF NO TROUBLE IS FOUND AN "X" IS PLACED NEXT TO THE DATE. A BOARD WITH 2 "X" 'S WILL BE REMOVED FROM THE PROGRAM.

CONTENTS PAGE

COMPUTER SPECIFICATIONS

Memory Cycle Time:	980nS
Microinstruction Execution Time:	196nS
I/O Slots in Mainframe:	14
Memory Size:	4K to 32K
Ambient Operating Temp:	0-55°C (32-131°F)
Weight:	91 pounds (41 kg) minimum 121 pounds (55 kg) maximum
Dimensions:	12" x 16.75" x 26" 30.1 cm x 42.6 cm x 66 cm

HARDWARE MANUALS

SHORT TITLE	P/N	MICROFICHE
HP 2100A I&M*	02100-90002	02100-90132
HP 2100A Diagrams	02100-90003	02100-90134
HP 2100A IPB**	02100-90004	02100-90067
HP 2100A Reference	02100-90001	
HP 2100S I&M*	02100-90162	02100-90163
HP 2100S Diagrams	02100-90164	02100-90165
HP 2100S IPB**	02100-90166	02100-90167
HP 2100S Reference	02100-90160	02100-90161

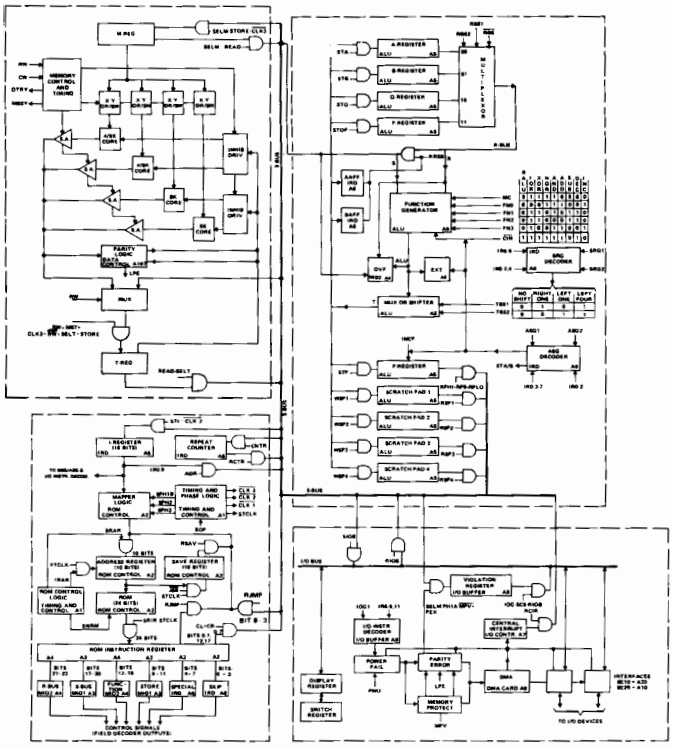
*Installation and Maintenance
**Illustrated Parts Breakdown

SOFTWARE TESTS AND DIAGNOSTICS

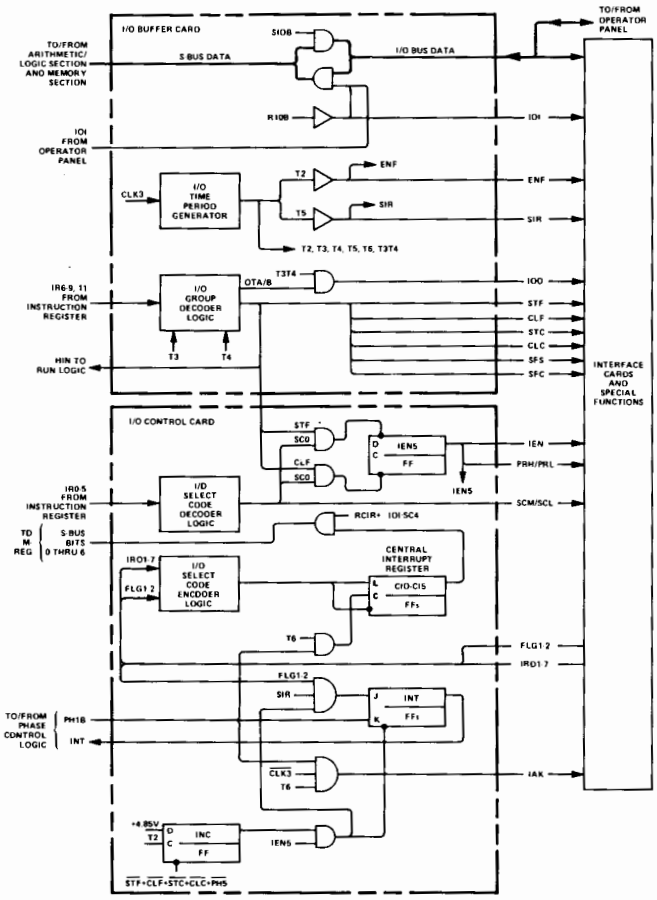
SHORT TITLE	TAPE P/N	MOD*
Low Memory Pattern Test	24193-60001	02100-90023
High Memory Pattern Test	24194-60001	02100-90023
Memory Parity Check Test	24198-60001	02100-90021
Power Fail Diagnostic	24206-6001	02100-90020
Alter-Skip Instruction Test	24208-60001	02100-90019
Mem. Ref. Instruction Test	24209-60001	02100-90018
Shift-Rotate Instruction Test	24210-60001	02100-90017
Low Memory Address Test	24211-60001	02100-90008
High Memory Address Test	24212-60001	02100-90008
Ext. Arith. Unit Test	24214-60001	02100-90007
Interrupt Test	24215-60001	02100-90025
Memory Protect Test	24222-60001	02100-90006
DMA Diagnostic	24195-60001	12578-90014
Floating Point Diagnostic	24251-60001	02100-90064
WCS Diagnostic	24284-60001	12908-90005
PROM Diagnostic	24282-60001	12909-60003

*Manual of Diagnostics

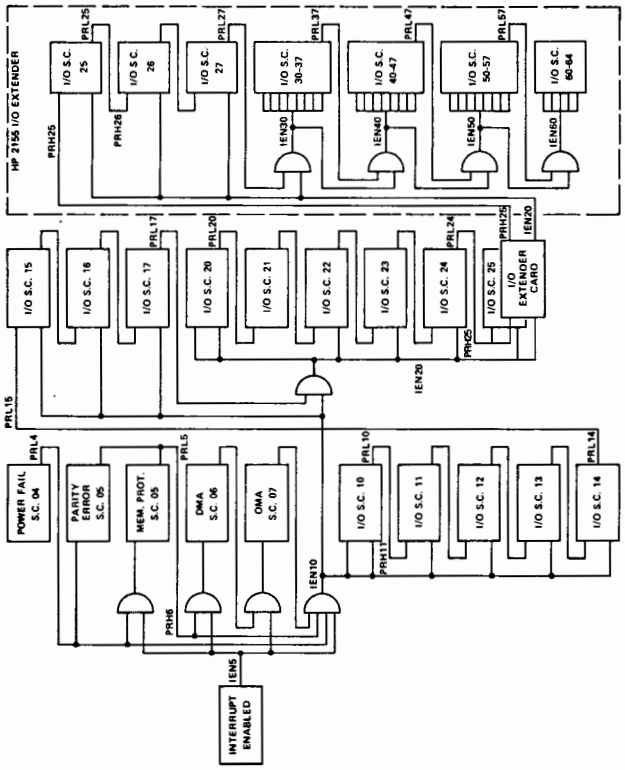
OVERALL BLOCK DIAGRAM



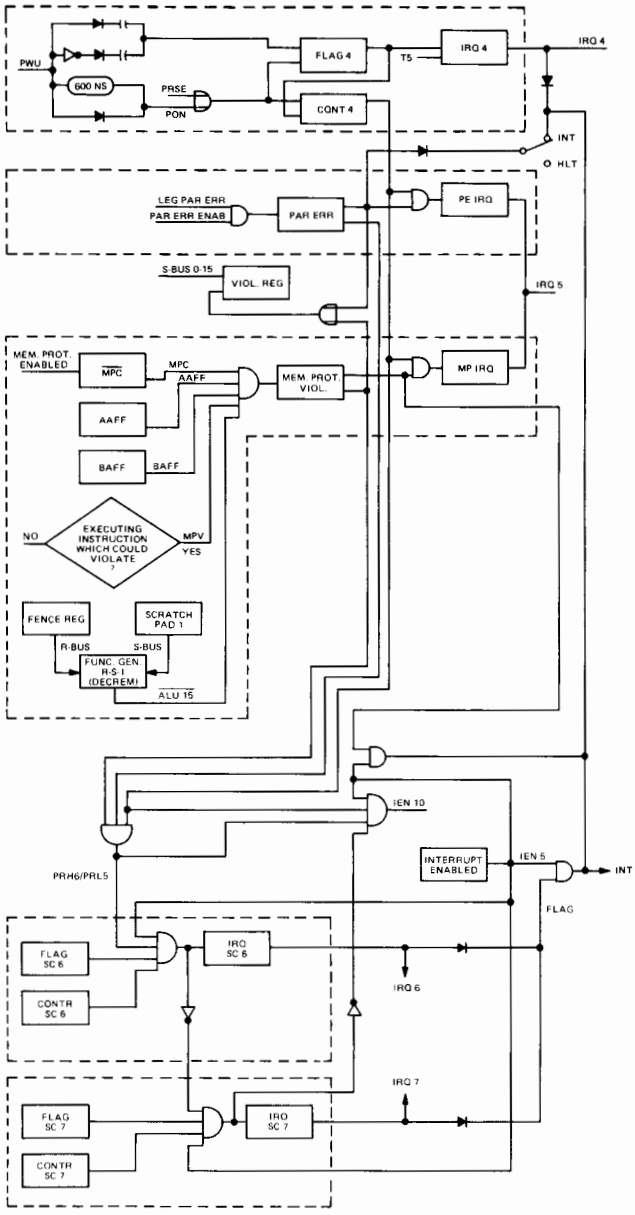
I/O SECTION FUNCTIONAL DIAGRAM



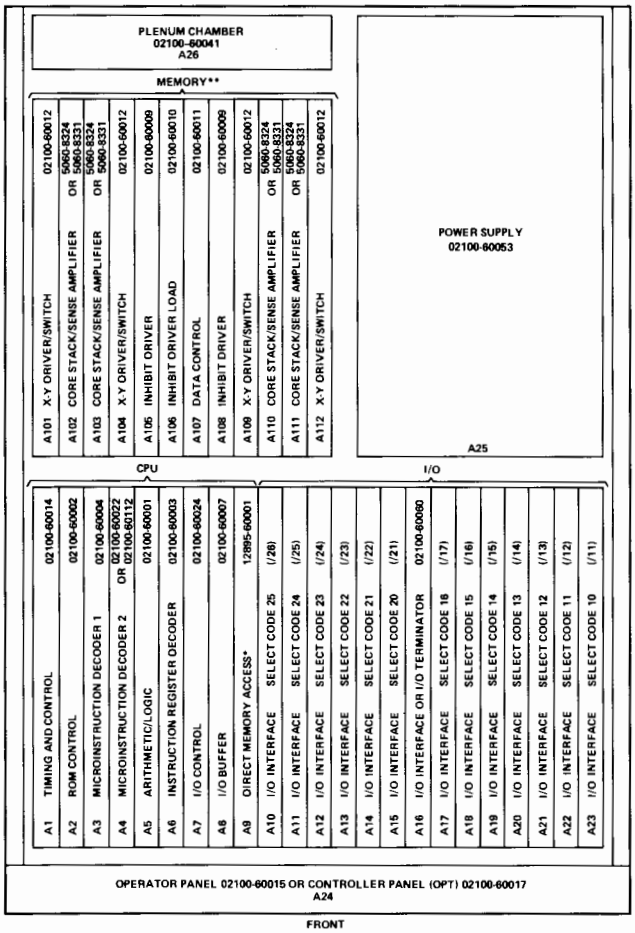
INTERRUPT PRIORITY SYSTEM BLOCK DIAGRAM



INTERRUPT PRIORITY FUNCTIONAL BLOCK



PRINTED-CIRCUIT CARD LOCATIONS

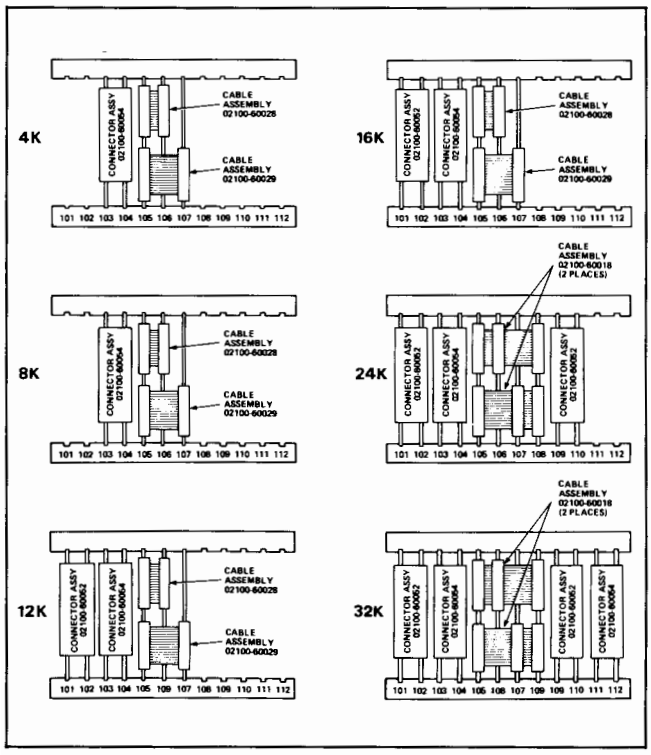


NOTES: *DIRECT MEMORY ACCESS CARD IS AN ACCESSORY TO THE COMPUTER AND IS NOT PART OF THE BASIC CONFIGURATION.

**MEMORY SECTION LOADING SHOWN IS FOR 32K MEMORY. REFER TO FIGURE 4-2 FOR OTHER MEMORY SIZE LOADING.

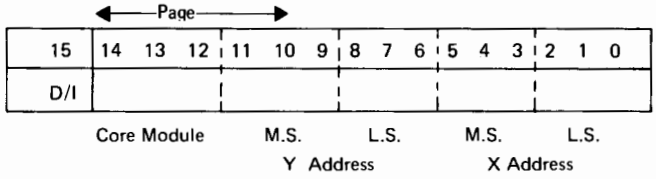
2133-3C

MEMORY CARD CAGE LOADING



MEMORY PAGING

M-REGISTER



The Memory Reference instruction provides 10 address bits (0-9). These bits are combined with the page bits 10-14 of the M-register to give the 15 bit operand address. Bit 10 in the Memory Reference instruction holds the M-register (10-14) for current page (bit 10=1) or clears M-register (10-14) for zero page (bit 10=0).

			$\overline{14}$		14	
			$\overline{13}$ (4-8K)	13 (12-16K)	$\overline{13}$ (20-24K)	13 (28-32K)
12	11	10	Page 7	Page 15	Page 23	Page 31
	11	$\overline{10}$	Page 6	Page 14	Page 22	Page 30
	$\overline{11}$	10	Page 5	Page 13	Page 21	Page 29
	$\overline{11}$	$\overline{10}$	Page 4	Page 12	Page 20	Page 28
$\overline{12}$	11	10	Page 3	Page 11	Page 19	Page 27
	11	$\overline{10}$	Page 2	Page 10	Page 18	Page 26
	$\overline{11}$	10	Page 1	Page 9	Page 17	Page 25
	$\overline{11}$	$\overline{10}$	Page 0	Page 8	Page 16	Page 24
			(0-4K)	(8-12K)	(16-20K)	(24-28K)

NON-EXISTING ROM JUMPERS

NER JUMPER POSITIONS

MODULE #	0	1	2	3
RAR 9	0	0	1	1
RAR 8	0	1	0	1

INSTALLED	W6	W3	W2	W1	W4	W5
MOD 0	H-L	F-E	D-K	B-A	IN	OUT
MOD 0,1	H-L	–	–	B-A	IN	OUT
MOD 0,2	–	F-E	D-K	–	OUT	IN
MOD 0,3	H-G	F-E	D-C	A-B	IN	IN
MOD 0,1,2	–	E-F	D-A	–	IN	OUT
MOD 0,1,3	H-G	–	–	B-A	IN	OUT
MOD 0,2,3	–	F-E	D-C	–	OUT	IN
MOD 0,1,2,3	–	–	–	–	IN	OUT

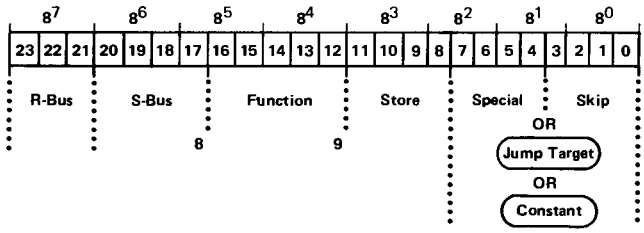
X-LINE AND Y-LINE DECOOERS

MODULE ADDRESSED	Y MSD DECODER		Y LSD DECODER		X MSD DECODER		X LSD DECODER	
	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE	READOUT	WRITE
0	A104U24	A104U23	A104U22	A104U21	A104U18	A104U17	A104U20	A104U19
1	A104U24	A104U23	A104U22	A104U21	A104U17	A104U18	A104U19	A104U20
2	A101U24	A101U23	A101U22	A101U21	A101U18	A101U17	A101U20	A101U19
3	A101U24	A101U23	A101U22	A101U21	A101U17	A101U18	A101U19	A101U20
4	A109U24	A109U23	A109U22	A109U21	A109U18	A109U17	A109U20	A109U19
5	A109U24	A109U23	A109U22	A109U21	A109U17	A109U18	A109U19	A109U20
6	A112U24	A112U23	A112U22	A112U21	A112U18	A112U17	A112U20	A112U19
7	A112U24	A112U23	A112U22	A112U21	A112U17	A112U18	A112U19	A112U20

NOTES:

1. The module addressed is indicated by bits MR14, MR13, and MR12.
2. The Y MSD is indicated by bits MR11, MR10, and MR9.
3. The Y LSD is indicated by bits MR8, MR7, and MR6.
4. The X MSD is indicated by bits MR5, MR4, and MR3.
5. The X LSD is indicated by bits MR2, MR1, and MR0.

MICROINSTRUCTION WORD FORMAT



MICROINSTRUCTION CODING

CODE (5-Bit / 4-Bit / 3-Bit Field)	R-Bus Field 3 Bits	S-Bus Field 4 Bits	Function Field 5 Bits	Store Field 4 Bits	Special Field 4 Bits	Skip Field 4 Bits
1 1 1 1 1	NOP	NOP	IOR	NOP	NOP	NOP
1 1 1 1 0	CQ	P	SOV	A	RW	UNC
1 1 1 0 1	AAB	CL	CLO	B	IOG1	EOP
1 1 1 0 0	CAB	CR	SFLG	AAB	CW	NAAB
1 1 0 1 1	F	S1	CFLG	CAB	ASG2	AAB
1 1 0 1 0	Q	S2	LWF	Q	ASG1	NMPV
1 1 0 0 1	B	S3	***	F	ECYN	CTR
1 1 0 0 0	A	S4	ARS	P	ECYZ	CTRI
1 0 1 1 1		COND	CRS	S1	LEP	TBZ
1 0 1 1 0		ADR	LGS	S2	AAB	FLG
1 0 1 0 1		CNTR	RSB	S3	SRG2	OVF
1 0 1 0 0		RRS	CJMP	S4	SRG1	COUT
1 0 0 1 1		M	JMP	IR	CNTR	NEG
1 0 0 1 0		T	JMP	T	R1	ODD
1 0 0 0 1		IOI	JSB	M	L1	RPT
1 0 0 0 0		CIR	JSB	IOO	RSS	ICTR
0 1 1 1 1			**			
0 1 1 1 0			XOR			
0 1 1 0 1			NOR			
0 1 1 0 0			AND			
0 1 0 1 1			ADD			
0 1 0 1 0			ADDO			
0 1 0 0 1			INC			
0 1 0 0 0			INCO			
0 0 1 1 1			**			
0 0 1 1 0			DEC			
0 0 1 0 1			SUB			
0 0 1 0 0			DIV			
0 0 0 1 1			MPY			
0 0 0 1 0			PIA			

**Undefined codes
***CJMP in later machines (A4 part No. 02100-60022)

MICROINSTRUCTION DEFINITIONS

R-BUS

A – A onto R-bus

B – B onto R-bus

AAB – A/B onto R-bus if addressed. If not addressed and COND is not in the S-bus then A-reg to R-bus. If COND in S-bus then zeroes to R-bus.

CAB – A/B (IR11=0/1) onto R-bus

CQ – Not to be used

F – F-reg onto R-bus

NOP – Zeroes onto R-bus

Q – Q-reg onto R-bus

S-BUS

ADR – Operand Address to S-bus
IR10=0,Zero page, then IR0-9 to S-bus
IR10=1,current page, then IR0-9 to S-bus
and P 10-15 to S-bus

CIR – Central Interrupt Register onto S-bus

CL – RIR0-7 onto S-bus 8-15

CNTR – CNTR 0-4 to S-bus 0-4
bit 4=1 if carryout from last increment

COND – A or B addressed then R-bus onto S-bus
A or B not addressed then T-reg onto S-bus and CPU freeze until DTRY

CR – RIR 0-7 onto S-bus 0-7

IOI – I/O bus onto S-bus

M – M-reg onto S-bus

NOP – Zeroes onto S-bus

P – P-reg onto S-bus

RRS – R-bus onto S-bus

SP1 – SP1 onto S-bus

SP2 – SP2 onto S-bus

SP3 – SP3 onto S-bus

SP4 – SP4 onto S-bus

T – T-reg onto S-bus. CPU freeze until DTRY.

MICROINSTRUCTION DEFINITIONS (CONT)

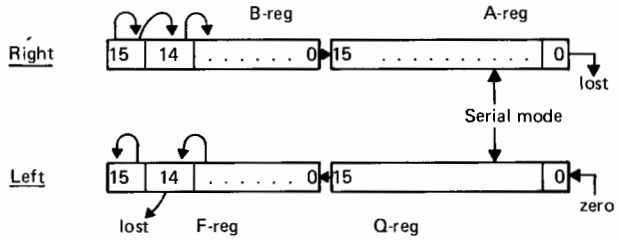
FUNCTION

ADD – Sum of R-bus and S-bus onto ALU-bus

ADDO – Sum of R-bus and S-bus onto ALU-bus
Enable setting of overflow
Enable setting of extend if MRG or ASG instruction

AND – AND of R-bus and S-bus, result to ALU-bus

ARS – 32 bit Arithmetic Shift, Direction (L1 or R1) in Special Field. On Left Shifts overflow set if ALU15=ALU14. IOR to Function Generator.

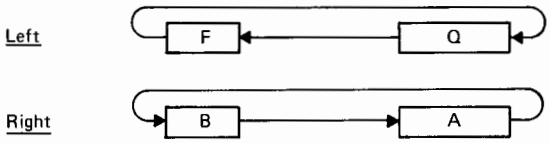


CFLG – Clear CPU Flag FF. IOR to Function Generator

CJMP – Conditional Jump. If in Single Cycle mode, halts machine but does not execute JMP.
If in Run mode and Front Panel Halt or Interrupt is detected, then JMP is executed, else NOP.

CLO – Clear Overflow, IOR to Function Generator.

CRS – 32 bit circular Rotate, Direction (L1 or R1) in Special Field, IOR to Function Generator.



DEC – R + S, S-bus is complemented and added to R-bus. R-bus data is decremented if NOP in S-bus Field.

DIV – Divide step. Normally used in a repeat loop as part of a divide algorithm. DIV subtracts the S-bus from the R-bus (two's complement) and checks the COUT (Carry Out) signal for a store decision. If COUT is "1", the result of the subtraction is left-shifted one place and stored in a register (normally the F-register). If COUT is "0", the existing contents of the F-register are shifted left one place internally in the F-register; the subtraction result is not stored. In either case, the Q-register also shifts left one place, COUT is shifted into bit 0 of the Q-register, bit 15 of the Q-register shifts into bit 0 of the F-register, and bit 15 of the F-register is lost. A valid divide step requires L1 in

MICROINSTRUCTION DEFINITIONS (CONT)

the Special field, F in the R-bus and Store fields, and an S-bus register (normally a Scratch Pad) specified in the S-bus field. DIV requires two CPU clock cycles to execute.

(Refer to Hardware microinstruction definitions and microprogram listing)

INC – R+S+1 onto ALU-bus

INCO – R+S+1, Enable overflow, Enable Extend if MRG or ASG instruction.

IOR – Inclusive OR of R-bus and S-bus

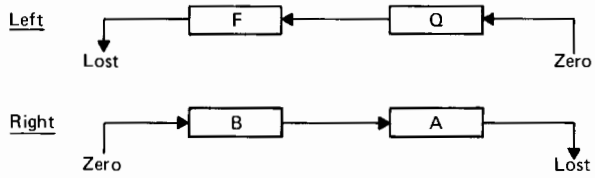
JMP – Target address;

RIR 0-7 ⟶ RAR 0-7
RIR 17 ⟶ RAR 8
RIR 12 ⟶ RAR 9

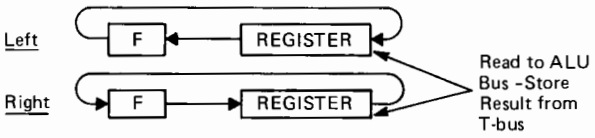
There are two JMP codes (22,23)
P in the S-bus Field is inhibited
JMP to MODULE 0 – P in S-bus, JMP (22)
MODULE 1 – NOP in S-bus, JMP (22)
MODULE 2 – P in S-bus, JMP (23)
MODULE 3 – NOP in S-bus, JMP (23)

JSB – Jump Subroutine, sets JSB FF to lock return address in Save Register. JSB FF reset by RSB or EOP.

LGS – 32 bit logical shift, Direction (R1 or L1) in Special Field, IOR to Function Generator.



LWF – If L1 in Special, Flag to LSI of shifter, ALU15 to Flag.
If R1 in Special, Flag to ALX16 of shifter, ALU 0 to Flag.



MPY – If A Register bit 0=1, sum of R and S onto ALU-bus.
If A Register bit 0=0, R-bus onto ALU-bus.
A register shifted right one in serial mode. A register bit 0 is lost, ALU bit 0 is shifted into A register bit 15.
(Refer to microprogram listing and hardware microinstruction definitions)

MICROINSTRUCTION DEFINITIONS (CONT)

NOR – "NOR" of the R-bus and S-bus. If Zeroes on one bus, result is complement of data on the other bus.

PIA – Set Phase 1A, used for diagnostics only.

RFE – Rotate Flag and Extend register contents
R-bus to ALU-bus

RFI – Not to be used

RSB – Return from ROM subroutine.
Save register to RAR.
NOP if not in subroutine

SFLG – Set CPU Flag FF, IOR to Function Generator.

SOV – Set overflow. IOR to Function Generator.

SUB – Two's complement subtract, R+S+1.
Sum of R-bus, complement of S-bus, and carry in.

XOR – Exclusive OR of R-bus and S-bus

STORE

A – T-bus stored in A-register

B – T-bus stored in B-register

AAB – Store T-bus in A-register if AAFF.
Store T-bus in B register if BAFF.
NOP if not A or B addressable.

CAB – T-bus stored into A/B if IR11=0/1

F – T-bus stored in F-register

IOO – S-bus read onto I/O bus

IR – S-bus stored into Instruction Register

M – S-bus stored in M, also in Violation Register if PHIA · NMPV

NOP – No store

P – T-bus stored in P-register

Q – T-bus stored in Q-register

S1 – T-bus stored in Scratch Pad 1

S2 – T-bus stored in Scratch Pad 2

S3 – T-bus stored in Scratch Pad 3

S4 – T-bus stored in Scratch Pad 4

T – S-bus stored in T-register

MICROINSTRUCTION DEFINITIONS (CONT)

SPECIAL

AAB – Clocks A and B addressable FF's.
AAFF set if T-bus bits 1-14=0, ALU bit 0=0.
BAFF set if T-bus bits 1-14=0, ALU bit 1=1.
Both cleared on any other condition.

ASG1 – Enables decoder which executes ASG instructions specified by Instruction register bits 0, 3-7. Microprogram reads register to ALU bus.

ASG2 – Enables decoder which executes ASG instructions specified by Instruction register bits 0,1,2. Microprogram reads register to ALU bus.

CNTR – S-bus bits 0-3 stored in counter. Bit 4 of counter is cleared.

CW – Clear Write memory cycle. CPU freeze until T6. The CW command is sent to memory only if the next microinstruction is skipped.

ECYN – Set PCRY FF if T-bus = 0.
Increment P at EOP · PH3

ECYZ – Set PCRY FF if T-bus = 0.
Increment P at EOP · PH3

IOG1 – Enables I/O decoder. CPU freeze until T2, decoder then executes I/O instructions specified by Instruction register.

L1 – See ARS, CRS, LGS in Function Field. If used with IOR in Function Field then left one to shifter, ALU 15 is lost, ALU 0-14 to T-bus 1-15, zero to T-bus 0.

LEP – Legal entry point. Prevents illegal entry into an Extended Arithmetic Group instruction microprogram through an incorrect MAC code. Causes the microprocessor to execute NOPs until LEP is detected, or until EOP is detected in the Skip field. LEP cannot be used for anything other than enabling entry points to the 2100 Extender Arithmetic Group instructions, coded only in module 0. LEP is never skipped.

NOP – No operation

R1 – See ARS, CRS, LGS in Function Field. If used with IOR in Function Field then right one to shifter, ALU0 lost, ALU15-1 to T-bus 14-0, T-bus 15=0.

RSS – Reverse skip sense of Skip Field microinstruction.

RW – Read Write memory cycle. CPU freeze until T6.

Clocks A and B addressable FF's.
AAFF set if T-bus bits 1-14=0, ALU0=0.
BAFF set if T-bus bits 1-14=0, ALU0=1.
Both cleared on any other condition

SRG1 – Enables SRG decoder, executes SRG instructions specified by Instruction register bits 6-9.
Sets SRGFF which enables CLE and SLA instructions during next cycle.

MICROINSTRUCTION DEFINITIONS (CONT)

SRG2 – Enables SRG decoder, executes SRG instructions specified by Instruction register bits 0-2,4.

SKIP

AAB – Skips the next microinstruction if either the A addressable FF or B Addressable FF is set.

COUT – Skips the next microinstruction if there is a carry-out(COUT) signal from the ALU.

CTR – Skips the next microinstruction if counter bits 0 through 3 are all "1"s (octal 17). Ignores bit 4.

CTRI – Skips the next microinstruction if counter bits 0 through 3 are all "1"s (octal 17). Ignores bit 4. Increments counter after testing.

EOP – End of phase. Sets the correct next phase flip-flop and executes a hardware jump through the mapper to the address which begins the next phase. EOP cannot be skipped.

FLG – Skips the next microinstruction if the CPU Flag flip-flop is set.

ICTR – Increments the counter.

NAAB – Skips the next microinstruction if T-bus bits 1 through 14 are not all-zero. Normally used to detect addressable A/B.

NEG – Skips the next microinstruction if the ALU output is negative (bit 15 is a "1").

NMPV – Skips the next microinstruction if memory protect is disabled and AAF and BAF are both clear, or if memory protect is enabled, AAF and BAF are both clear, and no violation is detected. If either AAF or BAF is set, no skip will occur.

NOP – No operation.

ODD – Skips the next microinstruction if the ALU output is odd (bit 0 is a "1").

OVF – Skips the next microinstruction if the Overflow flip-flop is set.

RPT – Causes the next microinstruction to be repeated until its skip condition is met. The next microinstruction cannot contain TBZ or RSS, TBZ; also, it cannot contain an add-type function (ADD, INC, etc.) if the Skip field contains NEG or ODD (with or without RSS in the Special field).

TBZ – Skips the next microinstruction if the T-bus contains all "0"s.

UNC – Skips the next microinstruction unconditionally.

CONDITIONAL MICROINSTRUCTIONS

The execution of some microinstructions is dependent upon status signals from I/O or memory. If the necessary conditions are not satisfied the CPU freezes (suspends execution of the microprogram by inhibiting CLK, $\overline{CLK1}$, $\overline{CLK2}$, STCLK) until the necessary status signal is present.

Inhibit clocks if:

MICROMNEMONIC	FIELD	FREEZE CONDITION
RW	SPECIAL	$\overline{T6}$
CW	SPECIAL	$\overline{T6}$
T	S-BUS	$\overline{DTRY}$
COND	S-BUS	$\overline{DTRY} \cdot \overline{ABFF}$
M	STORE	MBSY
IOG1	SPECIAL	$\overline{T2}$
DIV	FUNCTION	DT (196 nS Freeze)

Other Freeze conditions

PH5 – 1 memory cycle freeze during DMA transfer
PEX – 196 nS Freeze after Parity Error occurs
HT6 – 980 nS Freeze after Memory Protect Violation or Parity Error.

ROM SKIPS

A ROM SKIP CONDITION SATISFIED, results in the nulling of the next instruction. To null the instruction, the decoding of the STORE, SPECIAL, and SKIP fields is inhibited. The decoding of some functions is also inhibited. (JMP, JSB, MPY, SFLG, etc.)

The sequence of RAR and RIR contents in a microprogram is the same whether an instruction is skipped or not.

EOP and LEP can never be skipped.

ROM JUMPS

The ROM continues execution at the JMP target address.

Target Address (10 Bits) =

Bits 0-7 of RIR (SKIP and SPECIAL Fields) become RAR bits 0-7
Bit 17 of RIR (LSB of SBUS Field) becomes RAR bit 8
Bit 12 of RIR (LSB of FUNCTION Field) becomes RAR bit 9

P micro-op in the SBUS field is inhibited.

There are two JMP codes (22 &23)

JSB	(20 & 21)
CJMP	(24 & 31)

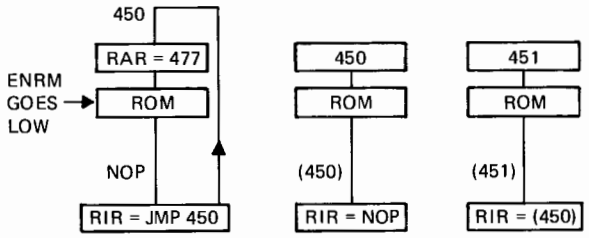
MICRO JMP EXECUTION

When microinstructions containing JMP, CJMP or JSB are executed ENRM goes low and output from ROM is all ones. We NOP thru the address following the JMP. (Execution really takes 2 ROM cycles).

For example:

```
476  - - JMP    - 450
477  A - IOR B  - EOP
```

RAR	RIR
476	(475)
477	(476)
450	NOP
451	(450)



I/O GROUP DECODER

INSTRUCTION	SIGNAL(S)	SOURCE	DESTINATION	TIME	COMMENTS
CLF(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	CLF	A8-51	*-7	T4	Clear Flag
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
STF(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	STF	A8-49	*-9	T3	Set Flag
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
SFC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	SFC	A8-52	*-5	T3-T6	Skip if Flag Clear
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
SFS(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	SFS	A8-59	*-25	T3-T6	Skip if Flag Set
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
STO	STF	A8-49	A4-73	T3	Set Overflow
	SC01	A7-49	A4-71	T3-T6	
CLO	CLF	A8-51	A4-76	T4	Clear Overflow
	SC01	A7-49	A4-71	T3-T6	
SOC	SFC	A8-52	A4-70	T3-T6	Skip if Overflow Clear
	SC01	A7-49	A4-71	T3-T6	
SOS	SFS	A8-59	A4-72	T3-T6	Skip if Overflow Set
	SC01	A7-49	A4-71	T3-T6	
HLT	HIN	A8-50	A1-65 A24-74	T3	Program Halt
STC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	STC	A8-55	*-22	T4	Set Control
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
CLC(xy)	IOG	A8-46	*-15	T3-T6	Input/Output Group
	CLC	A8-66	*-21	T4	Clear Control
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	
OTA/B	IOG	A8-46	*-15	T3-T6	Input/Output Group
	IOO	A8-78	*-16,34	T3-T4	Enable I/O Bus Data to Interface Card
	SCM(x)	A7	*-14,37	T3-T6	I/O Select Code
	SCL(y)	A7	*-16,34	T3-T6	

* Signals routed to all interface card slots.

ASG1 DECODER

INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
CLE	–	–	A6(internal)	Clears EXTEND FF
CME	–	–	A6(internal)	Complements EXTEND FF
CCE	–	–	A6(internal)	Sets EXTEND FF
†SEZ	If EXTEND FF	0	A6(internal)	
	Then SCRY	1	A6-28	Sets increment P-register logic
†SL*	If ALU0	0	A5-58	Select register, bit 0
	Then SCRY	1	A6-28	Sets increment P-register logic
†SS*	If ALU15	0	A5-21	Select register, bit 15
	Then SCRY	1	A6-28	Sets increment P-register logic

NOTES: † RSS (I-register, bit 0 = 1) reverses condition for skip.
* equals user choice of A- or B-register.

ASG2 DECODER

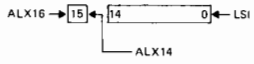
INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
IN*	$\overline{CIN}$	0	A6-84	Carry in to ALU Function Generator
†SZ*	If TBZ	1	A5-25	T-bus = all 0's
	Then SCRY	1	A6-28	Sets increment P-register logic

NOTES: † RSS (I-register, bit 0 = 1) reverses condition for skip.
* equals user choice of A- or B-register.

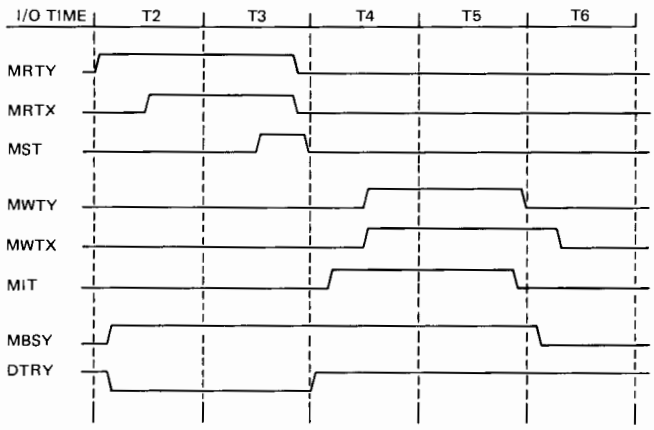
SRG DECODER

INSTRUCTION	SIGNAL(S)	LEVEL	SOURCE	COMMENTS
*LS	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then ALX14	1	A6-3	back in bit 15
*RS	SR1	1	A6-72	Shift right 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then ALX16	1	A6-17	back in bit 15
R*L	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then LSI	1	A6-20	in bit 0
R*R	SR1	1	A6-72	Shift right 1
	If ALU0	1	A5-58	Puts bit 0 content
	Then ALX16	1	A6-17	in bit 15
*LR	ARSS	0	A6-25	Right Shift A- or B-register
ER*	SR1	1	A6-72	Shift right 1
	If EXTEND FF	1	A6(internal)	Puts extend bit
	Then ALX16	1	A6-17	in bit 15
	If ALU0	1	A5-58	Puts bit 0 content
	Then EXTEND FF	1	A6(internal)	in EXTEND FF
EL*	SL1	1	A6-71	Shift left 1
	If ALU15	1	A5-21	Puts bit 15 content
	Then EXTEND FF	1	A6(internal)	in EXTEND FF
	If EXTEND FF	1	A6(internal)	Puts extend bit
	Then LSI	1	A6-20	in bit 0
*LF	$\overline{SL4}$	0	A6-50	Shift left 4
SL* (note 1)	If ALU0	0	A5-58	Least sig. bit = 0
	Then SCRY	1	A6-28	Set P-register increment logic
CLE (note 1)	–	–	A6(internal)	Clears EXTEND FF

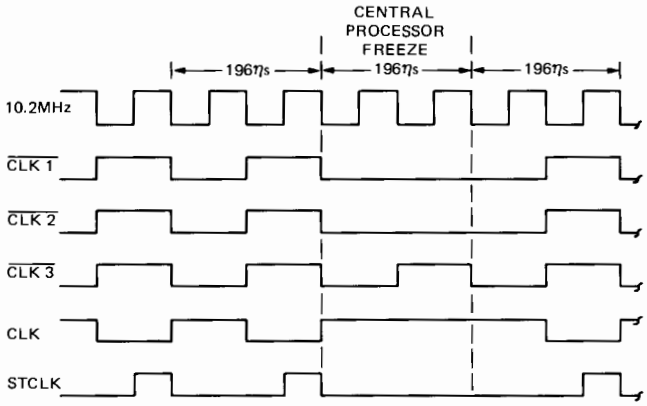
NOTES: 1. SL* and CLE is decoded after any SRG1 instruction and before any SRG2 instruction.
2. * equals users choice of A- or B-register.



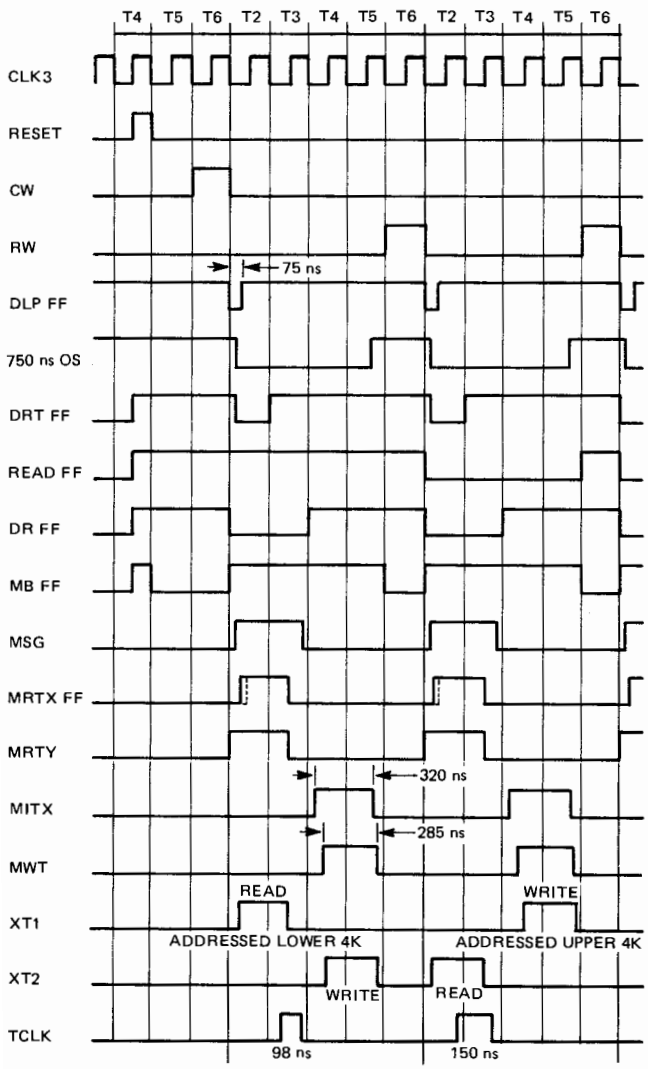
MEMORY SECTION TIMING DIAGRAM



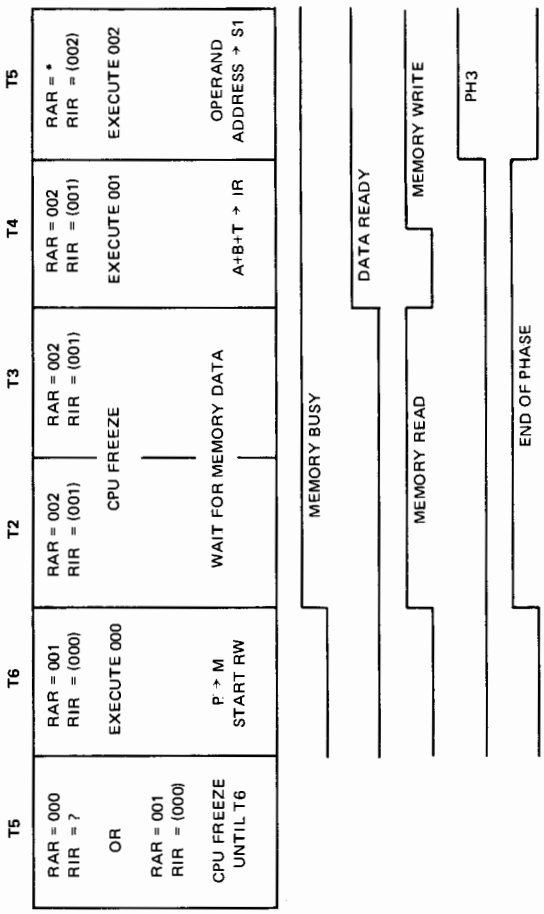
CENTRAL PROCESSOR TIMING DIAGRAM



DATA CONTROL CARD (A107) SIGNALS

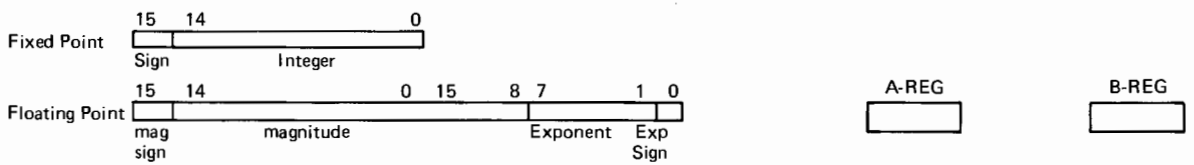


PH1A, NORMAL FETCH PHASE



* STARTING ADDRESS OF NEXT PHASE MICROPROGRAM

DATA FORMAT



INSTRUCTION:	ADD	SUBTRACT	MULTIPLY	DIVIDE	FIX	FLOAT
PURPOSE:	to add two floating point numbers, x and y	to subtract the floating point number y from the floating point number x	to multiply two floating point numbers, x and y	to divide the floating point number x by the floating point number y	to convert the floating point number x to integer format	to convert the integer i to floating point format
MACHINE CODE:	105000B	105020B	105040B	105060B	105100B	105120B
CALLING SEQUENCE:	FAD DEF Y[,I]	FSB DEF Y[,I]	FMP DEF Y[,I]	FDV DEF Y[,I]	FIX	FLT (i is assumed to be in the A register)
		(X is assumed to be in the A, B registers)				
ASSEMBLY LANGUAGE:	FAD Y	FSB Y	FMP Y	FDV Y	FIX	FLT (i is assumed to be in the A register)
		(X is assumed to be in the A, B registers)				

INSTRUCTION:	ADD	SUBTRACT	MULTIPLY	DIVIDE	FIX	FLOAT
RETURN:	Floating point result is left in the A, B registers				Integer result is left in the A register. Any fractional part is truncated. The content of the B register is meaningless.	Floating point result is left in the A,B registers
MINIMUM EXECUTION TIME: (including Fetch)	23.52 μsec	24.50 μsec	33.32 μsec	51.94 μsec	5.88 μsec	9.80 μsec
MAXIMUM EXECUTION TIME: (including Fetch)	59.78 μsec	60.76 μsec	41.16 μsec	55.86 μsec	8.82 μsec	24.50 μsec
EXECUTION TIME FOR EACH LEVEL OF INDIRECT:	.98 μsec	.98 μsec	.98 μsec	.98 μsec	– – –	– – –
ERROR CONDITION:	If the result is outside the range of representable floating point numbers, $[-2^{127}, 2^{127}(1-2^{-23})]$, the overflow flag is set and the result $2^{128}(1-2^{-23})$ is returned. If an underflow occurs, (result within the range $[-2^{-129}(1+2^{-22}), 2^{-129}]$), the overflow flag is set and the result 0 is returned.				If the floating point number is $\geq 2^{15}$, the integer 32767 (077777B) is returned and the overflow flag is set. If the floating point number is ≤ 0, the integer 0 is returned.	None

DIAGNOSTIC OPERATING PROCEDURES

The order the diagnostics should be run is only critical for the basic instruction groups. Run them in this order – MRG, ASG, SRG, EAG.

MEMORY REFERENCE INSTRUCTION TEST 24209-60001

1. Load tape using ABL
2. S.A. = 100_8, SW Reg. =0
3. RUN
4. Halts on errors
   a. Refer to listing
5. Switch Options:
   Bit 15 – Halt at end of current pass.

ALTER-SKIP INSTRUCTION TEST 24208-60001

1. Load tape using ABL
2. S.A. = 100_8, SW Reg. =0
3. RUN
4. Halts on errors
   a. RUN; Halt 102000
   b. A-Register contains binary code of failing instruction
5. Switch Options:
   a. Bit 0 – Loop on failing instruction. Halt 76 prior to execution
   b. Bit 15 – Halt at end of current pass

SHIFT-ROTATE INSTRUCTION TEST 24210-60001

1. Load tape using ABL
2. S.A. = 100_8, SW Reg. =0
3. RUN
4. Halts on errors
   a. RUN; Halt 102000
   b. A-Register contains binary code of failing instruction
5. Switch Options:
   Bit 0 – Loop on failing instruction. Halt 76 prior to execution

   Bit 15 – Halt at end of current pass

EXTENDED ARITHMETIC UNIT TEST 24214-60001

1. If TTY to be used load and configure S.I.O. driver
2. Load diagnostic tape
3. S.A. = 100_8, SW Reg. =0
4. RUN
5. Halts or prints message on errors
6. Switch Options:
   Bit 0 – Must be ON for other options to be implemented.
   Bit 1 – No TTY
   Bit 2-5 – Not used
   Bit 6 – Suppress number generator at beginning of each test
   Bit 7 – Suppress indirect addressing
   Bit 8 – Repeat current test with new data (SW 6 off)
   Bit 9 – Break out of any test if error found
   Bit 10 – Suppress non-error messages
   Bit 11 – Suppress error messages
   Bit 12 – HLT 77 at end of pass
   Bit 13 – Repeat test with same data
   Bit 14 – Suppress error halts
   Bit 15 – HLT 76 at end of test

DIAGNDSTIC OPERATING PROCEDURES (CONT)

INTERRUPT TEST 24215-60001

1. If TTY to be used, load and configure S.I.O. driver
2. Load diagnostic tape
3. S.A. = 100_8
4. If no TTY skip to step 5

    a. SW Reg. = 0
    b. RUN
    c. TTY prints "2100A INTP. TEST?"
    d. Set SW Reg.=3000_8
    e. Enter Select Codes to be tested from keyboard. Terminate input by entering "00" followed by CR,LF.
    f. Errors are printed on TTY
    g. No. of passes printed if SW 10 cleared and immediately set again.
    h. See Switch Options

5. No TTY then:

    a. SW Reg. =0
    b. RUN; HLT 107000
    c. Set SW Reg. 0-5 = select code to be tested
    d. RUN; HLT 107001
    e. Repeat steps 5.c.&d. for each select code to be tested
    f. Terminate input by setting SW Reg. =0
    g. RUN; HLT 107077
    h. SW Reg. = 041000_8
    i. Halt on errors
    j. No. of passes displayed in B & A Reg. when SW 9 is cleared and HLT 7 executed.

6. Switch Options:

    Bit 0-5 — select code to be tested (during initial part of diag.)
    Bit 8-6 — Not used
    Bit 9 — Suppress halt at end of pass
    Bit 10 — Suppress message at end of pass
    Bit 11 — Suppress error halts
    Bit 12 — Suppress error message
    Bit 13 — Suppress central Interrupt test
    Bit 14 — No TTY
    Bit 15 — Enter new slot parameters

DMA DIAGNOSTIC 24195-60001

1. If a 16 bit register card is available, install it in the slot to be tested. A 24-pin shorting connector with pin 22 and 23 connected together must be installed on the register card. If a register card is not used the test may be run using TTY card, but only 8 bits of data will be tested.
2. Load and configure TTY S.I.O. driver
3. Load diagnostic tape
4. S.A. = 2; SW Reg. = Select code of register card or TTY card and bit 6 if no TTY available.
5. INT & EXT PRESET
6. RUN; HLT 107076
7. SW Reg. = 040000 if register card used or
   = 040400 if TTY card used
8. RUN; HLT 107077
9. S.A. =100; SW Reg. =0

DIAGNOSTIC OPERATING PROCEDURES (CONT)

10. RUN; HLT 102027
11. INT & EXT PRESET
12. RUN
13. Halts on errors (except as in step 10); prints error if TTY is used
14. If additional I/O slots are to be tested, repeat from step 9 and refer to switch options before running.
15. Switch Options:
    - Bit 0 – Override internal SW Reg. & use ext SW Reg. options
    - Bit 1-5 – Not used
    - Bit 6 – Halt (103013) at start to allow change of select code
    - Bit 7 – Short test
    - Bit 8 – TTY to be used in test
    - Bit 9 – Omit PRESET test
    - Bit 10 – Suppress non-error messages
    - Bit 11 – Suppress error messages
    - Bit 12 – Halt (102077) after complete cycle
    - Bit 13 – Loop on current test
    - Bit 14 – Suppress error halts
    - Bit 15 – Not used

LOW MEMORY ADDRESS TEST 24211-60001

1. Load diag. tape
2. Set P.E. Switch (A8) to HALT
3. S.A. = 100; SW Reg. =0
4. INT. & EXT PRESET
5. RUN; HALT 102000
6. SW Reg. = 144_8 (1st address to be tested)
7. RUN; Halt 102001
8. SW Reg. = ABL-1 (last adr. to be tested)
9. RUN
10. Halts (102077) on errors. A Reg. = failing address B Reg. = contents on failing address
11. After test is complete set P.E. switch to desired position
12. Switch Options:
    - Bit 15 – Halts 102000. Allows 1st and last tested address to be changed

HIGH MEMORY ADDRESS TEST 24212-60001

1. Load diag. tape
2. Set P.E. switch (A8) to HALT
3. S.A. = 3600_8; SW Reg. =0

3a. INT & EXT PRESET

4. RUN, Halt 102000
5. SW Reg. - 1st adr. to be tested ($< 3600_8$ but $> 1_8$)
6. RUN; Halt 102001
7. SW Reg. = last adr. to be tested (3600_8)
8. RUN
9. Halt (102077) on errors. A Reg. = failing adr.
   B Reg. = contents of failing adr.
10. After test is complete, set P.E. switch to desired position.
11. Switch Options:

    - Bit 15 – Halts 102000. Allows 1st and last tested addresses to be changed.

DIAGNOSTIC OPERATING PROCEDURES (CONT)

LOW MEMORY PATTERN TEST 24193-60001

1. Load diag. tape
2. S.A. = 2; SW Reg. = 100000_8
3. RUN; Halt 102001
4. SW Reg. = 1st location to be tested (621_8 or greater)
5. RUN; Halt 102002
6. SW Reg. = last location to be tested (normally ABL-1)
7. RUN; Halt 102004
8. SW Reg. =0
9. RUN
10. Halts on Errors
11. Switch Options:

    Bit 0 – Hold current pattern (used with SW 12 or 13)
    Bit 1 – Store error data in table of errors
    Bit 2 – Not used
    Bit 3 – Reset table of errors upon return to START (used with SW 6)
    Bit 4 – Suppress error halts
    Bit 5 – Momentarily on to return to start
    Bit 6 – Halt upon return to start; A = next available error table address; B = No. of errors
    Bit 7 – Halt at end
    Bit 8-10 – Not used
    Bit 11 – No Memory Protect
    Bit 12 – Skip test 1 and 2 and loop on Test 3
    Bit 13 – Skip test 1 and 3 and loop on Test 2
    Bit 14 – Skip test 2 and 3 and loop on Test 1
    Bit 15 – Test user determined area Halt 102001 (Step 3)

HIGH MEMORY PATTERN TEST 24194-60001

1. Load diag. tape
2. S.A. = 2000 ; SW Reg. =0
3. RUN
4. Halts on errors
5. Switch Options – same as Low Memory Pattern

MEMORY PROTECT TEST 24222-60001

1. Load and configure TTY S.I.O. driver
2. Load diag. tape
3. S.A. =100_8; SW Reg. = S.C. of TTY
4. TTY prints "H7. Press Internal and External Preset, then press RUN"
5. Perform operations indicated in step 4
6. TTY prints "H13. Press Halt, then press Internal Preset, then press RUN in less than 15 seconds."
7. Perform operations indicated in step 6
8. Switch Options:

    Bit 0-5 – TTY Select Code
    Bit 6-10 – Not used
    Bit 11 – Suppress error halts
    Bit 12 – Halt after each test
    Bit 13 – Suppress all messages (except end of test)
    Bit 14 – Repeat current test
    Bit 15 – Suppress end of pass halt (102077) and PRESET tests

DIAGNDSTIC OPERATING PROCEDURES (CONT)

MEMORY PARITY CHECK TEST 24198-60001

NOTE: Standard interface in (not TBG) S.C. 10; $\overline{ARS}$ (A7); PE (A8) = INT

1. Load diag. tape
2. Store 0's in mem. location 5
3. S.A. =2_8; SW Reg. = Select Code of highest priority Interface
4. RUN; Halt 107074
5. SW Reg. = 10000_8
6. RUN; Halt 107077
7. S.A. =100; SW Reg. =0
8. RUN; Halt 102002; Parity lite on A107 off
9. Power off. Short E1 to E2 and E3 to E4 on A107 Data Control Card
10. Power on
11. S.A. =110; SW Reg. =0
12. INT & EXT. Preset
13. RUN; Halt 102003
14. Power off. Remove shorting jumpers on A107
15. P.E. SW to HALT
16. Power on
17. S.A. =111_8; SW Reg. =0
18. INT & EXT Preset
19. RUN; Halt with memory data -0 B Reg. -1 and front panel parity lite on
20. P.E. SW to INT
21. INT Preset. Parity lite off
22. EXT PRESET; RUN
23. Halt 102077 at end of test
24. Switch Options:

    Bit 0 – Override internal SW Reg.
    Bit 1-11 – Not used
    Bit 12 – Halt at end of complete cycle
    Bit 13 – Delete operator intervention after 1st cycle
    Bit 14-15 – Not used

POWER FAIL/AUTO-RESTART DIAGNOSTIC 24206-60001

1. Load and config. TTY S.I.O. driver
2. Load diag. tape
3. S.A. =100_8; SW Reg. =0

   NOTE: Set switch on A7 to ARS

4. Press internal and external preset and RUN
5. Count appears in the SW Reg.
6. Power off
7. Power on
8. Repeats steps 6 and 7 four times
9. Set switch 9
10. TTY prints number of test
11. Switch Options:

    Bits 0-7 – Reserved for program count
    Bit 8 – Not used
    Bit 9 – Prints number of tests completed if TTY available
    Bit 10 – Not used
    Bit 11 – Suppress all messages
    Bit 12 – Not used
    Bit 13 – If set at beginning, will assume no TTY.
    Bit 14 – Suppress error halt
    Bit 15 – Halt program

DIAGNOSTIC OPERATING PROCEDURES (CONT)

FLOATING POINT DIAGNOSTIC 24251-60001

1. S.A. =2_8 and TTY S.I.O. driver
2. SW options and RUN
   107001 = improper setting
   107077 = normal halt
3. S.A. = 100_8 and RUN
   107076 = end 100 cycles
   102077 = end of test

   SW 10 = terminate
   12 = halt end 100 cycles
   9 = display # cycles and errors
   14 = halt each error

CONTENTS PAGE

COMPUTER SPECIFICATIONS

2116B/2116C COMPUTER

2116C 8-32K memory size, 8K modules
2116B 8-16K memory size, 8K modules
(to 32K with 2150B extender)

Cycle Time	1.6 microseconds
I/O	16 slots*
Temperature	0° – 55°C
Humidity	0 – 95%
Weight	220#'s
Size	31.5"H x 16.7"W x 19.7"D
Power	115/230V ± 10%, 50/60 Hz, 1000 to 1600 watts

Options

EAU 12579A
DMA 12578A
Memory Protect 12581A
Power Fail w/Restart 12588A
Parity Check 12591A
Memory Expansion (8K): 12615A (2116C), 12592A (2116B)

2115A COMPUTER

Cycle Time	2.0 microseconds
I/O	8 slots*
Temperature	10° – 40°C
Weight	65# 's (shipping 99# 's)
Size	12"H x 16.7"W x 24.5"D
Power	Requires 2161A
Memory	4K (8K option M4)

Options

EAU 12579A
DMA 12578A
Parity Check 12580A
Power Fail w/Restart 12586A

2161 Power Supply

Weight	95# 's
Size	10.2"H x 16.7"W x 18.5"D
Power	115/230V ± 10%, 50/60 Hz, 1100 watts max

2114B COMPUTER

Cycle Time	2.0 microseconds
I/O	7 slots*
Temperature	10° – 40°C
Weight	102# 's (shipping 150# 's)
Size	12"H x 16.8"W x 24.5"D
Power	115V ± 10%, 50/60 Hz, 530 watts max
	Power Fail w/restart option – 08
Memory	4K (8K option M4)
Loading	PRESET, LOAD for automatic loading
Front Panel	Indicator lamps for T, M, and Switch Reg

Options

DMA 12607A (one channel)
High Speed I/O Channel 12616A
Multiplexed I/O 12595A
Parity Check 12598A

*I/O slots may be increased in number with 2150/2151 I/O Extender.

HARDWARE MANUALS

2114A

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02114-9002	
Inst. & Maintenance	02114-9003	
I/O System Operation	02114-9004	
Opt. 04 – 8K Memory	12611-9001	12611-90012
Opt. 08 – PF/ARS*	02114-90394	02114-90420
*Power Fail/Auto Restart		

2114B

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02114-90398	
Inst. & Maintenance	02114-90399	02114-90421
I/O System Operation	02114-90400	02114-90419
Opt. 04 – 8K Memory	12839-90001	12839-90004
Opt. 08 – PF/ARS*	02114-90394	02114-90420
*Power Fail/Auto Restart		

2115A

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02115-9011	
Inst. & Maintenance	02115-9012	02115-90198
I/O System Operation	02115-9013	
Opt. 04 – 8K Memory	02115-9014	

2116A

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02116-9010	
Inst. & Maintenance	02116-9011	
I/O System Operation	02116-9012	
Opt. 04 – 8K Memory	02116-9063	

2116B

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02116-9152	
Inst. & Maintenance	02116-9153	02116-91789
I/O System Operation	02116-9154	02116-91790
Opt. 05 – 16K Memory	12592-9001	12592-90012

2116C

TITLE	P/N	MICROFICHE
Spec. & Basic Operation	02116-91755	
Inst. & Maintenance	02116-91756	02116-91795
I/O System Operation	02116-91757	
Opt. 05, 06, 07 Memory Expansion	12615-90001	12615-90014

SOFTWARE TESTS AND DIAGNOSTICS

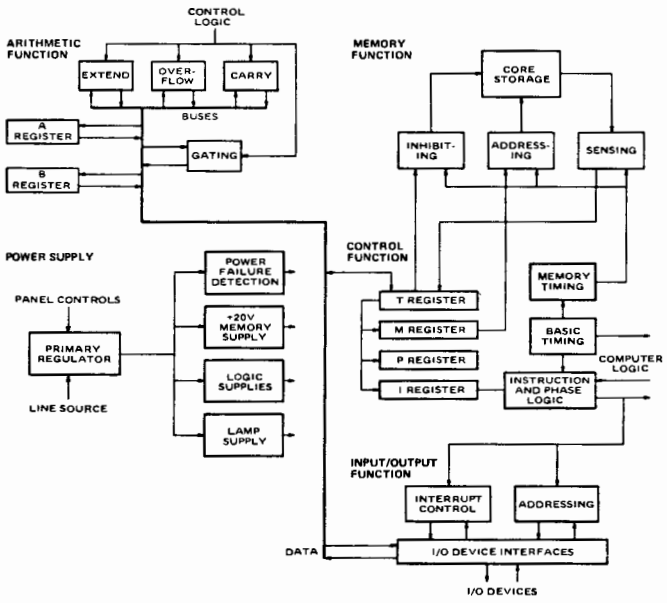
	TAPE P/N	MOD*	2114A	2114B	2115A	2116A	2116B	2116C
Alter-Skip Instruction Test	20400-60001	02116-91761	X	X	X	X	X	X
Mem. Ref. Instruction Test	20401-60001	02116-91762	X	X	X	X	X	X
Shift-Rotate Instruction Test	20402-60001	02116-91763	X	X	X	X	X	X
Low Memory Address Test	20403-60001	02116-91792	X	X	X	X	X	X
High Memory Address Test	20404-60001	02116-91792	X	X	X	X	X	X
Interrupt Diagnostic	20415-60001	02116-91768	X	X	X	X	X	X
High Memory Checkerboard	20512-60001	02114-90406	X	X	X	X		
	20406-60001	02116-9011					X	
	20426-60001	02116-91793						
Low Memory Checkerboard	20513-60001	02114-90406	X	X	X	X		
	20405-60001	02116-9011					X	
	20426-60001	02116-91793						X
High Memory Pattern Test	24162-60001	02116-91782						X
Low Memory Pattern Test	24161-60001	02116-91782						
4K SIO Dump	20301-60001		X	X	X	X	X	X
8K SIO Dump	20313-60001		X	X	X	X	X	X
16K SIO Dump	20335-60001							
Power Fail/Auto Restart Test	20428-60001	02116-91769	X	X	X	X	X	X
Memory Parity Check	20345-60001	05951-01320	X	X	X			
	24144-60001	12591-90011					X	X
Power Fail Interrupt	20434-60001	02116-91759					X	X
DMA Diagnostic	20524-60001			X				
	24185-60001	12578-90013			X	X	X	X
Ext. Arith. Unit Diagnostic	24186-60001	12579-90013			X	X	X	X
Time Base Gen. Test	20412-60001	12539-90003				X	X	X

*Manual of Diagnostics

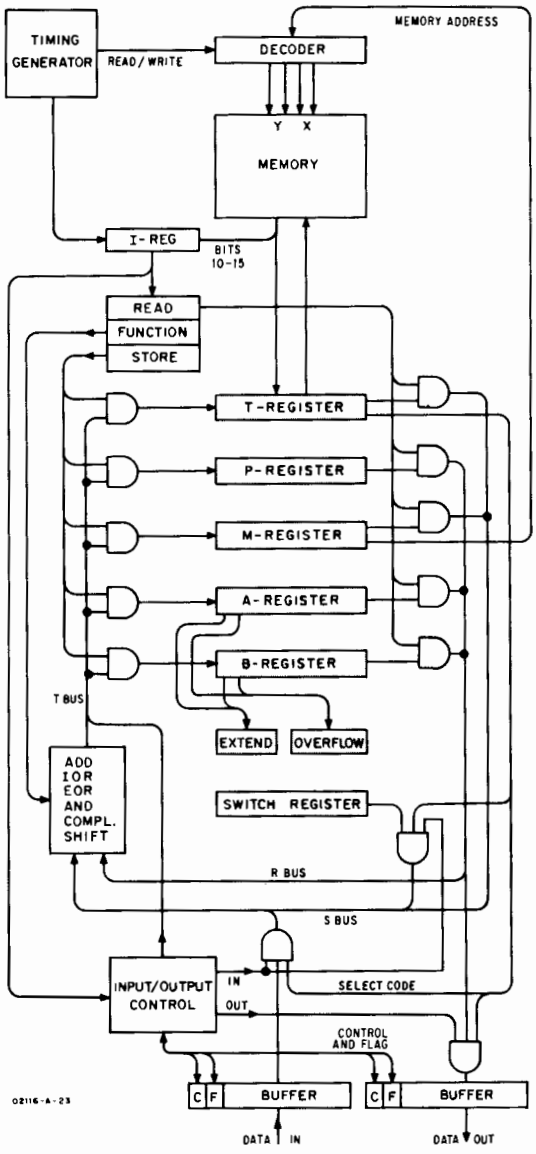
2115A/2116A MNEMONIC CHANGES

2115A 2116A	NEW MNEMONICS for Manuals	
OLD	**NEW**	
CMP	CMF	(Complement Function)
SLB	RLL	(Rotate Left to Least significant bit)
LRS	RRS	(Rotate Right to Sign bit)
IOCI	IOI	(I/O Input control)
RAR	RARB	(Read A onto R Bus)
RBR	RBRB	(Read B onto R Bus)
LDS	LMS	(Load Memory Switch)
MON	MNS	(Memory Normal Switch)
LNS	PNS	(Phase Normal Switch)
SIN	ILS	(Instruction Loop Switch
SIS	SCS	(Single Cycle Switch)
LPMS	LADS	(Load Address Switch)
IIR	EIR	(Enable Instruction Register)
RRT	RST	(Reset T-Register)
TOR	TAN	(T-Register Anded)
	TRD	(T-Register Display)
	PRD	(P-Register Display)
	MRD	(M-Register Display)
	ARD	(A-Register Display)
	BRD	(B-Register Display)
CPA	CPR	(Compare instruction decoded)
SSA	SWSA	(Switch Store A)
SSB	SWSB	(Switch Store B)
SSP	SWSP	(Switch Store P)
SST	SWST	(Switch Store T)
SSM	SWSM	(Switch Store M)
TOM	RPB	(Reset Parity Bit)
RPR	RPRB	(Read P onto R Bus)
RMS	RMSB	(Read M onto S Bus)
RTS	RTSB	(Read T onto S Bus)
IB0-7	SRA0-7	(Service Request Address)
SOR	TANS	(T-Register Anded, Summed)
CFF	SFF	(Skip Flip-Flop)
STA	STBA	(Store T-Bus in A)
STB	STBB	(Store T-Bus in B)
STT	STBT	(Store T-Bus in T)
PIR	RB0	
PIS	SB0	
IAL	SCL	(Select Code, Least significant bit)
IAH	SCM	(Select Code, Most significant bit)

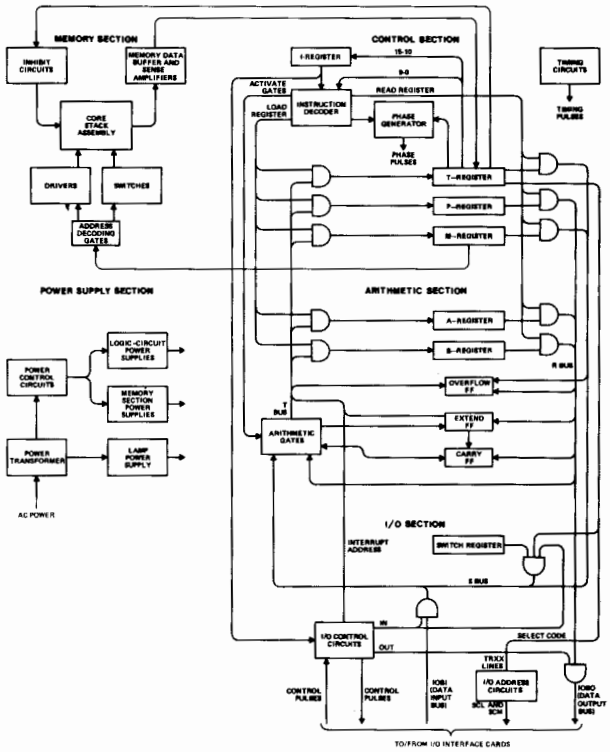
2114 COMPUTER BLOCK DIAGRAM



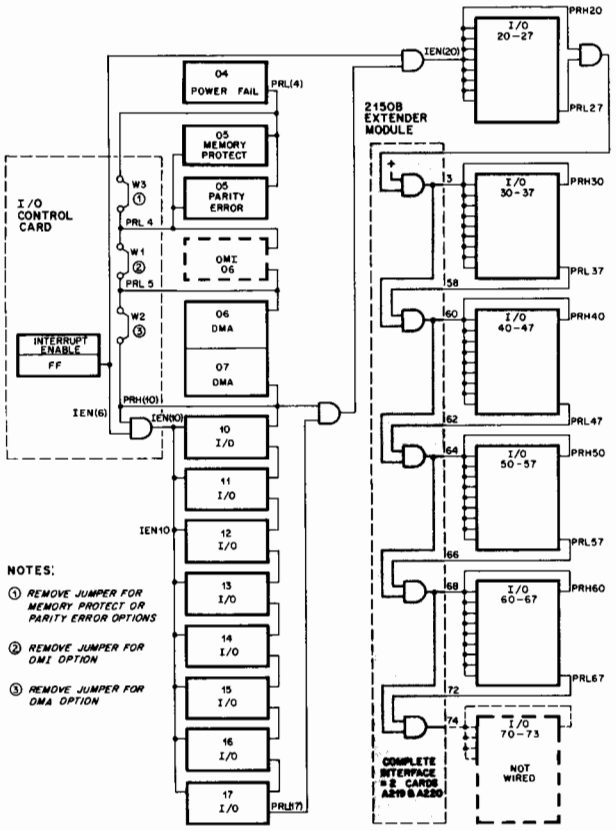
2115/16A/16B COMPUTER BLOCK DIAGRAM



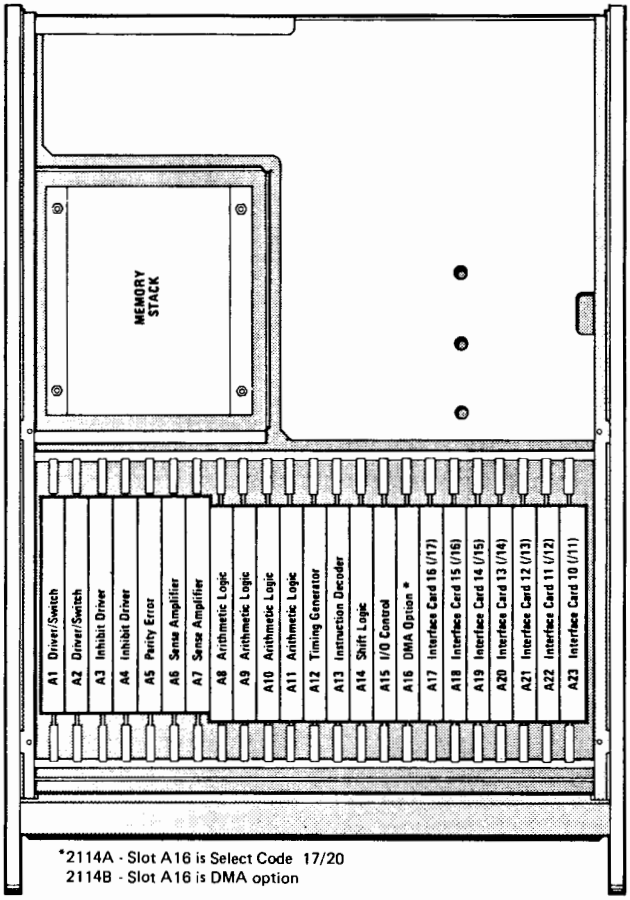
2116C COMPUTER BLOCK DIAGRAM



2116 COMPUTER PRIORITY CONTINUITY

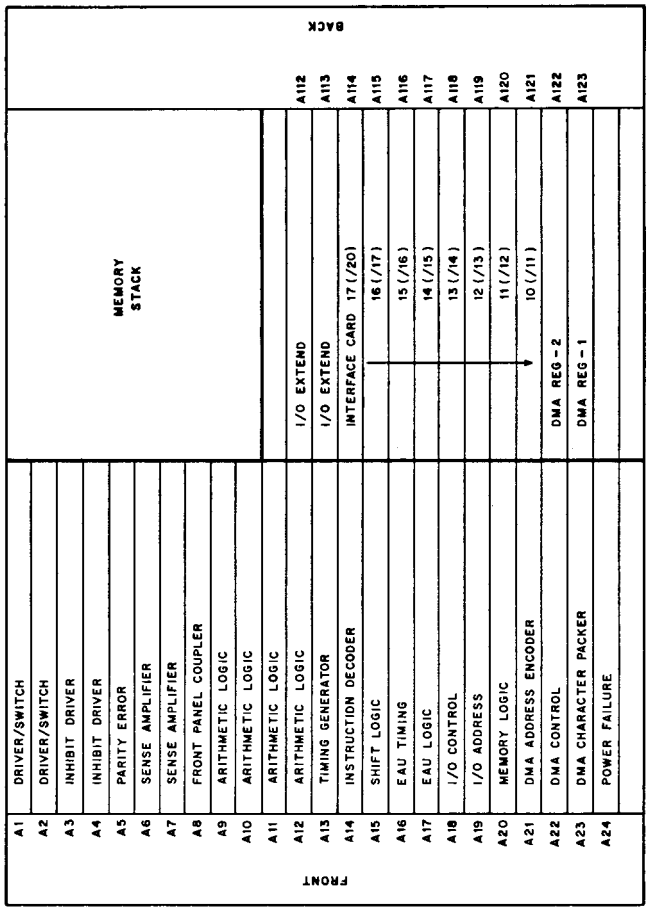


2114 COMPUTER CARD CAGE



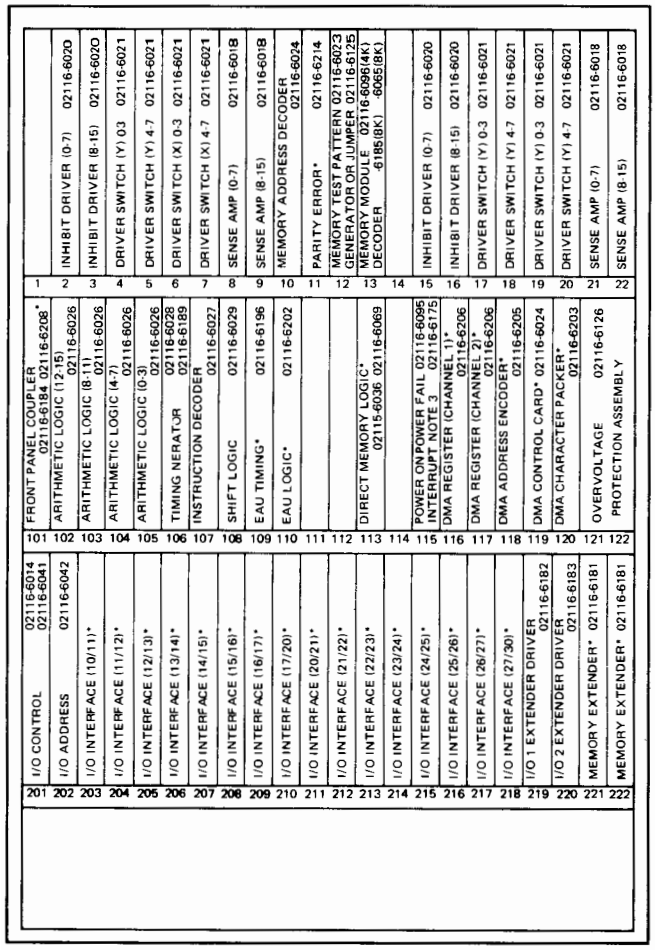
*2114A - Slot A16 is Select Code 17/20
2114B - Slot A16 is DMA option

2115 COMPUTER CARD CAGE



2116A COMPUTER CARD CAGE (FRONT)

2116A COMPUTER CARD CAGE (FRONT)

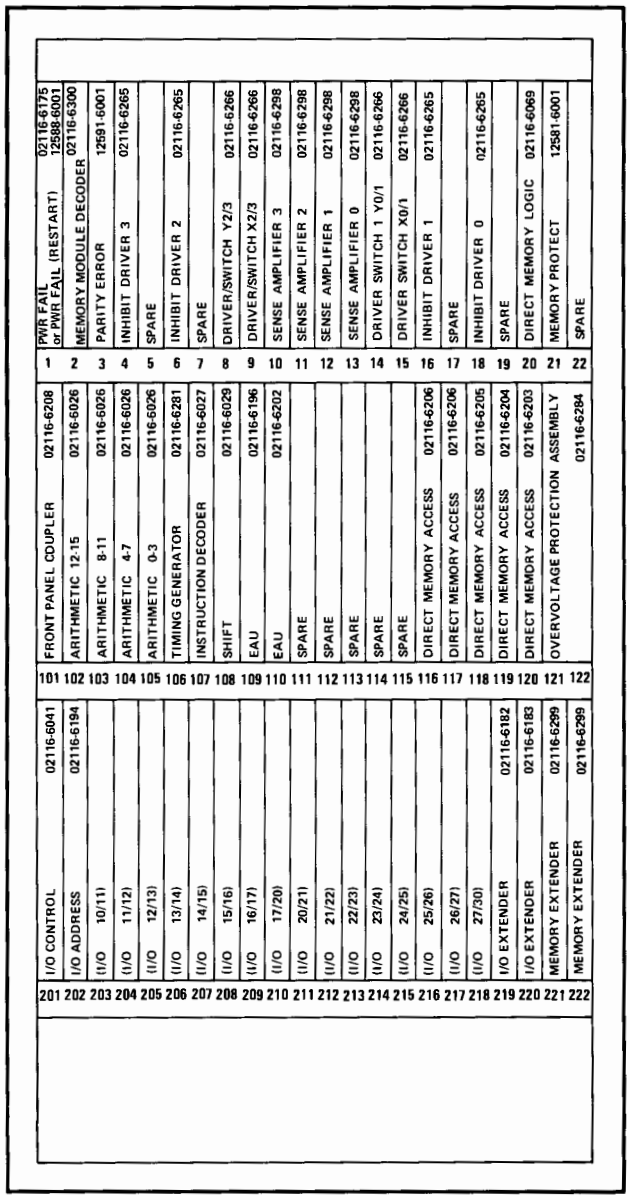


*NOTE 1: SEE IOSM ON 2116A, FOR FURTHER INFORMATION ON OTHER BOARDS THAT COULO BE USED.

NOTE 2: REFERENCE IOSM ON 2116A, FOR MORE INFORMATION.

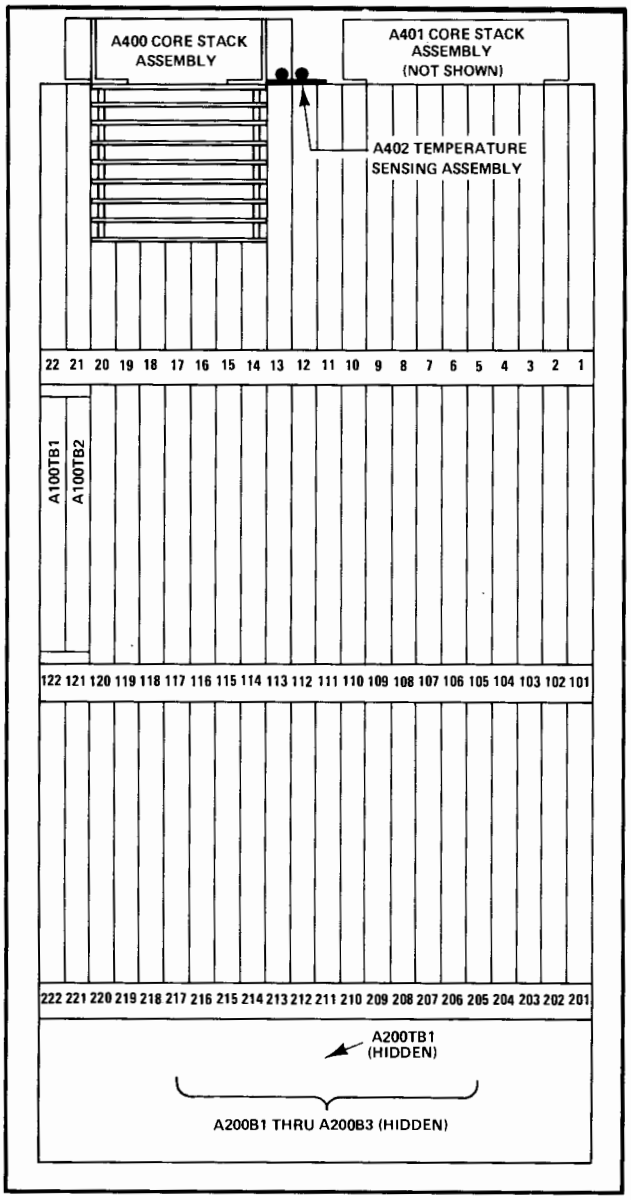
NOTE 3: SERIAL PREFIX 715 AND BELOW WILL INTERRUPT TO LOCATION 05 WITH POWER FAIL INTERRUPT 02116-6175.

2116B COMPUTER CARD CAGE (FRONT)

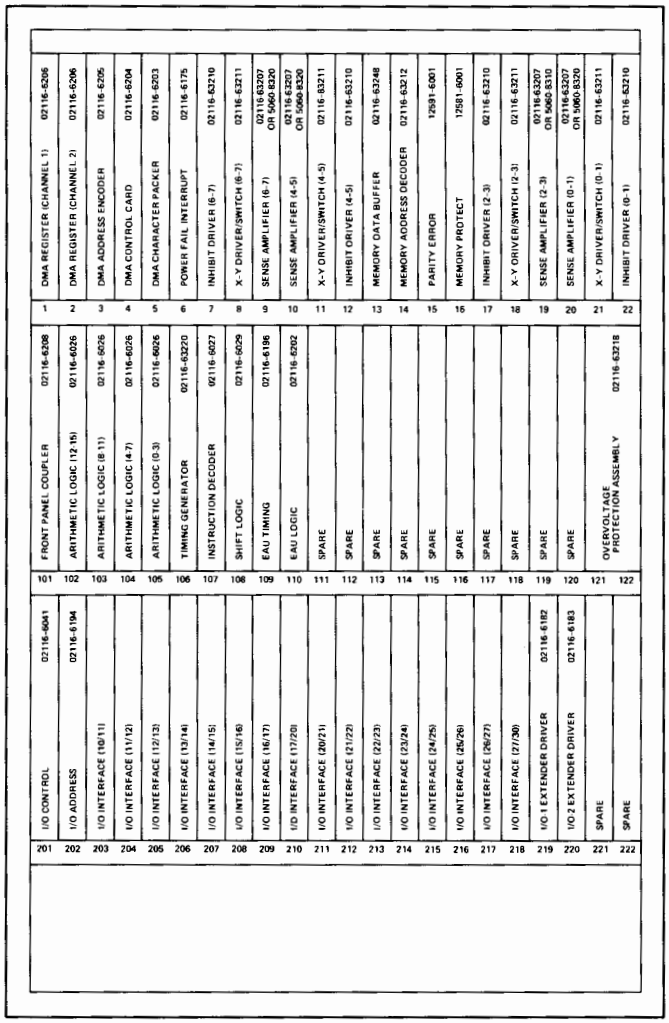


	I/O CONTROL	02116-6041	101	FRONT PANEL COUPLER	02116-6208	1	PWR FAIL or PWR FAIL (RESTART)	02116-6175 12588-6001														
	I/O ADDRESS	02116-6194	102	ARITHMETIC 12-15	02116-6026	2	MEMORY MODULE DECODER	02116-6300														
	(I/O 10/11)		103	ARITHMETIC 8-11	02116-6026	3	PARITY ERROR	12581-6001														
	(I/O 11/12)		104	ARITHMETIC 4-7	02116-6026	4	INHIBIT DRIVER 3	02116-6265														
	(I/O 12/13)		105	ARITHMETIC 0-3	02116-6026	5	SPARE															
	(I/O 13/14)		106	TIMING GENERATOR	02116-6281	6	INHIBIT DRIVER 2	02116-6265														
	(I/O 14/15)		107	INSTRUCTION DECODER	02116-6027	7	SPARE															
	(I/O 15/16)		108	SHIFT	02116-6029	8	DRIVER/SWITCH Y2/3	02116-6266														
	(I/O 16/17)		109	EAU	02116-6196	9	DRIVER/SWITCH X2/3	02116-6266														
	(I/O 17/20)		110	EAU	02116-6202	10	SENSE AMPLIFIER 3	02116-6298														
	(I/O 20/21)		111	SPARE		11	SENSE AMPLIFIER 2	02116-6298														
	(I/O 21/22)		112	SPARE		12	SENSE AMPLIFIER 1	02116-6298														
	(I/O 22/23)		113	SPARE		13	SENSE AMPLIFIER 0	02116-6298														
	(I/O 23/24)		114	SPARE		14	DRIVER SWITCH 1 Y0/1	02116-6266														
	(I/O 24/25)		115	SPARE		15	DRIVER SWITCH X0/1	02116-6266														
	(I/O 25/26)		116	DIRECT MEMORY ACCESS	02116-6206	16	INHIBIT DRIVER 1	02116-6265														
	(I/O 26/27)		117	DIRECT MEMORY ACCESS	02116-6206	17	SPARE															
	(I/O 27/30)		118	DIRECT MEMORY ACCESS	02116-6205	18	INHIBIT DRIVER 0	02116-6265														
	I/O EXTENDER	02116-6182	119	DIRECT MEMORY ACCESS	02116-6204	19	SPARE															
	I/O EXTENDER	02116-6183	120	DIRECT MEMORY ACCESS	02116-6203	20	DIRECT MEMORY LOGIC	02116-6069														
	MEMORY EXTENDER	02116-6299	121	OVERVOLTAGE PROTECTION ASSEMBLY	02116-6284	21	MEMORY PROTECT	12581-6001														
	MEMORY EXTENDER	02116-6299	122			22	SPARE															
	201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222																					

2116A/B COMPUTER CARD CAGE (REAR)



2116C COMPUTER CARD CAGE



REGISTERS

A A-register (primary accumulator).
A 16-bit register used to contain operands and results of arithmetic, logical, and I/O operations. All instructions can implicitly refer to A. A-reg = memory addr 000000.

B B-register (secondary accumulator).
A 16-bit register used to contain operands and results of arithmetic, logical, and I/O operations. All instructions except AND, IOR, and XOR can implicitly refer to B. B-reg = memory addr 000001.

E Extend/Carry Bit.
A 1-bit register used to contain a true arithmetic carry from the A- or B-registers; to link A and B with rotate instruction; and, as a program flag.

OV Overflow Bit.
A 1-bit register used to contain a true arithmetic overflow from the A- or B-registers and as a program flag. Set, Clear and test with flag SC 01.

P Program Counter.
A 15-bit register used to contain the address of the current instruction.

I Instruction Register.
A 6-bit register used to contain the indirect bit (for the first step of indirect addressing), operation code, and page bit of the instruction being executed (Bits 10-15).

M Memory Address Register.
A 16-bit register containing a 15-bit address, and an indirect bit for multilevel indirect addressing. M = P at start of every Fetch phase.

T Transfer Register.
A 16-bit register used to buffer all information read from, or to be written into memory.

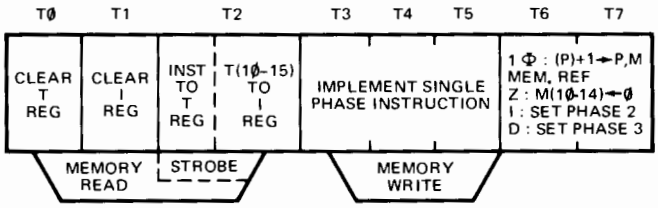
S Switch Register (console).
A 16-bit switch register used to enter information manually via the console or under program control via the I/O Bus. Select code = 01 (can be illuminated on 2114 OTA 1).

PHASES

The computer generates 8 equal time periods of length 200* nanoseconds (TØ to T7). The machine has 5 distinct modes of operation called Phases. Each allows a certain class of operations.

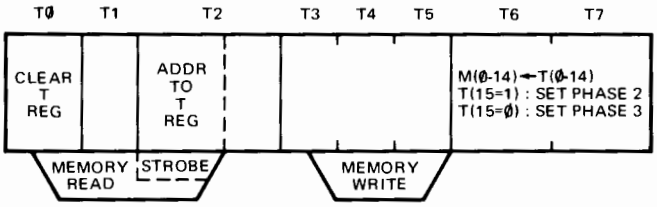
FETCH Phase 1. P- & M-Registers contain the memory location to be accessed. The T-Reg is cleared to receive the new instruction. A memory read cycle is initiated. The instruction is strobed into the T-Reg. Bits 10-15 are placed in the I-Register. The instruction is written back in the memory location. The instruction is implemented for all single phase instructions (Alter-Skip, Shift-Rotate, I/O, and direct JMP). Then (P)+1→P,M and Fetch Phase is set for the next instruction. For Memory Reference instructions bit 10 (Z/C) clears M-Register bits 10-14 for Zero page or holds for Current page; then replaces bits 0-9 for the complete address. It then sets a Phase 2 for Indirect or Phase 3 for Direct.

PHASE 1 FETCH



INDIRECT Phase 2. This phase allows reading the 15 bit address for Indirect Memory Reference addressing.

PHASE 2 INDIRECT

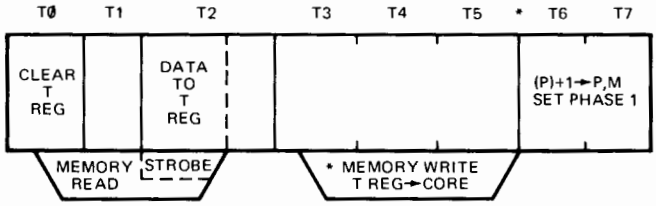


*2114/2115 requires 250 nanoseconds.

PHASES (CONT)

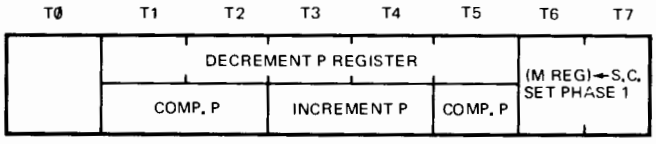
EXECUTE Phase 3. This phase allows completion of the Memory Reference instruction at the specified address.

PHASE 3 EXECUTE



INTERRUPT Phase 4. When an I/O device interrupts this phase forces a Phase 1, and sets the M-Register to the memory address corresponding to the select code. It also decrements the P-Register to ensure that a partially completed instruction will be restarted. No read/write cycle is required.

PHASE 4 INTERRUPT



DMA Phase 5. This phase is initiated by the DMA hardware on a cycle stealing basis. It suspends or holds off the normal CPU activities during the phase 5 cycle. The DMA hardware provides its own memory address register. A read/write cycle is required.

MACRO INSTRUCTION. The Extended Arithmetic instructions require from 2 to 13 cycles. During the Fetch phase when the Macro instruction is determined the EAU hardware takes control of the CPU. It does this by inhibiting the Instruction Register, and disabling the Phase FF signals. It utilizes the CPU Registers and buses. It achieves memory read/write cycles by providing a pseudo Phase 123 signal. It retains control until executing its EXIT sequence. Upon completion it sets Phase 1 and the next instruction is serviced (may be at P+1 or P+2 depending on the Macro). During execution of the Macro the computer is not in any of the 5 specified Phases.

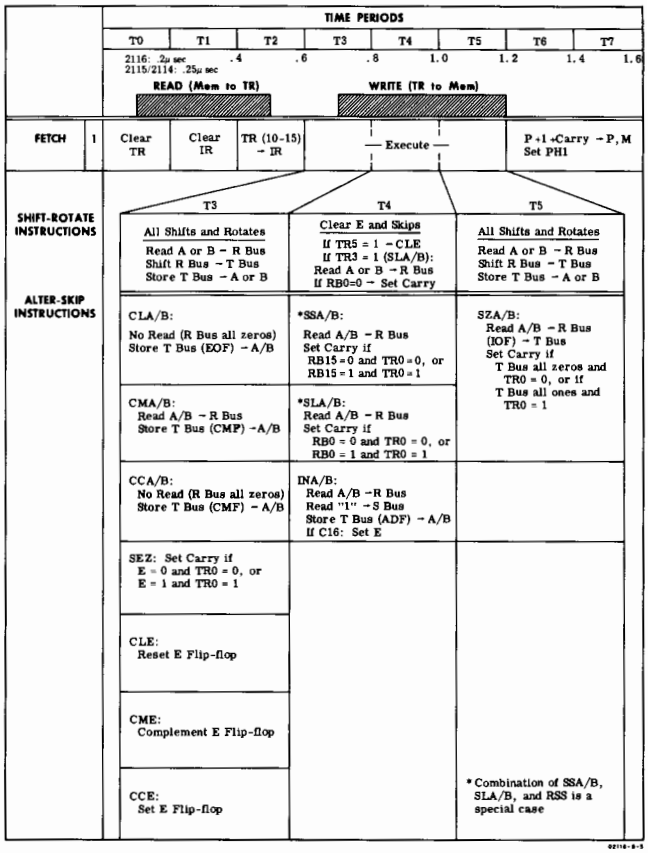
*ISZ requires 2 additional periods to increment T-Reg before memory write.

IMPLEMENTING MEMORY REFERENCE INSTRUCTIONS

PHASE		TIME PERIODS T0	T1	T2	T3	T4	T5	T6	T7
		2116: .2μ Sec 2115/2114: .25μ Sec	.4	.6	.8	1.0	1.2	1.4	1.6
		READ (Mem to TR)			WRITE (TR to Mem)				
FETCH (JMP)	1	Clear TR	Clear IR	TR(10-15) → IR (Set Functions)			If Z: 0 → P	If Z: 0 → M (10-15) If D: TR → P, M (0-9) and set PH1 If I: TR → M (0-9) and set PH2	
INDIRECT (JMP)	2	Clear TR						If D: TR → P, M and set PH1 If I: TR → M and set PH2	
FETCH	1	Clear TR	Clear IR	TR (10-15) → IR (Set Functions)				TR → M (0-9) If Z: 0 → M (10-15) If I: Set PH2 If D: Set PH3	
INDIRECT	2	Clear TR						TR → M If I: Set PH2 If D: Set PH3	
EXECUTE AND	3	Clear TR			Read A → R Bus Read TR → S Bus Store T Bus (ANF) → A			Read P → R Bus Read "1" → S Bus Store T Bus (ADF) → P, M Set PH1	
XOR		Clear TR			A (EOF) TR → A			P + 1 → P, M Set PH1	
IOR		Clear TR			A (IOF) TR → A			P + 1 → P, M Set PH1	
JSB		Clear TR Inhibit Mem. Data	P+1 → TR		M → P			P +1 → P, M Set PH1	
ISZ		Clear TR			TR+1 → TR If C16: Set Carry Inhibit Write		Write*	P+1+ Carry → P, M Set PH1	
ADA/B		Clear TR			If A: A (ADF) TR → A If B: B (ADF) TR → B If C16: Set E			P + 1 → P, M Set PH1	
CPA/B		Clear TR			If A: A (EOF) TR → T Bus If B: B (EOF) TR → T Bus If T Bus not zero, set Carry			P + 1 + Carry → P, M Set PH1	
LDA/B		Clear TR			If A: TR → A If B: TR → B			P +1 → P, M Set PH1	
STA/B		Clear TR Inhibit Mem. Data	If A: A → TR If B: B → TR					P + 1 → P, M Set PH1	

*2116: Add 0.4μS
2114/2115: Add 0.5μS

IMPLEMENTING REGISTER REFERENCE INSTRUCTIONS



IMPLEMENTING I/O INSTRUCTIONS

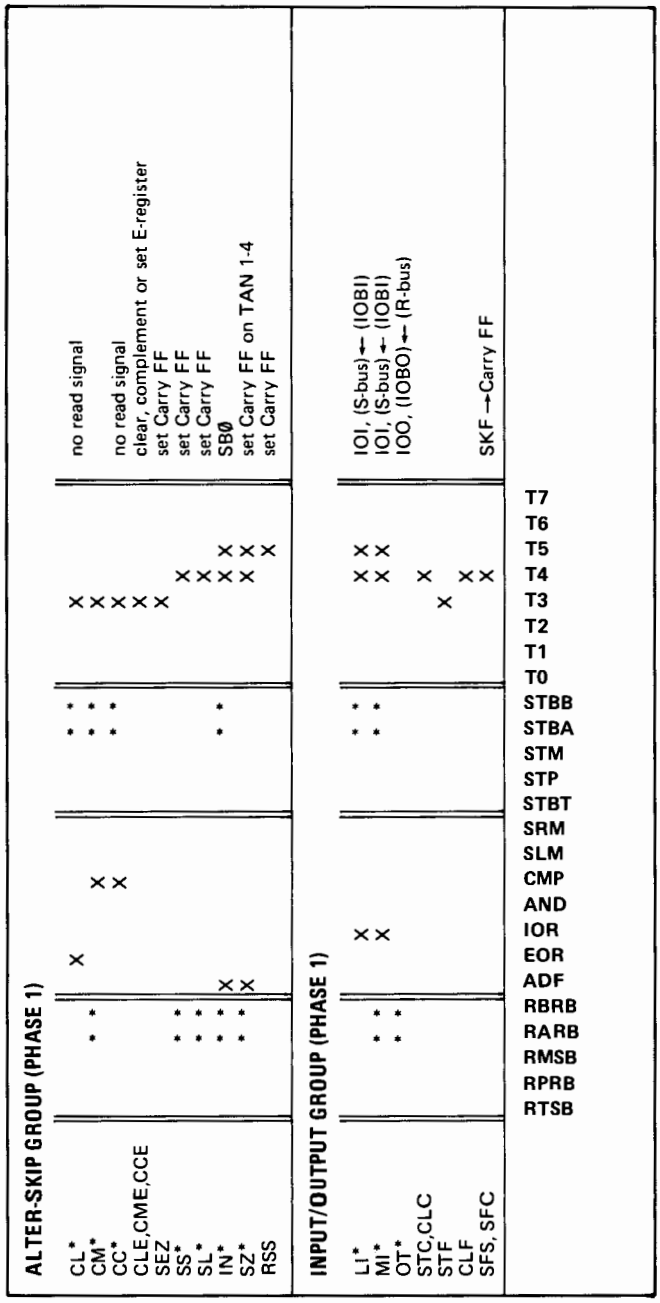
PHASE		TIME PERIODS T0	T1	T2	T3	T4	T5	T6	T7
		2116: .2μ Sec 2115/2114: .25μ Sec .4	.6	.8	1.0	1.2	1.4	1.6	
		READ (Mem to TR)		WRITE (TR to Mem)					
FETCH HLT	1	Clear TR	Clear IR	TR(10-15) → IR				P+1 → P, M Reset Run FF	
STF		Clear TR	Clear IR	TR → IR	Set Flag: Select Code			P+1 → P, M Set PH1	
CLF		Clear TR	Clear IR	TR → IR	Set Flag: Select Code	Clear Flag: Select Code		P+1 → P, M Set PH1	
SFC		Clear TR	Clear IR	TR → IR	SFC → Interface	SKF → Carry		P+1+Carry → P, M Set PH1	
SFS		Clear TR	Clear IR	IR → IR	SFS → Interface	SKF → Carry		P+1+Carry → P, M Set PH1	
MIA/B		Clear TR	Clear IR	TR → IR		Read A/B → R Bus Buffer → S Bus Store T Bus (IOF) → A/B TR9: CLF		P+1 → P, M Set PH1	
LIA/B		Clear TR	Clear IR	TR → IR		Buffer → S Bus Store T Bus (IOF) → A/B TR9: CLF		P+1 → P, M Set PH1	
OTA/B		Clear TR	Clear IR	TR → IR		Read A/B → R Bus R Bus → Buffer TR9: CLF		P+1 → P, M Set PH1	
STC		Clear TR	Clear IR	TR → IR		Set Control (Sel. Code)		P+1 → P, M Set PH1	
CLC		Clear TR	Clear IR	TR → IR		Clr. Control (Sel. Code)		P+1 → P, M Set PH1	
STO		Clear TR	Clear IR	TR → IR	STF → Overflow			P+1 → P, M Set PH1	
CLO		Clear TR	Clear IR	TR → IR		CLF → Overflow		P+1 → P, M Set PH1	
SOC		Clear TR	Clear IR	TR → IR	SFC → OVF	SKF Carry		P+1+Carry → P, M Set PH1	
SOS		Clear TR	Clear IR	TR → IR	SFS → OVF	SKF → Carry		P+1+Carry → P, M Set PH1	
INTERRUPT	4		Read P → R Bus Store T Bus (CMF) → P		Read P → R Bus Read "1" → S Bus Store T Bus (ADF) → P		Read P → R Bus Store T Bus (CMF) → P		Reset M (6-15) Store T Bus (0-5) → M Set PH1

02116-8-5

MICROPROGRAMS

INSTRUCTION	RTSB	RPRB	RMSB	RARB	RBRB	ADF	EOR	IOR	AND	CMP	SLM	SRM	STBT	STP	STM	STBA	STBB	T0	T1	T2	T3	T4	T5	T6	T7	
MEMORY REFERENCE INSTRUCTION (PHASE 3)																										
AND	X			X					X							X					X	X			ref Overflow & Extend
XOR	X			X			X									X					X	X				
IOR	X			X				X								X					X	X				
JSB		X	X			X							X	X					X	X						SB0, $\overline{\text{MST}}$, increment P (P) ← (M)
ISZ	X					X	X						X				*				X	X				RB0, set Carry, add 400 nsec, delay write cycle
AD*	X			*	*	X										*					X	X				ref Overflow & Extend
CP*	X			*	*		X														X	X				Set Carry FF
LD*	X						X									*	*				X	X				
ST*				*	*		X						X						X							$\overline{\text{MST}}$
JMP	X					X								X	X									X	X	Phase 1, STM (0-9), STP (0-9)
JMP	X					X								X	X									X	X	Phase 2
SHIFT-ROTATE GROUP (PHASE 1) bits (6-9) @ T3, bits (0-2,4) @ T5																										
*LS				*	*						X					*	*				X	X				(TB0) ← 0, SL14, (R15) ≠ (R14) → Overflow FF
*RS				*	*							X				*	*				X	X				(TB14) ← (TB15)
R*L				*	*						X					*	*				X	X				SL14, SL0
R*R				*	*							X				*	*				X	X				LRS
ER*				*	*						X					*	*				X	X				(TB15) ← (E), (E) ← (RB0)
EL*				*	*						X					*	*				X	X				(E) ← (TB15), (TB0) ← (E)
*LF				*	*											*	*				X	X				RLF
*LR				*	*						X					*	*				X	X				(TB0) ← 0, (TB15) ← 0
CLE																				X						Clear E-register
SL*				*	*															X		X	X			Set Carry FF

MICROPROGRAMS (CONT)



DIAGNOSTICS

LONG DIAGNOSTIC (ET-4515)
Load first 5 feet with loader, Hlt 77
A-reg = Reader SC bits 0-5
  bit 8 = 2116A
  bit 9 = 2116C (3 wire)
  bit 10 = 2114/2115
  bit 11 = 2116B
B-reg = TTY SC bits 0-5, bit 15 = 1 for Buf TTY board
S.A. = 15, PRESET, RUN, Hlt 1 @ P = 20
A-reg = upper limit of core test area (2114 LD ADDR=20)
Sw reg = 077777, RUN. Hlt 77 End of Test
  Hlt 30 during test 10, I/O Priority string broken

ALTER SKIP TEST (20400)
S.A. = 2000, Sw Reg = 077777, RUN, Hlt 1 @ P = 2001
  (halt inst works), RUN, loops (< 1 sec).

MEMORY REFERENCE TEST (20401)
Load 6 inches, Protect loader, S.A. = 7642, RUN, Hlt 1 @ P = 7662.
Load remainder, S.A. = 1000, Sw Reg = 077777, RUN, loops (< 1 sec).

SHIFT ROTATE TEST (20402)
S.A. = 6200, Sw Reg = 077777, RUN, loops (< 1 sec).

HIGH MEMORY ADDRESS (20403)
S.A. = 7600, Sw Reg = 2 (start addr of block), RUN, Hlt 1
@ P = 7604. Sw Reg = 7577 (ending addr), RUN, loops (< 1 sec).
Set bit 15 for new limits.

LOW MEMORY ADDRESS TEST (20404)
S.A. = 100, Sw Reg = 144 (starting addr), RUN Hlt 1 @ P = 104.
Sw Reg = (loader-1), RUN, loop (< 1 sec for 8K).
Set bit 15 for new limits.

LOW MEMORY CHECKERBOARD (20427 2116B, 20513 2114/2115)
S.A. = 11, Sw Reg = 204, PRESET, RUN, Hlt 1 @ P = 14
Sw Reg = (loader-1), RUN, loops.
Set bit 15 to change limits.

HIGH MEMORY CHECKERBOARD (20426 2116, 20512 2114/2115)
S.A. = 7501, Sw Reg = 2, RUN, Hlt 1 @ P = 7504.
Sw Reg = 7477, RUN, loops
Set bit 15 to change limits.

TTY DIAGNOSTIC (BUF) (20420)
S.A. = 100, Sw Reg = TTY SC bits 0-5, RUN, Hlt 1 @ P = 124.
Sw Reg = 70, RUN, Hlt 2. RUN, Punch tape, Hlt 3.
Read tape, RUN, Print out.
To halt set bit 0

TTY CONTROL WORDS

```
LDA   CONTL
OTA   TTY      control word
```

Label		Value	Function
INPUT	OCT	140000	Sets input FF
OUTPN	OCT	110000	Clears Input FF, Sets Punch FF
OUTPR	OCT	120000	Clears Input FF, Sets Print FF
OUTPP	OCT	130000	Clears Input FF, Sets Print & Punch FF

DIAGNOSTICS (CONT)

MEMORY ADDRESS TEST

MEM ADDR	CONTENTS	LABEL	INSTRUCTION
00002	006204		INB, CME
00003	060023		LDA FRST
00004	150000	CMPAR	CPA 0, I
00005	002001		RSS
00006	102000		HLT
00007	052022		CPA LAST
00010	024014		JMP START
00011	002004		INA
00012	024004		JMP CMPAR
00013	000000		NOP
00014	060023	START	LDA FRST
00015	170000	STORE	STA 0, I
00016	050022		CPA LAST
00017	024002		JMP CMPAR-2
00020	002004		INA
00021	024015		JMP STORE
00022*	007777	LAST	OCT 7777
00023	000024	FRST	OCT 00024

*For 8K machines (22) 017777
Use 007677 or 017677 if you do not desire to test protected area.
Starting address 14.
Depress PRESET and RUN. The computer shall run. If it halts, there is an address error.
Extend bit shall blink on and off, B-reg increments each pass.
Locations 00022 and 00023 may be changed to test any core area.
(requires ≈ 1 sec)

TIME BASE GENERATOR 12539

[20412 2116, 20421 2114/2115]

Load and Configure TT/SIO driver.
Load Diagnostic, S.A. = 100, A Reg = SC TBG, Sw Reg = 17000, PRESET, RUN.
Diagnostic types: "FT"
"IN"
"OP" (after 18 min)
"TI" (after 17 min)

Program loops.

SWITCH REG OPTIONS

Bit	Function			
15	exit Flag test "FT"			
14	exit Interrupt test "IN"			
13	exit Operation test "OP"			
12	exit Timing test "TI"			
6	terminate			
3	=0, ignore bits 0-2 and test all combinations =1 bits 0-2 specify time period for Operation test			
0-2	0	100 usec	4	1 sec
	1	1 msec	5	10 sec
	2	10 msec	6	100 sec
	3	100 msec	7	1000 sec

DIAGNOSTICS (CONT)

12586, 12588 POWER FAIL WITH RESTART (20428)

RESTART/HALT Switch up (Restart)

Load Tape, LOAD A (Loader - 1), S.A. = 2 (4K) / 3 (8K) / 24 (⩾ 16K), PRESET, RUN (notice registers increment).

1) Induce power failure (Power Switch, AC Line, variac, etc.), restore power computer should resume counting (refer A,B counter).

2) Computer running. Push HALT, induce power failure. Restore power T reg = 102077; P,M = 165; A, B = 0 Push PRESET, RUN. Starts Counting.

3) Computer running. Induce power failure. Hold HALT and restore power. Press PRESET. Computer stays halted. Registers random.

4) S.A. = 45, PRESET, RUN, Induce power failure. Hold PRESET and restore power, computer does not run and preset lamp is off, Registers random.

5) Restart addr = 45, PRESET, RUN, computer counting. Move RESTART/HALT switch down (HALT). Induce power failure. Restore power computer in HALT, registers random. Raise switch to Restart, computer resumes counting. End of test.

12591A PARITY ERROR 2116B/C (24144)

1. Load and configure SIO TTY driver.
2. Load diagnostic, SA = 2, SW Reg = SC TTY (bits 0-5), 6 = 1 no

   Memory Protect.

   RUN, HLT 74 @ P = 6062.
3. Sw Reg = 600, RUN, HLT 77 @ P = 6066
4. Parity error switch down (interrupt),

   SA = 100, PRESET, RUN
   HLT 1 @ P = 6242
   PRESET, RUN
   HLT 02 @ P = 6313 (If Parity bit light on - error).
5. Remove Parity board. SA = 110, Sw Reg = 0, PRESET, RUN. HLT 3 @ P = 6352.
6. Reinstall Parity board, Switch Up (HALT), SA = 111, Sw Reg = 0, PRESET, RUN. Parity HLT 1 @ P=6400. Parity HALT light on, Parity bit light on. PRESET. Parity HALT light off, bit light on.
7. Switch down, PRESET, RUN. HLT 77 @ P = 7024 (must reload to rerun).

DIAGNOSTICS (CONT)

EXTENDED ARITHMETIC UNIT (24186)

Board Locations

Board	2116C	2116A/B	2115A
02116-6196	A109	A109	A16
02116-6202	A110	A110	A17

Requires 2K min core (TTY optional).

Load and Configure TTY SIO Driver.
Load diagnostic, S.A. = 100, Set Switch Register:

Bit	Function
0	Use Switch Register for options
1	TTY not available
2-5	Spares
6	Suppress # generator (=0 to generate new arguments for each execution of test)
7	Suppress indirect addressing
8	Repeat current test with new arguments (6=0)
9	Leave test on error
10	Suppress non-error messages
11	Suppress error messages
12	Halt 77 at end of current pass
13	Repeat current test with the same arguments
14	Suppress error halts
15	Halt at end of test

Recommended Switch Register = 000001, RUN (about 45 sec per pass).

Test sequence: 1 DLD, 2 DST, 3 MPY, 4 DIV, 5 ASR, 6 ASL, 7 LSR, 10 LSL, 11 RRR, 12 RRL. A pass consists of 1500 loops through the ten tests each time with a new argument.

DIRECT MEMORY ACCESS

The direct memory access (DMA) is a plug-in-card option for the HP 2114B, 2115, and 2116 Computers. In the 2114B, it is a single channel; in all other models, it is dual channel. DMA enables the computer to transfer data directly between memory and input/output devices. In order to do this, the central processor and I/O system operation must be suspended. This is accomplished by generating a special computer phase called phase 5. During this phase, the running program is suspended for one machine cycle for each word that is transferred between memory and an I/O device. The word is written into or read from a predetermined memory location and the main or running program is then automatically resumed at the point where it was suspended. To be placed in operation, DMA must first be initialized by control words in the main program. In all cases, DMA may be used only with I/O devices which have select codes in the computer main frame.

DIRECT MEMORY ACCESS (CONT)

The DMA Option is programmed using HP Assembler language. The instruction, control, and data word formats used in the operation of DMA are shown in Figure 1 and defined below.

a. Input-Output Instruction Words. I/O Group instructions addressed to select codes 2, 3, 6, or 7, that permit the Central Processor to control the following DMA functions through the I/O select code addresses specified:

   (1) Select Code 2 (permits Control FF on DMA Channel 1 Register Card to be addressed by CLC and STC instructions);

   (2) Select Code 2 preceded by CLC2 instruction (permits DMA Channel 1 Memory Address Register to be addressed by an OTA instruction);

   (3) Select Code 2 preceded by STC2 instruction (permits DMA Channel 1 Word Count Register to be addressed by OTA and LIA instructions);

   (4) Select Code 3 (permits Control FF on DMA Channel 2 Register Card to be addressed by CLC and STC instructions);

   (5) Select Code 3 preceded by CLC3 instruction (permits DMA Channel 2 Memory Address Register to be addressed by an OTA instruction);

   (6) Select Code 3 preceded by STC3 instruction (permits DMA Channel 2 Word Count Register to be addressed by OTA and LIA instructions);

   (7) Select Code 6 (permits DMA Channel 1 switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions);

   (8) Select Code 7 (permits DMA Channel 2 switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions).

b. DMA Program Controls Words. Program constants that can be programmed to either DMA Channel (select code 6 or 7) to specify the following:

   (1) The I/O Channel select code address of the device to be serviced by the DMA Channel (Bits 0 through 5);

   (2) Clear (turn off) control on device I/O channel after last word or byte in data block is transferred (bit 13 = 1);

   (3) Do not clear control on device I/O Channel (bit 13 = 0);

   (4) Use character packing mode if memory input transfer, or use character unpacking mode if memory output transfer (bit 14 = 1);

   (5) Word input/output mode (bit 14 = 0);

   (6) Set (turn on) control on device I/O Channel after each word or byte in data block is transferred (bit 15 = 1);

   (7) Do not set control on device I/O Channel (bit 15 = 0).

DIRECT MEMORY ACCESS (CONT)

INPUT/OUTPUT INSTRUCTION WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IO GROUP					INSTRUCTION				SELECT CODES 2,3,6 OR 7					

DMA PROGRAM CONTROL WORD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	STC	BYTE	CLC	NOT USED							DEVICE SELECT CODE					
0	STC	WORD	CLC													

DMA ADDRESS WORD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	IN	PAGE ADDRESS					WORD ADDRESS									
0	OUT															

DMA BLOCK LENGTH WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED	WORD COUNT														

DATA INPUT/OUTPUT WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16-BITS															

CHARACTER INPUT/OUTPUT WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HIGH CHARACTER BITS 0 THRU 7								LOW CHARACTER BITS 0 THRU 7							

Figure 1. DMA Instruction and Control Word Formats

c. DMA Address Words. Program constants that can be programmed to either DMA Channel (select code 2 or 3) to specify the following:

   (1) Starting memory address for first word of input/output data block (bits 0 through 14);

   (2) Memory input from device I/O Channel (bit 15 = 1);

   (3) Memory output to device I/O Channel (bit 15 = 0).

d. DMA Block Length Words. Program constants that can be programmed to either DMA Channel (select code 2 or 3) to specify the number of words in data block. Word count is a decimal number expressed as the 2's complement of its positive binary equivalent.

e. Data Input/Output Words. Conventional data word format used to transfer data directly between the device I/O Channel and memory.

f. Character Input/Output Words. A word format used to transfer two character bytes between memory and the DMA packing/unpacking function.

DIRECT MEMORY ACCESS (CONT)

To check operation of the DMA word count register:

Address	Mnemonic	Octal
100B	LIA 1	102501
101	STC XX	1037XX
102	OTA XX	1026XX
103	LIB XX	1065XX
104	JMP *-4	024100

XX = DMA channel programming select code 2 or 3 sends data from switches as programmed word count. Reads actual word count from DMA word count register up to 2^{13}.

12578A DMA

Board Locations			
Board	2116C	2116A/B	2115A
02116-6203 Char Pack	A5	A120	A23
02116-6204 DMA Control	A4	A119	A22
02116-6205 Addr Encoder	A3	A118	A21
02116-6206 DMA Word Count	A1,2	A116,117	A122,123
02115-6044 Dir Mem Logic	--	A113	A20
Priority Jumper (I/O)	A201,W3	A201,W2	FPC

EXTENDED ARITHMETIC UNIT

The extended arithmetic unit (EAU) extends the hardware arithmetic capabilities of the HP 2115 and 2116 Computers. It is a two card plug-in option and contains all the logic necessary to do multiply and divide operations and long shifts and rotates at high rates of speed. It is also capable of doing double load and store operations. While EAU is in operation, it suspends CPU operation by inhibiting any instructions from being decoded by the instruction register. The EAU makes use of the macro signal to decode its various operations, and if for some reason the macro signal is generated with a combination of bits that do not form a legal EAU instruction, the results cannot be determined. This is possible because the EAU contains all necessary circuitry to perform memory read-write operations and register manipulation.

EXTENDED ARITHMETIC UNIT (CONT)

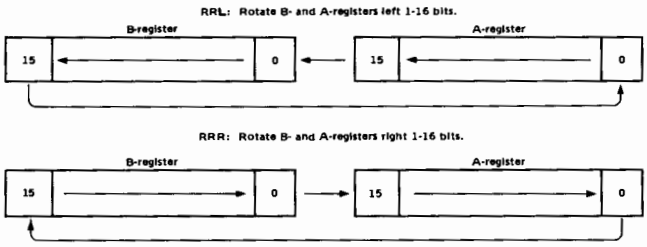


Figure 2. EAU Rotate Instructions RRL and RRR

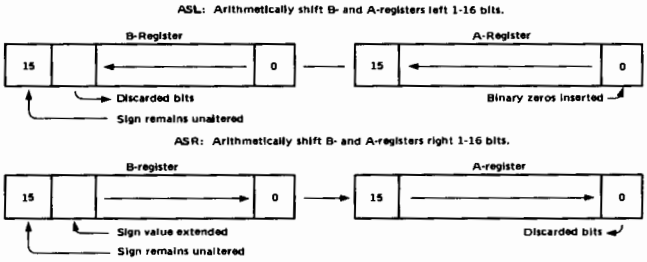


Figure 3. EAU Arithmetic Shifts ASL and ASR

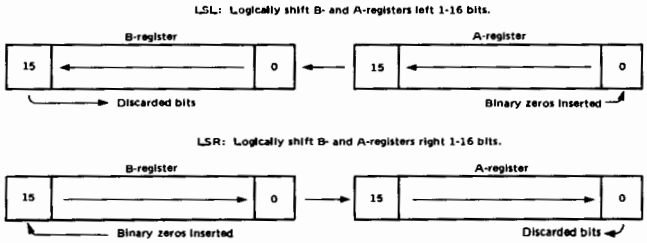


Figure 4. EAU Logical Shifts LSL and LSR

EXTENDED ARITHMETIC UNIT (CONT)

EAU MACHINE CODING

INSTRUCTION	15	14 13 12	11 10 9	8 7 6	5 4 3	2 1 0
MPY	1	0 0 0	0 0 0	0 1 0	0 0 0	0 0 0
DIV	1	0 0 0	0 0 0	1 0 0	0 0 0	0 0 0
DLD	1	0 0 0	1 0 0	0 1 0	0 0 0	0 0 0
DST	1	0 0 0	1 0 0	1 0 0	0 0 0	0 0 0
ASR	1	0 0 0	0 0 1	0 0 0	0 1	*n
ASL	1	0 0 0	0 0 0	0 0 0	0 1	*n
LSR	1	0 0 0	0 0 1	0 0 0	1 0	*n
LSL	1	0 0 0	0 0 0	0 0 0	1 0	*n
RRR	1	0 0 0	0 0 1	0 0 1	0 0	*n
RRL	1	0 0 0	0 0 0	0 0 1	0 0	*n

*N = number of shifts or rotates:

1 = 1 shift or rotate
2 = 2 shifts or rotates
3 = 3 shifts or rotates
4 = 4 shifts or rotates
5 = 5 shifts or rotates
6 = 6 shifts or rotates
7 = 7 shifts or rotates
8 = 8 shifts or rotates
9 = 9 shifts or rotates
10 = 10 shifts or rotates
11 = 11 shifts or rotates
12 = 12 shifts or rotates
13 = 13 shifts or rotates
14 = 14 shifts or rotates
15 = 15 shifts or rotates
0 = 16 shifts or rotates

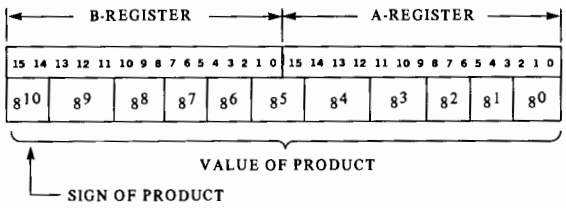
EAU Multiply

Example: MPY Value

DEF Value

Before Execution	After Execution
B = any value	B = 1/2 product
A = multiplicand	A = 1/2 product
Value = multiplier	Value = multiplier

EXTENDED ARITHMETIC UNIT (CONT)

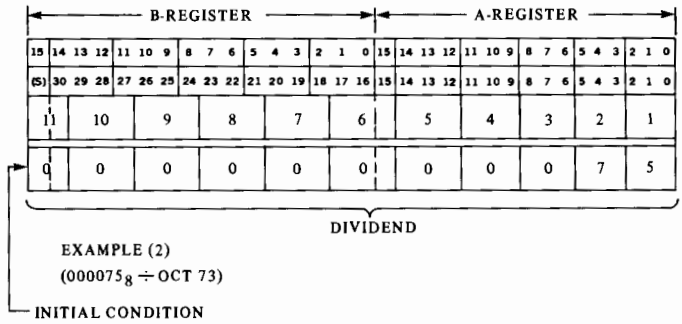


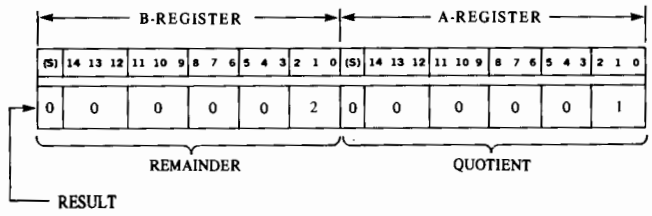
EAU Divide

Example: DIV SAM

DEF SAM

Before Execution	After Execution
B = 1/2 dividend	B = remainder
A = 1/2 dividend	A = quotient
SAM = divisor	SAM = divisor





EXTENDED ARITHMETIC UNIT (CONT)

EAU Double Load

```
Example:  DLD FOX
          DEF FOX
```

Contents of memory locations FOX and FOX + 1 are loaded into the A and B registers respectively.

EAU Double Store

```
Example:  DST JOE
          DEF JOE
```

Contents of the A and B registers are stored in memory locations JOE and JOE + 1 respectively.

POWER SUPPLIES

CONTENTS PAGE

2100 POWER SUPPLY

POWER REQUIREMENTS

LINE VOLTAGE:	115V ac ± 10%, single phase, 12A, or 230V ac ± 10%, single phase, 6A
LINE FREQUENCY:	47.5 to 66 Hz
POWER CONSUMPTION:	1400 volt-amperes, maximum

POWER CABLE (CONNECTED TO COMPUTER OR EXTENDER)

LENGTH:	10 feet (304, 8 centimeters)
CONNECTOR:	NEMA Type 5-15P (for 115V ac operation), or NEMA Type 6-15P (for 230V ac operation)

DC SUPPLY VOLTAGES AND CURRENTS

+30V, 0.1A
+12V, 5A for 2155A Extender; +12V, 3A for 2100 Computer
+4.85V, 50A
-2V, 23A
-12V, 5A for 2155A Extender; +12V, 3A for 2100 Computer
+20V, 6A
-20V, 0.5A } For 2100 Computer only

ENVIRONMENTAL LIMITS

AMBIENT TEMPERATURE RANGE:

Operating:	0° to 55°C (32° to 131°F)
Non-operating:	-40° to 75°C (-40° to 167°F)

RELATIVE HUMIDITY: 50 to 95% at 25° to 40°C (77° to 104°F) without condensation

ALTITUDE:

Operating:	15,000 feet (4572 meters)
Non-operating:	25,000 feet (7620 meters)

VENTILATION

AIR FLOW:	200 cubic feet (5,6634 cubic meters) per minute
HEAT DISSIPATION:	2300 BTUs (579,6 kilocalories) per hour, maximum

WEIGHT AND DIMENSIONS

WEIGHT:	36 pounds (16,344 kilograms)
HEIGHT:	10 inches (254 millimeters)
WIDTH:	7.75 inches (196,85 millimeters)
DEPTH:	12 inches (304,8 millimeters)

2100 POWER SUPPLY (CONT)

CONFIGURATION

POWER SUPPLY DATE CODE	CARD REVISION CODE					REMARKS
	A1	A2	A3	A4	A5	
1126	1133	1126	1132	1126	1125	
1140	1139	1126	1132	1126	1125	
1141	1140	1140	1132	1126	1139	
1146	1140	1140	1132	1126	1139	
1148	1140	1140	1132	1144	1139	(Note 1)
1149	1140	1140	1147	1144	1139	
1150	1140	1140	1147	1144	1150	
1215	1148	1140	1215	1144	1150	
1220	1148	1140	1215	1144	1150	(Note 2)
1229	1148	1140	1215	1144	1150	(Note 3)
1240	1224	1140	1243	1224	1150	(Note 4)
1243	1224	1140	1243	1224	1150	(Note 5)
1249	1249	1249	1243	1224	1150	
1250	1249	1249	1250	1224	1150	
1314	1249	1249	1250	1224	1150	(Note 6)
1320	1249	1249	1320	1224	1150	
1322	1249	1249	1322	1224	1150	
1330	1249	1330	1322	1224	1330	
1345	1249	1345	1322	1224	1330	

NOTES:
1. Cards A1 through A5 did not change. Part number of A6Q1 and A6Q2 changed to 1884-0219.
2. Cards A1 through A5 did not change. Change made to power supply to bring up to UL, CSA, and IEC standards.
3. Cards A1 through A5 did not change. Change made to A11 ±20 volts Regulator.
4. Part no. of cards A1, A3, and A4 changed to 02100-60108, 02100-60109, and 02100-60110, respectively.
5. Date code 1243 is identical to date code 1240.
6. Cards A1 through A5 did not change. Assembly A7 changed mechanically.

REGULATOR BOARDS

These boards cannot be indiscriminately changed from "old" to "new." The A1 and A4 boards must be changed as a pair when changing to the "new" A4 board. The A1 and A3 boards, however, can be changed separately.

ASSY	PART NO.	ASSY	PART NO.
A1 (old)	02100-60046	A4 (old)	02100-60061
A1 (new)	02100-60108	A4 (new)	02100-60110
A3 (old)	02100-60047	A2	02100-60058
A3 (new)	02100-60109		

2100 POWER SUPPLY (CONT)

DC SUPPLY VOLTAGES

TEST JACK	READING		RIPPLE AND NOISE VOLT. TOL. P-P
	MIN.	MAX.	
+30	+29.0	+31.5	<20%
+20*	+19.8	+20.2	±1%
+12	+12.0	+13.1	<2%
+4.85	+4.80	+4.90	<2%
-2	-1.85	-2.5	<2%
-12	-12.0	-13.1	<2%
-20*	-19.8	-20.2	±1%

*@25°C (room temperature)

CURRENT AVAILABLE FOR I/O CARDS

SUPPLY VOLTAGE	CURRENT AVAILABLE DEPENDING ON MEMORY SIZE (AMPERES)					
	4K	8K	12K	16K	24K	32K
+30	0.1	0.1	0.1	0.1	0.1	0.1
+12	3.0	3.0	3.0	3.0	3.0	3.0
+4.85	23.6	23.6	22.7	22.7	21.6	20.8
-2	10.9	10.9	10.1	10.1	9.3	8.5
-12	3.0	3.0	3.0	3.0	3.0	3.0

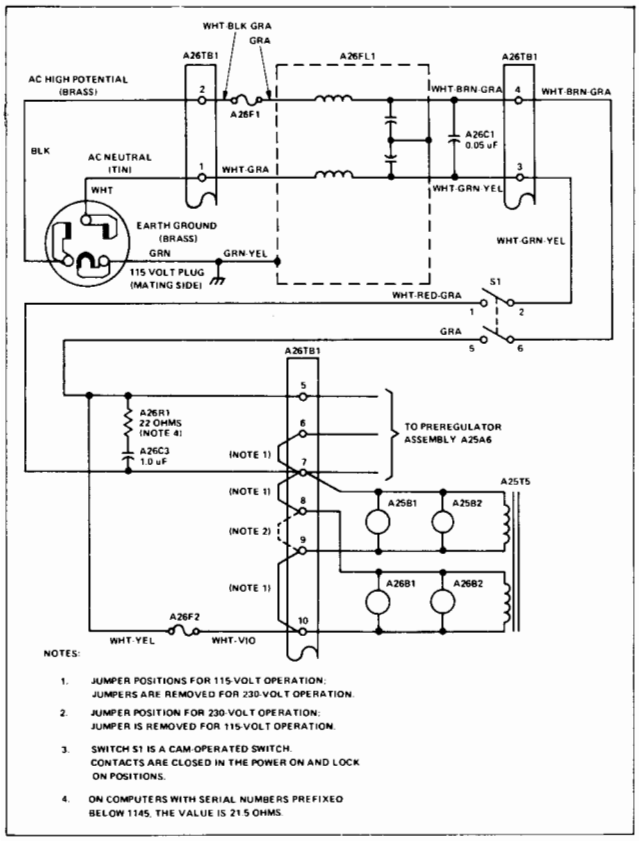
NOTE: The currents specified are available with the DMA accessory kit installed.

VOLTAGE RANGE FOR OVERVOLTAGE (CROWBAR TRIGGER CONDITION)

OUTPUT VOLTAGE	OUTPUT TERM.	OVERVOLTAGE (VDC) RANGE
-2	TB1-2,3	-2.8 to -3.1
+4.85	TB1-4,5	+5.3 to +5.75
-12	TB2-2	-14.0 to -15.5
+12	TB2-3	+14.0 to +15.5
-20	TB2-1	-23.5 to -27.0
+20	TB1-1	+23.5 to +25.5

2100 POWER SUPPLY (CONT)

AC POWER CONNECTIONS



When converting to 230V from 115V, or vice versa, change fuse current ratings as listed below. Also change power cord plug as described in 2100 Installation and Maintenance Manual.

VOLTAGE	A26F1	A26F2
115	12A	2A
230	6A	1A

2114A/B POWER SUPPLY

POWER REQUIREMENTS

LINE VOLTAGE:	115V ac ±10% single phase, 7A, or 230V ac ±10% single phase, 3.5A with stepdown transformer.
LINE FREQUENCY:	47.5 to 66 Hz
POWER CONSUMPTION:	800W maximum

ENVIRONMENTAL LIMITS

TEMPERATURE:	10° to 40°C (50° to 104°F)
RELATIVE HUMIDITY:	80% at 40°C (50°F)

VENTILATION

AIR FLOW:	400 cfm
HEAT DISSIPATION:	2200 BTU/hour, maximum

DIMENSIONS

HEIGHT:	12 inches
WIDTH:	16-3/4 inches
DEPTH:	24-3/8 inches

SUPPLY VOLTAGES

VOLTAGE BUS	VOLTS DC (MAX)*	VOLTS DC (MIN)**	AC RIPPLE V P-P
+5V	5.5	4.3	0.5
+12V	13.0	11.8	0.3
-12V	-13.0	-11.9	0.3
-2V	-2.8	-1.9	0.4
+30V	32.0	29.0	0.5
+30V Lamp	32.5	28.0	3.0
+20V	19.7***	19.3***	0.1

*High ac line (127 Vac), minimum computer load.
**Low ac line (103 Vac), maximum computer load.
***Depends upon ambient temperature: e.g., 19.5 ±0.2V dc at 25 ±2°C (77 ±3.6°F).

2116A/B POWER SUPPLY

POWER REQUIREMENTS

LINE VOLTAGE:	115V ac ±10%, single phase, 15A, or 230V ac ±10%, single phase, 7.5A
LINE FREQUENCY:	50 to 60 Hz
POWER CONSUMPTION:	1600W maximum

ENVIRONMENTAL LIMITS

TEMPERATURE:	0° to 55°C (32° to 131°F)
RELATIVE HUMIDITY:	95% at 40°C (50°F)

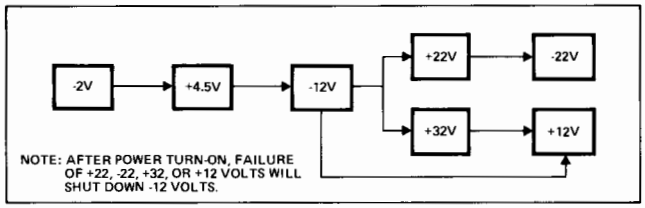
VENTILATION

AIR FLOW:	600 cfm
HEAT DISSIPATION:	5500 BTU/hour, maximum

DIMENSIONS

HEIGHT:	31-1/2 inches
WIDTH:	19 inches
DEPTH:	19-3/8 inches

POWER SUPPLY INTERDEPENDENCE



2116A/B POWER SUPPLY (CONT)

TROUBLESHOOTING HINTS

Shorting C56 on Logic Regulator A301 will disable the -12V Turn-Off circuit. This is sometimes desirable when troubleshooting one of the five regulated supplies affected by this circuit. It is often advisable to disengage all the circuit boards in the Memory and I/O section of the computer to reduce the current requirements on the faulty supply. Never remove all the circuit boards from the computer unless a load sufficient to draw 4A minimum is placed between the +4.5V supply and ground.

To enable the -2V supply to turn on when the +4.5V supply fails, jumper negative side of C54 on A301 to ground. Whenever troubleshooting any power supply, it is usually desirable to remove some of the circuit boards to reduce the current requirements on the faulty supply. The +4.5V supply may always draw up to 22.5A plus the current drawn by the -2V supply.

Note: Pin 11 of Regulator Board A301 must always have +4.5V on it; if not, it could indicate an open dc relay or open thermal switch (PSO line).

2116A/B POWER SUPPLY (CONT)

DC SUPPLY VOLTAGES

VOLTAGE	REGULATION (AC RIPPLE)	AMPS (MAX.)	BACKPLANE CURRENT (AMPS)			
			4K		8K	
			HALT	RUN	HALT	RUN
+4.5	1%	45	Refer to "Current Available and Requirements" table.			
-2.0	1%	22.5				
+12	1%	3				
-12	0.5%	3				
+22*	0.5%	1	0.16	0.46	0.32	0.62
-22**	0.5%	2.5	1.2	1.4	2.3	2.6
+32***	0.5%	2.5	0	2.0(TR=0)	0	2.0(TR=0)
+7†	none	3.0	(current for all lamps lit)			

†The 7V supply (full wave rectified and unfiltered) is used only for the front panel display lamps. One exception is the lamp behind the POWER pushbutton. This lamp is operated from the +12V supply and gives an indication of the status of the -12V Turn-Off circuit.

*+22V - (0.04) (T-25°C) V where T = ambient temperature of room
**-22V + (0.04) (T-25°C) V where T = ambient temperature of room
***+32V - (0.064) (T-25°C) V where T = ambient temperature of room

Note:

Memory voltage power transistors must all be balanced within ±10% of each other, otherwise the +20V or -20V might be dropped. It is also important that the +4.5V or -2V power transistors be within ±10% of each other.

2116A/B POWER SUPPLY (CONT)

CURRENT AVAILABLE AND REQUIREMENTS

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	3	3	22.5	*22.5
Computer and HP 2160A Power Supplies	3	3	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 8K Memory	540 ma	600 ma	15.2	26.4
Computer with 16K Memory	1.0	1.1	15.7	28.4
CURRENT AVAILABLE FOR OPTIONS				
Computer with 8K Memory	2.5	2.4	7.3	***11.3
Computer with 16K Memory	2.0	1.9	6.8	*** 9.8
Computer with 8K Memory and HP 2160A Power Supply Extender	2.5	2.4	17.3	***21.3
Computer with 16K Memory and HP 2160A Power Supply Extender	2.0	1.9	16.8	***19.8

NOTES: * Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 45 amperes.

** Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

*** Plus the current drawn from the -2V supply by the selected options.

2116C POWER SUPPLY

INTERNAL/EXTERNAL POWER REQUIREMENTS

REQUIREMENTS	SUPPLY CURRENTS (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply	6	6	22.5	*22.5
Computer and HP 2160A Power Supplies	6	6	32.5	**32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 8k Memory	0.15	0.25	14.3	23.0
Computer with 16k Memory	0.15	0.25	15.6	24.2
Computer with 24k Memory	0.15	0.25	16.9	25.4
Computer with 32k Memory	0.15	0.25	18.2	26.6
CURRENT AVAILABLE FOR OPTIONS				
Computer with 8k Memory	5.85	5.75	8.2	†13.8
Computer with 16k Memory	5.85	5.75	6.9	†13.9
Computer with 24k Memory	5.85	5.75	5.6	†14.0
Computer with 32k Memory	5.85	5.75	4.3	†14.1
Computer with 8k Memory and HP 2160A Power Supply Extender	5.85	5.75	18.2	†23.8
Computer with 16k Memory and HP 2160A Power Supply Extender	5.85	5.75	16.9	†23.9
Computer with 24k Memory and HP 2160A Power Supply Extender	5.85	5.75	15.6	†24.0
Computer with 32k Memory and HP 2160A Power Supply Extender	5.85	5.75	14.3	†24.1

NOTES: * Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 45 amperes.

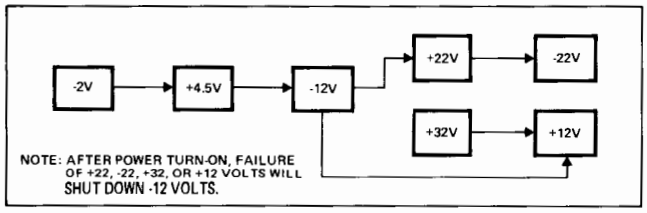
** Plus the current drawn from the -2V supply by the Computer with memory and options. Maximum available from +4.5V supply is 65 amperes.

† Plus the current drawn from the -2V supply by the selected options.

The power supply furnishes the following dc voltages to other sections of the computer (see 2116A/B power supply data on preceding pages):

-2V regulated
+4.5V regulated
+7V unregulated
±12V regulated
±20V regulated
+32V regulated
+35V unregulated

POWER SUPPLY INTERDEPENDENCE



2116C POWER SUPPLY (CONT)

±20V REGULATOR OUTPUT

TEMPERATURE (°C)	DC VOLTAGE RANGE			TEMPERATURE (°C)	DC VOLTAGE RANGE		
	MINIMUM	CENTER	MAXIMUM		MINIMUM	CENTER	MAXIMUM
0	20.50	21.00	21.50	28	19.38	19.88	20.38
1	20.46	20.96	21.46	29	19.34	19.84	20.34
2	20.42	20.92	21.42	30	19.30	19.80	20.30
3	20.38	20.88	21.38	31	19.26	19.76	20.26
4	20.34	20.84	21.34	32	19.22	19.72	20.22
5	20.30	20.80	21.30	33	19.18	19.68	20.18
6	20.26	20.76	21.26	34	19.14	19.64	20.14
7	20.22	20.72	21.22	35	19.10	19.60	20.10
8	20.18	20.68	21.18	36	19.06	19.56	20.06
9	20.14	20.64	21.14	37	19.02	19.52	20.02
10	20.10	20.60	21.10	38	18.98	19.48	19.98
11	20.06	20.56	21.06	39	18.94	19.44	19.94
12	20.02	20.52	21.02	40	18.90	19.40	19.90
13	19.98	20.48	20.98	41	18.86	19.36	19.86
14	19.94	20.44	20.94	42	18.82	19.32	19.82
15	19.90	20.40	20.90	43	18.78	19.28	19.78
16	19.86	20.36	20.86	44	18.74	19.24	19.74
17	19.82	20.32	20.82	45	18.70	19.20	19.70
18	19.78	20.28	20.78	46	18.66	19.16	19.66
19	19.74	20.24	20.74	47	18.62	19.12	19.62
20	19.70	20.20	20.70	48	18.58	19.08	19.58
21	19.66	20.16	20.66	49	18.54	19.04	19.54
22	19.62	20.12	20.62	50	18.50	19.00	19.50
23	19.58	20.08	20.58	51	18.46	18.96	19.46
24	19.54	20.04	20.54	52	18.42	18.92	19.42
25	19.50	20.00	20.50	53	18.38	18.88	19.38
26	19.46	19.96	20.46	54	18.34	18.84	19.34
27	19.42	19.92	20.42	55	18.30	18.80	19.30

NOTE: Voltages listed are negative for the -20 volt regulator.

2116C POWER SUPPLY (CONT)

VOLTAGE ADJUSTMENTS

ADJ SEQ	NOMINAL VOLTAGE	ADJUST	VOLTAGE RANGE		
			MIN	CENTER	MAX
1st	-2	R76*	-1.980	-2.000	-2.020
2nd	+4.5	R66*	+4.455	+4.500	+4.545
3rd	-12	R125**	-11.88	-12.00	-12.12
4th	+20†	R140**	+19.50	+20.00	+20.50
5th	-20†	R155**	-19.50	+20.00	-20.50
6th	+12	R96*	+11.88	+12.00	+12.12

NOTES:
*Situated on Logic Supply Regulator Card A301.
**Situated on Memory Supply Regulator Card A302.
†@25°C (room temperature)

2160 POWER SUPPLY EXTENDER

POWER REQUIREMENTS

LINE VOLTAGE:	115V ac ±10%, single phase, 3A or 230V ac ±10%, single phase, 1.5A
LINE FREQUENCY:	47 to 66 Hz

DC OUTPUTS: 20A at +4.50 ±0.14V dc, ripple <10m V rms
10A at -2.0 ±0.1V dc, ripple <10m V rms

ENVIRONMENTAL LIMITS

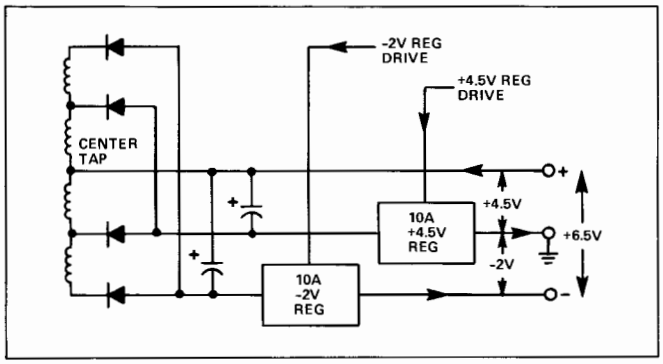
TEMPERATURE:	0° to 55°C (32° to 132°F)
RELATIVE HUMIDITY:	95% at 40°C (104°F)

HEAT DISSIPATION: 1180 BTU/hour

DIMENSIONS

HEIGHT:	6-3/4 inches (172 mm)
WIDTH:	16-3/4 inches (426 mm) without rack-mount kit
DEPTH:	18-3/4 inches (464 mm)

-2V AND +4.5V INTERCONNECTIONS



2160 POWER SUPPLY EXTENDER (CONT)

INTERNAL/EXTERNAL POWER REQUIREMENTS

REQUIREMENTS	SUPPLY CURRENT (AMPERES) -2V	SUPPLY CURRENT (AMPERES) +4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES		
HP 2115A Computer/HP 2161A Power Supply	25.0	*25.0
HP 2115A Computer/HP 2161A Power Supply with HP 2160A Power Supply Extender	35.0	**35.0
HP 2116 family Computer power supplies	22.5	***22.5
HP 2116 family Computer power supplies with HP 2160A Power Supply Extender	32.5	†32.5
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS		
HP 2115A Computer/HP 2161A Power Supply with 4K Memory or 8K Memory	15.0	26.0
HP 2116A Computer with 4K Memory	13.5	24.0
HP 2116A Computer with 8K Memory	14.0	28.0
HP 2116B Computer with 8K Memory	15.2	26.4
HP 2116B Computer with 16K Memory	15.7	28.4
HP 2116C Computer with 8K Memory	14.3	23.0
HP 2116C Computer with 16K Memory	15.6	24.2
HP 2116C Computer with 24K Memory	16.9	25.4
HP 2116C Computer with 32K Memory	18.2	26.6
CURRENT AVAILABLE FOR OPTIONS		
HP 2115A Computer/HP 2161A Power Supply with 4K Memory or 8K Memory	10.0	††14.0
HP 2115A Computer/HP 2161A Power Supply with 4K Memory or 8K Memory and HP 2160A Power Supply Extender	20.0	††24.0
HP 2116A Computer with 4K Memory	9.0	††12.0
HP 2116A Computer with 8K Memory	8.5	†† 8.5
HP 2116A Computer with 4K Memory and HP 2160A Power Supply Extender	19.0	††22.0
HP 2116A Computer with 8K Memory and HP 2160A Power Supply Extender	18.5	††18.5
HP 2116B Computer with 8K Memory	7.3	††11.3
HP 2116B Computer with 16K Memory	6.8	†† 9.8
HP 2116B Computer with 8K Memory and HP 2160A Power Supply Extender	17.3	††21.3
HP 2116B Computer with 16K Memory and HP 2160A Power Supply Extender	16.8	††19.8
HP 2116C Computer with 8K Memory	8.2	††13.8

2160 POWER SUPPLY EXTENDER (CONT)

REQUIREMENTS	SUPPLY CURRENT (AMPERES)	
	-2V	+4.5V
CURRENT AVAILABLE FOR OPTIONS (Continued)		
HP 2116C Computer with 16K Memory	6.9	††13.9
HP 2116C Computer with 24K Memory	5.6	††14.0
HP 2116C Computer with 32K Memory	4.3	††14.1
HP 2116C Computer with 8K Memory and HP 2160A Power Supply Extender	18.2	††23.8
HP 2116C Computer with 16K Memory and HP 2160A Power Supply Extender	16.9	††23.9
HP 2116C Computer with 24K Memory and HP 2160A Power Supply Extender	15.6	††24.0
HP 2116C Computer with 32K Memory and HP 2160A Power Supply Extender	14.3	††24.1

NOTES:

* Plus the current drawn from the -2 volt power supply by the computer with memory and options. Maximum available measurable current is 50 amperes.

** Plus the current drawn from the -2 volt power supply by the computer with memory and options. Maximum available measurable current is 70 amperes.

*** Plus the current drawn from the -2 volt power supply by the computer with memory and options. Maximum available measurable current is 45 amperes.

† Plus the current drawn from the -2 volt power supply by the computer with memory and options. Maximum available measurable current is 65 amperes.

†† Plus the current drawn from the -2 volt power supply by selected options.

An inspection of the current values in the columns above will show that the -2 volt and +4.5 volt power supplies in the HP 2160A Power Supply Extender are both 10 ampere capacity power supplies. Capacity of both supplies is shown in the total measurable current figure designated in notes above.

2160 POWER SUPPLY EXTENDER (CONT)

OPTION CURRENT REQUIREMENTS

OPTION		SUPPLY CURRENT REQUIRED (AMPERES)	
		-2V	+4.5V
12569A	Memory Parity Check (HP 2116A-002)	0.50	0.53
12570A	Memory Test (HP 2116A-003)	0.48	0.91
12571A	HP 2150A-001 I/O Expansion, for HP 2115A or HP 2116A Computer	0.80	3.00
12572A	HP 2150A-002 Second Additional 4K Memory, for HP 2115A or HP 2116A Computer	0.60	1.50
12574A	HP 2150A-004 Extender Memory Parity Check, for HP 2115A or HP 2116A Computer	0.03	0.00
12578A	Direct Memory Access (HP 2116B)	0.72	6.20
12578A-001	Direct Memory Access (HP 2115A and HP 2116A)	0.72	6.20
12579A	Extended Arithmetic Unit (HP 2115A, HP 2116A/B)	3.30	4.68
12580A	Memory Parity Check (HP 2115A)	0.50	0.91
12581A	Memory Protect (HP 2116B)	0.90	1.80
12586A	Power Fail with Auto Restart (HP 2115A)	0.04	0.25
12591A	Memory Parity Check (HP 2116B)	0.65	0.90
12594A	HP 2151A I/O Expansion, for HP 2115A	0.80	2.76
12596A	HP 2151A I/O Expansion, for HP 2116 Computer family	0.80	2.76
12598A	Memory Parity Error with Interrupt (HP 2114B)	0.13	0.86
12612A	HP 2150B-001 I/O Expansion, for HP 2116B Computer	0.90	3.90
12613A	HP 2150B-002 Second Additional 8K Memory, for HP 2116B Computer	0.90	0.90

2161 POWER SUPPLY

INPUT

115/230 Vac ±10%
50 to 60 Hz
9A at 115 Vac - Full load
4.5A at 230 Vac - Full load

OUTPUT

-2Vdc Regulated at 25A
+4.5Vdc Regulated at 50A
-12Vdc Regulated at 3A
+12Vdc Regulated at 3A
+20Vdc Regulated at 3A
+33Vdc Unregulated
+6Vdc Unregulated, unfiltered

ENVIRONMENTAL

Temperature: 10° to 40°C (50° to 104°F)
Relative Humidity: 95% at 40°C (104°F)

PHYSICAL DIMENSIONS

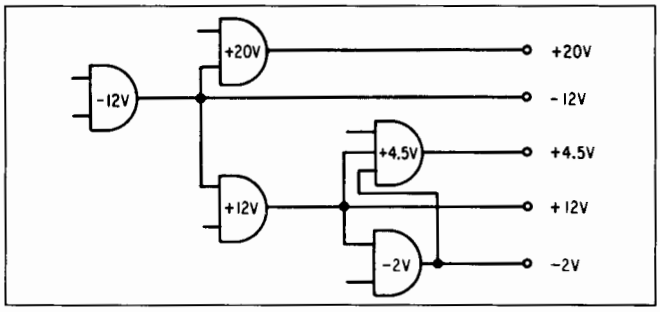
Width: 16-3/4 inches
Height: 10-3/4 inches
Depth: 20-1/2 inches
Weight: 95 pounds

POWER SUPPLY ADJUSTMENTS

SUPPLY	ADJUST TO	ADJUSTMENT	AC RIPPLE V P-P
-12V	-12.00V	R69	0.01
+12V	+12.00V	R55	0.01
+20V	*	R43	0.02
+4.5V	+4.50V	R14	0.01
-2V	-2.00V	R29	0.02

*+19.5V - (0.088)(T)(25) where T is ambient temperature in °C.

REGULATED SUPPLY LOGIC



2161 POWER SUPPLY (CONT)

CURRENT AVAILABLE AND REQUIREMENTS

REQUIREMENTS	SUPPLY CURRENT (AMP)			
	+12V	-12V	-2V	+4.5V
CURRENT AVAILABLE FROM POWER SUPPLIES				
Computer Power Supply (HP 2161A)	3	3	25.0	*25.0
Computer and 2160A Power Supplies	3	3	35.0	**35.0
CURRENT REQUIRED BY COMPUTER WITH NO PROCESSOR OR INPUT/OUTPUT OPTIONS				
Computer with 4K Memory	0.4	0.4	15.0	26.0
Computer with 8K Memory	0.6	0.6	15.0	26.0
CURRENT AVAILABLE FOR OPTIONS (with 2161A)				
Computer with 4K Memory	2.6	2.6	10.0	***14.0
Computer with 8K Memory	2.4	2.4	10.0	***14.0
Computer with 4K Memory and 2160A Power Supply	2.6	2.6	20.0	***24.0
Computer with 8K Memory and 2160A Power Supply	2.4	2.4	20.0	***24.0

NOTES: *Plus the current drawn from the -2V supply by the computer with memory and options. Maximum available from +4.5V supply is 50 amperes.

**Plus the current drawn from the -2V supply by the computer with memory and options. Maximum available from +4.5V supply is 70 amperes.

***Plus the current drawn from the -2V supply by the selected options.

All figures based on environmental temperatures of 0° to 40°C.

PERIPHERAL INTERFACE CURRENT DRAIN

INTERFACE	(AMPS) +4.5V	-2V
12531B Buffered Teleprinter Interface	0.76	0.05
12531C Buffered Teleprinter Interface	0.76	0.05
12531D High-Speed Terminal Interface	0.76	0.05
12532A High-Speed Punched Tape Interface	1.10	0.48
12538A Magnetic Tape I/O Interface	6.00	4.20
12538B Magnetic Tape I/O Interface	6.00	4.20
12539A/B Time Base Generator	1.10	0.42
12539C Time Base Generator	0.75	0.016
12540A Bell System Data Phone I/O Interface	1.40	0.90
12551B Relay Output Register	0.60	0.39
12551B-01 Relay Register With Interrupt	1.1	0.59
12554A 16-Bit Duplex Register	1.11	0.07
12555B Digital-To-Analog Converter	2.4	1.80
12557A Cartridge Disc Interface	3.5	0.17
12558A Card Reader Interface	1.30	0.07
12559A 9-Track Magnetic Tape Unit Interface	2.58	0.24
12560A Digital Plotter Interface	0.90	0.48
12565A Disc Interface	3.5	0.17
12566A/B Microcircuit Interface	1.10	0.05
12578A Direct Memory Access	6.2	0.72
12584A-002 Teleprinter Multiplexer	2.20	0.125
12584B/C Teleprinter Multiplexer	2.2	0.20
12587A/B Asynchronous Data Set Interface	1.6	0.07
12589A Automatic Dialer	0.65	0.055
12593A I/O Extender Interface	1.95	0.68
12594A I/O Extender Interface	2.76	1.30
12595A Multiplexed I/O Kit	1.0	0.05
12596A I/O Extender Interface	2.76	1.30
12597A 8-Bit Duplex Register	0.75	0.05
12597A-002 Tape Reader Interface	0.75	0.05
12597A-003 Tape Punch Interface	0.75	0.05
12597A-005 Tape Punch Interface	0.75	0.05
12602A/B Computer Interface for Optical Mark Reader	1.30	0.07
12606A Disc Interface	2.40	0.24
12606B Disc Memory Interface	2.40	0.24
12607A Direct Memory Access	1.8	0.47
12610A/B Drum Memory Interface	2.40	0.24
12610C Disc Memory Interface	2.40	0.24
12612A I/O Extender Kit	5.0	1.6
12616A High-Speed I/O Channel	1.8	0.47
12617A Line Printer Interface	1.11	0.06
12618A Synchronous Data Set Interface	1.3	0.10
12620A Breadboard Interface Kit	0.315	0.045
12621A Synchronous Data Set Interface	1.5	0.13
12622A Synchronous Data Set Interface	1.3	0.10

*Current drain from ±12V supplies not shown because individual or collective requirements do not approach power supply output.

PERIPHERAL INTERFACE CURRENT DRAIN* (CONT)

INTERFACE	(AMPS) +4.5V	-2V
12653A Line Printer Interface	1.10	0.05
12845A Line Printer Interface	1.79	0.10
12845A-001 Line Printer Interface	1.79	0.10
12849A Controller Microcircuit Interface	1.74	0.086
12849A-001 Controller Microcircuit Interface	2.30	0.15
12875A Processor Interconnect Kit	2.20	0.10
12880A Keyboard-Display Terminal Interface	0.76	0.05
12882A Card Reader Interface	0.97	0.43
12894A Multiplexed I/O Kit	1.0	0.05
12895A Direct Memory Access	2.9	1.2
12896A Direct Memory Access	0.5	0.2
12901A Floating Point Hardware Kit	0.78	
12908A/B Writeable Control Store	4.6	0.15
12909A Programmable ROM Writer	0.5	0.04
12920A Asynchronous Multiplexer	5.53	0.258
12920A-001 Asynchronous Multiplexer	6.97	0.360
12924A Card Reader Subsystem	0.97	0.43
12930A Universal Interface	2.2	0.1
13181A Digital Magnetic Tape Unit Interface	3.0	0.50
13182A Digital Magnetic Tape Unit Interface	2.8	0.085
13183A Digital Magnetic Tape Unit Interface	3.0	0.10
13184A Digital Magnetic Tape Unit Interface	2.65	0.17
13185A Microfilmer Interface	1.4	0.12
13210A Disc Drive Interface	4.0	0.14

*Current drain from ±12V supplies not shown because individual or collective requirements do not approach power supply output.

POWER SUPPLIES

2100 SERIES COMPUTER POWER REQUIREMENTS

		CURRENT AVAILABLE TO I/O				
		+30V	+5.0V +4.85V	-2.0V	-12.0V	+12.0V
COMPUTER:						
2100A + 32K MEMORY + DMA		0.10A	20.8A	8.5A	3.0A	3.0A
21-M/10 + 32K MEMORY,DCPC,MAX CTRL STR			6.0A	2.0A	1.0A	1.0A
21-M/20 + 32K MEMORY,DCPC,MAX CTRL STR			13.0A	4.0A	1.5A	1.5A

			CURRENT REQUIRED			
		+30V	+5.0 +4.85V	-2.0V	-12.0V	+12.0V
2100A OPTIONAL PROCESSOR ASSYS:						
MEMORY 4K			0.9A	0.8A		
MEMORY 8K			0.9A	0.8A		
12894A	MULTIPLEXED I/O 12595-6001		1.0A	0.05A		
12895A	DMA 12895-60001		2.5A			
12901A	FLOATING POINT		0.78A			
12907A	FAST FORTRAN		1.5A			
12908A	WCS 12908-60006		4.6A	0.15A		
21MX OPTIONAL PROCESSOR ASSYS:						
12892A	MEMORY PROTECT 2108		2.5A	0.20A		
12897A	DUAL CHANNEL PORT CONTROLLER		3.0A	0.20A		
12944A	POWER FAIL RECOVERY 3 BDS		0 A	0 A	0 A	0 A
	USER CONTROL STORE BASE SET		1.03A			
	USER CONTROL STORE 1K		1.2A			
12978A	WRITEABLE CTRL STR -60006		4.6A	0.15A		
	MEMORY CONTROLLER 21-X/1		1.14A			
	MEMORY CONTROLLER 21-X/2		1.50A			
	MEMORY MODULE 2101A 16K		0.412A			
	MEMORY MODULE 2102A 8K		0.380A			
	MEMORY EXPANSION MODULE 2108		3.50A			

			CURRENT REQUIRED			
		+30V	+5.0V +4.85V	-2.0V	-12.0V	+12.0V
2100 I/O ASSYS POWER SUPPLY LOAD						
2116-6002	TAPE READER 2737 INTFC		1.1A	0.48A	0.01A	0.03A
2116-6046	2401C DVM INTFC AMD		0.42A	0.24A	0.30A	0.00A
2116-6123	2911 X-BAR SCANNER INTFC					
12531-60022	TELEPRINTER INTFC		0.76A	0.05A	0.10A	0.05A
12531-60025	HP-SPD TELEPRINTER INTFC		0.76A	0.05A	0.01A	0.24A
12539-60003	TIME BASE GENERATOR		0.75A	0.016A		
12551-6001	RELAY OUTPUT REGISTER		0.6A	0.39A		0.24A
12551-6002	RELAY READ BACK REGISTER		1.1A	0.59A		0.24A
12554-60023	16-BIT DUPLEX REGISTER +		1.11A	0.06A	0.03A	0.023A
12554-60024	16-BIT DUPLEX REGISTER -		1.11A	0.06A	0.25A	0.025A
12554-60029	16-BIT DUPLEX REG DTL		1.11A	0.06A	0.25A	0.025A
12555-60001	D-A OUTPUT		2.40A	1.80A	0.36A	0.50A
12556-6002	40-BIT OUTPUT REGISTER +		0.9A	0.08A	0.01A	0.15A
12556-60022	40-BIT OUTPUT REGISTER GND		0.9A	0.08A	0.01A	0.15A
12560-6001	CAL COMP PLOTTER INTFC		0.9A	0.48A	0.06A	
12564-60001	A-D CONVERTER					
12565-60001	2883 DISC INTFC DATA		3.5A	0.17A		
12565-60002	2883 DISC INTFC COMMAND		3.5A	0.17A		
12566-60024	DUPLEX REGISTER GND MICRO CRT		1.1A	0.05A		
12566-60025	DUPLEX REGISTER + MICRO CRT		1.1A	0.05A		
12576-60031	2402A PROGRAMMER INTFC		0.46A	0.06A	0.05A	0.005A
12576-60032	2912A SCANNER INTFC AMD		0.48A	0.07A	0.01A	0.03A
12584-60135	MULTIPLEXER TTY INTFC		2.2A	0.20A	0.04A	0.10A
12587-60004	ASYNC DATA SET INTFC		1.6A	0.07A	0.045A	0.08A
12589-6001	801 AUTO CALLING INTFC		0.65A	0.055A	0.05A	0.05A
12597-6001	8-BIT DUPLEX REGISTER		0.75A	0.05A	0.02A	0.05A
12597-6002	8-BIT DUPLEX REGISTER NEG		0.75A	0.05A	0.05A	0.02A
12602-60022	2761A MARK CARD READER INTFC		1.30A	0.070A	0.030A	0.090A
12604-60001	DATA SOURCE INTFC	0.04	1.1A	0.35A	0.024A	0.01A
12606-6001	2770 DISC INTFC		1.2A	0.38A		
12606-6002	2700 DISC INTFC		1.2A	0.38A		
12610-6001	2766 DISC MEMORY INTFC DATA		1.2A	0.12A		
12610-6002	2766 DISC MEMORY INTEC COMM		1.2A	0.12A		

2100 SERIES COMPUTER POWER REQUIREMENTS

		CURRENT REQUIRED			
2100 I/O ASSYS POWER SUPPLY LOAD					
12621-60001	SYNC DATA SET INTFC REC.	1.4A	0.12A	0.35A	0.048A
12622-60001	SYNC DATA SET INTFC XMIT	1.4A	0.12A	0.35A	0.048A
12653-60002	2767 LINE PRINTER INTFC	1.1A	0.05A		
12657-6001					
12661-6001	DIGITAL VOLTAGE SOURCE	1.42A	0.06A	0.014A	0.137A
12661-6002	DIGITAL VOLTAGE SOURCE	1.42A	0.06A	0.014A	0.137A
12665-60001	2570 SERIAL DATA INTFC	1.6A	0.07A	0.095A	0.090A
12773-60001	COMPUTER MODEM INTFC	1.6A	0.07A	0.040A	0.040A
12841-6001	64 CHARACTER HOLLERITH				
12843-6001	64 CHARACTER DIAL				
12845-60001	LINE PRINTER 2607	1.8A	0.10A		
12849-60001	MICROCIRCUIT CONTROL GND	1.74A	0.086A		
12849-60002	MICROCIRCUIT CONTROL POS	1.74A	0.086A		
12880-60001	CRT INTFC	0.76A	0.05A	0.01A	0.24A
12889-60001	HARDWIRED SERIAL INTFC	2.25A	0.01A	0.05A	0.125A
12920-60001	MULTIPLEXER DATA USC	2.05A	0.031A	0.121A	
12920-60002	MULTIPLEXER DATA LSC	2.04A	0.125A	0.120A	0.085A
12922-60001	MULTIPLEXER CONTROL	1.44A	0.102A	0.236A	0.156A
12924-60001	CARD READER 2892	0.97A	0.440A		
12930-60001	UNIVERSAL INTFC	1.8A	0.10A		
12930-60006	UNIVERSAL INTFC	2.2A	0.10A		
12930-60005	UNIVERSAL INTFC	2.2A	0.10A		
12936-60001	PRIVILEGED INTERRUPT FENCE	0.30A	0.03A		
12962-60001	INTERFACE CARD				
12966-60001	ASYNC DATA INTFC	1.95A	0.066A	0.059A	0.018A
12967-60001	SYNC DATA INTFC	1.75A	0.06A	0.024A	0.013A
12968-60001	ASYNC DATA INTFC	1.32A	0.052A	0.035A	0.012A
13181-60010	MAG TAPE CONTROLLER	1.45A	0.045A		
13181-60040	MAG TAPE CONTROLLER	1.45A	0.045A		
13181-60070	MAG TAPE CONTROLLER	1.45A	0.045A		
13182-60010	MAG TAPE	1.45A	0.045A		
13182-60040	MAG TAPE	1.45A	0.045A		
13182-60090	MAG TAPE	1.45A	0.045A		
13183-60001	7970 MAG TAPE	1.30A	0.040A		
13183-60004	7970 MAG TAPE	1.30A	0.040A		
13183-60007	7970 MAG TAPE	1.30A	0.040A		
13184-60008	MULTI-FORMAT MAG TAPE	1.33A	0.085A		
13184-60009	MULTI-FORMAT MAG TAPE	1.33A	0.085A		
13185-60008	COMMAND INTFC	0.70A	0.060A		
13185-60009	COMMAND INTFC	0.70A	0.060A		
13210-60000	DISC INTFC	1.89A	0.067A	0.047A	0.03A
13210-60004	DISC INTFC	1.89A	0.067A	0.047A	0.03A
LIST END ****					

INPUT/OUTPUT

CONTENTS PAGE

RS-232C SIGNAL INTERFACE

DATA SET PIN	CIRCUIT	SIGNAL	HP MPX PIN
1	AA	Protective ground	1
2	BA	Transmitted data	3
3	BB	Received data	2
4	CA	Request to send	8
5	CB	Clear to send	22
6	CC	Data set ready	20
7	AB	Signal ground (common return)	7
8	CF	Carrier detect	4
9	–	(Reserved for testing	–
10	–	(Reserved for testing)	–
12	SCF	Secondary carrier detect	–
13	SCB	Secondary clear to send	–
14	SBA	Secondary transmitted data	12
15	DB	Transmission signal element timing (DCE source)	–
16	SBB	Secondary received data	11
17	DD	Receiver signal element timing (DCE source)	–
19	SCA	Secondary request to send	–
20	CD	Data terminal ready	6
21	CG	Signal quality detector	–
22	CE	Ring indicator	–
23	CH/CI	Data signal rate selector (DTE/DCE source)	23
24	DA	Transmit signal element timing (DTE source)	–

INTERFACE COMPATIBILITY

INTERFACE		PERIPHERAL	DIAG. AVAIL.	2100A/S	2114		2115A	2116			2105,08
					A	B		A	B	C	
12531A	Serial TTY	2752	Yes	X	X	X	X	X	X		
12531B	Buffered TTY	2752/2754	Yes	X	X	X	X	X	X	X	X
12531C	Buffered TTY	2752/2754	Yes	X	X	X	X	X	X	X	X
12531D	High-Speed Terminal		Yes	X	X	X	X	X	X	X	X
12532A	Tape Reader	2737	Yes	X	X	X	X	X	X	X	X
12536A	Tape Punch	2753	Yes	X	X	X	X	X	X	X	X
12538A	Mag. Tape I/O	2020	Yes			X	X	X	X	X	
12539A	Time Base Generator		Yes	X	X	X	X	X	X	X	
12539B	Time Base Generator		Yes	X	X	X	X	X	X	X	X
12539C	Time Base Generator		Yes	X	X	X	X	X	X	X	X
12540A	Bell System Dataphone I/O		Yes	X	X	X	X	X	X	X	
12549A	General Purpose Register	GP	Yes		X	X	X	X	X	X	X
12551A	Relay Register	GP	Yes	X	X	X	X	X	X	X	X
12551B	Relay Register	GP	Yes	X	X	X	X	X	X	X	X
12554A	16-Bit Duplex Register	GP	Yes	X	X	X	X	X	X	X	X
12555A	D/A Converter	GP	Yes		X	X	X	X	X	X	
12555B	D/A Converter	GP	Yes	X	X	X	X	X	X	X	

INTERFACE COMPATIBILITY (CONT)

INTERFACE		PERIPH-ERAL	DIAG. AVAIL.	2100A/S	2114		2115A	2116			2105/08
					A	B		A	B	C	
12557A	Cartridge Disc	2870/2871	Yes	X		X	X	X	X	X	U
12559A	Magnetic Tape	3030	Yes	X		X	X	X	X	X	
12560A	Digital Plotter	2791	Yes	X	X	X	X	X	X	X	U
12565A	Disc File	2883/84/85	Yes	X		X	X	X	X	X	X
12566A	16-Bit Microcircuit	GP	Yes		X	X	X	X	X	X	
12566B	16-Bit Microcircuit	GP	Yes	X	X	X	X	X	X	X	X
12578A	DMA*		Yes				X	X	X	X	
12582A	Direct Memory Increment		Yes				X	X	X		
12584A	16-Port TTY Multiplex		Yes	X	X	X	X	X	X	X	U
12584B	16-Port TTY Multiplex		Yes	X	X	X	X	X	X	X	U
12584C	16-Port TTY Multiplex		Yes	X	X	X	X	X	X	X	U
12587A	Async Data Set		Yes	X	X	X	X	X	X	X	U
12587B	Async Data Set		Yes	X	X	X	X	X	X	X	U
12589A	Auto Dialer		Yes	X	X	X	X	X	X	X	U
12593A	I/O Extender	2151	No		X	X					
12594A	I/O Extender	2151	No				X				
12595A	Multiplex I/O	GP	No	X	X	X					
12596A	I/O Extender	2151	No					X	X	X	
12597A	8-Bit Duplex Register	GP	Yes	X	X	X	X	X	X	X	X
12602A	Optical Mark Reader	2761-007	Yes		X	X	X	X	X	X	
12602B	Optical Mark Reader	2761-008	Yes	X	X	X	X	X	X	X	U
12606A/B	Disc Memory	2770/71/72	Yes			X	X	X	X	X	U
12607A	DMA	–	Yes			X					
12610A/B	Disc Memory	2773/74/75	Yes	X		X	X	X	X	X	U
12610C	Disc Memory	2766	Yes	X		X	X	X	X	X	U
12612A	I/O Extender	2150	Yes					X	X		
12616A	High-Speed I/O Chan.	GP	Yes			X					
12617A	Line Printer	2778	Yes	X	X	X	X	X	X	X	
12618A	Sync Data Set		Yes	X	X	X	X	X	X	X	U
12620A	Breadboard	GP	Yes	X	X	X	X	X	X	X	X
12621A	Sync Data Set (Rcv)		Yes	X	X	X	X	X	X	X	U
12622A	Sync Data Set (Xmt)		Yes	X	X	X	X	X	X	X	U
12653A	Line Printer	2767	Yes	X	X	X	X	X	X	X	X
12845A	Line Printer	2610/1614	Yes	X	X	X	X	X	X	X	X
12849A	Controller μCircuit	2870	Yes	X	X	X	X	X	X	X	
12875A	Processor Interconnect		Yes	X	X	X	X	X	X	X	X
12875B	Processor Interconnect		Yes	X	X	X	X	X	X	X	X
12880A	Keyboard-Display Term.	2600	Yes	X	X	X	X	X	X	X	X
12882A	Card Reader	2891	Yes	X	X	X	X	X	X	X	X
12889A	Hardwired Serial I/O		Yes	X	X	X	X	X	X	X	X
12894A	Multiplex I/O		No	X	X	X					
12895A	DMA		Yes	X							
12908A	WCS		Yes	X							
12908B	WCS**		Yes	X							X
12909A	PROM Writer		Yes	X							X
12909B	PROM Writer		Yes	X							X
12920A	Async Multiplexer			X	X	X	X	X	X	X	
12920B	Async Multiplexer			X	X	X	X	X	X	X	X
12930A	Universal Interface	GP	Yes	X	X	X	X	X	X	X	X
12966	Async Data Interface			X				X	X	X	X
12967	Sync Data Interface			X				X	X	X	X
12968	Async Data Interface			X				X	X	X	X
12978A	WCS			X							X
13181A	Digital Mag. Tape Unit	7970 9T	Yes	X	X	X	X	X	X	X	X
13182A	Digital Mag. Tape Unit	7970 7T	Yes	X	X	X	X	X	X	X	X
13183A	Digital Mag. Tape Unit	7970E	Yes	X		X	X	X	X	X	X
13184A	Digital Mag. Tape Unit	7970E-215	Yes	X		X	X	X	X	X	X
13185A	Microfilmer	–	Yes	X							U
13210A	Disc Drive	7900/7901	Yes	X		X	X	X	X	X	X

U Untested

*2116A serial prefix 803 or 807

**Should be Date Code 1436 or higher for 21MX

MAJOR PERIPHERAL DIAGNOSTIC

	BINARY	MOD	2105/8/12	210OA/S	2116C	2116B	2116A	2115A	2114B	2114A
2607	24340-16001	24340-90004	*	*	*	*	*	*	*	*
2610/14	24366-16001	24366-90001	*	*	*	*	*	*	*	*
2613/18	02618-16001	02618-90006	*	*	*	*	*	*	*	*
2640	02640-16001	02640-90020	*	*	*	*	*	*	*	*
2752/2754	12531-16001	12531-90042	*	*	*	*	*	*	*	*
2762A/B	02762-16001		*	*	*	*	*	*	*	*
2767	12984-16001	12984-90005	*	*	*	*	*	*	*	*
2883/4	12965-16001	12965-90009	*	*	*	*	*	*	*	
2892	12924-16001	12924-90006	*	*	*	*	*	*	*	*
2894	12989-16001	12989-90001	*	*						
7900/7901	12960-1600	12960-90003	*	*	*	*	*	*	*	
7970A/B/E	13181-16001	13181-90005	*	*	*	*	*	*	*	*
7970B	13028-60001	13182-90002	*	*	*	*	*	*	*	
12920A/B	12920-16001/2	12920-90009	*	*	*	*	*	*	*	
Reader/Punch	12597-16001	12597-90031	*	*	*	*	*	*	*	*
TBG	12539-16001	12539-90011	*	*	*	*	*	*	*	*

COMMON DATA SECTION

HP COMPUTERS I/O TIMING

	2114		2115/2116		2100A		21MX	
SIGNAL	DMA	CPU	DMA	CPU	DMA	CPU	DMA	CPU
STC	T34	T4	T34	T4	T3[1]	T4	T3	T4
CLC	T45	T4	T45	T4	T34[1]	T4	T3-T4	T4
CLF	T45	T4	T45	T4	T3[1]	T4	T3	T4
IOG	To-T7	T3-T0	T0-T5	T3-T0	T6-T5[2]	T3-T6		T3-T5
IOO	T34	T34	T34	T34	T34	T34	T3-T4	T3-T4
EDT	T45	–	T45	–	T45	–	T4-T5	T4-T5
SC	T0-T7	T3-T1	T0-T5	T3-T0	T6-T5[2]	TN-T6[4]	–	–
ENF	T2	T2	T2	T2	T2	T2	T2	T2
STF	–	T3	–	T3	–	T3	–	T3
IOCO	T45	T45	T45	T45	T45[6]	T45	–	–
SIR	T5	T5	T5	T5	T5	T5	T5	T5
T310	T3	T3	T3	T3	T3	T3	–	–
CRS	–	T4 or T5	–	T4 or T5	–	T4 or T5	T5	T5
POPIO	–	T5	–	T5	–	T5	T5	T5
SFS	–	T3-T0	–	T3-T0	–	T3-T6	–	T3-T5
IAK	–	T1	–	T1	–	T6[5]	T6	T6
IOI	T2	T45	T2	T45	T23[3]	T45	T2-T3	T4-T5

The 2100A I/O structure has five 196 nsec time periods, T2, T3, T4, T5, T6. Time periods T0, T1, and T7 were eliminated to enable DMA to steal consecutive 980 nsec memory cycles. DMA transfers start at the leading edge of T6 and end at the leading edge of the following T6. All I/O instructions are fetched in Phase 1A and executed in Phase 3 with the exception of I/O instruction in interrupt locations.

The 21MX I/O structure for five (T2-T6) 325 nsec time periods and I/O cycle is for T2 thru T6 and is 1.62 usec long.

1. Time periods of these signals were changed to allow DMA Transfer Rates.
2. Signal is high during entire PN5 on a DMA transfer.
3. Changed to enable DMA extension to 2155 I/O Extender.
4. If I/O instruction being executed is in A or B register the select code becomes valid 150 nsec into T2 of Phase 1A. If instruction is in memory the select code becomes valid 150 nsec into T4 of Phase 1A.
5. IAK is high during the last 100 nsecs of T6.
6. Data valid at trailing edge of IOO.

INTERRUPT SYSTEM STATUS CHECK

Address	Mnemonic	Octal
100	SFS	102300
101	JMP *-1	024100
102	HLT	102000

If program halts, interrupt system is enabled.

INTERRUPT SYSTEM OPERATION CHECK

Address	Mnemonic	Octal
100	STF	102100
101	STC XX, C	1037XX
102	STF XX	1021XX
103	JMP *	024103
XX	HLT XX	1020XX

XX = any device select code and its trap cell. If interrupt system and priority string okay, should execute the halt instruction in the trap cell. Otherwise, will remain at JMP * at 103B.

TELETYPE SERVICE DATA

TTY DIAGNOSTIC (BUF) (20420)
S.A. = 100, Sw Reg = TTY SC bits 0-5, RUN, Hlt 1 @ P = 124.
Sw Reg = 70, RUN, Hlt 2. RUN, Punch tape, Hlt 3.
Read tape, RUN, Print out.
To halt set bit 0

```
TTY CONTROL WORDS
     LDA   CONTL
     OTA   TTY      control word
```

Label		Value	Function
INPUT	OCT	140000	Sets input FF
OUTPN	OCT	110000	Clears Input FF, Sets Punch FF
OUTPR	OCT	120000	Clears Input FF, Sets Print FF
OUTPP	OCT	130000	Clears Input FF, Sets Print & Punch FF

TELETYPE SERVICE DATA (CONT)

TTY TEST 24201-60001

1. Load diag. tape
2. Ensure TTY card is in an unbroken priority string
3. Place unit in LINE mode and punch off (2754=kt)
4. S.A. =100; SW Reg. =TTY select code
5. RUN
6. TTY cycles then computers halts 102001
7. SW Reg. =0
8. RUN
9. Set SW 3,4,&5
10. TTY prints "Begin Basic Test" then "End Basic Test."
11. TTY prints "Begin Punch and Read"
12. Halt 102002
13. Turn on punch; RUN
14. Halt 102003
15. Turn off punch, place tape in reader and set reader to Start.
16. RUN
17. Compare lines printed during the punch operation with those printed during the read operation
18. TTY prints "End Punch and Read"
19. TTY prints "Begin Print and Keyboard" and then four lines of characters.
20. TTY prints "Use Keyboard Slowly (5 chs/sec.)
21. Enter random info from keyboard
22. Program may be halted by setting SW 0
23. Switch Options:

    Bit 0 – Halt at starting address
    Bit 1 – Halt at beginning of error buffer
    Bit 2 – Suppress non-error messages
    Bit 3 – Basic Test
    Bit 4 – Punch and Read Test
    Bit 5 – Print and Keyboard
    Bit 6-15 – Not used

Teletype Program Constants

110000	Data out punch only
120000	Data out print only
130000	Data out print and punch
140000	Data in no print no punch
150000	Data in and punch
160000	Data in and print
170000	Data in print and punch

TELETYPE SERVICE DATA (CONT)

TTY INPUT OPERATION CHECK

Address	Mnemonic	Octal
100	OTB TTY	1066 TTY
101	STC TTY, C	1037 TTY
102	SFS TTY	1023 TTY
103	JMP * -1	024102
104	LIA TTY	1025 TTY
105	JMP * -4	024101

Initialize: B Register to proper teletype input program constant.

TTY = Teletype select code
Octal equivalent of ASCII data typed or read on reader appears in A Register.

TTY OUTPUT OPERATION CHECK

Address	Mnemonic	Octal
100	OTB TTY	1066 TTY
101	LIA 01	102501
102	OTA TTY	1026 TTY
103	STC TTY, C	1037 TTY
104	SFS TTY	1023 TTY
105	JMP * -1	024104
106	JMP * -5	024101

Initialize: B Register to proper TTY Output program constant (120000, 130000, etc.)

TTY = Teletype select code

Prints and/or punches data from switch register.

PHOTO READER/HIGH SPEED PUNCH SERVICE DATA

PHOTO READER/HIGH SPEED PUNCH DIAGNOSTIC (12597-16001)

1. Load and Configure the Diagnostic Configurator.

2. Load diagnostic. S. A. = 100, S. W. Reg. bits 0-5 = S. C. of Punch S. W. Reg. bits 6-11 = S.C. of Reader (= 0 if N. A.), halt 74.

3. Set S. W. Reg. according to table below, preset, run.

SWITCH REGISTER OPTIONS

BIT	FUNCTION
0	Start/Exit Tests
1	Abort Test 3
2	Resync
3	Variable Record Length Output
4	Time Delays between Reads
5	2737 Reader
6	2753 Punch
7	Loop on sub tests 11, 12
8	Suppress tests requiring operator
9	Abort current test and halt 75
10	Suppress non-error messages
11	Suppress error messages
12	Repeat selected tests
13	Repeat last test
14	Suppress Error Halts
15	Halt 76 at end of each test

SUBTESTS

A REG	TEST	FUNCTION
0	0	BIO on punch I/O
1	1	BIO on Reader I/O
2	2	Punch all Char. Combos
3	3	Verify all Char. Combos
4	4	Continuous Loop Read Delays
5	5	Continuous Loop Variable Lengths
6	6	Punch/Verify
7	7	Punch loop (doesn't work on TTY Punch)
8	10	Punch S. W. Reg.
9	11	Reader Speed Test
10	12	Punch Speed Test
11	13	2753 Status Test
12	14	2895 Manual Functions Test

TAPE PUNCH SERVICE DATA (CONT)

TAPE PUNCH OPERATION CHECK

Address	Mnemonic	Octal
100 B	LIA 01	102501
101	OTA TP	1026TP
102	STC TP,C	1037TP
103	SFS TP	1023TP
104	JMP *-1	024103
105	JMP *-5	024100

TP = Tape Punch select code. Will continuously punch information in Switch Register.

TIME BASE GENERATOR SERVICE DATA

TIME BASE GENERATOR DIAGNOSTIC (12539)

[20412 2116, 20421 2114/2115]

Load and Configure TT/SIO driver.
Load Diagnostic, S.A. = 100, A Reg = SC TBG, Sw Reg = 17000, PRESET, RUN.
Diagnostic types: "FT"
"IN"
"OP" (after 18 min)
"TI" (after 17 min)

Program loops.

SWITCH REG OPTIONS

Bit	Function			
15	exit Flag test "FT"			
14	exit Interrupt test "IN"			
13	exit Operation test "OP"			
12	exit Timing test "TI"			
6	terminate			
3	=0, ignore bits 0-2 and test all combinations =1 bits 0-2 specify time period for Operation test			
0-2	0	100 usec	4	1 sec
	1	1 msec	5	10 sec
	2	10 msec	6	100 sec
	3	100 msec	7	1000 sec

PHOTO READER SERVICE DATA

PHOTO READER DIAGNOSTIC (20408C)

1. Load diagnostic. S.A. = 100, LOAD A = TTY SC, LOAD B = RDR SC, PRESET, RUN, HIt 0 @P=327.
2. SW Reg = 1, RUN, (punch tape on TTY), HIt 0 @P=1033, make into loop.
3. Sw REG = 0, RUN, after a few loops raise bit 1. To terminate raise bit 4.

Switch Reg options

Bit	Function
0	Punch (=0 for read)
1	Read non-stop (=0 for stop-start)
2	Special character punch and read (=0 standard data)
3	Pause
4	Terminate
5	Pause after resync
6	Bypass error messages
7	Test Interrupt control
8-15	Special character, used with bit 2

PHOTO READER OPERATION CHECK

Address	Mnemonic	Octal
100 B	STC PR, C	1037 PR
101	SFS PR	1023 PR
102	JMP * -1	024101
103	LIA PR	1025 PR
104	HLT	102000
105	JMP * -5	024100

PR = Photo Reader select code. When program halts, A Register contains character — just read from photo reader. Pushing RUN reads next character on tape.

TIME BASE GENERATOR SERVICE DATA (CONT)

TIME BASE GENERATOR TEST 24213-60001

1. Load and configure TTY S.I.O. driver
2. Load diag. tape
3. S.A. =111g; SW Reg. =0
4. RUN; Halt 107000
5. SW Reg. =TBG select code
6. RUN; Halt 107001
7. SW Reg. =050700g
8. RUN; Halt 107077
9. RUN
10. Errors are printed on TTY
11. Halt 102077 at end of pass
12. Switch Options:

Bit 15 – Halt 102076 at end of test
Test No. in A-Reg.
Bit 14 – Suppress error halts
Bit 13 – Repeat last test
Bit 12 – Halt 102077 at end of pass
Bit 11 – Suppress error messages
Bit 10 – Suppress non-error messages
Bit 9 – Not used
Bit 8 – Include 10 sec. test
Bit 7 – Include 100 sec. test
Bit 6 – Include 1000 sec. test
Bit 5 – Not used
Bit 4 – Jumper in W2 position
Bit 3 – Not used
Bit 2 – Delete EXT. Preset test
Bit 1 – No TTY
Bit 0 – Override internal SW Reg.

DISC/DRUM SERVICE DATA

2766A DISC (12610C INTERFACE)

2766-003	786,432 words	96 logical tracks
12865A adds	262,144	32
2766-004	1,048,576	128

SPECIFICATIONS

Data Rate	2.04 megahertz (118K words/sec)
Tracks	512 physical tracks max
Sectors	32 sectors/physical track
Disc Speed	3450 rpm @ 60 Hz
Access Time	17.4 msec max
Temp	$0^{\circ} - 50^{\circ}C$
Power	115V AC, 1 phase, 60 Hz 2 amp starting 0.6 amp running DC: +18V ± 5%, 1.5A, 1% reg + 5V ± 5%, 2.0A, 1% reg -12V ± 5%, 1.0A, 1% reg
Weight	185#'s (259#'s shipping)
Size	21.0"H x 20.0"D x 19.0"W

DISC/DRUM SERVICE DATA (CONT)

SOME SIGNALS

DW	DATA WRITE serial data from interface
W	WRITE low during Sector
R	READ low during Sector
T0-T9	TRACK ADDRESS
DR	DATA READ serial data from track
RWC	READ/WRITE CLOCK output present during DR, DW
SC	SECTOR CLOCK 32 pairs/rev
TOP	TRACK ORIGIN PULSE one/rev
RY	READY low when up to speed and ready

INDICATORS

MOTOR POWER ON	AC power applied, motor energized
DRUM SPEED LOW	On below 3300 rpm
ACTUATION PRESSURE LOW	on when below 1 5/8 psi, flash once per 10 min normal
DRUM TEMP HIGH	On when housing $\geqslant 150^{\circ}$F, or motor $\geqslant 270^{\circ}$F. Cool and push motor RESET
MOTOR RESET	Push to reapply AC voltage following high temp cut out.

DRUM 2773/2774/2775

		Logical Tracks	Physical Tracks
2773A	393,216 words	48	192
12553-001 adds	393,216	48	192
2774A	786,432	96	384
12553 adds	262,144	32	128
2774-003	1,048,576	128	512

12610B Interface
64 words/sector, 32 sectors/physical track
4 physical tracks/logical track

SPECIFICATIONS

Rotational Speed	3450 RPM @ 60 Hz
Data Rate	118K words/sec
Access Time	17.4 msec max.
Power	115V ± 10%, 60 Hz ± 5% 1 phase 1.7 KVA max, 0.35 KVA running
Temp Range	5° to 40°C
Weight	200# 's (300# 's shipping)
Size	40.3"H x 19"W x 23.5"D

12610B DRUM CONTROLLER
Data Channel 12610-6001 high priority
Command Channel 12610-6002 low priority

Programming:
bits 0 - 4 Sector address
bits 5 - 14 Track address
bit 15: =1 write, =0 read
Note: — these are physical tracks and do not correspond to logical tracks in operating systems. Each 128 logical track requires 4 physical tracks of 32 sectors each.

DISC/DRUM SERVICE DATA (CONT)

STATUS

Bit	Function
15	SECTOR FLAG logical 1 – sector is past this rotation
14-13	Not used
12-8	NEXT SECTOR ADDRESS
7	DRUM READY FLAG logic 1 – ready logic 0 – not ready due to low drum speed, heads switch not at the IN position, certain drum circuits defective, drum memory not connected to computer, low line voltage, drum power supply defective.
6	Not used
5	SECTOR ADDRESS COINCIDENCE FLAG logic 1 – coincidence has occurred since last STC instruction
4	Not used
3	ABORT FLAG logic 1 – bit 7 has been 0 since last STC indicating possible error (cleared by STC Data SC)
2	WRITING ENABLED FLAG logic 0 – track protected
1	PARITY ERROR FLAG logic 1 – read parity error has occurred (cleared by STC Data SC)
0	DRUM BUSY FLAG logic 1 – read/write in progress

Switch up for protected tracks.

FIXED HEAD DISC/DRUM DIAGNOSTIC (24184 AND 24207)

requires 8K, DMA, TTY, and any Cupertino Division fixed head disc/drum

1. Load and configure TTY SIO Driver.
2. Load diagnostic; S.A. = 2; Sw Reg (0-5) = TTY SC, (6-11) = Disc/Drum SC; set bit 12* for 2114/2115; set bit 14 for DMA ch 7 (=0 for ch 6); PRESET, RUN, Hlt 77 @ P = 12066. (*Bit 12 not used on 24207.)
3. S.A. = 100, Sw Reg for options: (recommend 000000), PRESET, RUN. (requires ≈ 11 min)

Bit	Function
0-1	spare
2	Alter track table and/or pattern table
3	Execute Operator designed test
4	Enter device parameters (in START) and Protect tracks
5	Shorten tests S3 & S5 and eliminate S2
6	Restricts track selection and shortens S2 & S4
7	Repeat last section
8	Repeat last section ON ERROR 5 times before Reporting
9	Halt after each section
10	Suppress all non-error messages
11	Suppress all messages
12	Halt at end current pass
13	Loop current operation
14	Suppress program halts after each error
15	Halt after current operation

TESTS:

INIT	Initialization routine, S.A. = 2
START	Prints preamble, gets tracks, and sectors and does Flag, Control, and Interrupt testing.
S1	Short reads and writes
S2	Checks bad tracks and marginal heads
S3	Verifies data transfer from random locations
S4	Fills device with check summed data for use in S5
S5	Reads and checks track, sector, and checksum
S6	Operator designed program

DISC/DRUM SERVICE DATA (CONT)

OPERATOR DESIGNED TEST INSTRUCTION	DESCRIPTION
AT [,[*tttt*] [,*ss*]]	ADDRESS TRACK positions logically, and reports status.
CB [,[*xxxx*] [,*yy*]]	COMPARE BUFFERS compares xxxx words of read and write buffers, and yy # of error printouts (default 64, 1)
DA [,[*ttt*] [,*ss*]]	DECREMENT ADDRESS
DB [,[*xxxx*] [,*yyyyyy* [,C]]]	DEFINE BUFFER fills xxxx words with yyyyyy pattern and allows alternate complement (default 64 words, random pattern).
EP	ERASE PROGRAM
GO, *LL*	TRANSFER CONTROL to label.
HT [,*xxxxxx*]	HALT and display value xxxxxx in A-Reg.
IA [,[*tttt*] [,*ss*]]	INCREMENT ADDRESS logically position and set status.
IR [,[*xxxx*] [,[*tttt*] [,*ss*]]]	INCREMENTAL READ reads xxxx words starting at track tttt and sector ss. (Default 64, 0, 0).
IW [,[*xxxx*] [,[*tttt*] [,*ss*]]]]	INCREMENT WRITE
LB, *LL*	LABEL defines 2-char label
LP [,*LL*]	LOOP terminates program. Starts at label but loops back to beginning.
RD [,[*xxxx*] [,[*tttt*] [,*ss*]]]	READ DATA and place in read buf. (default 64, 0, 0) word count 1024 max.
RR	RANDOM READ
RS	READ SAME used with RW
RT, *LL*, *x*	REPEAT go to label x times
RW	RANDOM WRITE writes random # words in random location
SC [,*xxxxxxxxxxxxxxxx*]	STATUS CHECK last status is compared with xxx . . . x
SS	SUPPRESS STATUS until next ST.
ST	STATUS perform hardware status
WD [,[*xxxx*] [,[*tttt*] [,*ss*]]]	WRITE DATA transfer from write buffer to Disc. (default 64, 0, 0)

2883 M.H. DISC SERVICE DATA

2883A Disc File (with controller)
2884A Disc File optional-additional drive
2885A Filter Box
12565A Disc Interface
12868A Disc pack

SPECIFICATIONS

Disc Pack

11 discs/20 surfaces
203 cylinders (0-202)
20 tracks/cyl. (0-19)
23 sectors/track (0-22)
128 words/sector in data field.
Address Field – cyl, head, sect # and defective or protected indicator
23,905,280 bytes

Disc Characteristics

2400 RPM (25 ms/revolution)
seek time 60 ms maximum
start up/stop 20 seconds
Temp 60° to 90°F
humidity 80% max
power 208/230V ± 10%, 3 phase, 60 Hz ± 1%
size H 40", W 30", D 24"
weight 390 #'s

M.H. DISC DIAGNOSTIC (24204 AND 24236)

Test requires TTY, DMA, 8K memory

1. Load and configure TTY SIO driver
2. Load Diagnostic. S.A. = 2; Sw reg (0-5) SC TTY, (6-11) SC Disc, set bit 12* for 2114/2115; PRESET, RUN, HLT 77. (*Bit 12 not used on 24204.)
3. S.A. = 100, Sw reg options

Bit	Function
2	Alter cylinder table and/or pattern table
3	Execute operator designed test
4	Test second drive
5	Shorten test (S 2, 3, 5, & 6) (≈ 12 min)
6	Restrict cylinder selection
7	Repeat current section
8	Test multiple drives
9	Halt end current section
10	Suppress all non-error messages
11	Suppress all messages
12	Halt end of current pass
13	Loop current operation
14	Suppress halt after each error (0=halt)
15	Halt after current selection

recommended Sw reg = 000000, PRESET, RUN (≈ 45 min)

2883A/2884A DISC FILE DIAGNOSTIC

12965-16001

1. Configured diagnostic start at step 5, using BBL or equivalent load diag. configurator and set it up. Load diagnostic, memory loc 126 = 111001.

2. P = 100, S = XADCTY (table 1), HALT = 107077.
   Table 1
   A = 0 - DMA (DCPC) CH 1 / A = 4 - DMA (DCPC) CH 2
   DC = Data channel select code
   TY = Console select code

3. To dump a configured copy use step 7 of the diagnostic configurator.

4. S = XXXXXX (Table 2), PRESET, RUN.

   Table 2

BIT	FUNCTION
0	Eliminates S3 thru S5
1	Execute write address test also timing EX 21 MX
2	Alter tables (cylinder, pattern)
3	Operator design
4	Select unit 1 at beginning of test
5	Shorten tests S2, S3, S4, and S5
6	Restrict cylinder selection
7	Repeat last section
8	Multiple drives to be tested
9	Halt after each section
10	Surpress non-error messages
11	Surpress all messages
12	Halt at end of pass
13	Loop on last operation
14	Surpress error halts
15	Halt after next operation

5. Start configured diagnostic or restart P = 2000 S = XXXXXX (Table 2), PRESET, RUN.

6. Operator designed routines

   a. Formatting the disc

      1. Set bit 3 in S reg. console prints "H55 enter inst".
      2. Enter program on console
         SD,X (X = unit selected)
         LB,XX (label)
         IT (increment track)
         WA (write address)
         RT,XX, 4059
         EN

7. For other operator designed tests refer to manual no. 12965.

Table 3-2. Switch Register Characteristics Following Configuration

BITS	FUNCTION
0	Spare (used by CE in Appendix A).
1	Skip to end of section when set. (Also used by CE in Appendix A).
2	If set to one, alter cylinder table and/or pattern table and/or select heads and/or change unit removal threshold and/or alter unit table. Reset to terminate requests.
3	If set to one, execute operator design program (OPDSN or Section 6).
4	If set to one, execute interactive part of S1. (Also used by CE in Appendix A).
5	If set to one, shorten test in S2, S3, S4 and S5. (Also used by CE in Appendix A).
6	If set to one, restrict cylinder selection.
7	If set to one, repeat last section.
8	If set to one, suppress spaces, print message 65 independent of bit 10 when an error occurs.
9	If set to one halt after each section of the program.
10	If set to one, all non-error messages will be suppressed, except current operation messages, message 51 and message 65 when bit 8 is set and an error occurred.
11	If set to one, all messages are suppressed.
12	If set to one, print timing messages in Sections 2 and 4. (See paragraph 2-9, step c.)
13	If set to one, loop on last step.
14	If set to zero, program will halt after each error.
15	If set to one, program will come to an orderly halt at the end of the current step.

NOTES: 1. When all switches are set to zero, disc drive 0 is tested in the long mode (18 minutes per pass). The program will halt on each error and will test the entire removable disc pack.

Table 3-2. Switch Register Characteristics Following Configuration (cont.)

NOTES: (cont.)

2. To restrict cylinder selection to a different set of values than are initially in the cylinder table (0, 1, 2, 4, 8, 16, 32, 64, 128, 202) set switch 2 at step b, paragraph 3-3. These are the only cylinders used when switch 6 is set (and switches 3 and 4 are reset). The cylinder table is a push-through stack.

3. To use other patterns then the ten initially in the pattern table (octal: 0, 177777, 125252, 52525, 7417, 170360, 162745, 163346, 155555, 22222) set switch 2 at step b, paragraph 3-3. The pattern table is used to write and read back ten patterns in each word of the pack in Section 2. The pattern table is a push through stack.

4. To test the fixed disc or both discs, set switch 2 at step b, paragraph 3-3. If heads 0 and 1 are selected, the removable pack is tested. If heads 2 and 3 are selected, the fixed pack is tested. Both discs may be tested alternately by selecting the third option. This selection is reset to heads 0 and 1 in Section 6. (7901 contains only the removable disc).

5. Units that have made 20 errors in one pass are removed from the unit table. This unit removal threshold may be changed by setting switch 2 at step b, paragraph 3-3. If no units remain in the unit table the program halts then restarts with only the last unit in the table.

6. To test other drives or multiple drives, switch 2 may be set at step b, paragraph 3-3. One drive will be tested each pass. The multiple drive test (Section 5) is performed after each drive has been tested.

7. If the user is running the operator designed section (Section 6) and executing a program he has created, he may regain control by resetting switch 3 (return to Section 1) or by quickly resetting switch 3, then setting it again (return to operator design program). This method is valid whenever the program is running (neither halted nor reporting an error).

8. Switch 4 causes the interactive part of Section 1 to be executed. These tests are not performed anywhere else in the program since they require user assistance. Switch 12 permits timing messages to be printed in Sections 2 and 4.

9. Any time switch 5 is set, Sections 2, 4, and 5 are shortened. Section 3 is also shortened if switch 5 is set when Section 3 starts.

Table 3-2. Switch Register Characteristics Following Configuration (cont.)

NOTES: (cont.)

10. When switch 6 is set, H53 is never printed. Switch 6 does not affect Section 1.

11. There are two options at the end of each section: First if switch 9 is set to one, the program will halt; if switch 7 is set to one, the section is repeated.

12. To run the tests without error reporting, set switches 11 and 14 to one.

13. Switch 13 allows the program to loop. It should be used when errors are occurring.

14. Switches 0, 1, 4 and 5 are used by the customer engineer to help align the heads and assure drive compatibility.

d. The diagnostic will output its peamble (message 0) and then run a short test on each of the two I/O channels being used.

e. If bit 2 of the switch register is set the operator is shown the cylinder table (the ten cylinders used when switch register bit 6 is set) and allowed to change it, shown the pattern table (the ten patterns used in Section 2) and allowed to change it, asked to select heads (0, 1 = removable disc; 2, 3 = fixed disc – 7900 only), shown the unit removal threshold and allowed to change it, and shown the unit table and allowed to change it. The requests repeat until bit 2 is reset. The cylinder and pattern tables are pushed through stacks, therefore as little as one new entry may be added at a time. The unit table must be totally reconstructed with each change.

2883 M.H. DISC SERVICE DATA (CONT)

OPERATOR INSTRUCTION LIST (CONT)

RD [,*xxxx*]	Read Data. xxxx no. of words.
RL	Reload. Resets RAR to value last loaded (ref RS).
RS	Random Seek. Random cyl-h-sect address is loaded in RAR, and disc seeks this position.
RT, *LL*, *x*	Repeat. Return control to label, x times.
SC [,*xxxxxx*]	Status Check. Check hardware status against xxxxxx status.
SD, X	Select Drive.
SR [,[*ccc*] [,[*h*] [,*ss*]]]	Seek Record.
SS	Suppress status, update and check.
ST	Status. Obtain hardware status.
WA [,*P*] or WA [,*D*]	Write Address. Use address in RAR and protect or flag if defective. FORMAT switch must be ON.
WD [,*xxxx*]	Write Data. xxxx number of words.

2870 M.H. DISC SERVICE DATA

2870A	Disc Drive
2871A	Controller
2881A	Power Supply
2882A	Cabinet
12557A	Interface

SPECIFICATIONS

Capacity	128 Words/sector 12 Sector/track 4 Tracks/cylinder 203 Cylinders 1,247,232 Words
Access Time	Move 85 ms max Rotation 40 ms max
Data Rate Speed	720,000 bits/sec 1500 RPM
Temp Humidity	15° to 35°C 30% to 80%
Power	115V ± 10%, 60 Hz ± 1% 1200 W interface +4.5V 2.3A, -2.0V 0.15A
Size Weight	H 72.1", W 23.1", D 34.0" 550 #'s
Disc Pack	12563-60001

2870 M.H. DISC SERVICE DATA (CONT)

M.H. DISC DIAGNOSTIC (24237)

1. Load and configure TTY SIO driver
2. Load Diagnostic Tape using BBL
3. Load Diagnostic S.A. = 2
4. Load Sw reg as follows:

Bits	Function
0-5	S.C. of TTY INTFC
6-11	S.C. of Disc 1 INTFC
12	0 = 2100/2116; 1 = 2114B/2115A
13	Spare
14	0 = DMA chan 6; 1 = DMA chan 7
15	Spare

5. Press RUN; halt 102077 in T-reg
6. Load address 100_8
7. Select desired Sw reg options as follows and press RUN

Bits	Function
0-1	Spares (Used only by CE in S7).
2	1 = alter cylinder table and/or pattern table and/or select heads.
3	1 = execute operator design program (OPDSN).
4	1 = execute write address test S0 before S1.
5	1 = shorten test in S2, S3, S5 and S6.
6	1 = restrict cylinder selection.
7	1 = repeat last section.
8	1 = multiple drives are to be tested.
9	1 = halt after each section of the program.
10	1 = all non-error messages for TTY will be suppressed.
11	1 = all messages for TTY will be suppressed.
12	If = 1 and bit 10 and bit 11 = 0, timing messages will be printed in S2 and S5. NOTE: Timing messages will not be accurate on an HP 2100 Computer.
13	1 = loop on last operation.
14	0 = program will halt after each error.
15	1 = program will come to an orderly halt.

2870 M.H. DISC SERVICE DATA (CONT)

STATUS WORDS

Bit	Function
0	ANY ERROR.
1	DATA ERROR.
2	DRIVE BUSY executing seek record.
3	FLAGGED CYLINDER write protected or defective.
4	ADDRESS ERROR address read ≠ expected.
5.	END OF CYLINDER attempt to cross cylinder boundary.
6	NOT READY drive not connected, or not sequenced up and heads loaded, (manual intervention).
7	NOT USED.
8	SEEK CHECK cylinder # > 202 or seek command while positioning taking place (seek record).
9	SEEK INCOMPLETE servo positioning operation failed (seek record).
10	ACCESS HUNTING servo system misadjustment (seek record).
11	ACCESS UNSAFE unusual drive access condition (recycle power).
12	READ/WRITE UNSAFE drive read/write problems (remove and reinsert cartridge).
13	OVERRUN data transfer - flag race condition.
14	FIRST SEEK gone not ready to ready bit is also set (status check).
15	ATTENTION operation termination. (Operation) required to clear condition.

7900/7901 M.H. DISC SERVICE DATA

7900	EQUIPMENT
7900	Disc Drive
13215	Power Supply
13210	Interface
12869	Disc Pack

7900 SPECIFICATIONS

Capacity:	128 words/sector 24 sectors/track 4 tracks/cylinder 203 cylinders 4.8 megawords
Access Time:	7 ms track to track (avg) 30 ms random average 55 ms max seek (203 tracks) 25 ms rot. latency (max.)
Data Rate Speed:	2.5M bits/sec 2400 rpm
Temperature:	10-40°C (50-104°F)
Humidity:	8-80% noncondensing
Power	60Hz ±2%, 100/120V ±10%, 3.4A, 1Φ 200/220/240V ±10%, 1.7A, 1Φ 50Hz ±2%, 100/120V ±10%, 4.1A, 1Φ 200/220/240 ±10%, 2.0A, 1Φ Interface +4.5V 4A, -2V 0.14A
Size:	
7900:	10-1/2"H, 19"W, 22-15/16"D
13215:	7"H, 16-3/4"W, 19-3/4"D

7900/7901 M.H. DISC SERVICE DATA (CONT)

7901	EQUIPMENT
7901	Disc Drive
13210	Interface
12869	Disc Pack

7901 SPECIFICATIONS

Capacity:	128 words/sector 24 sectors/track 2 tracks/cylinder 203 cylinders 2.4 megawords
Access Time:	10 ms track to track (avg) 35 ms random average 65 ms max seek (203 tracks) 25 ms rot. latency (max.)
Data Rate Speed:	2.5M bits/sec 2400 rpm
Temperature:	10-40°C (50-104°F)
Humidity:	8-80% noncondensing
Power:	60Hz ±2%, 100/120V ±10%, 3.4A, 1Φ 200/220/240V ±10%, 1.7A, 1Φ 50Hz ±2%, 100/120V ±10%, 4.1A, 1Φ 200/220/240 ±10%, 2.0A, 1Φ Interface +4.5V 4A, -2V 0.14A
Size:	10-1/2"H, 19"W, 22-15/16"D

M. H. DISC DIAGNOSTIC (12960-16001)

1. Load and configure diagnostic configuration.
2. Load unconfigured diagnostic tape.
3. Load diagnostic SA 100_8.
4. Load SW reg as follows.

   0-5 SC of disc 1 interface
   14 0 = DMA chan 6;1 = DMA chan 7

5. Press preset button(s), then RUN.
6. T = req = 102074
7. Load address 2000_8.
8. Select desired SW reg options as follows and press RUN

   page 8 and 9 of reference manual Table 3-2 and notes

7900/7901 M.H. DISC SERVICE DATA (CONT)

FORMATTING

To format a new disc pack using operator design (S7), type in the following program:

```
SD, X
FU      (or FL for Fixed - 7900)
EN
```

STATUS WORDS

Bit	Function
0	Any Error.
1	Data Error.
2	Drive Busy.
3	Flagged Cylinder (when write operation attempted and OVER-RIDE switch not on).
4	Address Error.
5	End of Cylinder.
6	Not Ready.
7	Not Used.
8	Seek Check.
9	Not Used
10	Write Protected (when write operation attempted).
11	Drive Unsafe.
12	Not Used.
13	Overrun.
14	First Seek.
15	Not Used.

2610/2614 LINE PRINTER SERVICE DATA

2610 SPECIFICATIONS

Printing Speed:

200 lines per minute (64 character set)
150 lines per minute (96 character set)

Power Required:

115V ± 10%; 60Hz±0.6Hz
(230V ± 10%; 50Hz±0.5Hz Optional)
6 amps at 115V
(3 amps at 230V AC)

Operating Conditions:

Operating Temperature: 32° to 104°F (0° to 40°C)
Storage Temperature: -4° to + 150°F (-20° to 65°C)
Humidity: 30% to 95% R.H. (non-condensing)

Physical Characteristics:

Height: 15-1/2 inches (39.37 cm) without stand
Width: 37 inches (94 cm)
Depth: 25-1/2 inches (64.8 cm)
Weight: 500 pounds with stand (225 kg)
Shipping Weight: 550 pounds (247 kg)

Indicators:

Paper Out
Paper Fault (paper tear or runaway)

Operating Supplies Available:

Format Tape Punch	Part No. 9164-0023
Adhesive, 3 fl. oz.	Part No. 0470-0391
Blank Format Tape	Part No. 1535-2094
General Purpose Format Tape	Part No. 1535-2097
Ribbon	Part No. 1535-2098
Paper, fanfold, 15 lb. bond	Part No. 9320-1659

Forms Specifications:

Single Part:	15 to 25 pounds
Multiple Part:	15 pounds 1st part, 12 pounds for 5 copies
Multiple Copy:	Up to six parts
Length:	Up to 22 inches
Width:	4 to 20.5 inches

2610/2614 LINE PRINTER SERVICE DATA (CONT)

2614 SPECIFICATIONS

Printing Speed:

600 lines per minute (64 character set)
400 lines per minute (96 character set)

Power Required:

115V ± 10%, 60±0.6Hz
15 amps turn on, 9.5 amps operating, 9 amps idling
(230V, 50Hz, optional)

Operating Conditions:

Operating Temperature: 10° to 40°C (50° to 104°F)
Humidity: 10 to 95% R.H. (non-condensing)

Physical Characteristics

Height:	46 inches (1.17m)
Width:	46 inches (1.17m)
Depth:	34 inches (864mm)
Mounting:	Wheels and leveling screws
Weight:	900 pounds (409 kg)
Shipping Weight:	990 pounds (449 kg)

Indicators:

Paper Out
Paper Fault (paper tear or runaway)

Operating Supplies Available:

Ribbon, Printer	
14-1/2 inches wide	Part No. 9282-0505
Black Ribbon	Part No. 1535-2109
Silver Ribbon	Part No. 1535-2108
Format Tape Punch	Part No. 9164-0023
Blank Format Tape	Part No. 1535-2094
General Purpose Format Tape	Part No. 1535-2097
Adhesive, 3 fl. oz.	Part No. 0470-0391
Paper, Fanfold 15 lb. bond	Part No. 9320-1659

Forms Specifications:

Single Copy: 15 lbs. min. max. stock thickness of 0.006 inch.
Multiple Copy: Original and five copies.
Paper Dimensions: 3-1/2 to 20-5/8 inches wide, edge punched holes (1/2 inch, center to center; 1/4 inch, center to edge).
Paper Compartment: Accommodates fanfold forms in page lengths up to 22 inches when stacked on floor or 11 inches stacked in rear basket.

2610/2614 LINE PRINTER SERVICE DATA (CONT)

LINE PRINTER DIAGNOSTIC (24275)

1. Load and configure TTY driver
2. Load Diagnostic Tape, S.A. = 110_8, press RUN
3. Following configuration dialogue occurs:
   a. H1 TYPE SELECT CODE (OCTAL)
   a. H1 TYPE SELECT CODE (OCTAL)
      Enter I/O S.C. of LP followed by CR LF

   b. H2 TYPE TIME CONSTANT
      Enter 252 for 2100, 248 for 2114/15, or 311 for 2116 followed by CR LF

   c. H3 DMA?
      Enter YES or NO followed by CR LF

   d. H4 CHARACTER SET? TYPE 64 OR 96
      Enter 64 or 96 followed by CR LF

   e. H5 ENTER SWITCH REGISTER OPTIONS, PRESS RUN

   Select desired Sw reg options as follows:

Bits	Function
0	1 = override internal Sw register and read program options for hardware Sw register.
1	1 = execute basic I/O test.
2	1 = execute preset and status test.
3	1 = execute character set.
4	1 = execute ripple test.
5	1 = execute triangular printing test.
6	1 = execute vertical format control test.
7	1 = execute DMA test.
8	1 = execute manual printing test.
9	1 = execute long for vertical format control test.
10	1 = suppress non-error messages.
11	1 = suppress all messages
12	1 = HLT at end of complete test cycle.
13	1 = loop on current test.
14	1 = suppress error HLT.
15	1 = HLT after each test.

   f. H6 DIAGNOSTIC CONFIGURED

4. Press INTERNAL and EXTERNAL PRESET. Press RUN.

HP 2607A LINE PRINTER SERVICE DATA

INTERFACE 12845 A/B
2607A SPECIFICATIONS:

Printing Speed:
- 200 lines per minute (64 character set)
- 165 lines per minute (128 character set)

Power Required:
- 105-140 Vac single phase, 60 Hz ± 3 Hz
- 90-110 Vac single phase, 50 Hz ± 3 Hz
- 187-264 Vac single phase, 50 Hz ± 3 Hz
- 35 amps (INRUSH) 7 amps printing @ 115 Vac
- 17.5 amps (INRUSH) 3.5 amps printing @ 230 Vac

Operating Conditions:

Operating Temperature:	10°C to 40°C (50°F to 104°F)
Humidity:	10% to 95% (noncondensing)

Physical Characteristics:

Height:	11 inches w/o stand - 40 inches with stand.
Width:	28 inches
Depth:	25 inches
Weight:	168 lbs w/o stand - 207 lbs with stand
Shipping Weight:	233 lbs w/o stand - 253 lbs with stand

Indicators:
- Audio paper out signal

Operting Supplies Available:

Ribbon	9282-0531
VFU tape 6 lines/IN	02607-80024
VFU tape kit	1150-0897
Paper, fanfold 15lb bond	9320-1659

Forms Specifications:

Single copy:	15lbs min. max. stock thickness of 0.006 in.
Multiple copy:	15 lbs first part, 12 lbs - 5 part with 8 lbs single shot carbon.
Paper dimensions:	4 to 14 7/8 inches wide with edge punched holes.

HP 2607A LINE PRINTER SERVICE DATA (CONT)

LINE PRINTER DIAGNOSTIC (24340-16001)

1. Load and configure diagnostic configurator (24296) per instructions under diagnostic configurator in Geneal Data Section.

2. Load 2607 diagnostic.

3. Set P-register to 100_8 - S-register to S.C. of line printer.

4. Press preset (INT/EXT) and run HLT 102074. If HLT 102073, S. C. less than or equal to 7_8 correct and push run.

5. Enter switch register options

SELECT DESIRED SW REG OPTIONS AS FOLLOWS

BITS	FUNCTION
0	Reserved
1	Suppress character "H" in dot matrix test
2	Suppress character "I" in dot matrix test
3	Suppress character "#" in dot matrix test
4	Suppress character "." in dot matrix test
5	Reserved
6	Reserved
7	Reserved
8	Suppress test requiring operator intervention
9	Abort current run and perform HALT with MDR = 102075_8; user sets bits of A-register with test selection where bit *i* selects test *i*; e.g. bit 0 set selects test 0, bit 1 selects test 1, etc. Clear switch register bit 9, press run.

A REGISTER TEST

BITS	FUNCTION
0	Basic I/O Channel Functions
1	Manual Control
2	Ripple Print
3	Triangular Print
4	Vertical Format Control
5	Character Set
6	Dot Matrix
7	DMA
8	Operator Design
10	Suppress all non error messages.
11	Suppress printing of error messages.
12	Repeat all selected tests of the diagnostic except those requiring operator intervention.
13	Repeat the currently executing test (LOOP)
14	Suppress error HLTS
15	Halt at end of each test. HLT 102076

2767 LINE PRINTER SERVICE DATA

SPECIFICATIONS

Speed	20 char	1110	lpm
	40 char	650	lpm
	60 char	460	lpm
	80 char	356	lpm
Data Lines	bits 0 to 6		
Power	115V ± 10%, 60 ± 3 Hz, 330 watts		
Temp	50°F to 110°F		
Humidity	30-90%		
Size	H 22.8", W 23.5", D 22.0"		
Weight	185 #'s		
Print	64 characters. 80 columns		
Hidden lines	Line visible after 8 lines of print		
Signals	Data IOBO Ø to 6, and Strobe (control)		
	Status IOBO Ø busy, 15 ready		
	(flag and status bit Ø are tied together)		
Paper	Fan fold 9280-0218		
Ribbon	9300-0427		

STATUS

Bit 0 Low - Line Printer Ready, on-line, not busy
High - Busy
Bit 15 Low - Paper loaded, gate closed, speed okay, power on, temperature okay.
High - Not ready
Note: may not be ON LINE.

CONTROL

ASCII	FUNCTION
Form = 014	Top of form (3 lines below perforation). Includes carriage return.
Line Feed = 012	Single line advance (includes automatic perforator, advance 6 lines). Includes carriage return.
Carriage Return = 015	Returns to left margin.

2767 LINE PRINTER SERVICE DATA (CONT)

LINE PRINTER DIAGNOSTIC

(20999 for 2114/15/16)
(24205 for 2100)

Load and Configure TTY Driver
Load diagnostic, SA = 2,
Sw Reg = (0-5) SC TTY, (6-11) SC Line Printer
[bit 12* set for 2114/2115], PRESET,
RUN, HLT 77 @ P=6441, S.A. = 100,
Set Sw Reg (Recommend 000000), Printer ON LINE.
*Bit 12 not used on 24205

BITS	FUNCTION
3	User designed exercise
5	Shorten test 1 and 3, omit test 2
6	Used for test 4 to terminate ribbon movement
7	Repeat current routine
8	Perform test 4, (manual tests) after test 3
9	Halt at end of each routine
10	Suppress all non-error messages
11	Suppress all messages
12	Halt 77 end of complete cycle
13	Loop on last diagnostic operation
14	Halt after each error (bit 14 = 0)
15	Pause (Lower bit and RUN to resume)

PRESET, RUN, (requires 2 min). Raise bit 8 for manual tests.

Test 1	Paper handling and print cyclic patterns
Test 2	Prints blocks of characters for alignment
Test 3	Prints patterns for worst-case timing
Test 4	Conversational exercise
Test 5	Operator designed exercise

Instruction set for operator designed exercise

CP [, *xx*]	Print cyclic pattern
DB, [*xx*], Z	Define buffer: xx long, any ASCII char.
EE	Erase last entry (rubout delete current line)
EN [, *LL*]	End of instruction series. Start at beginning or at LL label.
EP	Erase entire program
FF	Form Feed
GO, *LL*	Go to label LL
HT [, *xxxxxx*]	Halt and display octal value xxxxxx in A reg.
LB, *LL*	Define label LL
LF	Line Feed
LP [, *LL*]	End of instruction, loop to label during run.
PF [, *xx*]	Print xx characters from buffer and Form-Feed.
PL [, *xx*]	Print xx characters from buffer and Line-Feed.
PR [, *xx*]	Print xx characters from buffer and carriage return.
RC	Return Carriage (resets zone counter)
RT, *LL* , [*r*]	Repeat all instructions from label r times.
SC [, *xxxxxx*]	Status check. Compare with xxxxxx.
ST	Hardware status check (LIA)
TX, any text	Print first 80 char, Line-Feed.

HP 2613/2618 LINE PRINTER SERVICE DATA

INTERFACE 12845B

2613A SPECIFICATIONS

Printing Speed:
- 300 Line per minute (64 character set)
- 240 Lines per minute (96 character set)

Power Required:
- 115 V ± 10%, 60 Hz ± 2% - 230 V ± 10%, 50 Hz ± 2%.

Operating Conditions:

Operating Temperature:	10°C to 38°C (50°F to 100°F)
Humidity:	30% to 90% (non condensating)

Physical Characteristics:

Height:	45 in.	(1.14 m)
Width:	32 in.	(813 mm)
Depth:	22 in.	(559 mm)
Weight:	340 lbs.	(155 kg)

Indicators:
- Hammer Fault
- Format Fault
- Ribbon Fault
- Gate Open
- Tape Fault (format)
- Paper Fault

Operating Supplies Available

Ribbon	9282-0545
Format Tape Punch	9164-0023
Blank Format Tape	4114-0371
Standard Format Tape 6 LPI	02613-80001
Standard Format Tape 8 LPI	02618-80003
Paper Fanfold 15lb Bond	9320-1659
Adhesive, Carriage Tape	0470-0391

HP 2618A LINE PRINTER SERVICE DATA INTERFACE 12845B

2618A SPECIFICATIONS

Printing Speed:
- 1250 Lines per minute (64 character set)
- 925 Lines per minute (96 character set)

Power Required:
- 115 V ± 10% - 60 Hz ± 2% - 230 V ± 10% - 50 Hz ± 2%
- 40 amps turn on, 17 amps operating

Operating Conditions:

Operating Temperature:	10°C to 43°C (50°F to 110°F)
Humidity:	10% to 95% (noncondensating)

Physical Characteristics:

Height:	46 in.	(1.17 m)
Width:	48.5 in.	(1.23 m)
Depth:	36.5 in.	(927 mm)
Weight:	800 lbs	(363 kg)
Shipping Weight	900 lbs	(408 kg)

Indicators:
- Drum Gate Open
- Paper Fault
- Print Inhibit

Operating Supplies Available

Ribbon, 14 1/2 wide	9282-0543
Format Tape Punch	9164-0023
Blank Format Tape	4114-0371
Standard Format Tape	02618-80001
Paper, Fanfold 15lb Bond	9320-1659
Adhesive, Carriage Tape	0470-0391

HP 2613/2618 LINE PRINTER SERVICE DATA (CONT.)

LINE PRINTER DIAGNOSTIC P/N 02618-16001

1. Load and configure the diagnostic configuration (24296) per instructions in the Diagnostic Configuration Manual.
2. Load line printer diagnostic using protected loader.
3. Set "P" register to 100_8, "S" bits 0-5 register to S.C. of L.P. interface. Set B14 7 if 8 LPI.
4. Press preset (Int/Ext) and run HLT 102074
   If HLT 102073 occurs, the select code input was less than or equal to 7_8; correct the select code and press run.
5. Enter switch register options, press press (Int/Ext) and run.

SELECT DESIRED SWITCH REGISTER OPTIONS AS FOLLOWS:

BIT	FUNCTION
0	thru 7 reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and HLT 102075. User may specify a new group of test in "A" register, clear bit 9 and press run.

A REGISTER TEST

BIT	FUNCTION
0	Basic I/O operation
1	Manual Control Test
2	Ripple Print Test
3	Triangular Print Test
4	Vertical Format Control Test
5	Character Set Test
6	Over Print Test
7	DMA Operation Test
8	OP Design Test

10	Suppress non error messages.
11	Suppress error message.
12	Repeat all selected tests.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (102076) at end of each test.

HP 2613/2618 LINE PRINTER SERVICE DATA (CONT)

INTERFACE 12617A (12554-60024 Neg)

SPECIFICATIONS

Power	115V ± 10%, 60 ± .3 Hz 15 amp turn on, 9 amp operating
Temperature	15°–32°C
Humidity	30–80%
Size	44"H, 46"W, 25"D
Weight	860 #'s
Speed	300 lpm
Columns	120/132
Ribbon	9282-0074
Paper	Fanfold 9320-1515

LINE PRINTER DIAGNOSTIC

(20895 for 2114/15/16)
(24218 for 2100)

Load and Configure TTY SIO DRIVER
Load Diagnostic, SA = 100, Set Sw-reg.

(0-5)	SC Line Printer
8*	Set for 2114/2115
9	0 120 char/line, 1 132 char/line
10	Error halts omitted
11	Halt after each Section
12	Allows operator to select character
13	All printout suppressed
14	Loop on test just completed
15	Loops on entire diagnostic (eliminates printer ready)

*Bit 8 not used on 24218

Line Printer ON-Start.
PRESET, RUN. (Follow printed instructions.)

STATUS

Bit Ø	(IOBI Ø) Busy (gnd true) due to Buffer load cycle, Print cycle, or Paper Advance cycle.
Bit 15	(IOBI 15) READY (gnd true) due to out of paper, hammer drive fuse blown, Print drum arm not latched, STOP switch on.

CONTROL

Data IOBO 0-5, 15
for data (bit 15 = Ø)
64 characters from 0XXX00 to 0XXX77 in order @, A, B, C, D, E . . . Z, [, \ ,] , ↑ , ←, Blank, !, ", #, $, %, &, ', (,), *, +, ', -, ., /, Ø, 1 . . . 9, :, ;, < , = , > , ?

2778 LINE PRINTER SERVICE DATA (CONT)

LINE PRINTER OPERATION CHECK

Address	Mnemonic	Octal
100 B Start	CLA	002400
101	OTA LP	1026LP
102	STC LP, C	1037LP
103	SFS LP	1023LP
104	JMP * -1	024103
105	INA	002004
106	CPA LF5	050111
107	JMP Start	024100
110	JMP Start + 1	024101
111 LF5	OCT 100005	100005

LP = Select code of Line Printer

Will print one line which contains every available character, skip 5 lines and print again.

3030 MAG TAPE SERVICE DATA

MAG TAPE INTERFACE 12559A

MAG TAPE DIAGNOSTIC (20433)

INITIALIZE: Load Tape, S.A. = 100, Sw Reg = SC Mag Tape One (Bit 15 = 1 for 2114/2115), PRESET, RUN, Hlt Ø @ P = 121.
Sw Reg = SC Buf TTY, RUN, HLT Ø @ P = 127
Sw Reg = X7777 (Upper limit of core), RUN,
HLT Ø @ P = 134 (If error – reload Tape).

Set Sw Reg Options (recommend 000022), RUN, Restart address = 2000.

Bit	Function
0	Rewind & SOT
1	Extensive Read-Write
2	Write-Ring HLT 74 Remove Ring, RUN HLT 75 Replace, RUN
3	Rewind & Unload (HLT 76, AUTO, PRESET, RUN)
4	DMA Test
12	Print Cycles completed
13	Halt on error
14	Loop on Test
15	Halt after Current Test

HALTS

HLT 11	Not on automatic
13	Too long in command wait
15	Controller busy
55	Sw 13 & Error
74, 75	Write Ring
76	Rewind & Unload
77	Completion Halt

Auxiliary Tests
SA 1000 Writes Sw Reg (0-7) & Reads into B
SA 1100 Outputs Sw Reg to Command Ch.
SA 1200 Alternate write bits 0-7 and 8-15
SA 1300 Use switches to select tape motion

0 Write, 1 Write File Mark
2 Gap, 3 Read, 4 Forward Space
5 Backspace, 6 Rewind, 7 Unload
8 Start-Stop forward, 9 Start-Stop backward

12559A 3030 CONTROLLER

OCT	COMMANDS MNEMONIC	OPERATION
3	FSR	Forward Space Record
11	GAP	Write 3" Blank Tape
23	RCC	Read Characters
31	WCC	Write Characters
35	WFM	Write File Mark
41	BSR	Backspace Record
101	RWS	Rewind and Standby
201	REW	Rewind
300	CLR	Clear

3030 MAG. TAPE SERVICE DATA (CONT)

STATUS

Bit	Meaning
0	Busy (Tape in motion or local status)
1	Parity Error
2	Write not enabled or tape rewinding
3	Reject 1. Motion Req'd & Controller Busy 2. Backward motion Req'd & at Load Point 3. Write command given & no write ring
4.	Timing Error
5	End of Tape
6	Start of Tape
7	End of File
8	Local Mode

2020 MAG. TAPE SERVICE DATA

MAG. TAPE INTERFACE 12538B

MAG. TAPE DIAGNOSTIC 20516

INITIALIZE: Load Tape S.A. = 100; A-reg bits 0-5 = data channel SC; A-reg bit 15 = 1 for 2114/2115; B-reg bits 0-5 = TTY SC.

Set Sw Reg Options, RUN, Restart address = 1300

Bit	Function
0	Rewing and SOT Test
1	Extensive Read/Write
2	Write Ring Test
3	Not Used
12	Halt/Print #Cycles
13	Halt On Errors
14	Loop On Check/No Print
15	Pause

HALTS

HLT 11	Tape Unit Not On Automatic
13	Too Long in Command Wait
14	Too Long in Data Flag Wait
15	Operation Required and Controller Busy
55	Switch 13 Up and an Error
73	Switch 12 Up
74	Write Ring Tests. Remove Write Ring
75	Write Ring Tests. Replace Write Ring
76	Halt After Rewind and Unload
77	OK HALT, Switch 15 up

AUXILIARY TESTS

S.A. 1300 Sw Reg Options

Bit	Function
0	Write Odd Parity
1	Write Even Parity
3	Read Odd Parity
4	Read Even Parity
9	Write 1's/Read Into B-reg

7970A/B 7-TRACK MTU SERVICE DATA

7-TRACK INTERFACE 13182A

7-TRACK DIAGNOSTIC (13028)

INITIALIZE: Load and Configure SIO for TTY, S.A. = 100, Sw Reg = S.C. Mag Tape 1, PRESET, RUN, HLT 0, Sw Reg = Bit 15 is set for 2114, Bit 11 for 2100/21MX. Both Bits clear for 2116, Bit 0 = 12-1/2 IPS, Bit 1 = 25 IPS, Bit 2 = 37.5 IPS, Bit 3 = 45-1/2 IPS, Bits 12 and 13 Reset [for Even and then Odd Parity Mode], PRESET, RUN, HLT 1.

Set Sw Reg Options, RUN, Restart address = 2000

Bit	Function
0-3	Unit Select
4	Inhibit Extension Data Test
5	Inhibit Intercord Gap Creep Test
6	Write Enable Test
7	Inhibit Rewind
8	Inhibit DMA
9	Rewind Off-Line
10	Disable All Error Printout
11	Print All Data Errors (when clear print only 1st error)
12	Halt at End of Complete Cycle
13	Repeat Current Test
14	Halt on Error
15	See 13182 Manual of Diagnostics

HALTS

HLT 10	After Rewind/Unload
11	All Units off-line
55	After Error with Sw 14
56	Write Enable Halt to Remove Ring
57	Write Enable Halt to Replace Ring
76	With 15 Set After Current Test
77	With 12 Set After Complete System

AUXILIARY

SA 110=Unit Select
SA 111=Density Test
SA 112=Parity Select
SA 113=TV Command Exercise
SA 114=Write Routine from Sw Reg
SA 115=Write All "1's" and "0's"
SA 116=Controller Command Routine

0=Write, 1=EOF, 2=GAP, 3=GAP and EOF, 4=Read
5=FSR, 6=BSR, 7=FSF, 8=BSF, 9=Rewind, 10=Rewind Off-Line
11=Write Backspace Error Test

SA 117=Parity Error Test

7970A/B 7-TRACK MTU SERVICE DATA (CONT)

STATUS BITS

Bit	Status
0	Controller Busy
1	Parity Error
2	Timing Error
3	Reject
4	E.O.T.
5	LP
6	E.O.F.
7	No Write Ring
8	Local
9	T.U. Busy
10	Rewind
11-12	Density

MESSAGE ANALYSIS

CB=Controller Busy, PT=Parity Error, CR=Command Reject
TM=Timing Error, ET=E.O.T., LP=Load Point,
FM=File Mark, FP=No Write Ring, OF=T.U. Off-Line,
TB=T.U. Busy, RW=T.U. Rewind

13182A CONTROLLER COMMANDS

CODE (OCTAL)	MNEMONIC	FUNCTION
301	WCC	Write Record*
121	GAP	Write 3 Inches Blank Tape
203	RCC	Read Record*
3	FSR	Forward Space 1 Record
5	BSR	Backspace Record
31	RWO	Rewind and Off-Line
11	REW	Rewind
110	CLR	Clear Controller
141	WFM	Write File Mark**
1400	SEL0	Select Unit 0
2400	SEL1	Select Unit 1
4400	SEL2	Select Unit 2
10400	SEL3	Select Unit 3
43	FSF	Forward Space File**
45	BSF	Backspace File**
161	GWFM	Gap and Write File Mark**

*Bit 15 set with any of the Read/Write commands indicates BCD mode of data transfer.

**File Mark oriented commands should be given in BCD mode to prevent indicating the file mark as having a parity error.

7970A/B/E 9-TRACK MTU SERVICE DATA

7970A/B INTERFACE 13181A DIAGNOSTIC 13181-16001
7970E INTERFACE 13183A DIAGNOSTIC 13181-16001

Initialize

1. Load and configure diagnostic configurator HP P/N 24296-60001.

2. Load 7970 diagnostic P/N 13181-16001 using the protected loader.

3. SA = 100 switch register setting per following table press PRESET (INT/EXT), run HLT 102074

   SW BITS

0-5	Select code mag tape 1
6 thru 8	Not used
9	Non-DMA (DCPC) for 13183
10	13181 Interface
11	13183 Interface
12	12.5 IPS
13	25 IPS
14	37.5 IPS
15	45 IPS

4. Make selection of switch register options per following table press PRESET (INT/EXT), run. Program will execute.

   Restart address is 2000

   To re-configure start at address 100

SW BITS	MEANING IF SET
0-3	Unit select (if reset auto select) [auto select for multi-unit only]
4*	Use DMA (DCPC) channel 1 on all Read/Write
5*	Use DMA (DCPC) channel 2 on all Read/Write
6	Inhibit test with enbedded rewinds
7	Delete CRCC and LRCC checks (13181 only)
8	Suppress test which require operator intervention
9	Go to User Test Selection Section. Selected test in A or B register. See table below.
10	Suppress non-error messages
11	Suppress error messages
12	Loop on diagnostic
13	Loop on last test
14	Suppress error halts
15	Halt 76 at end of each test

*If DMA (DCPC) is not available, the program will override switch register setting.

List of test with A/B-register settings.

BIT POSITION TEST NUMBER A REG B REG OCTAL	DECIMAL		TEST TITLE
0	0	0	Basic I/O
1	1	1	Initial clear controller and unit selection
2	2	2	Beginning of tape (BOT)
3	3	3	Command reject at BOT
4	4	4	Write command execution time
5	5	5	Gap command execution time
6	6	6	File mark command
7	7	7	Multiple file mark
8	10	8	Initial Write/Read
9	11	9	125125 Write/Read
10	12	10	Force data and timing error status
11	13	11	Record spacing
12	14	12	File spacing
13	15	13	Clear time check during a motion command command
14	16	14	Interrecord gap
15	17	15	Negative interrecord gap creep
0	20	16	Write/Read single rotating bit pattern
1	21	17	Write/Read channel sawtooth pattern
2	22	18	Write/Read track sawtooth pattern
3	23	19	Write/Read (non DMA) random data
4	24	20	DMA channel 1 write/read with random data
5	25	21	DMA channel 2 write/read with random data
6	26	22	Rapid write
7	27	23	Echo check on all on-line units

List of test with A/B-register settings (continued)

BIT POSITION TEST NUMBER A REG B REG OCTAL	DECIMAL		TEST TITLE
8	30	24	Controller check for multi-unit operation
9	31	25	Inter-unit compatibility
10	32	26	Write ring enable
11	33	27	Rewind off-line
12	34	28	Write all ones record
13	35	29	Read an all ones record
14	36	30	Operator service routine
15	37	31	Operator Design*

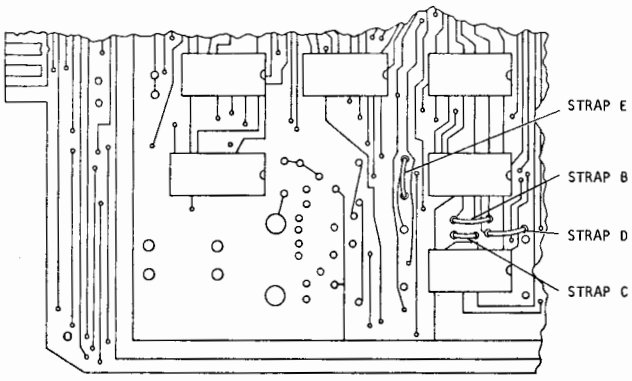
*For operator design procedure consult MOD.

7970A/B/E 9-TRACK MTU SERVICE DATA (CONT)

13181A SPEED-STRAPPING

Tape speed strapping is shown below and described as follows:

a. For 12.5 IPS speed, use straps B, D, and E.
b. For 25 IPS speed, use straps B and E.
c. For 37.5 IPS speed, use strap D.
d. For 45 IPS speed, use strap D and change from 300-kHz crystal (part no. 0410-0163) to 360-kHz crystal (part no. 0410-0431).



9866A LINE PRINTER SERVICE DATA

9866 SPECIFICATIONS

Printing Speed:	240 lines/minute (64 character set)	
Power Required:	Nom. - 100, 120, 220, 240 V ac; ± 5 to 10% ea. range (48 Hz to 66 Hz) Power - 250 volt-amps, max.	
Operating Conditions:	Operating Temp:	0°C to 45°C
	Humidity Range:	95% R.H. (non-condensing)
Physical Characteristics:	Size:	17 3/4" x 16" x 6" (45.09 cm x 40.64 cm x 15.24 cm)
	Weight:	45 lbs.
Operating Supplies Available:	Printer Paper:	2 ea. Blue Printout P/N 9281-0414 2 ea. Black Printout P/N 9281-0413
	Paper Dimensions:	8 3/4" wide, thermal sensitive paper

LINE PRINTER INTERFACE 12597A

LINE PRINTER DIAGNOSTIC (12996)

Load Diagnostic Configurator

Load Diagnostic, SA = 100
SW Reg = (0-5) sc line printer PRESET RUN, HLT 74

Enter sw reg. options, PRESET RUN

Note: Use test options if DMS/DCPC not present.

Set Sw options as follows: Restart = 2000

BIT	FUNCTION
0-6	Reserved
7	Inhibit messages on LP
8	Inhibit Operator Intervention test
9	HLT after current section (HLT 75) enter test options in A REG. RESET Sw Reg Bit 9 press RUN.
10	Inhibit non-error messages
11	Inhibit error messages
12	Do not HLT
13	Loop current test
14	Inhibit error halt
15	HLT 76

TEST OPTIONS

A-Reg Bit	Test
0	Basic I/O
1	Status & Buffer
2	Cyclic Pattern
3	Triangle & Over Buffer Full
4	Non-Print Characters
5	Worst Case Pattern
6	DMA/DCPC
7	Pseudo Opdesign

2892 CARD READER SERVICE DATA

SPECIFICATIONS

Reading Speed:	600 cards/minute
Card Type:	Standard 80-column cards
Hopper Size:	7.25 inches
Stacker Size:	7.25 inches
Power:	115V ±10%, 60 Hz, 1ϕ
	230V ±10%, 50 Hz, 1ϕ
	1350VA turn on, 450VA running
Size:	16-1/4"H, 23-1/16"W, 18"D
Weight:	77 lb.
Temperature:	50°-100°F
Humidity:	30 - 90% non-condensing

CARD READER DIAGNOSTIC (24267)

1. Load and configure TTY SIO DRIVER.
2. Load Diagnostic, SA = 2.
3. Set Sw reg bit 0 = 0 to configure the following options:

Bit	Function
0	Override Internal Sw. Reg.
1	Basic I/O
2	Status Test
3	Functional Test
4	Standard Data
5	Read Rate
6	Not Used
7	Flag Count
8	Timed Pick Rate Test
9	Execute List
10	Suppress Non-Error Messages
11	Suppress All Messages
12	HLT After One Cycle
13	Loop Current Test
14	Do not HLT
15	Orderly HLT

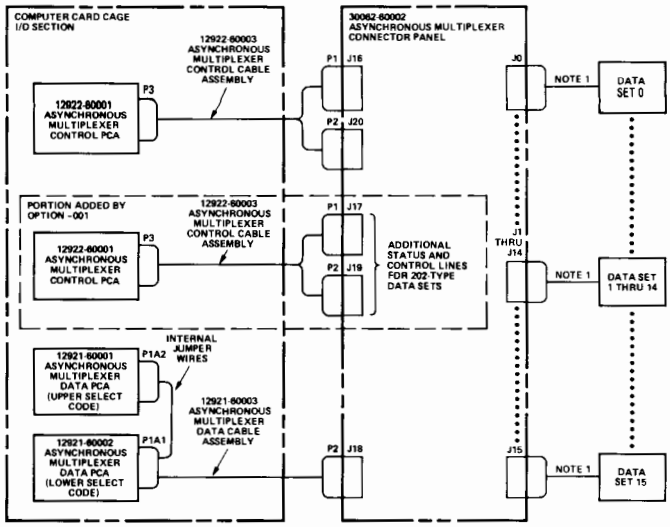
4. Press INTERNAL and EXTERNAL PRESET; press RUN.
5. After HLT 77, restart address 100, press RUN.

TERMINAL CABLES

	INTERFACE		CABLE NO.
2100	12889A	–	12889-60003
21MX	12889A	–	12889-60003
2600A	12966A	–	12966-60004
	12968A	–	12966-60004
	12880A	–	12880-60003
	12587B	001	12587-60010
	12920B	–	30062-60006
	12920B	–	30062-60009
	12920B	–	30062-60012
2615A	12966A	–	12966-60004
	12968A	–	12966-60004
	12920B	–	30062-60006
	12880A	–	12880-60003
	12587B	001	12587-60010
	12920B	–	30062-60009
	12920B	–	30062-60012
2640-6	12880A	–	12880-60001
2640A	12966A	001	12966-60005
	12968A	001	12966-60005
	12920B	–	02640-60043
2749B	12966A	003	12966-60007
	12968A	003	12966-60007
	12920B	–	30062-60006
	12531C	001	12531-60021
	12920B	–	30062-60009
	12920B	–	30062-60012
2762A	12966A	–	12966-60004
	12968A	–	12966-60004
	12920B	–	30062-60006
	12531D	001	12531-60026
	12587B	001	12587-60010
	12920B	–	30062-60009
	12920B	–	30062-60012
2762B	12966A	–	12966-60004
	12968A	–	12966-60004
	12920B	–	30062-60006
	12531D	001	12531-60026
	12587B	001	12587-60010
	12920B	–	30062-60009
	12920B	–	30062-60012
3000	12889A	–	12889-60003

TERMINAL CABLES (CONT)

	INTERFACE		CABLE NO.
801ACU	125B9A	–	12589-60004
CPU	12889A	–	12889-60003
CPU	12889A	–	12889-60003
M103FX	12966A	002	12966-60006
	12968A	002	12966-60006
	12920B	–	30062-60004
	12531C	002	12531-60024
	12531D	002	12531-60024
	12587B	–	12587-60006
	12920B	–	30062-60007
	12920B	–	30062-60010
M201FX	12967A	–	12967-60004
	12618A	–	12618-60001
M201HX	12967A	–	12967-60004
	12618A	–	1261B-60001
M202FX	12966A	002	12966-60006
	12968A	002	12966-60006
	12920B	–	30062-60004
	12587B	002	12587-60011
	12920B	–	30062-60007
	12920B	–	30062-60010
M202HX	12966A	002	12966-60006
	12968A	002	12966-60006
	12920B	–	30062-60004
	12587B	–	12587-60006
	12920B	–	30062-60007
	12920B	–	30062-60010
M208FX	12967A	–	12967-60004
	12618A	–	12618-60001
M208HX	12967A	–	12966-60004
	12618A	–	12618-60001



NOTES:

1. DATA SET CONNECTOR CABLES ARE FABRICATED AS REQUIRED. REFER TO PARAGRAPH 2-8
2. THE ASYNCHRONOUS MULTIPLEXER TEST CABLE, PART NO. 30062-60003, IS CONNECTED BETWEEN ANY TWO DATA SET CONNECTORS (J0 THRU J15) WHEN RUNNING DIAGNOSTIC PROGRAMS.
3. REFER TO THE INTERCONNECTING DIAGRAM, FIGURE 5-5 FOR CONNECTOR PIN NUMBERS.

PARTS

CONTENTS PAGE

LAMPS

2100	2140-0364
2114	2140-0240
2115	2140-0035
2116	2140-0035
2737	2140-0252

SWITCHES

2100 Panel	3101-1531
2115/2116	
Sw Register	3101-1051
"LOAD"	3101-0715
Power Pushbutton	3101-0714
Power Toggle	3101-0005
21MX	
White	5040-6076
Gray	5040-6077

TELETYPE

Ribbon	9283-0002
Tape Spool	1530-1436
TTY Kit	5080-6610

DISC SCRATCH PACKS

2870	12536A
2883/2884	12868A
7900/7901	12869A

MAGNETIC TAPE

IBM Alignment Tape	9162-0027
1200' Magnetic Tape	9162-0026
2400' Magnetic Tape	9162-0025

LED'S

21MX	1990-0325

MISCELLANEOUS

Spring Contact	02108-00014
Switch Retainer	02108-40002

INTEGRATED CIRCUITS

*	1820-0054	* IC,QUAD 2-INPUT NAND GATE,TTL	* 01295	* SN7400N
*	1820-0068	* IC,TRIPLE 3-INPUT NAND GATE,TTL	* 01295	* SN7410N
*	1820-0069	* IC,DUAL 4-INPUT NAND GATE,TTL	* 01295	* SN7420N
*	1820-0076	* IC,DUAL J-K FLIP-FLOP W/PRESET AND CLOCK,TTL	* 01295	* SN7476N
*	1820-0077	* IC,DUAL D FLIP-FLOP,TTL	* 01295	* SN7474N
*	1820-0140	* IC,DUAL 4-INPUT AND BUFFER,TTL	* 04713	* MC3026P
*	1820-0141	* IC,QUAD 2-INPUT AND GATE,TTL	* 04713	* MC3001P
*	1820-0142	* IC,DUAL 4-INPUT OR/NOR GATE,ECL	* 04713	* MC1004P
*	1820-0174	* IC,HEX INVERTER,TTL	* 01295	* SN7404N
*	1820-0175	* IC,HEX INVERTER,OPEN-COLLECTOR,TTL	* 01295	* SN7405N
*	1820-0205	* IC,QUAD 2-INPUT OR GATE,TTL	* 04713	* MC3003P
*	1820-0215	* IC,TRANSISTOR,NPN	* 28480	* 1820-0215
*	1820-0239	* IC,QUAD 2-INPUT NOR GATE,TTL	* 04713	* MC3002P
*	1820-0246	* IC,TRANSISTOR,NPN	* 07263	* 2N3643
*	1820-0261	* IC,MONOSTABLE MULTIVIBRATOR,TTL	* 01295	* SN13617
*	1820-0262	* IC,4-BIT PAR-IN SER-OUT SHIFT REGISTER,TTL	* 27014	* DM8590N
*	1820-0269	* IC,QUAD 2-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN7403N
*	1820-0281	* IC,DUAL J-K M-S FLIP-FLOP W/SEP CLK INPUTS,TTL	* 01295	* SN13618
*	1820-0282	* IC,QUAD 2-INPUT EXCLUSIVE OR GATE,TTL	* 01295	* SN13603
*	1820-0294	* IC,4 BIT SER-IN PAR-OUT SHIFT REGISTER,TTL	* 27014	* SD9935
*	1820-0301	* IC,QUAD BISTABLE D LATCH,TTL	* 01295	* SN4463
*	1820-0301	* IC,QUAD BISTABLE D LATCH,TTL	* 01295	* SN7475N
*	1820-0328	* IC,QUAD 2-INPUT NOR GATE,TTL	* 01295	* SN4467
*	1820-0367	* IC,4-BIT RT/LT SHIFT REGISTER PAR IN/OUT,TTL	* 01295	* SN7495N
*	1820-0370	* IC,HS QUAD 2-INPUT NAND GATE,TTL	* 01295	* SN74H00N
*	1820-0371	* IC,HS TRIPLE 3-INPUT NAND GATE,TTL	* 01295	* SN74H10N
*	1820-0372	* IC,TRIPLE 3-INPUT AND GATE,TTL	* 01295	* SN74H11N
*	1820-0373	* IC,HS DUAL 4-INPUT NAND GATE,TTL	* 01295	* SN74H20N
*	1820-0374	* IC,HS DUAL 4-INPUT AND GATE,TTL	* 01295	* SN74H21N
*	1820-0375	* IC,HS 8-INPUT NAND GATE,TTL	* 01295	* SN74H30N
*	1820-0376	* IC,HS DUAL 4-INPUT NAND BUFFER,TTL	* 01295	* SN74H40N
*	1820-0379	* IC,HS 2-2-2-3-INPUT EXP AND-OR GATE,TTL	* 01295	* SN74H52N
*	1820-0381	* IC,HS 4-WIDE 2-2-2-3-INPUT AND-OR INVERT GATE,TTL	* 01295	* SN4489

INTEGRATED CIRCUITS (CONT)

*	1820-0342	* IC,HS 4-INPUT EXP AND-OR-INVERT GATE,TTL	* 01295	* SN74H55N
*	1820-0384	* IC,HS TRIPLE 3-INPUT EXPANDER,TTL	* 01295	* SN74461N
*	1820-0424	* IC,HS HEX INVERTER,TTL	* 01295	* SN74H04N
*	1820-0435	* IC,8-BIT ODD/EVEN PARITY GENERATOR/CHECKER,TTL	* 01295	* SN14656
*	1820-0469	* IC,HS J-K FLIP-FLOP,TTL	* 01295	* SN19234
*	1820-0471	* IC,HEX INVERTER OPEN-COLLECTOR (30V),TTL	* 01295	* SN19235
*	1820-0491	* IC,BCD/DECIMAL DECODER/DRIVER,TTL	* 01295	* SN74145N
*	1820-0511	* IC,QUAD 2-INPUT AND GATE,TTL	* 01295	* SN20572
*	1820-0512	* IC,HS DUAL D FLIP-FLOP,TTL	* 01295	* SN74H74N
*	1820-0515	* IC,DUAL RE-TRIG ONE SHOT WITH RE-SET,TTL	* 07263	* U6B960259X
*	1820-0535	* IC,DUAL PERIPHERAL 2-INPUT AND DRIVER,TTL	* 01295	* SN75451AP
*	1820-0545	* IC,4-BIT BINARY UP/DN COUNTER,TTL	* 01295	* SN23172
*	1820-0574	* IC,QUAD D FLIP-FLOP W/PAR CLK AND CLEAR,TTL	* 27014	* DM855IN
*	1820-0598	* IC,LP QUAD 2-INPUT EXCLUSIVE OR GATE,TTL	* 27014	* DM74L86N
*	1820-0602	* IC,LP 8-BIT SHIFT REGISTER,TTL	* 27014	* DM86L70N
*	1820-0603	* IC,LP 4-BIT MAGNITUDE COMPARATOR,TTL	* 27014	* DM82L85N
*	1820-0604	* IC,DUAL 4-INPUT NAND POWER GATE,TTL	* 04713	* MC3025P
*	1820-0605	* IC,HS QUAD 2-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN74H01N
*	1820-0606	* IC,ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR,TTL	* 01295	* SN74181N
*	1820-0607	* IC,ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR,TTL	* 01295	* SN74181N
*	1820-0608	* IC,4-BIT RIGHT/LEFT SHIFT REGISTER,TTL	* 04713	* MC4012P
*	1820-0609	* IC,1-OF-4 DECODER,TTL	* 04713	* MC4006P
*	1820-0610	* IC,DUAL J-K FLIP-FLOP,TTL	* 04713	* MC3061P
*	1820-0611	* IC,DUAL 4-INPUT MULTIPLEXER,TTL	* 04713	* MC8309P
*	1820-0612	* IC,LOOK-AHEAD CARRY GENERATOR,TTL	* 01295	* SN74182N
*	1820-0613	* IC,4-BIT (4X2) RAM,CTL	* 07263	* U6490305QX
*	1820-0614	* IC,HS HEX INVERTER,OPEN COLLECTOR,TTL	* 01295	* SN74H05N
*	1820-0615	* IC,LP DUAL 4-BIT LATCH,TTL	* 07263	* U6N93L0859X
*	1820-0616	* IC,9-INPUT MULTIPLEXER,TTL	* 04713	* MC8312P
*	1820-0617	* IC,2-INPUT 4-BIT MULTIPLEXER,TTL	* 07263	* U7B932259X
*	1820-0618	* IC,QUAD 2-INPUT EXCL.NOR GATE,TTL	* 04713	* MC3022P
*	1820-0619	* IC,HEX BUFFER/DRIVER,OPEN COLLECTOR,TTL	* 01295	* SN7417N
*	1820-0619	* IC,HS DUAL 4-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN74H22N

INTEGRATED CIRCUITS (CONT)

*	1820-0620	* IC:DUAL 4-INPUT MULTIPLEXER,TTL	* 01295	* SN74153N
*	1820-0621	* IC:QUAD 2-INPUT NAND BUFFER,OPEN COLLECTOR,TTL	* 01295	* SN7438N
*	1820-0622	* IC:8-INPUT MULTIPLEXER,TTL	* 01295	* SN74151N
*	1820-0623	* IC:4-BIT COMPARATOR,TTL	* 27014	* DM8200N
*	1820-0624	* IC:DUAL COMPARATOR,ECL	* -	* 1820-0624
*	1820-0625	* IC:MTL TRIPLE LEVEL TRANSLATOR (TTL-TO-MTL)	* 04713	* MC666P
*	1820-0626	* IC:4-BIT LATCH,TTL	* 07263	* U7A931459X
*	1820-0627	* IC:LP BCD/DECIMAL DECODER,TTL	* 07263	* U7B93L0159X
*	1820-0628	* IC:64-BIT (16X4) RAM,TTL	* 01295	* SN7489N
*	1820-0629	* IC:HS DUAL J-K FLIP-FLOP,EDGE TRIGGERED,TTL	* 01295	* SN74S112N
*	1820-0630	* IC:PHASE/FREQUENCY DETECTOR,TTL	* 04713	* MC4044P
*	1820-0631	* IC:HS DUAL J-K FLIP-FLOP,EDGE TRIGGERED,TTL	* 01295	* SN74H108N
*	1820-0632	* IC:CONTROL	* 28480	* 1820-0632
*	1820-0633	* IC:TIME BASE	* 28480	* 1820-0633
*	1820-0634	* IC:HEX DECADE CNTR	* 28480	* 1820-0634
*	1820-0635	* IC:LED SCANNER-DRIVER	* 28480	* 1820-0635
*	1820-0636	* IC:4-BIT BINARY CNTR/STORAGE ELEMENT,TTL	* 18324	* C4820A
*	1820-0637	* IC:TRIPLE 3-INPUT NOR GATE,TTL	* 18324	* N8875A
*	1820-0638	* IC:WAFER	* 28480	* 1820-0638
*	1820-0639	* IC:BCD-BINARY/BINARY-BCD CONVERTER,TTL	* 04713	* MC4001P
*	1820-0640	* IC:16-INPUT MULTIPLEXER,TTL	* 01295	* SN74150N
*	1820-0655	* IC:DUAL 4-INPUT NOR GATE,TTL	* 01295	* SN7425N
*	1820-0656	* IC:LP 2-INPUT 4-BIT MULTIPLEXER,TTL	* 01295	* SN74L98N
*	1820-0657	* IC:8-INPUT PRIORITY ENCODER,TTL	* 07263	* U7A931859X
*	1820-0658	* IC:LP 8-INPUT MULTIPLEXER,TTL	* 07263	* U7B93L1259X
*	1820-0659	* IC:LP SYNCHRO 4-BIT SHIFT REG W/PAR IN/OUT,TTL	* 07263	* U7B93L0059X
*	1820-0660	* IC:2240 BIT ROM,CHAR GEN	* -	* 1820-0660
*	1820-0661	* IC:QUAD 2-INPUT OR GATE,TTL	* 01295	* SN7432N
*	1820-0663	* IC:SOLID STATE DISPLAY SCANNER,VS=5V 5%	* 28480	* 1820-0663
*	1820-0665	* IC:4-BIT LATCH,DTL	* 04713	* MC1R14P
*	1820-0666	* IC:DUAL 4-INPUT OR-NOR GATE,OPEN EMITTER,ECL	* 04713	* MC1006P
*	1820-0667	* IC:64-BIT LATCH W/STROBED OUTPUTS,ECL	* 04713	* MC1040P
*	1820-0668	* IC:HEX DRIVER,OPEN COLLECTOR,TTL	* 01295	* SN7407N

INTEGRATED CIRCUITS (CONT)

*	1820-0669	* IC,DECADE COUNTER,(LOW POWER),TTL	* 07263	* U7893L1059X
*	1820-0671	* IC,CONTROL LOGIC CHIP,MOS,PD=300MW,PKG-24	* 28480	* 1820-0671
*	1820-0681	* IC,HS QUAD 2-INPUT NAND GATE,TTL	* 01295	* SN74S00N
*	1820-0682	* IC,HS QUAD 2-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN74S03N
*	1820-0683	* IC,HS HEX INVERTER,TTL	* 01295	* SN74S04N
*	1820-0684	* IC,HS HEX INVERTER,OPEN COLLECTOR,TTL	* 01295	* SN74S05N
*	1820-0685	* IC,HS TRIPLE 3-INPUT NAND GATE,TTL	* 01295	* SN74S10N
*	1820-0686	* IC,TRIPLE 3-INPUT AND GATE,SCHOTTKY TT	* 01295	* SN74S11N
*	1820-0687	* IC,HS TRIPLE 3-INPUT AND GATE,OPEN COLLECTOR,TTL	* 01295	* SN74S15N
*	1820-0689	* IC,HS DUAL 4-INPUT NAND GATE,TTL	* 01295	* SN74S20N
*	1820-0689	* IC,HS DUAL 4-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN74S22N
*	1820-0690	* IC,HS DUAL 4-INPUT NAND BUFFER,TTL	* 01295	* SN74S40N
*	1820-0691	* IC,HS 4-WIDE 4-2-3-2-INPUT AND-OR-INVERT GATE,TTL	* 01295	* SN74S64N
*	1820-0692	* IC,HS 4-2-3-2-INPUT AND-OR-INVERT GATE,OPEN COLLECTOR,TTL	* 01295	* SN74S65N
*	1820-0693	* IC,HS DUAL D FLIP-FLOP W/DIRECT CLEAR,TTL	* 01295	* SN74S74N
*	1820-0694	* IC,HS QUAD 2-INPUT EXCLUSIVE-OR GATE,TTL	* 01295	* SN74S86N
*	1820-0695	* IC,HS DUAL J-K FLIP-FLOP W/PRESET,TTL	* 01295	* SN74S113N
*	1820-0696	* IC,HS DUAL J-K FLIP-FLOP,EDGE TRIGGERED,TTL	* 01295	* SN74S114N
*	1820-0697	* IC,HS DUAL 4-INPUT NAND BUFFER(LINE DRIVER),TTL	* 01295	* SN74S140N
*	1820-0698	* IC,TRI DECADE BUFFER,MOS	* 28480	* 1820-0698
*	1820-0699	* IC,ADDER CHIP,MOS ALGEBRIC ADD	* 28480	* 1820-0699
*	1820-0700	* IC,HS DUAL 3-INPUT 3-OUT SERIES TERM LINE DRIVER,TTL	* 04713	* MC3029P
*	1820-0701	* IC,LP 4-BIT LATCH,TTL	* 07263	* U7893L1459X
*	1820-0702	* IC,LP 1-OF-16 DECODER,TTL	* 07263	* U6N93L1159X
*	1820-0703	* IC,DECADE COUNTER,PRESETTABLE(LOW POWER),TTL	* 18324	* N8292A
*	1820-0704	* IC,MONOSTABLE MULTIVIBRATOR RETRIG W/CLEAR,TTL	* 01295	* SN74122N
*	1820-0705	* IC,DECADE COUNTER,SYNCHRO,PRESETTABLE,TTL	* 07263	* U7B931059X
*	1820-0706	* IC,5-BIT COMPARATOR,TTL	* 07263	* U7B932459X
*	1820-0707	* IC,BCD/DECIMAL DECODER/DRIVER,TTL	* 01295	* SN74141N
*	1820-0708	* IC,LP DUAL 4-INPUT MULTIPLEXER,TTL	* 07263	* U6A93L0959X
*	1820-0709	* IC,LP 8-BIT SHIFT REGISTER,TTL	* 07263	* U7B93L2859X
*	1820-0712	* IC,BINARY PRESCALER,ECL	* 28480	* 1820-0712
*	1820-0713	* IC,4-BIT BINARY COUNTER,SYNCHRO,PRESETTABLE,TTL	* 01295	* SN74163N

INTEGRATED CIRCUITS (CONT)

*	1820-0714	* IC,QUINARY DIVIDER	* 28480	* 1820-0714
*	1820-0715	* IC,HS DUAL J-K FLIP-FLOP EDGE TRIGGERED,TTL	* 01295	* SN74H106N
*	1820-0716	* IC,4-BIT BINARY COUNTER,W/CLEAR,TTL	* 01295	* SN74161N
*	1820-0717	* IC,DUAL 40-BIT STATIC SHIFT REGISTER,MOS	* 27014	* MM5052
*	1820-0718	* IC,TRANSLATOR/2-PHASE CLOCK DRIVER,TTL-TO-MOS	* 27014	* NH0025CN
*	1820-0719	* IC,QUAD EXCLUSIVE NOR GATE,OPEN COLLECTOR,TTL	* 18324	* MC7242P
*	1820-0720	* IC,DUAL DIFFERENTIAL LINE DRIVER,TTL	* 27014	* DM8830N
*	1820-0721	* IC,DUAL DIFF LINE RECEIVER W/STROBE,TTL	* 27014	* DM8820AN
*	1820-0722	* IC,DUAL LINE DRIVER,TTL	* 01295	* SN75109N
*	1820-0723	* IC,DUAL LINE RECEIVER W/STROBE,TTL	* 01295	* SN75107N
*	1820-0724	* IC,DUAL 1-OF-4 DECODER W/ENABLE,TTL	* 04713	* MC4007P
*	1820-0725	* IC,16-BIT RAM (4X4),TTL	* 01295	* SN74170J
*	1820-0726	* IC,8-BIT SHIFT REGISTER PAR,IN/OUT,TTL	* 01295	* SN74199N
*	1820-0727	* IC,DUAL 1-OF-4 DECODER W/ENABLE,TTL	* 07263	* U7893215QX
*	1820-0728	* IC,DUAL 50-BIT SR,MOS,VCC=5V,TO-77	* 28480	* 1820-0728
*	1820-0729	* IC,BCD-TO-DECIMAL DECODER/DRIVER(NIXIE),TTL	* 28480	* 1820-0729
*	1820-0730	* IC,LP RE-TRIG/RE-SET MONOSTABLE MULTIVIBRATOR,TTL	* 34335	* U7896L0259X
*	1820-0731	* IC,AMPL-TRIG	* 28480	* 1820-0731
*	1820-0732	* IC,DECADE UP/DN COUNTER W/ZERO DETECTOR,TTL	* 28480	* 1820-0732
*	1820-0733	* IC,QUAD 256-BIT DYNAMIC SHIFT REGISTER,MOS	* 34649	* P1402
*	1820-0734	* IC,DECADE UP/DN COUNTER,SYNCHRO,20MHZIN,TTL	* 01295	* SN74190N
*	1820-0736	* IC,D FLIP-FLOP	* 28480	* 1820-0736
*	1820-0737	* IC,12-INPUT PARITY GENERATOR/CHECKER,TTL	* 07263	* U7893485QX
*	1820-0738	* IC,DUAL 1-OF-4 DECODER W/SEP ENABLE,COMM SELECT,TTL	* 01295	* SN74155N
*	1820-0739	* IC,HS J-K FLIP-FLOP,EDGE TRIGGERED,TTL	* 01295	* SN74H101N
*	1820-0740	* IC,HS 4-BIT TRUE/COMPLEMENT 0/1 ELEMENT,TTL	* 01295	* SN74H87N
*	1820-0741	* IC,DUAL 8-BIT SHIFT REGISTER,TTL	* 07263	* U7893285QX
*	1820-0742	* IC,DUAL 4-BIT LATCH,TTL	* 07263	* U6N9308S9X
*	1820-0743	* IC,4-BIT BI-DIRECTIONAL UNIV SHIFT REGISTER,TTL	* 01295	* SN74194N
*	1820-0744	* IC,6-BIT BINARY COUNTER,SYNCHRO,25MHZ MIN,TTL	* 01295	* SN7497N
*	1820-0745	* IC,QUAD 2-2-2-4-INPUT NOR GATE,TTL	* 07263	* U6B901559X
*	1820-0746	* IC,DECODER,LED DRIVER,CHIP-DGTL	* 28480	* 1820-0746
*	1820-0747	* IC,DECODER & LED DRIVER,CHIP-DGTL	* 28480	* 1820-0747
*	1820-0748	* IC,DECODER,LED DRIVER,CHIP-DGTL	* 28480	* 1820-0748

INTEGRATED CIRCUITS (CONT)

*	1820-0752	* IC,MS DUAL J-K M/S FLIP-FLOP W/PRESET,CLEAR,TTL	* 01295	* SN74H76N
*	1820-0753	* IC,DUAL 3-INPUT LOGIC GATE,ECL	* 28480	* 1820-0753
*	1820-0754	* IC,AMP-LIMITER,FECL FAMILY	* 28480	* 1820-0754
*	1820-0755	* IC,8-BIT DRIVER NON-INVERTING(TRI-STATE),TTL	* 28480	* 1820-0755
*	1820-0756	* IC,8-BIT DRIVER INVERTING(TRI STATE),TTL	* 28480	* 1820-0756
*	1820-0757	* IC,LP 8-BIT DRIVER NON-INVERTING(TRI-STATE),TTL	* 28480	* 1820-0757
*	1820-0758	* IC,LP 8-BIT DRIVER NON-INVERTING,OPEN EMIT OUTPUT,TTL	* 28480	* 1820-0758
*	1820-0759	* IC,LP 8-BIT RECEIVER NON-INVERTING(TRI-STATE),TTL	* 28480	* 1820-0759
*	1820-0760	* IC,8-BIT RECEIVER INVERTING(TRI-STATE),TTL	* 28480	* 1820-0760
*	1820-0761	* IC,HEX-INVERTER/DRIVER	* 01295	* SN7406N
*	1820-0762	* IC,QUAD 2-INPUT MULTIPLEXER W/COMMON SELECT,TTL	* 01295	* SN74157N
*	1820-0763	* IC,1024-BIT DYNAMIC SHIFT REGISTER,MOS	* 34649	* M1404A
*	1820-0765	* IC,4-BIT BINARY COUNTER,PRESETTABLE,50MHZ MIN,TTL	* 01295	* SN74197N
*	1820-0767	* IC,POWER NAND GATE,DTL	* 28480	* 1820-0767
*	1820-0768	* IC,POWER NAND GATE,DTL	* 28480	* 1820-0768
*	1820-0769	* IC,QUAD 2-INPUT NAND POWER GATE,DTL	* 28480	* 1820-0769
*	1820-0770	* IC,DUAL 100-BIT DYNAMIC SHIFT REGISTER,MOS	* 27014	* MM5006H
*	1820-0771	* IC,WAFER, 7.1MA OPT	* 28480	* 1820-0771
*	1820-0772	* IC,WAFER, 5.0MA OPT	* 28480	* 1820-0772
*	1820-0773	* IC,WAFER, 3.5MA OPT	* 28480	* 1820-0773
*	1820-0774	* IC,TRIPLE 3-INPUT OR GATE,TTL	* 18324	* SP374A
*	1820-0775	* IC,1024-BIT,RANDOM ACCESS MEM ORGANIZED,MOS	* 34649	* 1820-0775
*	1820-0777	* IC,LP BCD/DECIMAL DECODER,TTL	* 01295	* SN74L42N
*	1820-0778	* IC,4-BIT BINARY COUNTER,PRESET(LOW PWR),TTL	* 07263	* 07893L1659X
*	1820-0780	* IC,QUAD SINGLE/DUAL DIFFERENTIAL LINE DRIVER,TTL	* 27014	* DM8831N
*	1820-0781	* IC,TRANSLATOR/DUAL 2-PHASE CLOCK DRIVER,TTL-TO-MOS	* 32293	* IM5013COD
*	1820-0782	* IC,TRIPLE 3-INPUT NOR GATE,TTL	* 01295	* SN7427N
*	1820-0783	* IC,256-BIT READ/WRITE MEMORY(RAM)(TRI-STATE),TTL	* 01295	* SN74200N
*	1820-0785	* IC,1-OF-8 DECODER W/INHIT,TTL	* 04713	* MC7250P
*	1820-0788	* IC,HEX D-TYPE FLIP-FLOP W/CLEAR,TTL	* 01295	* SN74174N
*	1820-0789	* IC,4-BIT BINARY COUNTER,PRESETABLE(LOW PWR),TTL	* 18324	* N8293A
*	1820-0790	* IC,DUAL 4-INPUT OR/NOR GATE(HIGH Z),ECL	* 04713	* MC1660L
*	1820-0791	* IC,QUAD 2-INPUT TRANSLATOR,ECL-TO-TTL	* 04713	* MC1068P

INTEGRATED CIRCUITS (CONT)

*	1820-0792	* IC,1-OF-8 DECODER,ECL	* 04713	* MC1043P
*	1820-0793	* IC,TRIPLE 2-INPUT EXCLUSIVE NOR GATE(HIGH Z),ECL	* 04713	* MC1674L
*	1820-0794	* IC,D-TYPE FLIP-FLOP(HIGH Z),ECL	* 04713	* MC1670L
*	1820-0795	* IC,QUAD 2-INPUT OR GATE(HIGH Z),ECL	* 04713	* MC1664L
*	1820-0796	* IC,QUAD 2-INPUT NOR GATE(HIGH Z),ECL	* 04713	* MC1662L
*	1820-0797	* IC,TRIPLE 2-INPUT EXCLUSIVE OR GATE(HIGH Z),ECL	* 04713	* MC1672L
*	1820-0799	* IC,DUAL PERIPHERAL 2-INPUT NAND DRIVER,TTL	* 01295	* SN75452P
*	1820-0401	* IC,QUAD 2-INPUT OR/NOR GATE W/STROBE,ECL	* 04713	* MC10101L
*	1820-0402	* IC,QUAD 2-INPUT NOR GATE,ECL	* 04713	* MC10102L
*	1820-0403	* IC,TRIPLE 2-3-2-INPUT OR/NOR GATE,ECL	* 04713	* MC10105L
*	1820-0404	* IC,TRIPLE 3-3-4-INPUT NOR GATE,ECL	* 04713	* MC10106L
*	1820-0405	* IC,TRIPLE 2-INPUT EXCLUSIVE OR/NOR GATE,ECL	* 04713	* MC10107
*	1820-0406	* IC,DUAL 4-5-INPUT OR/NOR GATE,FCL	* 04713	* MC10109L
*	1820-0407	* IC,DUAL 3-INPUT 3-OUTPUT OR GATE,ECL	* 04713	* MC10110L
*	1820-0408	* IC,DUAL 3-INPUT 3-OUTPUT NOR GATE,ECL	* 04713	* MC10111L
*	1820-0409	* IC,QUAD LINE RECEIVER W/CMPLMY OUTPUTS,ECL	* 04713	* MC10115
*	1820-0410	* IC,TRIPLE DIFF LINE RECEIVER W/CMPLMY OUTPUTS,ECL	* 04713	* MC10116L
*	1820-0411	* IC,DUAL 2-WIDE 2-3-INPUT OR-AND/OR-AND-INVERT GATE,FCL	* 04713	* MC10117L
*	1820-0412	* IC,DUAL 2-WIDE 3-INPUT OR-AND GATE,ECL	* 04713	* MC10118L
*	1820-0413	* IC,4-WIDE 4-3-3-INPUT OR-AND GATE,ECL	* 04713	* MC10119L
*	1820-0415	* IC,4-WIDE OR-AND/OR-AND-INVERT GATE,ECL	* 04713	* MC10121L
*	1820-0416	* IC,DUAL D LATCH W/SEP CLOCK,ECL	* 04713	* MC10130L
*	1820-0417	* IC,DUAL D M/S FLIP-FLOP W/SEP CLOCK,ECL	* 04713	* MC10131L
*	1820-0418	* IC,QUAD D LATCH,ECL	* 04713	* MC10133L
*	1820-0419	* IC,DUAL 2-INPUT MUXR W/CLOCKED LATCHES,ECL	* 04713	* MC10134L
*	1820-0420	* IC,DUAL J-K M/S FLIP-FLOP W/SET/RESET,ECL	* 04713	* MC10135L
*	1820-0421	* IC,4-BIT BINARY UP/DN COUNTER PRESETTABLE,ECL	* 04713	* MC10136L
*	1820-0422	* IC,DECADE UP/DN COUNTER PRESETTABLE,ECL	* 04713	* MC10137L
*	1820-0424	* IC,64-BIT (64X1) RAM,ECL	* 04713	* MC10140AL
*	1820-0425	* IC,4-BIT BI-DIR SHIFT REG,, W/SER/PAR IN/OUT,ECL	* 04713	* MC10141L
*	1820-0426	* IC,12-BIT PARITY GENERATOR/CHECKER,ECL	* 04713	* MC10160L
*	1820-0427	* IC,1-OF-8 DECODER W/ENABLE,ECL	* 04713	* MC10161L
*	1820-0428	* IC,1-OF-8 DECODER W/ENABLE,ECL	* 04713	* MC10162L

INTEGRATED CIRCUITS (CONT)

*	1820-0829	* IC,8-INPUT MULTIPLEXER W/ENABLE,ECL	* 04713	* MC10164L
*	1820-0830	* IC,LOOK-AHEAD-CARRY GENERATOR,ECL	* 04713	* MC10179L
*	1820-0831	* IC,4-BIT ARITHMETIC LOGIC UNIT,ECL	* 04713	* MC10181L
*	1820-0832	* IC,TRANSLATOR/CLOCK DRIVER,TTL-TO-MOS	* 27014	* SH15994
*	1820-0833	* IC,4-BIT ADDRESSABLE LATCH,TTL	* 02763	* U7A933459X
*	1820-0834	* IC,1-OF-8 DECODER W/INVERSION CONTROL,TTL	* 04713	* MC4043P
*	1820-0835	* IC,2-INPUT 4-BIT DIGITAL MULTIPLEXER W/OPEN COLL,TTL	* 18324	* N8267A
*	1820-0836	* IC,DUAL 4-BIT PARITY TREE,TTL	* 04713	* MC4010P
*	1820-0837	* IC,DUAL 4-INPUT NOR GATE,TTL	* 18324	* NA815A
*	1820-0839	* IC,QUAD D FLIP-FLOP W/CLEAR,TTL	* 01295	* SN74175N
*	1820-0841	* IC,QUAD 2-INPUT EXCLUSIVE OR GATE,TTL	* 04713	* MC3021P
*	1820-0842	* IC,4-BIT PARITY TREE,TTL	* 04713	* MC4008P
*	1820-0843	* IC,DUAL DATA DISTRIBUTOR(1-OF-4&1-OF-2 DECODER),TTL	* 04713	* MC4002P
*	1820-0844	* IC,DUAL 3-INPUT PULSE SHAPER/DELAY AND GATE,TTL	* 04713	* MC426
*	1820-0845	* IC,8-BIT CONTENT ADDRESSABLE MEMORY(CAM),TTL	* 18324	* N8220A
*	1820-0846	* IC,QUAD BUFFER (TRI-STATE),TTL	* 27014	* DM8094N
*	1820-0847	* IC,DUAL 2-BIT CARRY/SAVE FULL ADDERS H/S,TTL	* 01295	* SN74H183N
*	1820-0848	* IC,ARITH R REG,MOS,16 PIN DIP(UNIQUE TO DIV 22)	* 31471	* C-1746
*	1820-0849	* IC,CONTROL & TIMING,MOS,28 PIN DIP(UNIQUE TO DIV 22)	* 31471	* C-1747
*	1820-0850	* IC,UNIQUE TO DIV 22	* 31471	* -
*	1820-0851	* IC,UNIQUE TO DIV 22	* 31471	* -
*	1820-0852	* IC,UNIQUE TO DIV 22	* 31471	* -
*	1820-0855	* IC,2-PHASE CLOCK DR,MOS,8 PIN DIP	* 28480	* 5064A-0150
*	1820-0856	* IC,QUAD 2-INPUT NAND GATE,TTL	* 07263	* SN7400J
*	1820-0857	* IC,DUAL 4-INPUT NAND GATE,TTL	* 07263	* SN7420J
*	1820-0858	* IC,DUAL J-K M/S FLIP-FLOP,TTL	* 07263	* SN7476J
*	1820-0859	* IC,QUAD D FLIP-FLOP,TTL	* 07263	* SN7474J
*	1820-0860	* IC,MONOSTABLE MULTIVIBRATOR,DTL	* 07263	* MC8516
*	1820-0861	* IC,QUAD 2-INPUT NAND GATE,DTL	* 07263	* MC846L
*	1820-0862	* IC,CLOCKED FLIP-FLOP,DTL	* 07263	* MC844L
*	1820-0863	* IC,QUAD 2-INPUT NAND BUFFER,OPEN COLLECTOR,DTL	* 07263	* U6A9158S9X
*	1820-0864	* IC,QUAD 2-INPUT NAND GATE,W/OPEN COLLECTOR,TTL	* 07263	* SN7403J
*	1820-0865	* IC,DUAL 4-INPUT EXP. NAND BUFFER,OPEN COLL,DTL	* 07263	* MC844L

INTEGRATED CIRCUITS (CONT)

*	1820-0866	* IC.QUAD 2-INPUT NAND GATE,DTL	* 07263	* MC849J
*	1820-0867	* IC.HS DUAL 4-INPUT NAND BUFFER,TTL	* 07263	* SN74H40J
*	1820-0868	* IC.DUAL 5-INPUT NAND GATE,DTL	* 07263	* MC1801L
*	1820-0869	* IC.HEX INVERTER,OPEN COLLECTOR,DTL	* 07263	* MC835L
*	1820-0870	* IC.QUAD 2-INPUT AND GATE,TTL	* 07263	* SN7408J
*	1820-0871	* IC.10MA OPTION	* 28480	* 1820-0871
*	1820-0875	* IC.MONOSTABLE MULTIVIBRATOR,RE-SET/TRIG,TTL	* 07263	* U6A960059X
*	1820-0876	* IC.LP QUAD 4-BIT BISTABLE LATCH,TTL	* 01295	* SN74L75N
*	1820-0877	* IC.DECADE COUNTER,TTL	* 01295	* SN8490N
*	1820-0878	* IC.2-INPUT POS NAND GATE,TTL	* 01295	* SN8400N
*	1820-0879	* IC.DUAL J-K MASTER-SLAVE FLIP-FLOP,TTL	* 01295	* SN84L73N
*	1820-0880	* IC.MONOSTABLE MULTIVIBRATOR,TTL	* 01295	* SN84121N
*	1820-0881	* IC.4-BIT BISTABLE LATCH,TTL	* 01295	* SN8475N
*	1820-0882	* IC.4-LINE TO 10-LINE DECODER,TTL	* 01295	* SN8442N
*	1820-0883	* IC.HEX INVERTER,TTL	* 01295	* SN84L04N
*	1820-0884	* IC.DUAL 4-INPUT POS NAND GATE,TTL	* 01295	* SN84L20N
*	1820-0885	* IC.QUADRUPLE 2-INPUT POS NAND GATE,TTL	* 01295	* SN84L00N
*	1820-0886	* IC.J-K MASTER-SLAVE FLIP-FLOP,TTL	* 01295	* SN84L72N
*	1820-0887	* IC.TRIPLE 3-INPUT POS NAND GATE,TTL	* 01295	* SN84L10N
*	1820-0888	* IC.QUADRUPLE 2-INPUT POS NOR GATE,TTL	* 01295	* SN8402N
*	1820-0889	* IC.HEX INVERTER,TTL	* 01295	* SN8404N
*	1820-0890	* IC.DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP,TTL	* 01295	* SN84L74N
*	1820-0891	* IC.4-BIT ODD/EVEN PARITY GEN/CHECKERS,TTL	* 01295	* SN84L85
*	1820-0894	* IC.HEX INVERTER,TTL	* 07263	* SN7404J
*	1820-0895	* IC.HEX SET-RESET LATCH,TTL	* 01295	* SN74118N
*	1820-0896	* IC.QUAD NAND SCHMITT-TRIGGER,TTL	* 01295	* SN74132N
*	1820-0897	* IC.QUAD 2-INPUT AND GATE,ECL	* 04713	* MC1047P
*	1820-0898	* IC.VARIABLE MODULO COUNTER,TTL	* 07263	* U7A930559X
*	1820-0899	* IC.DECADE COUNTER W/ASYNCHRO CLEAR,TTL	* 01295	* SN74160N
*	1820-0900	* IC.TRIPLE 3-INPUT NOR GATE,TTL	* 18324	* SP370A
*	1820-0902	* IC.DUAL PERIPHERAL 2-INPUT AND DRIVER,TTL	* 01295	* SN75450AN
*	1820-0903	* IC.LP 4-BIT SER/IN PAR/OUT SHIFT REGISTER,TTL	* 01295	* SN74L164N
*	1820-0904	* IC.LP 5-BIT COMPARATOR,TTL	* 07263	* U7H93L2459X

INTEGRATED CIRCUITS (CONT)

*	1820-0906	* IC,DUAL 4-INPUT MULT. W/COM SELECT(TRI-STATE),TTL	* 27014	* DM8214N
*	1820-0907	* IC,TRIPLE 3-INPUT NAND GATE,OPEN COLLECTOR,TTL	* 01295	* SN7412N
*	1820-0908	* IC,DUAL D FLIP-FLOP W/BUFFERED OUTPUTS,TTL	* 04713	* MC7479P
*	1820-0909	* IC,SYNCHRONOUS DECADE RATE MULTIPLIER,TTL	* 01295	* SN74167N
*	1820-0910	* IC,4-BIT BINARY FULL ADDER,TTL	* 01295	* SN74LS83N
*	1820-0911	* IC,DECADE UP/DN COUNTER,SYNCHRO,(LOW PWR),TTL	* 01295	* SN74L192N
*	1820-0912	* IC,4-BIT BINARY UP/DN COUNTER,(LOW PWR),TTL	* 01295	* SN74L193N
*	1820-0913	* IC,LP MONOASTABLE MULTIVIBRATOR,RETRIG W/CLEAR,TTL	* 01295	* SN74L122N
*	1820-0914	* IC,BCD/SEVEN SEGMENT DECODER,TTL	* 07263	* U6B9307S9X
*	1820-0916	* IC,QUAD 2-INPUT NOR GATE,ECL	* 04713	* MC1062P
*	1820-0917	* IC,TRIPLE LINE RECEIVER,ECL	* 04713	* MC1065P
*	1820-0919	* IC,A/D COMPARATOR,ECL	* 04713	* MC1650L
*	1820-0920	* IC,QUAD LINE RECEIVER,ECL	* 04713	* MC1692L
*	1820-0921	* IC,4-BIT MAGNITUDE COMPARATOR,TTL	* 01295	* SN7485N
*	1820-0923	* IC,QUAD 2-INPUT NOR GATE,TTL	* 18324	* N8885A
*	1820-0924	* IC,TRIPLE SER ADDER W/INVERTCOM CLK,CMOS	* 02735	* CD4038AE
*	1820-0925	* IC,TRIPLE SER ADDER W/INVERTCOM CLK,CMOS	* 02735	* CD4032AE
*	1820-0926	* IC,4-BIT FULL ADDER,CMOS	* 02735	* CD4008AE
*	1820-0927	* IC,BCD/DECIMAL DECODER,CMOS	* 02735	* CD4028AE
*	1820-0928	* IC,QUAD TRUE/COMPLEMENT BUFFER,CMOS	* 02735	* CD4041AE
*	1820-0929	* IC,DIVIDE-BY-A COUNTER W/DECODED OUTPUTS,CMOS	* 02735	* CD4022AE
*	1820-0930	* IC,DECADE COUNTER W/7 SEGMENT DECODER,CMOS	* 02735	* CD4026AE
*	1820-0931	* IC,BINARY/DECADE UP/DN COUNTER,PRESETTABLE,CMOS	* 02735	* CD4029AE
*	1820-0932	* IC,DECADE COUNTER W/7 SEGMENT DECODER,CMOS	* 02735	* CD4033AE
*	1820-0933	* IC,DECADE COUNTER W/DECODED OUTPUTS,CMOS	* 02735	* CD4017AE
*	1820-0934	* IC,VARIABLE MODULO COUNTER,CMOS	* 02735	* CD4018AE
*	1820-0935	* IC,14-BIT BINARY COUNTER,CMOS	* 02735	* CD4020AE
*	1820-0936	* IC,7-BIT BINARY COUNTER W/RESET,CMOS	* 02735	* CD4024AE
*	1820-0937	* IC,12-BIT BINARY RIPPLE-CARRY COUNTER,CMOS	* 02735	* CD4040AE
*	1820-0938	* IC,DUAL J-K FLIP-FLOP W/SET,CMOS	* 02735	* CD4027AE
*	1820-0939	* IC,DUAL D FLIP-FLOP W/SET/RESET,CMOS	* 02735	* CD4013AE

INTEGRATED CIRCUITS (CONT)

1820-0940	IC,QUAD (TRI-STATE) NAND R-S LATCH,CMOS	02735	CD4044AE
1820-0941	IC,QUAD (TRI-STATE) NOR R-S LATCH,CMOS	02735	CD4043AE
1820-0942	IC,DUAL 3-INPUT NOR GATE,PLUS INVERTER,CMOS	02735	CD4000AE
1820-0943	IC,TRIPLE 3-INPUT NAND GATE,CMOS	02735	CD4023AE
1820-0944	IC,TRIPLE 3-INPUT NOR GATE,CMOS	02735	CD4025AE
1820-0944	IC,TRIPLE 3-INPUT NOR GATE,CMOS	02735	CD4025AE
1820-0945	IC,TRIPLE AND/OR GATE PAIR,CMOS	02735	CD4037AE
1820-0946	IC,QUAD 2-INPUT NOR GATE,CMOS	02735	CD4001AE
1820-0947	IC,QUAD EXCLUSIVE-OR GATE,CMOS	02735	CD4030AE
1820-0948	IC,DUAL 4-INPUT NOR GATE,CMOS	02735	CD4002AE
1820-0949	IC,QUAD 2-INPUT NAND GATE,CMOS	02735	CD4011AE
1820-0950	IC,DUAL 4-INPUT NAND GATE,CMOS	02735	CD4012AE
1820-0951	IC,QUAD 2-INPUT MULTIPLEXER,CMOS	02735	CD4019AE
1820-0952	IC,DUAL 2-INPUT NOR GATE,CTL	07263	U6A995279X
1820-0953	IC,TRIPLE 2-2-3-INPUT AND GATE,CTL	07263	U6A995379X
1820-0954	IC,DUAL 4-INPUT AND GATE,CTL	07263	U6A995479X
1820-0955	IC,8-INPUT 2-OUTPUT AND GATE,CTL	07263	U6A995579X
1820-0956	IC,DUAL 2-INPUT AND BUFFER,CTL	07263	U6A995679X
1820-0957	IC,DUAL RANK R-S FLIP-FLOP,CTL	07263	U6A995779X
1820-0958	IC,QUAD CLOCKED D LATCH,CMOS	02735	CD4042AE
1820-0959	IC,32-BIT (4X8)RAM W/BINARY ADD,CMOS	02735	CD4036AE
1820-0960	IC,32-BIT (4X8)RAM W/DIRECT ADD,CMOS	02735	CD4039AE
1820-0961	IC,8-BIT STATIC SER-IN PAR-OUT SHIFT REG,CMOS	02735	CD4021AE
1820-0962	IC,18-BIT STATIC SHIFT REG. W/COM CLOCK,CMOS	02735	CD4006AE
1820-0963	IC,64-BIT STATIC SHIFT REG. W/MODE CONTROL,CMOS	02735	CD4031AE
1820-0964	IC,TRIPLE 3-3-1-INPUT AND GATE,CTL	07263	U6A996479X
1820-0965	IC,QUAD 1-INPUT AND GATE,CTL	07263	U6A996579X
1820-0966	IC,2-INPUT AND: PLUS 2-WD 2-INPUT AND-OR GATE,CTL	07263	U6A996679X
1820-0967	IC,DUAL RANK J-K FLIP-FLOP,CTL	07263	U6A996779X
1820-0968	IC,HS DUAL GATED LATCH,CTL	07263	U6A996879X
1820-0969	IC,4-BIT SHIFT REGISTER PARIN/OUT,CMOS	02735	CD4035AE
1820-0970	IC,8-BIT STATIC SHIFT RFG. PAR/SER TO SERIAL,CMOS	02735	CD4014AE
1820-0971	IC,DUAL 2-WIDE 2-INPUT AND-OR GATE,CTL	07263	U6A997179X

INTEGRATED CIRCUITS (CONT)

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*  1820-0972  *  IC,RELAXED VERSION OF 1820-0952,CTL          *  07263  *  U6A995279X  *
*  1820-0973  *  IC,RELAXED VERSION OF 1820-0953,CTL          *  07263  *  U6A995379X  *
*  1820-0974  *  IC,RELAXED VERSION OF 1820-0956,CTL          *  07263  *  U6A995679X  *
*  1820-0975  *  IC,RELAXED VERSION OF 1820-0967,CTL          *  07263  *  U6A996779X  *
*  1820-0976  *  IC,DUAL 4-BIT STATIC SHIFT REG, SER TO PAR,CMOS  *  02735  *  CD4015AE  *
*  1820-0977  *  IC,4-BIT PAR/SER IN/OUT BUS REGISTER,CMOS     *  02735  *  CD4034AE  *
*  1820-0978  *  IC,DUAL COMPLEMENTARY PAIR,PLUS INVERTER,CMOS  *  02735  *  CD4007AE  *
*  1820-0979  *  IC,HEX BUFFER/TRANSLATOR,INVERTING,CMOS       *  02735  *  CD4009AE  *
*  1820-0980  *  IC,HEX BUFFER/TRANSLATOR,CMOS                 *  02735  *  CD4010AE  *
*  1820-0981  *  IC,QUAD BILATERAL SWITCH,CMOS                 *  02735  *  CD4016AE  *
*  1820-0982  *  IC,DIFFERENTIAL AMPL/LIMITER                  *  28480  *  1820-0982  *
*  1820-0984  *  IC,4-BIT SHIFT REG, SER/PAR IN/OUT,TTL        *  04713  *  MC7270P  *
*  1820-0985  *  IC,DUAL 5-INPUT NAND GATE,DTL                 *  04713  *  MC1800P  *
*  1820-0986  *  IC,LP DECADE COUNTER,TTL                      *  27014  *  DM86L75N  *
*  1820-0987  *  IC,LP 8-INPUT PRIORITY ENCODER,TTL            *  07263  *  U9B93L1859X  *
*  1820-0988  *  IC,256-BIT (256X1)RAM,OPEN COLLECTOR,TTL      *  07263  *  A7B93410S9X  *
*  1820-0989  *  IC,4-BIT SHIFT REG, W/DIRECT RESET,TTL        *  18324  *  N8271A  *
*  1820-0990  *  IC,QUAD NAND LINE RECIEVER,DTL                *  04713  *  MC1489AL  *
*  1820-0992  *  IC,DECADE COUNTER,TTL                         *  01295  *  SN5490N  *
*  1820-0995  *  IC,9CD/7-SEGMENT DECODER/DRIVER,TTL           *  01295  *  SN7447AN  *
*  1820-0996  *  IC,3-INPUT MULTIPLEXER,ECL                    *  28480  *  1820-0996  *
*  1820-0998  *  IC,SHS 4-INPUT MUXR W/COM SELECT,TTL          *  01295  *  SN74S153N  *
*  1820-0999  *  IC,SHS ARITH LOGIC UNIT/FUNCTION GEN,,TTL     *  01295  *  SN74S181N  *
*  1820-1001  *  IC,DUAL THRESHOLD DETECTOR W/STRETCHER        *  28480  *  1820-1001  *
*  1820-1007  *  IC,DUAL LINE DRIVER,TTL                       *  18324  *  N8T23A  *
*  1820-1027  *  IC,4-BIT SHFT REG PAR IN/OUT J-K SER-IN,TTL   *  01295  *  SN74195N  *
*  1820-1033  *  IC,QUAD D FLIP-FLOP,TRI STATE OUTPUT,TTL      *  18324  *  N8T110A  *
*  1820-1053  *  IC,HEX SCHMITT TRIGGER                        *  01295  *  SN7414N  *
*  1820-1066  *  IC,TRIPLE 3-INPUT AND GATE,TTL                *  07263  *  U9A741159X  *
*  1820-1100  *  IC,QUAD 2-INPUT MULTIPLEXER                   *  01295  *  SN74298N  *
*  1820-1107  *  IC,8-BIT SHFT REG PAR/SER IN SER OUT          *  01295  *  SN74166N  *
*  1820-1116  *  IC,DUAL J-K FLIP-FLOP POS EDGE TRIGGERED      *  01295  *  SN74109N  *
*  1820-1131  *  IC,6-BIT COMPARATOR W/STROBE,TTL              *  27014  *  DM8160N  *
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CONTENTS PAGE

Table 1-1. Specifications

PROCESSOR	
CONTROL STORE	
Type:	Bipolar LSI ROM semiconductor. Up to sixteen 256-word modules.
CONTROL PROCESSOR	
Address Space:	4,096 words.
Word Size:	24 bits.
Word Formats:	Four.
Word Fields:	Five.
ROM Cycle:	325 nanoseconds.
REGISTERS	
Accumulators:	Two (A and B), 16 bits each. Implicitly addressable; also explicitly addressable as memory.
Index:	Two (X and Y), 16 bits each.
Memory Control:	Two (T and P), 16 bits each; one (M) 15 bits.
Supplementary:	Two (overflow and extend), one bit each.
Manual Data:	One (display), 16 bits.
Scratch Pads:	Twelve, 16 bits each; accessible to microprogrammer.
MEMORY PARITY CHECK	
HP 2105A Processor:	Monitors all words read from memory. Switch selectable to either halt or ignore parity when detected. A parity indication is displayed on operator panel.
HP 2108A Processor:	Same as for HP 2105A. With memory protect option, interrupt on parity error occurs.
POWER FAIL INTERRUPT	
Priority:	Highest priority interrupt.
Power Failure:	Detects power failure and generates an interrupt to trap cell for user-written power-failure routine, terminates activities, and halts processor. A minimum of 500 μS is available for the routine. Automatic restart is provided as a memory system option.

Table 1-1. Specifications (Continued)

PROCESSOR (Continued)

PROTECTION

Loaders: All loaders reside in special ROM's separate from control ROM and are loaded into last 64 words of main memory by activating operator panel switches. Paper tape loader is standard; three additional switch-selectable loader spaces are provided to accommodate other modes of operation as a user option. User-generated loaders may be written in Assembly Language.

Volatility: Mains ac standby mode and sustaining power for line loss of 2.5 Hz before entering power fail routine. Power fail recovery is a memory system option.

INPUT/OUTPUT

Priority Interrupt: Multilevel vectored priority interrupt determined by interface channel assignment.

I/O Channels: HP 2105A: four internal I/O channels; expandable to 36 channels with two I/O extenders.
HP 2108A: nine internal I/O channels; expandable to 41 channels with two I/O extenders.

Current Available to I/O

SUPPLY	HP 2105A	HP 2108A
+5V	6.0A	13.0A
-2V	2.0A	4.0A
+12V	1.0A	1.5A
-12V	1.0A	1.5A

Note: Current availability to I/O assumes 32K memory, dual-channel port controller, and maximum available control store installed in mainframe.

Table 1-1. Specifications (Continued--

PROCESSOR (Continued)	
PHYSICAL CHARACTERISTICS	
Width:	16-3/4 inches (42.55 cm) behind rack mount; 19 inches (48.26 cm) operator panel width on sides.
Depth:	23-1/2 inches (59.69 cm); 23 inches (58.42 cm) behind operator panel.
Height:	HP 2105A: 5-1/4 inches (13.31 cm) in rack mount. HP 2108A: 8-3/4 inches (22.23 cm) in rack mount.
Weight:	HP 2105A: 39 pounds (17.69 kg). HP 2108A: 45 pounds (20.41 kg).
ELECTRICAL CHARACTERISTICS	
Input Line Voltage:	110V or 220V ac (±20%), single phase.
Line Frequence:	47 to 66 Hz.
Power:	HP 2105A: 400W maximum. HP 2108A: 525W maximum.
Line Overvoltage Protect:	Input crowbar in series with line fuse.
Output Protect:	All voltages protected against overvoltage and overcurrent.
Output Voltage Regulation:	±5%
Thermal Sensing:	Monitors internal temperature and automatically shuts down if temperature exceeds specified level.
ENVIRONMENTAL LIMITATIONS	
Ambient Temperature:	Operating: 32° to 131°F (0° to 55°C). Nonoperating: -40° to 167°F (-40° to 75°C).
Altitude:	Operating: 15,000 feet (4,573 meters). Nonoperating: 25,000 feet (7,622 meters).
Relative Humidity:	50 to 95% at 77° to 104°F (25° to 40°C).
Shock:	Tested for 30g shock for 11 milliseconds over a 1/2 sine wave shape.
Vibration:	Can withstand vibration of 1g at 44 cycles per second.
VENTILATION	
Air Flow:	Intake on left-hand side; exhaust on right-hand side.
Heat Dissipation:	HP 2105A: 1365 BTU's (344 kilocalories)/hour, max. HP 2108A: 1795 BTU's (452 kilocalories)/hour, max.

Table 1-1. Specifications (Continued)

MEMORY SYSTEMS	
HP 2101A MEMORY	
Density:	High density; 16K words per module.
Configuration:	Available in 8K or 16K configuration; only one 8K module allowed per system.
HP 2102A MEMORY	
Density:	Medium density; 8K words per module.
Configuration:	Available in 4K or 8K configuration; only one 4K module allowed per system.
MEMORY ORGANIZATION	
Type:	4K chip N-channel MOS/RAM semiconductor.
Word Size:	16 bits plus parity bit.
Configuration:	Controller and multiple plug-in memory modules.
Page Size:	1,024 words.
Direct Addressing:	2 pages.
Indirect Addressing:	32K.
System Cycle Time:	650 nanoseconds.
Volatility Protection	Mains ac standby mode and sustaining power for line loss of 10 Hz is standard. Power fail recovery system is optional.
MEMORY PROTECT (HP 2108A only)	
Installation:	Plugs into slot 111 of memory PCA cage.
Priority:	Second highest priority interrupt (shared with memory aprity).
Operation:	Initiated under programmed control; protects any amount of memory, I/O, or privileged instruction when implemented in the HP 2108A Processor.
Fence Register:	Set under program control; memory below fence is protected.
Interrupt:	Interrupts to trap cell for subroutine when user program (1) attempts to alter a protected location. (2) attempts to jump into the protected area, (3) or attempts to execute an I/O instruction except those with Select Code 01.
Violation Register:	Contains memory address of violating instruction.

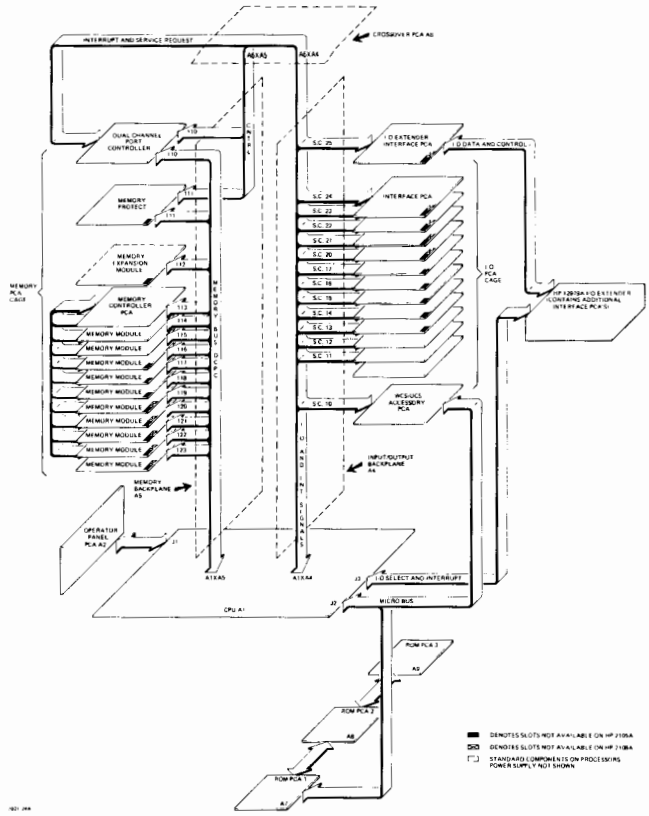
Table 1-1. Specifications (Continued)

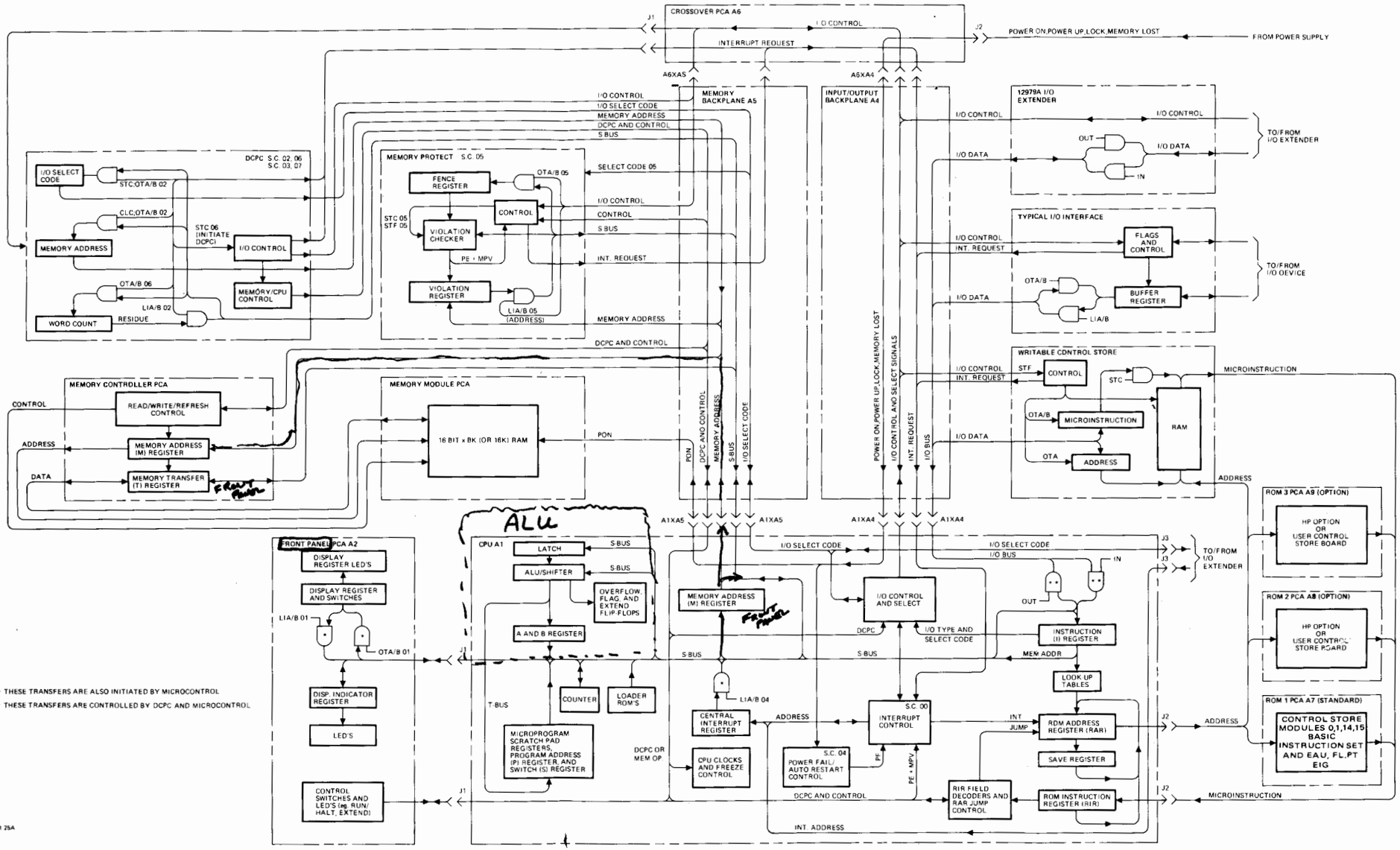
MEMORY SYSTEMS (Continued)	
MEMORY PROTECT (HP 2108A only continued)	
Parity Error Interrupt:	Provides interrupt signal when parity error is detected; saves address of error in violation register.
Infinite Indirect Protect:	Interrupts are enabled after three levels of indirect addressing.
DUAL-CHANNEL PORT CONTROLLER	
Installation:	Plugs into slot 110 of memory PCA cage.
Number of Channels:	Two.
Number of Memory Ports:	One.
Registers/Channel:	Two (word count and address).
Word Size:	16 bits.
Maximum Block Size:	32,768 words.
I/O Assignable:	Assignable to any two I/O channels; all logic necessary to facilitate bidirectional direct memory to and from I/O is contained on this controller.
Transfer Rate:	616,666 words per second maximum.
Priority:	Highest: DCPC Channel 1. Middle: DCPC Channel 2. Lowest: Processor.
POWER FAIL RECOVERY SYSTEM	
Power Restart:	Detects resumption of power and generates an interrupt to trap cell for user-written restart program which has been protected in memory by the sustaining battery.
Power Control and Charge Unit:	Monitors battery charge status and provides trickle charge.
Sustaining Battery:	Type: 12V nickel cadmium. Charging rate: 350 milliamperes Capacity: 4 ampere-hours; will sustain 32K main memory for 2 hours.

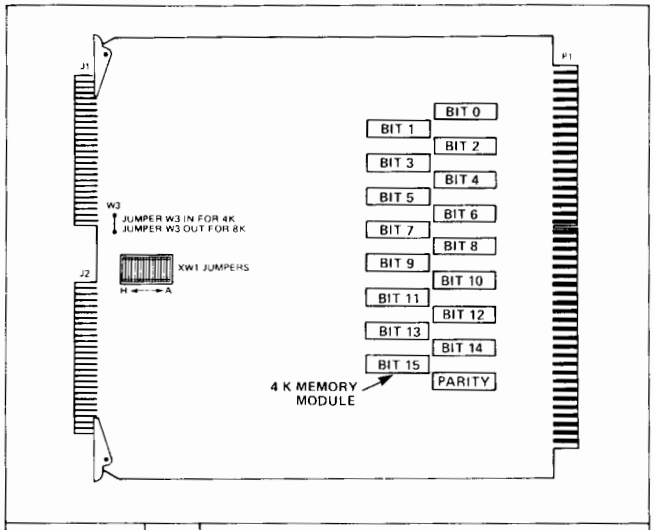
Table 1-2. Options and Accessories

DESCRIPTION	OPTION NO.	ACCESSORY NO.
2105A OR 2108A PROCESSOR		
Scientific Instruction Set	-003	12977A
Writeable Control Store	-005	12978A
Disc Loader Rom	-014	12992A
230V, 50-Hz Operation	-015	--
User Control Store Board	--	12945A
Programmable ROM Writer	--	12909B
2101A MOS MEMORY SYSTEM		
Dual-Channel Port Controller	-001	12897A
Memory Protect*	-003	12892A
8K Memory Module	-008	12999A
16K Memory Module	-016	12997A
Memory System Cable	--	12993A
Power Fail Recovery System	--	12944A
2102A MOS MEMORY SYSTEM		
Dual-Channel Port Controller	-001	12897A
Memory Protect*	-003	12892A
4K Memory Module	-004	12994A
8K Memory Module	-008	12998A
Memory System Cable	--	12993A
Power Fail Recovery System	--	12944A
12979A I/O EXTENDER		
Dual-Channel Port Controller	-001	12898A
2nd I/O Extender	-010	--
230V, 50-Hz Operation	-015	--

*For HP 2108A Processor only.


INTERRUPT AND SERVICE REQUEST
A5XA5
A5XA4
CROSSOVER PCA A5
DUAL CHANNEL PORT CONTROLLER
MEMORY PROTECT
MEMORY EXPANSION MODULE
MEMORY CONTROLLER PCA
MEMORY MODULE
MEMORY BACKPLANE A5
OPERATOR PANEL PCA A2
I/O EXTENDER INTERFACE PCA
I/O DATA AND CONTROL
INTERFACE PCA
I/O PCA CAGE
MEMORY PCA CAGE
MEMORY BUS
I/O BUS
INPUT/OUTPUT BACKPLANE A4
MCS/UCL ACCESSORY PCA
I/O SELECT AND INTERRUPT
MICRO BUS
CPU A1
ROM PCA 3
ROM PCA 2
ROM PCA 1
DENOTES SLOTS NOT AVAILABLE ON HP 2105A
DENOTES SLOTS NOT AVAILABLE ON HP 2108A
STANDARD COMPONENTS ON PROCESSORS POWER SUPPLY NOT SHOWN


CROSSOVER PCA A6
I/O CONTROL
INTERRUPT REQUEST
POWER ON,POWER UP,LOCK,MEMORY LOST
FROM POWER SUPPLY
A6XA5
A6XA4
MEMORY BACKPLANE A5
INPUT/OUTPUT BACKPLANE A4
I/O CONTROL
I/O SELECT CODE
MEMORY ADDRESS
DCPC AND CONTROL
S BUS
DCPC S.C. 02, 06
S.C. 03, 07
I/O SELECT CODE
STC;OTA/B 02
CLC;OTA/B 02
STC 06 (INITIATE DCPC)
MEMORY ADDRESS
I/O CONTROL
MEMORY/CPU CONTROL
OTA/B 06
LIA/B 02
WORD COUNT
RESIDUE
MEMORY PROTECT S.C. 05
FENCE REGISTER
OTA/B 05
CONTROL
STC 05
STF 05
VIOLATION CHECKER
PE + MPV
VIOLATION REGISTER
LIA/B 05 (ADDRESS)
SELECT CODE 05
I/O CONTROL
CONTROL
S BUS
INT. REQUEST
MEMORY ADDRESS
DCPC AND CONTROL
12979A I/O EXTENDER
I/O CONTROL
I/O DATA
OUT
IN
TO/FROM I/O EXTENDER
TYPICAL I/O INTERFACE
FLAGS AND CONTROL
OTA/B
BUFFER REGISTER
LIA/B
INT. REQUEST
TO/FROM I/O DEVICE
WRITABLE CONTROL STORE
STF
CONTROL
STC
OTA/B
MICROINSTRUCTION
OTA
ADDRESS
RAM
MICROINSTRUCTION
ADDRESS
MEMORY CONTROLLER PCA
CONTROL
ADDRESS
DATA
READ/WRITE/REFRESH CONTROL
MEMORY ADDRESS (M) REGISTER
MEMORY TRANSFER (T) REGISTER
MEMORY MODULE PCA
16 BIT x 8K (OR 16K) RAM
PON
DCPC AND CONTROL
MEMORY ADDRESS
S BUS
I/O SELECT CODE
POWER ON,POWER UP,LOCK,MEMORY LOST
I/O CONTROL AND SELECT SIGNALS
INT. REQUEST
I/O BUS
A1XA5
A1XA4
ALU
FRONT PANEL PCA A2
DISPLAY REGISTER LED'S
DISPLAY REGISTER AND SWITCHES
LIA/B 01
OTA/B 01
DISP. INDICATOR REGISTER
LED'S
CONTROL SWITCHES AND LED'S (eg. RUN/ HALT, EXTEND)
CPU A1
LATCH
ALU/SHIFTER
OVERFLOW, FLAG, AND EXTEND FLIP-FLOPS
A AND B REGISTER
T-BUS
COUNTER
LOADER ROM'S
MICROPROGRAM SCRATCH PAD REGISTERS, PROGRAM ADDRESS (P) REGISTER AND SWITCH (S) REGISTER
DCPC OR MEM OP
CPU CLOCKS AND FREEZE CONTROL
MEMORY ADDRESS (M) REGISTER
CENTRAL INTERRUPT REGISTER
LIA/B 04
I/O CONTROL AND SELECT
DCPC
I/O TYPE AND SELECT CODE
S.C. 00
INTERRUPT CONTROL
S.C. 04
POWER FAIL/ AUTO RESTART CONTROL
PF
PE + MPV
INSTRUCTION (I) REGISTER
MEM ADDR
LOOK UP TABLES
ROM ADDRESS REGISTER (RAR)
SAVE REGISTER
RIR FIELD DECODERS AND RAR JUMP CONTROL
ROM INSTRUCTION REGISTER (RIR)
INT. JUMP
ADDRESS
DCPC AND CONTROL
INT. ADDRESS
MICROINSTRUCTION
TO/FROM I/O EXTENDER
ROM 3 PCA A8 (OPTION)
HP OPTION OR USER CONTROL STORE BOARD
ROM 2 PCA A8 (OPTION)
HP OPTION OR USER CONTROL STORE BOARD
ROM 1 PCA A7 (STANDARD)
CONTROL STORE MODULES 0,1,14,15 BASIC INSTRUCTION SET AND EAU, FL.PT EIG
FRONT PANEL PROBLEMS
* THESE TRANSFERS ARE ALSO INITIATED BY MICROCONTROL
** THESE TRANSFERS ARE CONTROLLED BY DCPC AND MICROCONTROL
7021 25A

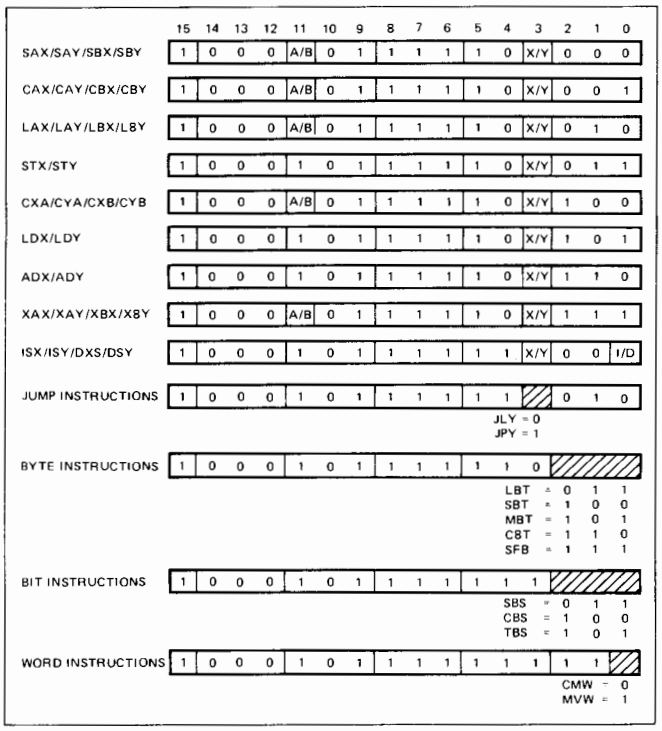


MEMORY MODULE		W3	XW1 JUMPERS							
			A	B	C	D	E	F	G	H
0	0-4K	IN	IN	IN	IN	IN	IN	IN	IN	IN
0	0-8K	OUT	X	IN	IN	IN	IN	IN	IN	IN
1	8-12K	IN	IN	OUT	IN	IN	IN	IN	IN	IN
1	8-16K	OUT	X	OUT	IN	IN	IN	IN	IN	IN
2	16-24K	OUT	X	IN	OUT	IN	IN	IN	IN	IN
3	24-32K	OUT	X	OUT	OUT	IN	IN	IN	IN	IN
4	32-40K	OUT	X	IN	IN	OUT	IN	IN	IN	IN
5	40-48K	OUT	X	OUT	IN	OUT	IN	IN	IN	IN
6	48-56K	OUT	X	IN	OUT	OUT	IN	IN	IN	IN
7	56-64K	OUT	X	OUT	OUT	OUT	IN	IN	IN	IN

Note: Half-loaded memory module (i.e., 4K) must always be highest module number

REGISTER DESIRED	POINTER (15 14 ... 3 0)
X	10 0000
Y	10 0001
COUNTER	10 0010
S3	10 0011
S4	10 0100
S5	10 0101
S6	10 0110
S7	10 0111
S8	10 1000
S9	10 1001
S10	10 1010
S11	10 1011
S12	10 1100
CIR	10 1101
OVERFLOW	10 1110
EXTEND	10 1111

EXTENDED INSTRUCTION GROUP CODES IN BINARY



INSTRUCTION CODES IN OCTAL

Ext. Inst. Group

ADX	105746
ADY	105756
CAX	101741
CAY	101751
CBS	105774
CBT	105766
CBX	105741
CBY	105751
CMW	105776
CXA	101744
CXB	105744
CYA	101754
CYB	105754
DSX	105761
DSY	105771
ISX	105760
ISY	105770
JLY	105762
JPY	105772
LAX	101742
LAY	101752
LBT	105763
LBX	105742
LBY	105752
LDX	105745
LDY	105755
MBT	105765
MVW	105777
SAX	101740
SAY	101750
SBS	105773
SBT	105764
SBX	105740
SBY	105750
SFB	105767
STX	105743
STY	105753
TBS	105775
XAX	101747
XAY	101757
XBX	105747
XBY	105757

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

PAPER TAPE LOADER

```
X7700  107700  START   CLC  O,C        TURN OFF THE INTERRUPT
                                          SYSTEM
X7701  002401          CLA, RSS
X7702  063756  CONT    LDA  M.11       FEED FRAME COUNTER
X7703  006700          CLB, CCE        SET E TO READ BYTE
X7704  017742          JSB  READ       GET # OF CHAR
X7705  007306          CMB,CCE,INB,SZB 2'S COMP)
X7706  027713          JMP  *+5        NON ZERO BYTE
X7707  002006          INA, SZA        FEED FRAME COUNTER
X7710  027703          JMP  *-5
X7711  102077          HLT  77B        END OF TAPE
X7712  027700          JMP  START
X7713  077754          STB  WD.CT      WORDS IN RECORD
X7714  017742          JSB  READ       GET FEED FRAME
X7715  017742          JSB  READ       GET ADDRESS
X7716  074000          STB  0          INITIATE CHECKSUM
X7717  077755          STB  ADDR
X7720  067755  CHECK   LDB  ADDR
X7721  047777          ADB  MAXAD      CHECK ADDR BELOW
                                          LOADER
X7722  002040          SEZ             E  OK
X7723  027740          JMP  HLT55      ADDR>=LOADER
X7724  017742          JSB  READ       GET NEXT WORD
X7725  040001          ADA  1          CONTINUE CHECKSUM
X7726  177755          STB  ADDR, I
X7727  037755          ISZ  ADDR
X7730  000040          CLE
X7731  037754          ISZ  WD.CT
X7732  027720          JMP  CHECK
X7733  017742          JSB  READ
X7734  054000          CPB  0
X7735  027702          JMP  CONT
X7736  102011          HLT  11B        CHECKSUM ERROR
X7737  027700          JMP  START
X7740  102055  HLT55   HLT  55B        ADDRESS>=LOADER
X7741  027700          JMP  START
X7742  000000  READ    NOP             E  READ WORD =1 BYTE
X7743  006600          CLB, CME        E REG BYTE POINTER
X7744  1037KK          STC  RDR,C      START THE READER
X7745  1023KK          SFS  RDR           CHECK THESE IF $$
X7746  027745          JMP  *-1           LOADER BOMBED $1
X7747  1064KK          MIB  RDR        GOT BYTE
X7750  002041          SEZ, RSS
X7751  127742          JMP  READ,I
X7752  005767          BLF, CLE,BLF
X7753  027744          JMP  *-7
X7754  000000  WD.CT    NOP
X7755  000000  ADDR     NOP
X7756  177765  M.11     DEC-11          FEED FRAME CONST.
X7777          MAXAD   EQU  X7777B     LOADER ADDRESS
00010          RDR     EQU  KKB        READER SELECT CODE
                       END
```

X = 1 for 8K
2 for 12K
3 for 16K
4 for 20K
5 for 24K
6 for 28K
7 for 32K

KK = Paper Tape Reader

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

DISC LOADER (DOS III, 2000F)

X7700	002400	BOOT1	CLA		ISSUE SEEK TO DRIVE 0, HEAD 0
X7701	1026DD		OTA	DC	
X7702	1037DD		STC	DC,C	
X7703	067760		LDB	SEEK	
X7704	1066CC		OTB	CC	
X7705	1037CC		STC	CC,C	
X7706	1023DD		SFS	DC	
X7707	027706		JMP	*-1	
X7710	006400		CLB		SET FOR HEAD 0, SECTOR 0
X7711	1066DD		OTB	DC	
X7712	1037CC		STC	DC,C	
X7713	1023CC		SFS	CC	
X7714	027713		JMP	*-1	
X7715	1025CC		LIA	CC	IF NO ATTENTION BITS, THEN 2883
X7716	006400		CLB		
X7717	002003		SZA,	RSS	
X7720	067763		LDB	S2883	
X7721	077764		STB	STAT	SET STATUS COMMAND
X7722	067761		LDB	R7900	"B" = READ COMMAND
X7723	002003		SZA,	RSS	
X7724	067762		LDB	R2883	
X7725	063776		LDA	DMACW	READ TRACK 0, SECTOR 0
X7726	102606		OTA	6	
X7727	063765		LDA	ADDR1	INTO MEMORY LOCATION 2011
X7730	102602		OTA	2	
X7731	063757		LDA	N128	READ ONE SECTOR
X7732	102702		STC	2	
X7733	102602		OTA	2	
X7734	1066CC		OTB	CC	"B" HAS READ COMMAND
X7735	1037DD		STC	DC,C	
X7736	103706		STC	6,C	
X7737	1037CC		STC	CC,C	
X7740	1023CC		SFS	CC	
X7741	027740		JMP	*-1	
X7742	102106		STF	6	
X7743	1037DD		STC	DC,C	
X7744	063764		LDA	STAT	
X7745	1067CC		CLC	CC	
X7746	1026CC		OTA	CC	
X7747	1037CC		STC	CC,C	
X7750	1023DD		SFS	DC	
X7751	027750		JMP	*-1	
X7752	1025DD		LIA	DC	GET STATUS
X7753	001200		RAL		
X7754	002020		SSA		
X7755	027700		JMP	BOOT1	FIRST SEEK - READ AGAIN
X7756	027772		JMP	GO	TRANSFER TO PRE-BOOT PROCESSOR
X7757	17760	N128	DEC	-128	
X7760	030000	SEEK	OCT	030000	
X7761	020000	R7900	OCT	020000	
X7762	040000	R2883	OCT	040000	

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

DICS LOADER - Continued

```
X7763  010000  S2883   OCT  010000
X7764  000000  STAT    NOP
X7765  102011  ADDR1   OCT  102011
X7766  102055  ADDR2   OCT  102055

X7767  000000          NOP
X7770  000000          NOP

X7771  000000          NOP

X7772  163766  GO      LDA  ADDR2,I      GET 1ST WORD OF
                                           PRE-ROOT
X7773  002002          SZA               IS IT A NOP? (REV B OR
                                           LATER?)
X7774  127766          JMP  ADDR2,I      YES-JSB-CONFIGURE
                                           WITH DMACW
X7775  117766          JSB  ADDR2,I      YES-JSB-CONFIGURE
                                           WITH DMACW
X7776  1200DD  DMACW   ARS  120000B+DC   MUST IMMEDIATELY
                                           FOLLOW JSB
X7777  000000          NOP               SET TO LAST WORD
                                           AVAILABLE MEM
                       END
```

X = 2 for 12K
3 for 16K
4 for 20K
5 for 24K
6 for 28K
7 for 32K

DD – Lower Number (Highest Priority)

CC – Higher Number (Lower Priority)

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

DISC LOADER
(DOS III, 2000F, RTE II)

```
X7700  002500  START   CLA, CLE
X7701  106501          LIB  1
X7702  005710          BLF, SLB
X7703  027717          JMP  READ
X7704  017741          JSB  SEEK        ACTUAL 2883, TEST 7900
X7705  063757          LDA  BIT14       2883 READ
X7706  1065CC          LIB  CC
X7707  006003          SZE, RSS
X7710  027717          JMP  READ        NO ATTENTION = 2883
X7711  106501          LIB  1
X7712  063714          LDA  BIT9
X7713  004010          SLB
X7714  001000  BIT9    ALS              SAME AS ZERO
X7715  017741          JSB  SEEK        ACTUAL 7900 SEEK
X7716  063760          LDA  BIT 13      7900 READ
X7717  067776  READ    LDB  DMACW
X7720  106606          OTB  6
X7721  067761          LDB  ADDR1
X7722  106602          OTB  2
X7723  067763          LDB  N128
X7724  102702          STC  2
X7725  106602          OTB  2
X7726  002003          SZA, RSS
X7727  027765          JMP  NEW
X7730  1026CC          OTA  CC
X7731  1037DD          STC  DC,C
X7732  103706          STC  6,C
X7733  1037CC          STC  CC,C
X7734  1023CC          SFS  CC
X7735  027734          JMP  *-1
X7736  002240          SEZ, CME         READ TWICE
X7737  027775          JMP  EXIT
X7740  027717          JMP  READ

X7741  000000  SEEK    NOP              A HAS HEAD AND
                                          CYLINDER
X7742  1026DD          OTA  DC          CYLINDER
X7743  1037DD          STC  DC,C
X7744  067756          LDB  SEEKC
X7745  1066CC          OTB  CC
X7746  1037CC          STC  CC,C
X7747  1023DD          SFS  DC
X7750  027747          JMP  *-1
X7751  1026DD          OTA  DC          HEAD AND SECTOR
X7752  1037DD          STC  DC,C
X7753  1023CC          SFS  CC
X7754  027753          JMP  *-1
X7755  127741          JMP  SEEK,I      B HAS SEEKC
X7756  030000  SEEKC   OCT  30000
X7757  040000  BIT14   OCT  40000

X7760  020000  BIT13   OCT  20000
X7761  102011  ADDRI   OCT  102011
X7762  102055  ADDR2   OCT  102055
X7763  177600  N128    OCT  -200
X7764  000200  BIT?    OCT  200

X7765  1067DD  HEW     CLC  DC
X7766  106501          LIB  1
X7767  006011          SLB, RSS
X7770  063764          LDA  BIT7        HEAD 2
X7771  1036DD          OTA  DC,C
X7772  103706          STC  6,C
```

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

DISC LOADER - Continued

```
X7773   1023DD          SFS   DC
X7774   027773          JMP   *-1
X7775   117762  EXIT    JSB   ADDR2,I
X7776   120015  DMACU   ABS   120000B+DC
X7777   140100          ABS   -START
                        END
```

X = 2 for 12K
3 for 16K
4 for 20K
5 for 24K
6 for 28K
7 for 32K

DD – Lower Number (Highest Priority)

CC – Higher Number (Lowest Priority)

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

MTRS LOADERS

```
X7700  063774          LDA  SL0RW      SELECT UNIT 0
X7701  1026CC          OTA  CMND       AND
X7702  1037CC          STC  CMND,C     REWIND TAPE.
X7703  106501          LIB  SSW        GET ORDINAL NUMBER
                                         OF PROGRAM.
X7704  007307          CMB,CCE,INB,SZB, MAKE < 0, PRESET –E–.
                         RSS
X7705  067767          LDB  DFALT      USE DEFAULT IF SWREG
                                         = 0.
X7706  077772          STB  PROG#      SAVE FOR COUNTER.
X7707  063773  READ    LDA  RRF        OUTPUT
X7710  1026CC          OTA  CMND       READ COMMAND
X7711  1025CC          LIA  CMND       AND
X7712  001323          RAR, RAR        TEST
X7713  001310          RAR, SLA        FOR REJECT.
X7714  027707          JMP  READ       REJECTED, KEEP TRYING
                                         UNTIL O.K.
X7715  1037CC          STC  CMND,C     START TAPE.
X7716  1037DD          STC  DATA,C     INITIALIZE DATA CHANNEL
                                         CHANNEL.
X7717  063772          LDA  PROG#      GET PROG ORDNL CNTR
                                         - 0 IF LOAD.
X7720  006644          CLB,SEZ,CME,INB -B ← DATA RECORD MASK.
X7721  067771          LDB  MASK1      -B- ← POST REC MASK
                                         (S.A. ONLY).
X7722  002042          SEZ, SZA        IF DATA RECORD AND
                                         NOT LOADING,
X7723  027707          JMP  READ       IGNORE THE RECORD.
X7724  1022CC          SFC  CMND       POST RECORD OR (DATA
                                         RECORD AND
X7725  027741          JMP  DONE       LOADING), WAIT FOR
                                         DATA OR
X7726  1023DD  LOOP    SFS  DATA       FOR TAPE TO STOP.
X7727  027724          JMP  *-3
X7730  1035DD          LIA  DATA,C     GET WORD FROM TAPE.
X7731  004031          SLB, BRS        TEST IF WE STORE,
                                         SHIFT MASK.
X7732  027726          JMP  LOOP       NO STORE, GET NEXT
                                         WORD.
X7733  073775          STA  S.A.       WE DO, SAVE WORD IN
                                         S.A. TOO.
X7734  002041          SEZ, RSS        IF THIS IS POST RECORD,
X7735  027726          JMP  LOOP       SKIP STORE AND ADDRESS
                                         BUMP.
X7736  173776          STA  PTR,I      STORE THE WORD, THEN
X7737  037776          ISZ  PTR        BUMP ADDRESS POINTER'
X7740  027726          JMP  LOOP       RETURN FOR NEXT WORD.
X7741  073776  DONE    STA  PTR        STORE LOAD ADDR IF
                                         POST RECORD.
X7742  067772          LDB  PROG#      GET PROGRAM ORDINAL
                                         COUNTER.
X7743  063775          LDA  S.A.       GET PROGRAM STARTING
                                         ADDRESS.
X7744  006021          SSB, RSS        ARE WE LOADING?
X7745  027750          JMP  *+3        YES, SKIP S.A. TEST.
X7746  002020          SSA             NO, IS THIS DUMMY END-
                                         OF FILE?
X7747  102001  HLT1    HLT  1          YES, OR PARITY ERROR,
                                         HALT.
                                       !!!HALT IS NOT
                                         PROTECTED!!!
X7750  002241          SEZ,CME,RSS     NO ERROR, IF WE READ
                                         DATA RECORD
```

SERVICE NOTE – HP MODEL 21MX ROM LOADERS

MTRS LOADERS - Continued

```
X7751  002003          SZA, RSS        OR CONTINUATION POST
                                         RECORD.
X7752  027756          JMP  ZTEST      SKIP INITIAL POST REC
                                         STEPS.
X7753  033766          IOR  JMP        INITIAL POST REC,
                                         INCLUDE JUMP
X7754  006007          INB,SZB,RSS     TO STARTING ADDRESS.
                                         IF THIS
X7755  070002          STA  2          IS OUR PROG, STORE THE
                                         JUMP.
X7756  006220  ZTEST   CME, SSB        IF WE HAVEN'T FOUND
                                         OUR PROG YET
X7757  027706          JMP  READ-1     UPDATA PROG#, READ
                                         NEXT REC.
X7760  1025CC          LIA  CMND       OUR PROG OR POST
                                         RECORD OF NEXT
X7761  001332          RAR,SLA,RAL     ONE, IF IT HAS A PARITY
                                         ERROR
X7762  027747          JMP  HLT1       GO NO FURTHER.
X7763  006003          SZB, RSS        1ST POST REC OF NEXT
                                         PROGRAM?
X7764  027706          JMP  READ-1     NO, UPDATE PROG#,
                                         CONTINUE.
X7765  063770          LDA  HLT70      YES, STORE FINAL
                                         HALT.
X7766  024000  JMP     JMP  A          GO TO IT.
00000          A       EQU  0          -A- REGISTER ADDRESS
                                         DEFINITION.
000DD          CMND    EQU  DATA+1     MAG TAPE COMMAND
                                         CHANNEL S.C.
X7767  177774  DEFAULT ABS -DEFLT       -(PROGRAM ORDINAL
                                         DEFAULT).
X7770  102070  HLT70   HLT  70B        FINAL HALT (GOOD
                                         HALT).
X7771  000677  MASK1   OCT  677        POST RECORD READ MASK.
X7772  000000  PROG#    NOP            PROGRAM ORDINAL COUN-
                                         TER.
X7773  000023  RRF     OCT  23         MT READ ONE RECORD
                                         COMMAND CODE.
X7774  001501  SL0RW   OCT  1501       MT SELECT 0/REWIND
                                         COMMAND CODE.
00001          SSW     EQU  1          SWITCH REG ADDRESS
                                         DEFINITION.

       THE LOCATIONS OF THE FOLLOWING TWO WORDS MUST NOT
       BE CHANGED TO PRESERVE 2105, -08, ETC. BOOT LOADER
       CAPABILITY.

X7775  600000  S.A.    BSS  1          PROG START ADDR (IN
                                         POST REC).
X7776  000000  PTR     BSS  1          DATA RECORD LOAD
                                         ADDRESS.
                       END
```

X = 2 for 12K
3 for 16K
4 for 20K
5 for 24K
6 for 28K
7 for 32K

DD – Lower Number (Higher Priority)

CC – Higher Number (Lower Priority)

SATTALITE START-UP

P= 077700
S = 32, PRESET, PRESET, L,EN, RUN
HLT = 77
P= 2
S = Φ
R RESET, PRESET, RUN
TTY = :
TYPE - RUN BBTEST

DOWNLOAD BBL FROM MASTER

P=077700
S= 75
PRESET, PRESET,(L,EN,) RUN
HLT 77
LOAD DIAGNOSTICS FROM
075700

SATTALITE 8
START-UP

LOAD 07900 DISC DIAGNOSTIC

LOAD DISC CONFIGURATOR # 24296-60001
REV. 1534 INTO READER.

P = 077700
S = CLEAR
PRESET, PRESET, LOADER EN., RUN
HALT - 77
P = 100
S = SC of CRT (24)
RUN

CRT TERM = INPUT DEVICE AND SC of DEVICE
PHOTO READER (2748) (22)
ANSER QUESTIONS ON CRT IN FOLLOWING MANOR
1, NO
2, NONE

7900 DISC DIAGNOSTIC

LOAD DIAGNOSTIC INTO TAPE READER = 12960-16001
ENTER SERIAL NO# of DIAG. ON CRT - 111002
DIAGNOSTIC LOADS FROM READER
HALT - 77
P = 100
S = SC of DISC DRIVE (11)
RUN
HALT 77
P = 2000
S = op DESIGN (10)
RUN

SR, 22 SEEK RECORD
0 DR-0
RD = READ
EN = END STATEMENT
LP = LOOP BETWEEN RECORD

CRT TERM.
HSS - ENTER
SD, 0 = SEEK DRIVE 0, RECORD 0
SD, 1 =

SAMPLE

H65 ENTER INSTRUCTION

SD = SEEK DRIVE
SR = " RECORD OR TRACK
0-3 4 SIDES of 2 DISCS

(SD,1 RT LF) SELECT DRIVE 1
(SR 100,1) RTLF SEEK RECORD 100 - HEAD 1
EN ENABLE

EXTENDER

CONTENTS PAGE

SPECIFICATIONS FOR 2150A

POWER REQUIREMENTS

a. Line voltage: 115 volts ac ± 10 percent (15 amperes), or 230 volts ac ± 10 percent (7.5 amperes) if option 015 installed.

b. Line frequency: 47.5 to 66 Hz.

c. Main unit power consumptions: with internal power supply loaded to capacity by plug-in options, 1600 watts maximum; with on the teleprinter interface option, 1000 watts minimum.

d. Power cable: 3-prong connectors (two power prongs, one ground prong); used for either 115- or 230-volt operation.

DC SUPPLY VOLTAGES AND CURRENTS

a. -2 volts dc, 22.5 amperes

b. +4.5 volts dc, 22.5 amperes (plus current drawn from the -2 volt supply, up to a maximum of 45 amperes).

c. +12 volts dc, 6 amperes

d. -12 volts dc, 6 amperes

e. +22 volts dc, 1 ampere

f. -22 volts dc, 3 amperes

g. +32 volts dc, 3 amperes

ENVIRONMENTAL LIMITS

a. Temperature 0° to 55°C (32° to 131°F).

b. Relative humidity 50 to 95 percent at 25° to 40°C (77° to 104°F).

VENTILATION

a. Intake on sides and back at bottom, exhaust at top.

b. Air flow: 600 cubic feet per minute.

c. Heat dissipation: 5500 BTU/hour maximum.

DIMENSIONS AND WEIGHTS (See Figure 1)

a. Width: 16.75 inches (425,45 millimeters).

b. Panel height: 31.5 inches (800,1 millimeters)

c. Depth behind panel: 19.750 inches (501,65 millimeters)

DIMENSIONS AND WEIGHTS (continued)

d. Net weight: 230 pounds(104,42 kilograms)

e. Shipping weight: 330 pounds (149,82 kilograms)

CLEARANCE REQUIREMENTS

a. Recommended cable clearance at rear: 5 inches minimum (127 millimeters)

b. Recommended air exhause clearance at top: 3 inches minimum (76,2 millimeters)

c. Recommended air exhause clearance at sides: 2 inches minimum (50,8 millimeters)

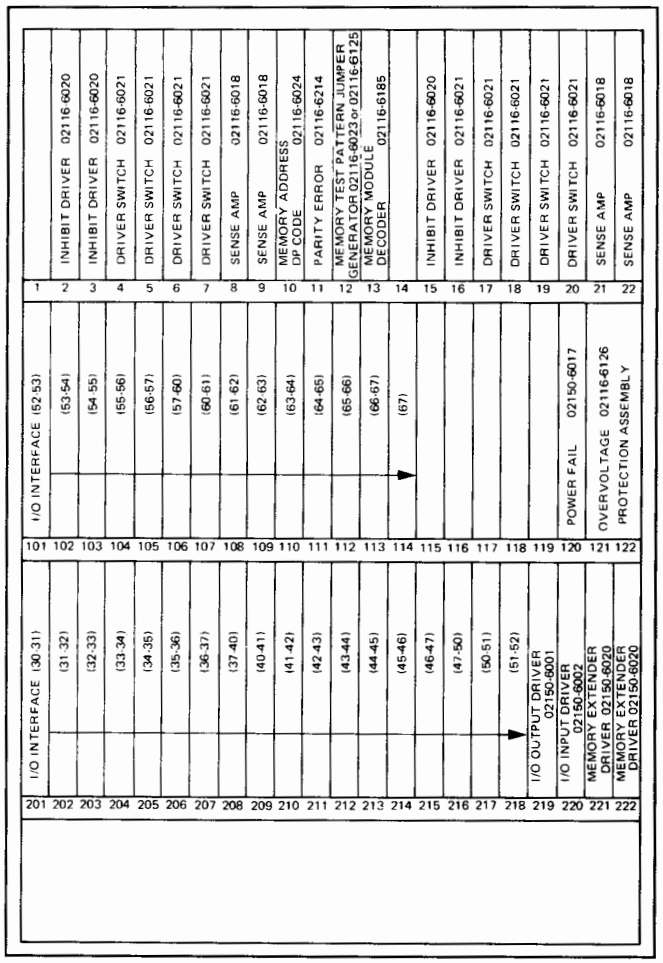
ACCESSORIES

a. 5060-6236 Rack Mount Kit

b. 5060-2267 Power Cord

c. 02150-6019 Ground Cable

2150A I/O AND MEMORY EXTENDER (FRONT)



NOTE: 2150A WORKS WITH 2116A OF SERIAL PREFIX 746 OR GREATER.

POWER REQUIREMENTS

a. Line voltage: 115 volts ac ± 10 percent (15 amperes), or 230 volts ac ± 10 percent (7.5 amperes) if option 015 is installed.

b. Line frequency: 47.5 to 66 Hz.

c. Main unit power consumption: with internal power supply loaded to capacity by plug-in options, 1600 watts maximum: with only the teleprinter interface option, 1000 watts minimum.

d. Power cable: 3 prong connectors (two power prongs, one ground prong); used for either 115- or 230-volt operation.

DC SUPPLY VOLTAGES AND CURRENTS

a. -2 volts dc, 22.5 amperes

b. +4.5 volts dc, 22.5 amperes (plus current drawn from the -2-volt supply up to a maximum of 45 amperes)

c. +12 volts dc, 6 amperes

d. -12 volts dc, 6 amperes

e. +22 volts dc, 1 ampere

f. -22 volts dc, 3 amperes

g. +32 volts dc, 3 amperes

ENVIRONMENTAL LIMITS

a. Temperature 0° to 55°C (32° to 131°F).

b. Relative humidity 50 to 95 percent at 25° to 40°C (77° to 104°F).

VENTILATION

a. Intake on sides and back at bottom, exhaust at top.

b. Air flow: 600 cubic feet per minute.

c. Heat dissipation: 5500 BTU/hour maximum.

DIMENSIONS AND WEIGHTS. (See figure 1-3.)

a. Width: 16.75 inches (425,45 millimeters).

b. Panel height: 31.5 inches (800,1 millimeters).

c. Depth behind panel: 19.750 inches (501,65 millimeters).

DIMENSIONS AND WEIGHTS (continued)

d. Net weight: 230 pounds (104,42 kilograms).

e. Shipping weight: 330 pounds (149,82 kilograms).

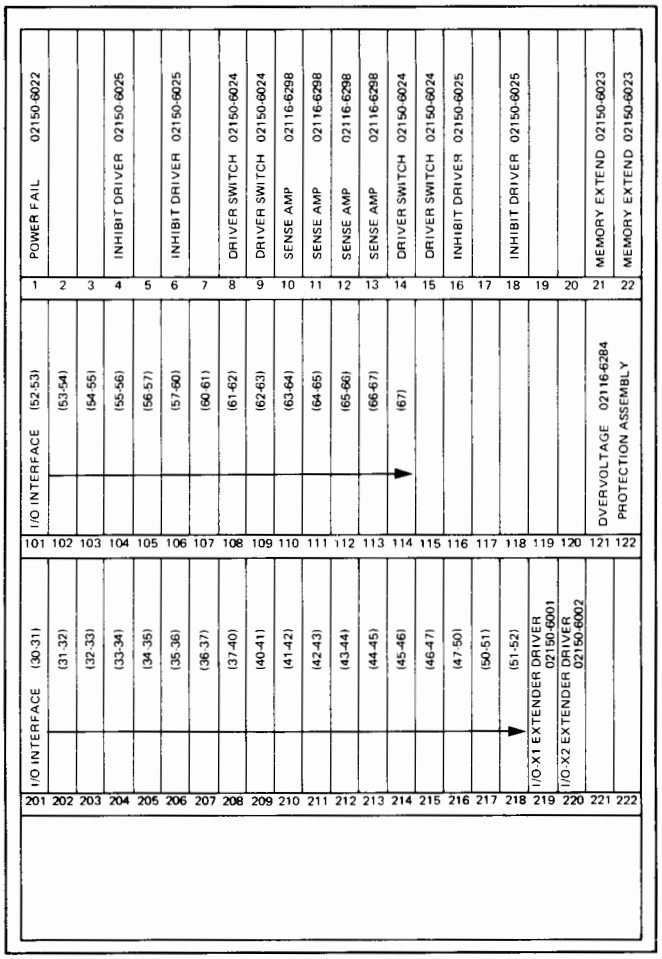
CLEARANCE REQUIREMENTS

a. Recommended cable clearance at rear: 5 inches minimum (127 millimeters).

b. Recommended air exhaust clearance at top: 3 inches minimum (76,2 millimeters).

c. Recommended air exhaust clearance at sides: 2 inches minimum (50,8 millimeters).

2150B I/O AND MEMORY EXTENDER



NOTE 1: IF COMPUTER IS USING POWER FAIL AUTO RESTART 12588-6001, INSERT JUMPER W2 IN POSITION "2116B WITH 2150B".

NOTE 2: RESISTANCE LOAD CARDS (02116-6047) MAY BE INSERTED IN SLOTS A114 AND A218.

NOTE 3: IF THE 2116B HAS SENSE AMPS 02115-6001, THAN THE SENSE AMPS MUST BE CHANGED TO 02116-6298; i.e., THE 2150B AND THE 2116B MUST HAVE THE SAME SENSE AMP PART NO.

NOTE 4: REFER TO IOSM FOR 2150B FOR FURTHER INFORMATION.

2151A SPECIFICATIONS

POWER REQUIREMENTS

a. Line voltage: 115 volts ac ± 10 percent (4.5 amperes) or 230 volts ac ± 10 percent (2.25 amperes) with option 015.

b. Line frequency: 50- to 60-Hz ± 10 percent.

c. Power cable: 3-prong connector (two power, one ground).

d. DC voltages (refer to table 1-2)

ENVIRONMENTAL LIMITS

a. Temperature: 10° to 40°C (50° to 104°F).

b. Relative humidity to 95 percent at 40°C (104°F).

VENTILATION

a. Intake at back, exhaust on sides.

b. Air flow: 200 cubic feet per minute.

c. Heat dissipation: 1638 BTU/hour maximum.

PHYSICAL DIMENSIONS

a. Width: 19 inches (482,6 millimeters) for standard rack mounting.

b. Panel height: 12.25 inches (311.15 millimeters).

c. Depth behind panel: 22.5 inches (571,5 millimeters).

d. Recommended air exhaust clearance at sides: 2 inches minimum (50, 8 millimeters).

e. Net weight: 100 pounds (45, 4 kilograms); shipping weight 125 pounds (56,75 kilograms).

EQUIPMENT SUPPLIED

HP 2151A I/O Extender (with internal power supply) which includes 2 Interface Cables, HP Part No. 02150-6003.

Plus one of the following interface kits:

HP 12593A I/O Extender Interface Kit for the HP 2114A/B which consists of:

Resistance Load Card, HP Part No. 02116-6047
I/O Extender Driver Card, HP Part No. 12593-6003
I/O-X1 Extender Card, HP Part No. 12593-6004
I/O-X2 Extender Card, HP Part No. 12593-6005

HP 12594A I/O Extender Interface Kit for the HP 2115A which consists of:

I/O-1 Extender Driver Card, HP Part No. 02116-6182
I/O-2 Extender Driver Card, HP Part No. 02116-6183
Interconnecting Cable, HP Part No. 02150-6018
I/O-X1 Extender Card, HP Part No. 12594-6004
I/O-X2 Extender Card, HP Part No. 12594-6005

HP 12596A I/O Extender Interface Kit for the HP 2116B which consists of:

I/O-1 Extender Driver Card, HP Part No. 02116-6182
I/O-2 Extender Driver Card, HP Part No. 02116-6183
Interconnecting Cable, HP Part No. 02150-6018
I/O-X1 Extender Card, HP Part No. 12596-6004
I/O-X2 Extender Card, HP Part No. 12596-6005

Direct Memory Access is available only to mainframe channels.

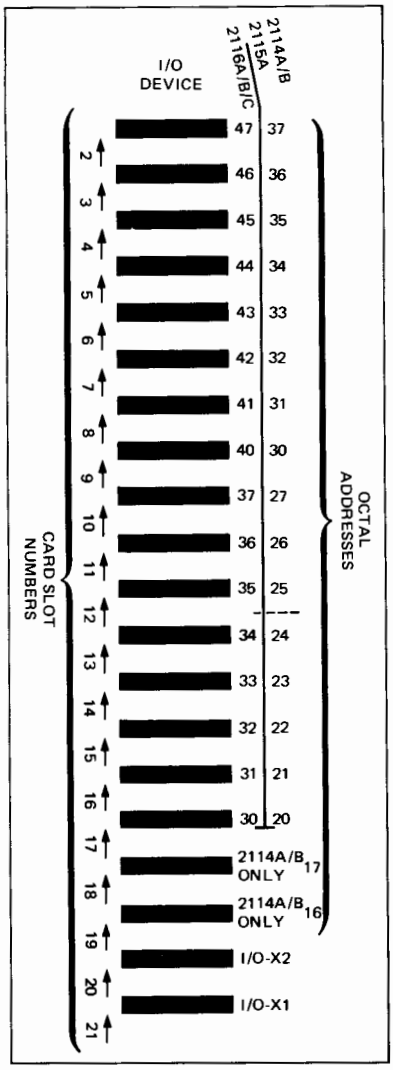
DC Voltage and Current Specifications

BUS VOLTAGE (VOLTS)				MAXIMUM CURRENT (A)
NOMINAL	*MAXIMUM	**MINIMUM	**AC RIPPLE (P-P, TYPICAL)	
+ 5	5.3	4.5	0.45	23
+12	12.6	12.0	0.25	3
-12	12.6	12.0	0.25	3
- 2	2.7	2.0	0.3	6
+30	33.0	30.0	1.4	1

*High ac line, no load (applicable accessory kit installed but no interface kits installed).
**Low ac line, maximum load.

HP 2151A Extender Usability

FEATURE	HP COMPUTER				
	2114A	2114B	2115A	2116A	2116B/C
Computer I/O Addresses:					
Without Extender	10-17	10-16	10-17	10-27	10-27
With Extender	10-16	10-15	10-17	10-27	10-27
Extender I/O Address:	17-37	16-37	20-37	30-47	30-47
Additional Channels Using Extender	16	17	16	16	16
Interface Kit Required	12593A	12593A	12594A	12596A	12596A


2114A/B
2115A
2116A/B/C
I/O
DEVICE
47
46
45
44
43
42
41
40
37
36
35
34
33
32
31
30
37
36
35
25
24
23
22
21
20
2114A/B ONLY 17
2114A/B ONLY 16
I/O-X2
I/O-X1
OCTAL
ADDRESSES
CARD SLOT
NUMBERS
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21

2155A I/O EXTENDER SPECIFICATIONS

POWER REQUIREMENTS

Line Voltage:	115V ac ± 10%, single phase, 12A, or 230 ac ± 10%, single phase, 6A
Line Frequency:	47.5 to 66 Hz
Power Consumption:	800 Watts (1400 Volt-Amperes), maximum

POWER CABLE

Length:	10 feet
Connector:	NEMA Type 5-15P (for 115V ac operation), or NEMA Type 6-15P (for 230V ac operation)

DC SUPPLY VOLTAGES AND CURRENTS

+30V, 0.1A
+12V, 5A
+4.85V, 50A
-2V, 23A
-12V, 5A

ENVIRONMENTAL LIMITS

Ambient Temperature Range:

Operating:	0°to 55°C (32° to 131°F)
Non-operating:	-40° to 75°C (-40° to 167°F)

Relative Humidity: 50 to 95% at 25° to 40°C (77° to 104°F) without condensation

Altitude:

Operating:	15,000 feet
Non-operating:	25,000 feet

VENTILATION

Air Flow:	400 cubic feet per minute
Heat Dissipation:	2300 BTUs per hour, maximum

WEIGHT AND DIMENSIONS

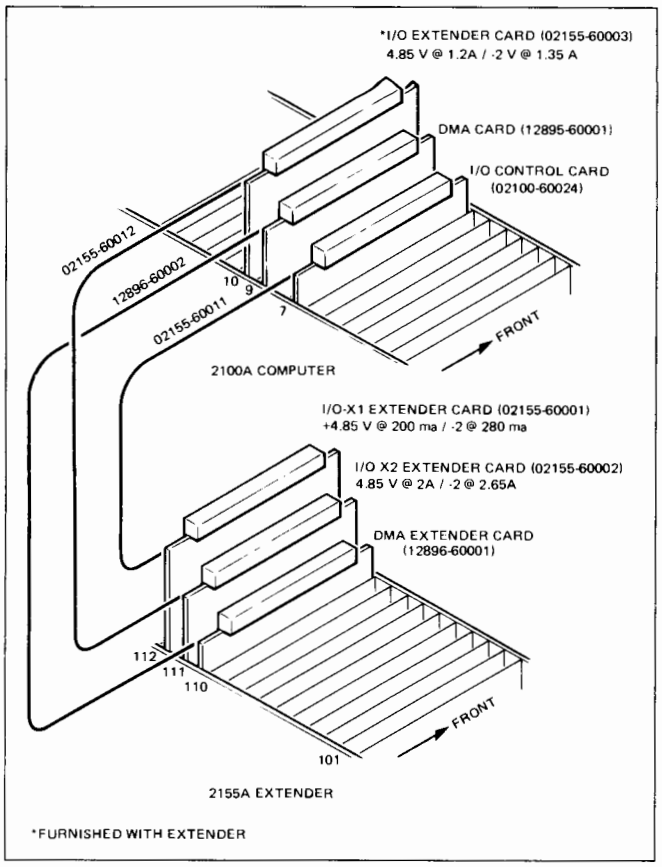
Weight:	115 pounds (52,21 kilograms) with card cage filled
Height:	12 inches (304,8 millimeters) for rack mounting 12.5 inches (317,5 millimeters) with stand-alone feet
Width:	16.75 inches (425,5 millimeters)
Depth:	23.75 inches (603.25 millimeters)

2155A I/O EXTENDER SPECIFICATIONS

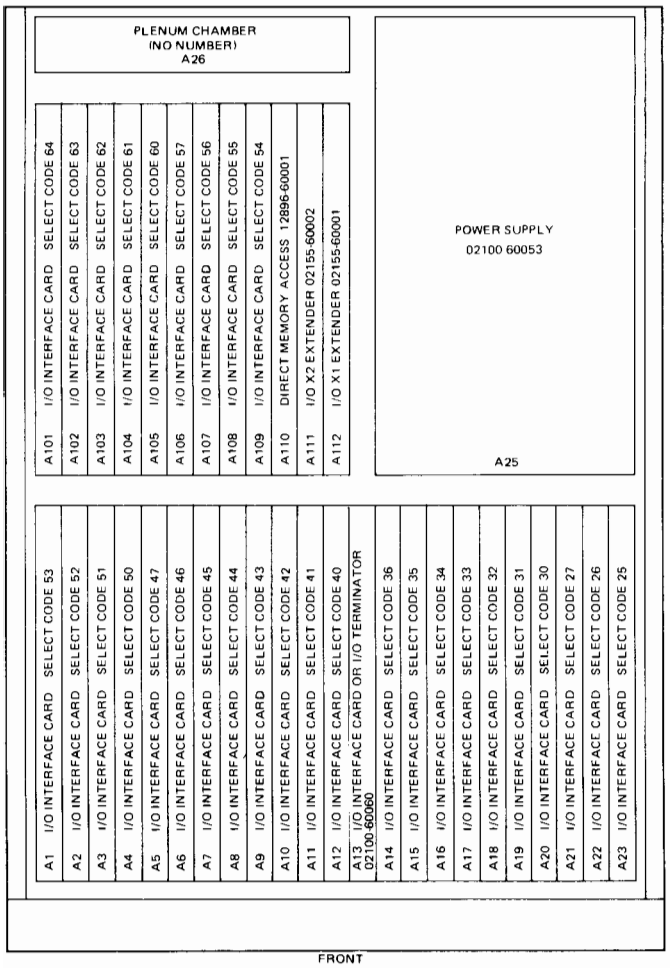
POWER REQUIREMENTS (Continued)

CLEARANCE REQUIREMENTS

Recommended Cable Clearance at Rear:	5 inches (127 millimeters), minimum
Recommended Air Exhaust Clearnce at Top:	3 inches (76.2 millimeters), minimum
Recommended Air Exhaust Clearance at Sides:	2 inches (50,8 millimeters), minimum



I/O Extender with 12896A DMA Kit, Interface to Computer



NOTE: *DIRECT MEMORY ACCESS CARD IS AN ACCESSORY TO THE EXTENDER AND IS NOT PART OF THE BASIC CONFIGURATION.

Location of Assemblies in 2155A I/O Extender

CLEAR MEMORY DIAG.

	MD	LOC
INB - 6004		20
STA 0,I - 170001		21
JMP *-2	024020	22

CLEAR A REG.

SET B REG TO 22

SET P REG TO 20

RUN

CLR MEM

TIMESHARE/ACCESS

CONTENTS PAGE

2000 A

SYSTEM GENERATION

a. Check to see all equipment is turned on and that the I/O devices reside in the proper I/O channels.

b. Place TSB Loader in photo reader.

c. Initiate the BBDL using the starting address of 037700_8.

d. After the TSB Loader has been successfully read in, place the first (of two) TSB System tapes in the photo reader.

e. Start TSB Loader at 2000_8, the computer will print

LIBRARY?

respond with *NO*

f. The computer prints

SECTORS/TRACK ON DISC-0?

respond with the decimal number of logical sectors per track on the first disc. Refer to the following for the correspondence between devices and sectors per track.

DEVICE	TYPE	SECTORS/TRACK	# TRACKS
2770A-01	disc	90	64
2771A	disc	90	64
2711A-01	disc	90	128
2773A	drum	128	48
2774A	drum	128	96
2775A	drum	128	192

g. DISC MODIFICATIONS?

Respond: DISC – *disc number, select code, track length*

where:

disc number
is a number from 1 to 3 indicating the disc logical number

track length
is a decimal number from 90 to 128 indicating the number of sectors per track

select code
is the select code of disc.

Each DISC command is terminated by a carriage return. The entire sequence of DISC commands is terminated by a single carriage return.

h. GIVE LOCK, UNLOCK or LOAD COMMAND

Respond with a lock or unlock command if a track is to contain user programs

LOCK(UNLOCK)-*n*, *track*1 [,*track*2]

where:

n
is the disc logical number (0 through 3)

*track*1
is a decimal quantity specifying the beginning track on that disc

*track*2
is the optional ending track.

Terminate the sequence with a LOAD command.

i. If a Disc Operating System is present on the disc, respond to the

DISC MONITOR PRESENT?

message with a *YES*; if not, a *NO*.

j. The first TSB System tape will be read in through the teleprinter. When the computer halts (102077) respond to

DATE

with Julian calender date followed by the year (e.g. 361/74).

k. Respond to

TIME

with a four-digit representation of the current hour and minute on a twenty-four hour clock.

l. The completion of the loading process is signified by the message

READY

UPDATING A PRE-EXISTING SYSTEM

a. Load the TSB Loader, start at 2000_8.

b. Respond to the

LIBRARY?

question with a *YES*.

c. Respond to the

MAG TAPE SELECT CODE?

with a carriage return, indicating that the current library on the disc is to be used. At this point the above sequence will continue as after DISC MODIFICATIONS.

RELOADING FROM MAGNETIC TAPE

a. Load TSB Loader and start at 2000_8.

b. Respond to the

LIBRARY

question with *YES*.

c. Respond to

MAG TAPE SELECT CODE?

with the octal select code of the lower channel containing the magnetic tape unit interface cards, followed by an asterisk if the 7970 controller card is used.

TSB LOADER OPTION

If the switch register bit 15 is set while loading the TSB System from either punched tape or magnetic tape, the TSB Loader will execute a halt (102015_8) just prior to transferring each module of TSB System to disc. The first halt is for the core resident part of the TSB System. Each subsequent halt is for a disc-resident module of the system. This provides a way to patch or alter one or more of these modules.

TSB LOADER DIAGNOSTIC AND HALTS

Halt	Messages & Interpretations
102001	UNEXPECTED END-OF-FILE/END-OF-TAPE Irrecoverable halt, use earlier sleep tape. TAPE CANNOT BE READ Tape being read is bad, use earlier sleep tape. OUT OF DISC SPACE This error can be corrected only by unlocking some disc tracks on a subsequent load attempt. DISC FAILURE The offending track is specified on the teleprinter. The track must be loaded on a subsequent load attempt.
102004	There has been a power failure during loading. Restart the loading procedure from the beginning.
102011	TAPE BAD OR TOO SHORT Loading of the dump tape may be retried by pressing RUN.
102015	Put switch register bit 15 down and press RUN.
102022	Load TSB Loader Tape using BBDL.
102033	WRITE NOT ENABLED Put write ring into the tape reel and press RUN.
102044	CHANGE MAG TAPE TO AUTO Change to ON-LINE or AUTO and press RUN.
102055	ILLEGAL ADDRESS The address read from the paper tape (displayed in the A-Register) cannot belong to the TSB System. The cause may be a dirty tape or photo reader. Reposition the offending tape record under the photo reader and press RUN. Alternatively, restart the loading procedure from the beginning.
102066	CHECKSUM ERROR The checksum read from the tape (which is displayed in the A-register) does not match that calculated from the tape record as it was read in. The corrective action is the same as for halt 102055.
102077	END OF TAPE If the TSB System tape is actually on several different binary tapes, place the next one in the photo reader and press RUN. Otherwise, restart the loader procedure from the beginning.

LOADING THE 2114 SYSTEM

a. Turn on all equipment both in the system processor and front end processor.

b. Load the 2114 tape in the reader.

c. Load the first program on the tape using BBDL of the system processor.

d. Set switch register of the system processor to 2_8, and press RUN.

e. Start BBDL of the front end processor. The front end processor's tape should read in followed by a halt when loading is complete. If not, check BBDL and restart procedure.

f. Halt the system processor, and press RUN on front end processor.

g. Press the ESC (Escape) key on any user terminal that is connected to the front end processor. If the terminal does not respond with a "\" and a carriage return linefeed, reload the front end processor again (Step a).

GENERATING AN INITIAL SYSTEM

a. Load and start front end processor program.

b. Load TSB Loader tape using BBDL.

c. Place the first system tape (2000 B, Part 1) in the photo reader.

d. Start loader at 2000_8; the computer prints.

LIBRARY

respond *NO*. The rest of the generation is the same as in the 2000 A.

UPDATING THE TSB SYSTEM

Same as in 2000 A

RELOADING FROM MAGNETIC TAPE

Same as in 2000 A

TSB LOADER OPTION

Same as in 2000 A

2000A/B SELECTED USER/OPERATOR COMMANDS

Command	Function
BYE	Log the user off of the terminal.
CAT	List the names and lengths of user library programs.
ECH-OFF	Permit use of half-duplex coupler.
ECH-ON	Return user to full-duplex mode.
HEL-idcode, password	Log the user onto his terminal. User must provide the idcode and password.
KIL-name	Delete the named program from the user's library.
LIB	List the names and lengths of the system library programs.
SAV	Saves the current program in the user's library.
SLEEP	Provide an orderly shutdown of the Time Shared system.

2000 C/C'/F

SYSTEM GENERATION

a. Load protected loader.

b. Load IOP. Start IOP at P=2.

c. Load TSB loader. Start at P=2000.

d. Put system tape 1 of 3 in photo reader.

e. The following query is printed:

IS THE SYSTEM CONSOLE AN HP 2762A?

Respond YES if the console is a 2762A, otherwise respond NO. (Note that this question only appears when in 2000F opt. 200/205.)

LIBRARY?

Enter NO

f. If entering patches by hand, set bit 15.

g. The following query is printed:

CONFIGURATION OPTIONS?

If multiple drums or discs, answer YES. Then enter *DISC-(logical number), (select code), (unit on controller)* or enter *DRUM- (logical number), (select code).*

If fewer than 32 ports, answer *YES.*

Otherwise, answer *NO.*

The following steps apply to 2000 C'/F only.

h. Enter *MAG-0* and then *SLEEP.*

i. Load 2000 C'/F patch program. Start at P=2000.

j. Bring up system from P=77760 (drum) or P=77750 (disc).

SYSTEM UPDATE FROM PAPER TAPE (2000 C/C'/F)

a. Sleep or hibernate system.

b. Load TSB Loader. Start at P=2000.

c. Put system tape 1 of 3 in the photoreader.

d. After asking what type of system console is being used, the following query is printed:

LIBRARY?

Answer *YES*

e. If entering patches by hand, set bit 15.

f. The following query is printed:

MAG TAPE SELECT CODE?

Enter carriage return.

The following 3 steps are for 2000 C'/F only.

g. Enter *MAG-0* and then *SLEEP.*

h. Load 2000 C'/F patch program. Start at P=2000.

i. Bring up system from P=77760 (drum) or P=77750 (disc).

j. Enter *MAG- (mag tape select code)* and then *SLEEP.*

k. Bring up the system from P=77760 (drum) or P=77750 (disc).

MAGNETIC TAPE RELOAD (2000 C/C'/F)

a. Load TSB loader. Start at P=2000.

b. After asking what type of system console is being used, the following query is printed:

LIBRARY?

Answer *YES.*

c. If entering patches by hand, set bit 15.

d. The following query is printed:

MAG TAPE SELECT CODE?

Enter the mag tape select code.

The following steps are for 2000 C'/F only.

e. Enter *MAG-0* followed by *SLEEP.*

f. Load the 2000 C'F patch program. Start at P=2000.

g. Bring up the system from P=77760 (drum) or P=77750 (disc).

SYSTEM CRASH (2000 C)

a. Obtain Telekludge dump. Start at P=77000

b. Run diagnostics.

c. Perform magnetic tape reload.

SYSTEM CRASH (2000 C'/F)

a. Obtain Cold Dump tape. Mag tape select code is loaded into the S-register. Start at P=77000.

b. Run diagnostics.

c. Perform a magnetic tape reload.

DISC/DRUM ALLOCATION

Type STA on the system console or A000 for system allocation.

Type DIR on the system console or A000 for user allocation.

ERROR CONDITIONS

If bringing up system from protected loader and the system

a. does not halt after starting at 77760 (BBDL) or 77750 (BMDL), then the disc or drum is not ready,

b. halts with 102000 displayed, the system is unable to read the bootstrap from drum sector zero,

c. halts with 102001 displayed, the system is unable to read the bootstrap from drum sector one or from the system disc,

d halts with 102002 displayed, a read error occurred and the status is displayed in the A-register. If status=177777, there is a disc zero timing problem. Press Run to try again.

Time Shared Basic loader halts are always accompanied with a message except halts:

102004 which indicates a power failure. The remedy is to simply restart whatever activity was in progress.

102005 which indicates a parity halt.

Halts can occur while the Time Shared Basic system is up and running. Halts fall into two groups: those that are recoverable and those that are not. For recoverable halts, load the TSB loader and start the system at P=3000. For irrecoverable halts, a Cold Dump (2000 C'/F) or a Telekludge dump (2000 C) must be taken to discover the problem.

Halt	Discussion
102002	An erroneous system transfer has occurred (it is probably a memory wraparound). Recovery is not recommended.
102004	(2000 C only) A power failure has occurred. Check restart switch positions. Recovery is not recommended.
102005	A parity error has occurred. Recovery is not recommended.
102011	An unexpected interrupt has come from the interconnect kit. Recovery is not recommended.
102030	The disc driver is busy. Recovery is impossible.
102031	The disc that was called does not exist. If the system is the 2000 C, a bad ADT (Available drum/disc table) address was generated. Recovery is impossible.

Halt	Discussion
102032	(2000 C'/F) A disc error occurred while writing a system track. Recovery is possible. (2000 C) A directory track could not be found. Recovery is impossible.
102033	(2000 C'/F) A disc error occurred while reading a track or writing a non-essential track. Recovery is possible. (2000 C) System tables are incompatible due to a disc error. Recovery is impossible.
102034	(2000 C'/F) System tables are incompatible due to disc error. Recovery is impossible.
102035	(2000 C'/F) A directory track could not be found. Recovery is impossible.
102036	(2000 C'/F) A power failure has occurred. Check the power fail restart switch position. Recovery is impossible.
102037	(2000 C'/F) A bad ADT (Available drum/disc table) address was generated. Recovery is impossible.

SYSTEM COMMAND FORMATS (A USEFUL SUBSET)

Command	Meaning
ANN-ALL,*message*	Send *message* to all ports.
ANN-port #,*message*	Send *message* to *port #*.
DIR	Obtain a complete directory.
DIR-*account ID*	Obtain a directory starting at *account ID.*
DIS-*logical unit, sc, physical unit*	Associate logical drive *logical unit* with physical drive *physical unit* which is on select code *sc.* (This is a configuration option only.)
DIS-*logical unit,* 0	Remove disc from system. (This is a configuration option only.)
DRU-*drum number, sc*	Associate drum *drum number* with controller on select code *sc.* (This is a configuration option only.)
DRU-*drum number,* 0	Remove drum from system. (This is a configuration option only.)
HIB	Back up entire system on magnetic tape.
LOC-*n, track1, track2*	Make drum tracks unavailable. *n* is the drum number, *track1* is the beginning track, and *track2* (optional) is the ending track.
MAG-*sc*	Tell the system which select code *sc* has the mag tape.
MAG-*sc**	(2000 C/C' only) A 7970 mag tape is on select code *sc.*
MAG-0	Tell the system that no mag tape is in system.
MLO-*block1,block2*	Make disc tracks unavailable. *block1* is the first block to be locked and *block2* (optional) is the last block to be locked.

Command	Meaning
MUN-*block1,block2*	Make previously locked disc blocks available. *block1* is the first block to be unlocked and *block2* (optional) is the last block to be unlocked.
NEW-*ID,password,* *time limit,* *disc space*	Create a new user ID in the system.
PHO-*n*	Specify how long the system waits for "HELLO" after answering the telephone
POR	(2000 C'/F only) Get a listing of port speeds.
PRI-*sc*(*(*))	(2000 C'/F only) Indicate the type of line printer used: *sc* means HP 2778 *sc** means HP 2610A or HP 2614A *sc*** means HP 2767
REP	List IDs, time used, and space used.
REP-ID	List IDs, time used, and space used starting at the specified ID.
ROS	List the ports in use.
SDI	List the directory of programs and files on drum.
SDI-ID	List the directory of programs and files on drum starting at the specified ID.
SLE	Sleep the system. If the mag tape select code is zero (MAG-0), sleep to disc only. If a mag tape select code is specified, sleep is to mag tape.
SPE-*baud rate,* *character size,* *port number(,* *port number . . .)* or SPE-*baud rate,* *character size,* ALL	(2000 C'/F only) Set port speeds. Common settings are: SPE-130,2,*port number* (10 CPS) SPE-95,1, *port number* (15 CPS) SPE-47,1, *port number* (30 CPS) SPE-11,1,*port number* (120 CPS) SPE-5,1,*port number* (240 CPS) SPE-106,*,*port number* (14.9 - IBM 2741)
STA	Print the system status report.
UNL-*n,track1,track2*	Make the specified drum tracks available: *n* is the drum number, *track1* is the beginning track and *track2* (optional) is the ending track.

USER COMMAND FORMATS (A USEFUL SUBSET)

Command	Action
BYE	Log off the system.
CAT	List the programs/files in the user account.
ECH-ON	Turn on the echo.
ECH-OFF	Turn off the echo.
GRO	List programs/files in the group account.
HEL-*ID,password, terminal type*	Log on the system. *Terminal types* are:

2000C	2000 C'/F	
1	0	HP 2600, HP 2749, IBM 2741
2	1	Execuport 300, TI Silent 700
3	2	ASR-37
4	3	HP 2762, Terminet 300
5	4	Memorex 1240
6		DCT-500

LIB	List programs/files in the A000 library.
LPR	(2000 C'/F) Send output to the line printer.
MES-*text*	Send *text* to the system console.

2000 TSB HARDWARE

Table T-1. 2000A Hardware

SC		
10	MPX	12584-6001
11	TTY	12531-6001
12	TBG	02116-6119
13	RDR	12597-6001
14	DISC	12610-6001
15	DISC	12610-6002
16	optional	
17	optional	

Power Fail switch up
Parity Check switch up
Disc/Drum switch down

Table T-2. 2000B Hardware

2116B/C		2114A/B	
PROC INT	12566-6001	MPX (DATA)	12584-6001
PROC INT	12566-6001	MPX (DATA)	12584-6001
TTY	12531-6001	PROC INT	12566-6001
RDR	12597-6001	PROC INT	12566-6001
DISC	12610-6001	MPX (PHO CONT)	12584-6001
DISC	12610-6002	MPX (PHO CONT)	12584-6001
TBG	02116-6119	unused	
optional		unused	

Table T-3. 2000C Hardware

	MAIN CPU 2100A/S OR 2116B/C		I/O CPU 2100A/S, 2114A/B OR 2116B/C	
SC				
10	PROC INT A	12566-6001	MPX (DATA)	12584-6001
11	PROC INT B	12566-6001	MPX (DATA)	12584-6001
12	TTY	12531-6001	PROC INT A	12566-6001
13	RDR	12597-6001	PROC INT B	12566-6001
14	FH DISC 1	12610-6001	MPX (PHO CONT)	12584-6001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12584-6001
16	TBG	12539-60001		
17	MH DISC 1*	12565/13210		
20	MH DISC 2*	12565/13210		

Table T-4. High-Speed 2000C Hardware

	MAIN CPU 2100A/S OR 2116B/C		I/O CPU 2100A/S, 2114B,** OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	CONSOLE	12531-6001	TBG	12539-60001
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	FH DISC 1	12610-6001	1st MPX (DATA)	12921-60001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12922-60001
16	TBG	12539-60001	2nd MPX (DATA)	12921-60002
17	MH DISC 1*	12565/13210	2nd MPX (DATA)	12921-60001
20	MH DISC 2*	12565/13210	MPX (PHO CONT)	12922-60001
21	MAG TAPE 1	13181-60070	Optional	
22	MAG TAPE 2	13181-60010		

*MH Discs can be either 2883A's or 7900A.s, but not both.

**I/O Extender must be used with 2114B if two multiplexers are to be used in system.

Table T-5. 2000F OPT 200/205 Hardware

	MAIN CPU 2100A/S ONLY		I/O CPU 2100A/S, 2114B,** OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	TTY CONSOLE	12531-6001	TBG	12539-60003
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	TBG	12539-60003	1st MPX (DATA)	12921-60001
15	MH DISC 1*	13210/12565	MPX (PHO CONT)	12922-60001
16	MH DISC 2*	13210/12565	2nd MPX (DATA)	12921-60002
17	MAG TAPE 1	13181-60070	2nd MPX (DATA)	12921-60001
20	MAG TAPE 2	13181-60010	MPX (PHO CONT)	12922-60001

Table T-6. 2000F OPT 210/215 Hardware

	MAIN CPU 2100A/S ONLY		I/O CPU 2100A/S, 2114B,** OR 2116B/C	
SC				
10	PROC INT A	12566-6001	PROC INT A	12566-6001
11	PROC INT B	12566-6001	PROC INT B	12566-6001
12	CONSOLE	12531-6001	TBG	12539-60001
13	RDR	12597-6001	1st MPX (DATA)	12921-60002
14	FH DISC 1	12610-6001	1st MPX (DATA)	12921-60001
15	FH DISC 2	12610-6002	MPX (PHO CONT)	12922-60001
16	TBG	12539-60001	2nd MPX (DATA)	12921-60002
17	MH DISC 1*	12565/13210	2nd MPX (DATA)	12921-60001
20	MH DISC 2*	12565/13210	MPX (PHO CONT)	12922-60001
21	MAG TAPE 1	13181-60070	Optional	
22	MAG TAPE 2	13181-60010		

*MH Discs can be either 2883A's or 7900A's, but not both.
**I/O Extender must be used with 2114B if two multiplexers are to be used in system.

2000E

HARDWARE CONFIGURATION

I/O Channel	Device
10_8	System Console
11_8-12_8	HP 7900A DISC
13_8	Paper Tape Reader
14_8-15_8	Multiplexer
16_8	Phones Control
17_8	Time Base Generator
20_8-above*	Optional Mag Tape

*NOTE: One HP 7970A/B/E magnetic tape unit and one additional HP 7900A or HP 7901A disc device will be allowed by the 2000E System.

SYSTEM GENERATION

1.	Load the 2000E TSB Loader/Utility tape with the BBL/BMDL. (HLT 77 indicates a good load of the tape.)	
2.	"P" Register to 2000_8; press RUN.	
3.	System replies with:	2000 LOADER/UTILITY *
4.	You reply with:	*LOAD CR*
5.	System prints:	IS THE SYSTEM CONSOLE AN HP 2762A?
	If the system console is an HP 2762A enter: otherwise enter:	*YES CR* *NO CR*
	System prints:	*LIBRARY?*
6.	If this is a new system you will reply:	*NO CR*
7.	System prints:	SYSTEM ID NUMBER?
8.	You enter *any* decimal value value from 0 to 32766:	*1111 CR*
9.	System requests:	NUMBER OF PORTS?
10.	Reply from 1 to 16:	*10 CR* NOTE: *Be sure* to have first system tape loaded in photo reader prior to hitting the carriage return.
11.	System begins loading first TSB system tape. After tape is loaded, system prints: and a HALT 77 will occur.	END OF TAPE
12.	Load second TSB system tape in photo reader; press RUN. System will load second tape then respond with:	DATE?
13.	Input the date (Julian day/year)	*148/74 CR*
14.	System responds with:	TIME?
15.	Input time (hour 0-23 minutes 0-59)	*1627 CR*
16.	System prints:	READY
17.	The system is now up and running but you have *no* ID's and no libraries. Place ID's on system (A000 at least) and perform disc sleep to obtain copy of TSB system on removable cartridge.	
18.	For system update, use 2000E TSB patch utility program; System's Analyst note TS. General-4, dated October 25, 1973.	

SYSTEM OPERATOR COMMANDS

Table T-7. 2000E System Operator Commands

Command	Function
ANNOUNCE	Transmits a message from the operator to a specific active user or to all active users.
CHANGE	Modifies an idcode's password, terminal time limit, or disc space limit.
DIRECTORY	Returns a list of library programs and files.
DISC	Informs the system of addition or removal of a user disc. Used during system startup or shutdown and to add or remove disc packs.
KILLID	Removes an idcode from the system.
MOVE	Transfers programs and files from one disc to another.
NEWID	Enters a new idcode into the system.
PHONES	Sets the maximum number of seconds which a user has to log onto the system (through a data set).
PORT	Returns current configuration list for all ports.
PURGE	Removes library programs and files which have not been used since a specified date.
REPORT	Returns a list of each idcode's total time used and amount of disc space in use.
RESET	Resets Terminal time clock of one idcode or all idcodes.
ROSTER	Returns a list of currently active idcodes and ports.
SLEEP	Causes orderly shutdown of the TSB system.
SPEED	Informs the system of a new configuration (baud rate and number of stop bits) for a specific port or for all ports. Speed settings are 10/15/30 cps.

LOADER/UTILITY PROGRAM

Starting address of 2000_8.

Table T-8. 2000E Loader/Utility Program Command

Command	Function
COPY	Copy one disc subchannel to another.
SLOAD	Selective disc load from mag tape.
SDUMP	Selective disc dump to mag tape.
FORMAT	Format a *user* disc.
PACK	Pack a *user* disc.
DLOAD	Load TSB system from subchannels 0 or 1.

SYSTEM OVERLOAD CONDITIONS

When attempting to SAVE programs or OPEN files, the user may receive an OVERLOAD message. This message may result from any of the following conditions; if the user informs the operator that he has received the message, the operator may determine the condition causing the message and take the appropriate action.

1. No user disc has been added to the system.	Use the DISC-UP command to add a user disc.
2. The storage spece required is not available on any user disc.	One of these alternatives: a. Replace a user disc. b. Use the loader to PACK the existing user disc(s). c. Transfer programs to other discs using the MOVE command. d. Wait until existing programs are deleted.
3. The directory track is full.	One of these alternatives: a. Replace a user disc. b. Transfer programs to another disc, with the MOVE command. c. Wait until existing entries are deleted.

HALT CODES

Table T-9. 2000E System Halts

Display Reg	Reason
102004	Power Failure
102005	Parity Error
102010	Disc Error - System Routines (see note)
102011	a. Disc Error – Utility Routines (see note)
	b. After "INSERT CARTRIDGE . . ." msq during SLEEP
	c. Checksume error from BBL
102033	After bootstrap operation of transferring system from sub 1 to 0.
102077	a. END OF TAPE during sys gen.
	b. Successful load from BBL.
102066	Checksum error during sys gen.
102015	Senseswitch 15 on during sys gen.
102001	Follows error message being output to system console – utility routines.
102055	a. Invalid address encountered during system generation.
	b. Illegal address when using BBL.

Table T-9. 2000E System Halts (continued)

Note: A-register status determines type of disc error.

Bits	Status	Bits	Status
0	Any error	7	Not used
1	Data error	8	Seek check
2	Drive busy	9	Not used
3	Flagged cylinder	10	Data protect
4	Address error	11	Drive unsafe
5	End of cylinder	12	Not used
6	Not Ready	13	Overrun
		14	First status

I/O CONFIGURATION:

MAIN PROCESSOR

Select Code	Required	Interface
10 & 11	*	Processor Interconnect
12	*	System Console (2762/2754)
13	*	Paper Tape Reader (2748)
14	*	TBG (12539C)
15	*	First Disc Controller
		a. if 7900/2883 use 15 and 16 b. if 7905 use 15 only
16	(see Note 1)	Second Disc Controller
17/20		Mag Tape Controller

I/O PROCESSOR

Select Code assignments depend on USER configuration.

Suggested Configuration:

Select Code	Note	Interface
10 & 11	2	Processor Interconnect
12		TBG
13, 14, 15	3	MUX
16 -	up to 7 each	Line Printer/Card Rdr./Punch

Note 1: Select Code 16 through 27 can be used by disc controllers (provided the number of disc-drives does not exceed 8) and mag tape controller. There must be no open I/O channels between the controllers.

Note 2. If a Synchronous Modem interface is to be used it should receive a high priority, can take 10 & 11 and push other devices down by 2 S.C.

Note 3: If 2 sets of multiplexers are used, 6 contiguous select codes must be used.

I/O DEVICE SUPPORTED ON 2000 ACCESS

User Terminals

1. HP 2640A Interactive Display Terminal

2. HP 2762A/B Teleprinter Terminal

3. HP 2749B Teleprinter Terminal

4. HP 2600A Keyboard-Display Terminal

General Electric TermiNet 300 Data Communications Terminal, Model B, with Paper Tape Reader/Punch (10/15/30 characters per second)

General Electric TermiNet 1200 Data Communications Terminal (10/30/120 characters per second)

Note: These terminals must be strapped for "ECHO-PLEX".

Memorex 1240 Communications Terminal (10/15/30 characters per second)

Texas Instruments Silent 700 KSR Electronic Data Terminal

Execuport 300 Data Communications Transceiver Terminal

ASR 37 Teleprinter Terminal with Paper Tape Reader/Punch

Note: If this terminal is equipped with the Shift Out (SO) feature, SO must be disabled because the HP 2000 Access system does not permit use of this feature.

IBM 2741 Communication Terminal

Note: This terminal should be connected to the computer over telephone lines. In addition, it must be equipped with the following features:

- Interrupt, Receive (IBM #4708) and Transmit (IBM #7900) associated with the terminal's ATTN key.
- Dial-up (IBM #3255) to enable system connection through a 103A type modem or acoustic coupler.

I/O DEVICES SUPPORTED ON 2000 ACCESS (Cont.)

Line Printers	Card Readers	Paper Tape Punch
1. HP 2607A	1. HP 2892A	1. HP 2753B
2. HP 2610A	2. HP 7261	2. HP 2895A
3. HP 2613A	Synchronous Modem	Mag Tape
4. HP 2614A	HP 12618A	
5. HP 2617A		1. 7970 8 7 TRK (1 each)
6. HP 2618A		2. 7970 B/E 9 TRK (4 each)
7. HP 2767A		
8. HP 2778A		

SYSTEM RECOVERY (REFERENCE SECTION V OPERATOR'S MANUAL)

Self Recovery

System will attempt to recover if a disc addressing problem occurs, System will report to the operator.

"EMERGENCY SLEEP. MOUNT REEL NUMBER 1. PRESS RETURN"

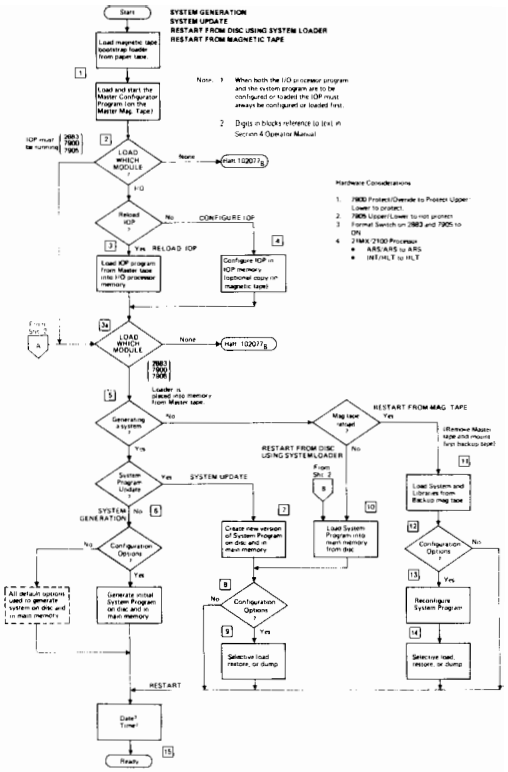
- If sleep is impossible, system reports "EMERGENCY SLEEP ABORTED"
- If sleep is possible and completed, system reports. "DONE, SYSTEM SHUT DOWN"

Action = > Reload System from mag tape. Use RESTORE command to load emergency sleep tape.

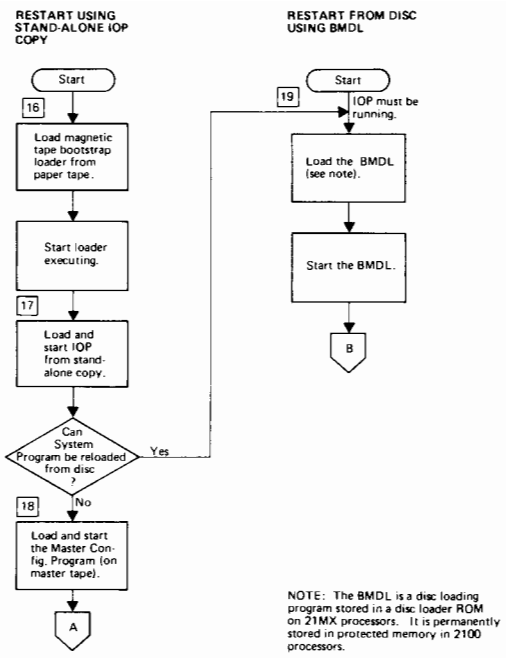
COLD DUMP

Fill Out Cold Dump Sheet!

1. Halt Main Processor (if Halted record HLT number)
2. Halt I/O Processor (if Halted record HLT number)
3. Mount Mag Tape
   a) Write ring installed
   b) Unit 0
4. IOP to 2000, Run
5. Main to 77000, Run
6. Successful HLT 102077
7. Other HLT's
   a) 102033 Write not enabled
   b) 102044 Mag tape off line
   c) 102022 disc 0 does not respond
   d) 102055 Mag tape bad or too short.



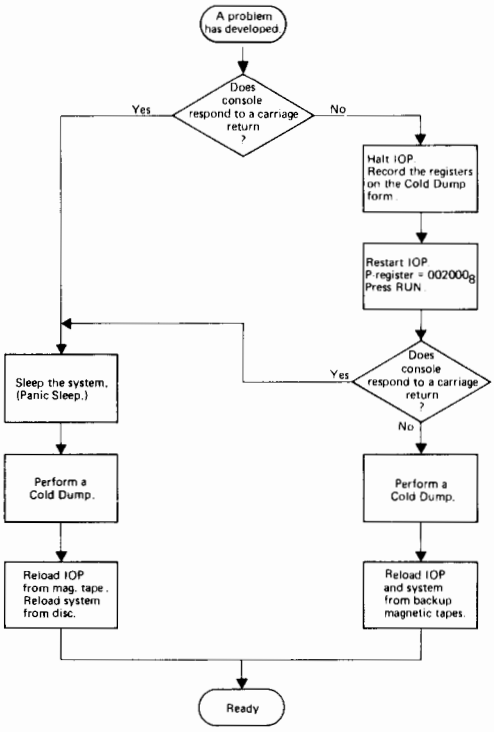
Operating Procedures Overview, Flow Diagram (Sheet 1 of 2)



Operating Procedures Overview, Flow Diagram (Sheet 2 of 2)

PANIC SLEEP

Always Used in Conjunction With a Cold Dump.



Troubleshooting Procedures Flow Diagram

IOP MEMORY SIZE GUIDELINES

	Words			Total Words
*Fixed Overhead:	12,300	☐		12,300
+16 Addt'l Ports:	2,500	☐		____
+2741 Terminal Support:	700	☐		____
+One or More Peripheral(s) And/Or Sync. Interface:	1,500	☐		____
+Card Reader(s):	1,000	☐		____
+Per Card Reader:	200 X	___	QTY =	____
+Line Printer(s)	700	☐		____
+Per Line Printer:	200 X	___	QTY =	____
+P.T. Punch(es):	700	☐		____
+Per Punch:	200 X	___	QTY =	____
+IBM Sync. Comm:	9,000	☐		____
		or		
+CDC Sync. Comm:	8,000	☐		____
	** Approximate Total Memory Req'd			____

*Fixed overhead for a 16 port system; no peripherals; no 2741 terminals; no RJE.

**All figures shown are for configuration default size buffers.

Note: Mag tapes and paper tape reader do not require comm. processor memory.

TEST

MICRO CIRCUIT INTERFACE CARD

MEM LOC	CONTENT	
2 WORD —	102100	- INT. ON WORD
3	060038	- LDA ANY WORD
4	102325	- SFS 25
5	024004	- JMP *-1
6	102625	- OTA-25
7	103725	- STC 25, C
10	NOP	NOP
11	024010	JMP *-1
25	014100	JSB 100
35 ANY WORD		
NOP	100	NOP
101	102525	LIA 25
102	102601	OTA-SW REG
103	124100	JMP 100, I

PROCEEDURE FOR 2100 LONG DIAG.

1. DOWN LOAD BBL FROM MASTER
   - A- SET P= 077700
   - B — S= 75
   - C — PP RUN
   - D - HLT 77

2. LOAD TAPE INTO RDR
   - A - SET P= 75700
   - B S = CLR
   - C PP##, RUN
   - D HLT 77
   - E P= 100
   - F S= SC of TBR=34 0-5
   - G. S= " " TTY=33 6-11
   - H. PP RUN

3. 2100 DIAG STAND ALONE
   - A. LOAD DIAG Config. (24296-60001) INTO RDR
   - B.

2100A LONG DIAG

LONG DIAGNOSTIC 2100A

1 TAPE

P=075700
S=0
PRESET, PRESET, RUN
HLT, 77
P=100
S=0-5 SC of TPR = 34
S=6-11 " " TTY = 33
PRESET, PRESET, RUN
BITS 14-15 = # of PASSES
00 = 1 PASS
01 = 10 PASS
10 = 100 PASS
11 = 65K PASS
BIT 12 = skips, MRG, ASG, SRG, MEM PRT.
13 = RESERVED

2 TAPE

INSERT TAPE
S=REG = 2100 - BIT 3, 4, 21MX NONE Req.
RUN

2100A LONG DIAG

3 TAPE

INSERT TAPE S-REG 1-3-4
RUN
HALT - 10700
SREG = ENTER OPTION IO SC
RUN
SREG = ENTER OPTION IO SC 10-34
END S REG. CIR
RUN

RESTART - 077677 - NEXT DIAG.

077676 - CURRENT DIAG