PRELIMINARY INFORMATION

FOR

8–BIT DUPLEX REGISTER

MODEL 15166A

STANDARD and OPTIONS 01 through 06

This manual contains service information for instruments with the serial number prefix

958

For supplementary information pertaining to instruments with higher prefix numbers, refer to the manual for those instruments.

15166–90001

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SECTION I

INTRODUCTION AND DESCRIPTION

1–1 INTRODUCTION

1–2 The Model 15166A 8–Bit Duplex Register Interface Kit provides a general purpose interface between Hewlett-Packard computers and an external device for 8–bit input or output operations. The kit is specially designed for use with specified tape-punch and teletype units (see Options Specifications below). The Interface Kit is available in either positive or negative versions and with various cables for interfacing to specific devices. The standard version and available options are described in paragraphs 1–3 through 1–15.

1–3 Standard Kit configuration for the Hewlett-Packard 15166A 8–Bit Duplex Register is given as follows:

a. 8–Bit Duplex Register Interface Card, Hewlett-Packard Part Number 15166–66501 (Positive-In/Positive-Out).

b. Connector Kit, 48–pin, Hewlett-Packard Part Number 02166–6178.

c. Connector Kit, 24–pin, Hewlett-Packard Part Number 1251–0332.

d. 8–Bit Duplex Register Test Binary Tape (Duplex Register Diagnostic).

e. The standard Duplex Register Interface Card contains the following jumpers, W4, W6, W8, W10, and W1 and W2 connected in the A position, and W14 through W21 in circuit.

1–4 Option 01

1–5 Option 01 of the 15166A is identical to the standard kit except that a Negative-In/Negative-Out Interface Card (Part Number 15166–66502) replaces the Positive-In/Positive-Out Card.

1–6 Option 02

1–7 Standard Card with jumper W13 included and an interconnecting cable (Part Number 15166–61602) for connection to an HP 2748A Tape Reader and an HP 2758A Reader Re-roller. BCS and SIO Drivers included for 8K memory.

1–8 Option 03

1–9 Standard Card with jumper W13 included and an interconnecting cable (Part Number 15166–61603) for connection to an HP 2753A Tape Punch. BCS and SIO Drivers included for 8K memory.

1–10 Option 04

1–11 Standard Card and an interconnecting cable (Part Number 15166–61601) for connection to an HP 8100A Tape Punch. BCS and SIO Drivers included for 8K memory.

1–12 Option 05

1–13 Same as Option 04, with Interconnecting Cable (Part Number 15166–61601) for connection to a Facit 4070 Tape Punch. BCS and SIO Drivers included for 8K memory.

1–14 Option 06

1–15 Standard Card and an Interconnecting Cable (Part Number 15166–61604) for connection to an Olivetti SV 40 High Speed Printer. BCS and SIO Drivers included for 8K memory.

1–16 Sections II through VI provide installation and programming, theory of operation, and replaceable parts information for the 8–Bit Duplex Register Card. Section VI also contains a description of the Diagnostic Program. Maintenance Information will be provided at a later date.

1–17 DESCRIPTION

1–18 The 8–Bit Duplex Register Card permits bidirectional transfer of data between the HP Computer and the Input/Output (I/O) devices and operates with the I/O Interrupt System. This card contains two eight-bit data storage registers, control and interrupt logic, and provides an Encode Command (action) signal to the I/O device and a Device Flag (action completed) from the I/O device. The 15166A is a single address I/O card and plugs into any of the computer Input/Output slots. The Data Registers operate with bits Ø through 7 of the computer word. The supplied diagnostic test binary tape, used with a 24-pin jumper plug, enables verification of the operation of the interface card without using the external I/O device.

1–19 The Connector Kit contains the connector (and its hood) which mates with the 48-pin side of the 15166A Duplex Register Card. The external device connector and cabling may be supplied by the user.

1–20 SPECIFICATIONS

1–21 Input/Output specifications are outlined in the following Table 1–1.

Table 1–1. 8–Bit Duplex Register Specifications

CHARACTERISTICS	POSITIVE-IN/POSITIVE-OUT HP 15166A–66501	NEGATIVE–IN/NEGATIVE–OUT HP 15166A–66502 OPT. 01
Output Levels		
"1" state	+ 12 V, 2.87K source	– 12 V, 2.87K source
"0" state	0 to + 0.5 V, 12 mA sink max.	0 to + 0.5 V, 12 mA sink max.
Input Levels		
"1" state, "0" state (Bit 5 is negated)	0 to + 0.5 V, 12 mA sink max. + 8 V	– 8 V 0 to + 0.5 V, 12 mA sink max.
Bias and Impedance	+ 8 V through 700 OHMS	– 8 V through 700 OHMS
Current Requirements		
+ 12 V	0.08 A	0.02 A
– 12 V	0.02 A	0.08 A
– 2 V	0.05 A	0.05 A
+ 4.5 V	0.8 A	0.8 A
Encode Output	Command signal to external device. Data ready in output register. Terminated by a Device Flag input.	
Device Flag Input	External device command to interface card. Signal strobes data into input storage register and sets Flag flip-flop on interface card.	
Dimensions		
Width	7–3/4 inches (196.8 mm)	
Height	8–11/16 inches (220.7 mm)	
Weight		
Net	18 ounces (511.3 grms)	
Shipping	4 pounds (2.27 kg)	

SECTION II

INSTALLATION AND PROGRAMMING

2–1 INSTALLATION

2–2 Plug the 8–Bit Duplex Register into the I/O slot assigned for the particular system in use. Run the Duplex Register Diagnostic Program described in Section VI using the 24-pin connector. If the diagnostic is completed without error, the system operates correctly.

2–3 Since the Duplex Register card is designed for use with various external devices, either the supplied cable must be used for the specified external device, or an interconnecting cable must be fabricated for the particular external device being used. Table 2–1 lists the parts which are supplied with the connector kit, and Figure 2–1 shows the connector kit assembly diagram which must be prepared by the user. The 48-pin connector slides onto the end of the Duplex Register card containing the 48 printed circuit paths (24 on each side of the card). As an aid to interconnecting cable fabrication, Table 2–2 lists the signals to and from the external I/O device and their pin assignments. Tables 2–3 through 2–6 list the pin connections to and from the specific external devices listed in the options information for the 15166A. After the cable has been fabricated connect the I/O device to the computer as follows:

a. Turn all power off.

b. Open the computer for access to the Input/Output slots.

c. Pass the cable connector which mates with the Duplex Register Card through the slot at the bottom rear of the computer and up to the front.

d. Slide the connector onto the card and close the computer.

e. Turn all power on.

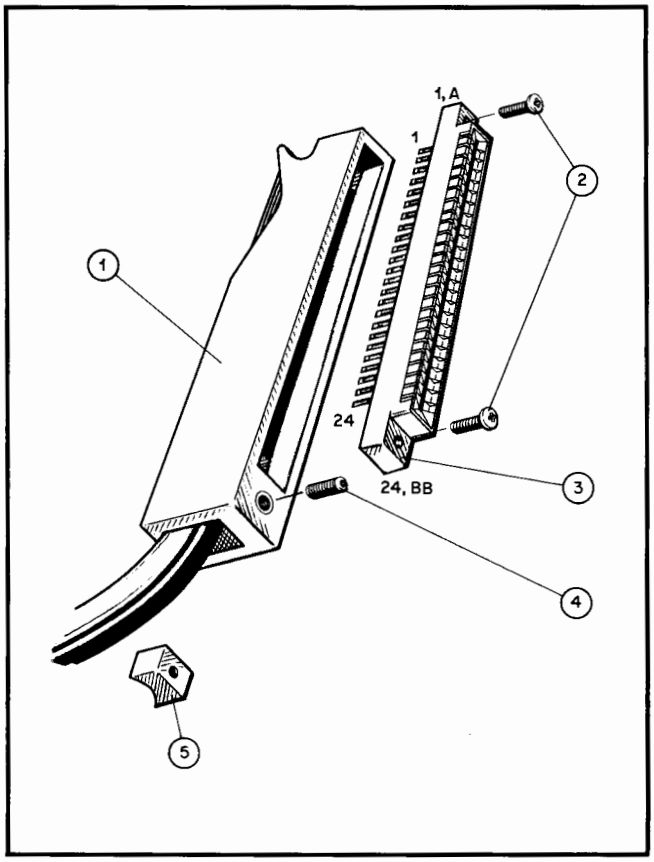


Figure 2–1. Connector Kit Assembly Diagram

Table 2–1. 48-Pin Connector Kit Parts List

ITEM	QTY	DESCRIPTION	PART NO.
1	1	Hood	02116–4001
2	2	Tapping Screw	0624–0096
3	1	Connector, 48–pin	1251–0335
4	1	Set Screw	3030–0143
5	1	Cable Clamp	02116–4003

Table 2–2. Connector Pin Assignments (Standard and Option 01)

TO I/O DEVICE		FROM I/O DEVICE	
PIN	SIGNAL	PIN	SIGNAL
A	Bit Ø	1	Bit Ø
B	Bit 1	2	Bit 1
C	Bit 2	3	Bit 2
D	Bit 3	4	Bit 3
E	Bit 4	5	Bit 4
F	Bit 5	6	Bit 5
H	Bit 6	7	Bit 6
J	Bit 7	8	Bit 7
		21	Status Enable
AA	Device Encode	23	Device Flag
BB	Ground	24	Ground

Table 2–3. 2748A and 2758A Connector Pin Assignments (Option 02)

48-PIN CONNECTOR	READER CONNECTOR	SIGNAL
1	B	Bit 1
2	F	Bit 2
3	L	Bit 3
4	R	Bit 4
5	V	Bit 5
6	Z	Bit 6
7	d	Bit 7
8	j	Bit 8
AA	AA	Read
23	FF	Feed Hole
24, BB	HH	Ground

Table 2–4. 2753A Connector Pin Assignments (Option 03)

48-PIN CONNECTOR	TAPE PUNCH CONNECTOR	SIGNAL
A	B	Bit 1
B	F	Bit 2
C	L	Bit 3
D	R	Bit 4
E	V	Bit 5
F	Z	Bit 6
H	d	Bit 7
J	j	Bit 8
AA	DD	Punch
23	FF	Device Flag
6	AA	Lo Tape
21, 24, BB	HH	Ground

Table 2–5. 8100A and Facit 4070 Connector Pin Assignments (Options 04/05)

48-PIN CONNECTOR	TAPE PUNCH CONNECTOR	SIGNAL
A	1	1
B	2	2
C	3	3
D	4	4
E	5	5
F	6	6
H	7	7
J	8	8
AA	11	Punch
23	12	Device Flag
6	21	Lo Tape
24, BB	25	Ground
	9, 24	

Table 2–6. Olivetti SV 40 Connector Pin Assignment (Option 06)

48-PIN CONNECTOR	TAPE PUNCH CONNECTOR	SIGNAL
A	2	1
B	3	2
C	4	3
D	5	4
E	6	5
F	7	6
H	8	7
AA	9	Print
23	10	Device Flag
6		
24, BB	1	Ground

2–4 PROGRAMMING

2–5 The programs listed in Tables 2–7 through 2–9 are examples of input and output and combined input/output programming through the Duplex Register using Assembler Language. The Duplex Register is assumed to be assigned the select code NTWE.

2–6 Input

2–7 Command the external device to acquire and transfer 8 bits of information to the computer. The results are left in the A–Register. Refer to Table 2–7 for the operation of this program.

2–8 Output

2–9 Output 8 bits of information from the A–Register to the external device and command it to accept the data. Refer to Table 2–8 for the operation of this program.

2–10 Combined Input/Output

2–11 Output 8 bits of command information, command the external device to take action, then read in 8 bits of data from the device. Command data is then retained in the A–Register, and input data is retained in the B–Register. Refer to Table 2–9 for the operation of this program.

2–12 CIRCUIT BOARD JUMPERS

2–13 Table 2–10 lists the wire jumpers present on the 8–Bit Duplex Register card and the required positions for the indicated operations. See Figure 5–1 for the physical positions of the jumpers.

Table 2–7. Input Program

```
MAIN PROGRAM

Label       Operation    Operand
                .
                .
            JSB          INPUT      Jump to input subroutine
            STA          CODE       Store A-Register contents in memory location CODE.
                .
                .
                .
SUBROUTINE
INPUT       NOP                     Entry point
            STC          NTWE, C    Encode external device to perform its function
            SFS          NTWE       Is operation complete?
            JMP          *-1        No, jump back to SFS instruction
            LIA          NTWE       Yes, transfer input data to A-Register
            JMP          INPUT,I    Jump to main program
```

Table 2–8. Output Program

```
MAIN PROGRAM

Label       Operation    Operand
                .
                .
            LDA          N          Load A-Register with contents of memory location N.
            JSB          OUTPT      Jump to output subroutine
                .
                .
                .
SUBROUTINE
OUTPT       NOP                     Entry point
            SFS          NTWE       Is External device busy?
            JMP          *-1        Yes, jump back to SFS instruction
            OTA          NTWE       No. transfer output data to duplex register
            STC          NTWE,C     Encode external device to accept the data
            JMP          OUTPT, I   Jump to main program
```

Table 2–9. Input/Output Program

```
MAIN PROGRAM

Label          Operation      Operand

                  .
                  .
               LDA            N          Load A-Register with contents of memory location N.
               JSB            IOSB       Jump to input/output subroutine
               STB            CODE       Store B-Register contents in memory location CODE
                  .
                  .
                  .
SUBROUTINE
IOSB           NOP                       Entry point
               OTA            NTWE       Transfer data to duplex register
               STC            NTWE, C    Encode external device to accept or act on the data
               SFS            NTWE       Is External device busy?
               JMP            *-1        Yes, jump back to SFS instruction
               LIB            NTWE       No, transfer input data to B-Register
               JMP            IOSB, I    Jump to main program
```

Table 2–10. Jumper Strappings

JUMPER	POSITION	FUNCTION
W1	A	CLEAR COMMAND, – SIGNAL
	B	CLEAR COMMAND, + SIGNAL
W2	A	FLAG, – SIGNAL
	B	FLAG, + SIGNAL
W3		NEGATIVE GOING DEVICE ENCODE SIGNAL (SEE W8)
W4		GATES DATA INTO INPUT REGISTER WHEN THERE IS A DEVICE FLAG SIGNAL
W5	– 12 V	POSITIVE-IN/POSITIVE-OUT
	OPEN	NEGATIVE-IN/NEGATIVE-OUT
W6	– 2 V	POSITIVE-IN/POSITIVE-OUT
	OPEN	NEGATIVE-IN/NEGATIVE-OUT
W7	+ 12 V	POSITIVE-IN/POSITIVE-OUT
	OPEN	NEGATIVE-IN/NEGATIVE-OUT
W8		POSITIVE GOING DEVICE ENCODE SIGNAL (SEE W3)
W9		GATES DATA INTO INPUT REGISTER WITH STF INSTRUCTION
W10	OPEN	POSITIVE-IN/POSITIVE-OUT
	+ 12 V	NEGATIVE-IN/NEGATIVE-OUT
W11	OPEN	POSITIVE-IN/POSITIVE-OUT
	– 12 V	NEGATIVE-IN/NEGATIVE-OUT
W12	OPEN	POSITIVE-IN/POSITIVE-OUT
	– 12 V	NEGATIVE-IN/NEGATIVE-OUT
W13	OPEN	OUTPUT LEVEL "1" STATE = + 12 VOLTS, "0" STATE = 0 VOLTS INPUT LEVEL "1" STATE = "0" VOLTS, "0" STATE = + 12 VOLTS EXCEPT BIT 5 WHICH IS NEGATED
	0 V	OUTPUT LEVELS AND INPUT BIT 5 ARE NEGATED
W14 thru W21	OPEN	ONLY FOR OPTION 01 NEGATIVE-IN/NEGATIVE-OUT CARD
	IN	FOR OPTIONS; STANDARD, AND 02 THRU 06

SECTION III

THEORY OF OPERATION

3–1 GENERAL THEORY OF OPERATION

3–2 Input Operations

3–3 Refer to Figure 3–1 for the simplified logic diagram of the standard (Positive-In/Positive-Out) HP 15166A Interface card and to Figures 5–2 and 5–3 for the complete logic diagram of the interface card. A Set Control, Clear Flag (STC, CLF) instruction initiates the input of 8 bits of data from the I/O device. To enable the interrupt system a Set Flag (STF) instruction with a Select Code of 00 (octal) must be programmed. This sets the Interrupt System Enable flip-flop on the I/O Control Card.

3–4 The STC portion of the STC, CLF instruction sets the Command flip-flop which applies an Encode signal to the device, initiating its input function. The STC portion of the instruction also sets the Control flip-flop which provides an enable signal to the Interrupt Control logic on the 8–Bit Register Card. The CLF portion of the instruction resets the Flag flip-flop to prevent an interrupt signal from being sent to the Computer before the I/O device has transferred data to the Duplex Register Card.

3–5 When the I/O device is ready to transfer data to the Duplex Register Card, it applies a Device Flag signal to the card. This Flag signal enters data into the Input Storage Register and sets up a request for service (Skip Flag, SKF, if interrupt system is not being used, or Interrupt Request, IRQ). At time T2, the Duplex Register Card receives the Enable Flag (ENF) signal from the Computer. This signal and the output from the set-side of the Flag Buffer flip-flop sets the Flag flip-flop. If a device of higher priority has not requested an interrupt, the Flag flip-flop output initiates an interrupt signal to the Computer, indicating that data is available in the Input Storage Register.

3–6 The Computer must now accept the data from the Input Storage flip-flops of the Duplex Register Card by a Load Into A (LIA), Load Into B (LIB), Merge Into A (MIA), or Merge Into B (MIB) instruction before another input operation is initiated. If it is not accepted before another STC, CLF instruction is issued, the data will be lost. The IOI signal to the Duplex Register Card from the Computer, as a result of the LIA, LIB, or MIA, MIB instruction, enables the data of the input "and" gates (bits Ø–7) of the Card to the Computer.

3–7 The set or reset condition of the Flag slip-flop may also be tested with a Skip on Flag Set (SFS) or Skip on Flag Clear (SFC) instruction to determine data availability to the Computer. When using this method, the Interrupt System Enable flip-flop on the I/O Control Card must be reset by a CLF instruction with a Select Code of 00 (octal).

3–8 Output Operations

3–9 Refer to the simplified logic diagram, Figure 3–1. The interrupt system is assumed to be enabled by previously setting the Interrupt System Enable flip-flop on the I/O Control Card with a Set Flag (STF) instruction and a Select Code of 00 (octal). This makes the input pin 8 (IEN) go true.

3–10 An Output from A (OTA) or an Output from B (OTB) instruction must be issued by the Computer program to output 8 data bits (Ø–7) from the A or B Register of the Computer to the Duplex Register Card and then to the I/O device. The IOO signal to the card, as a result of the OTA/B instruction, sets the Output Storage Register flip-flops. This transfers the data from the Computer into the Storage Register on the Duplex Register Card and makes the data available to the I/O device at a logical level according to the setting of jumper W13 (see Table 2–10).

3–11 An STC, CLF instruction must then be issued by the Computer program. The STC portion of the instruction sets the Command flip-flop on the Register Card which applies a Device Encode signal to the I/O device, indicating that output data is available. The STC portion of the instruction also sets the Control flip-flop which provides an enable signal to the Interrupt Control logic on the Duplex Register Card. The CLF portion of the instruction resets the Flag and Flag Buffer flip-flops to prevent an interrupt signal from being sent to the Computer before the I/O device has accepted data and performed its operations. A CLF instruction is not necessary if no response is required back from the external device.

3–12 The device must now respond with a Device Flag signal to tell the Computer that the I/O device is ready for additional data. At time T2, the Duplex Register Card receives the ENF signal from the Computer. The ENF signal and the output from the set-side of the Flag Buffer flip-flop sets the Flag flip-flop. If a device of higher priority has not requested an interrupt, the Flag Flip-flop initiates an inter rupt signal to the Computer.

3–13 To output additional data, the Computer must transfer the new data to the Duplex Register Card before issuing another STC, CLF instruction. If the STC, CLF instruction precedes the output of new data, erroneous data may be received by the I/O device.

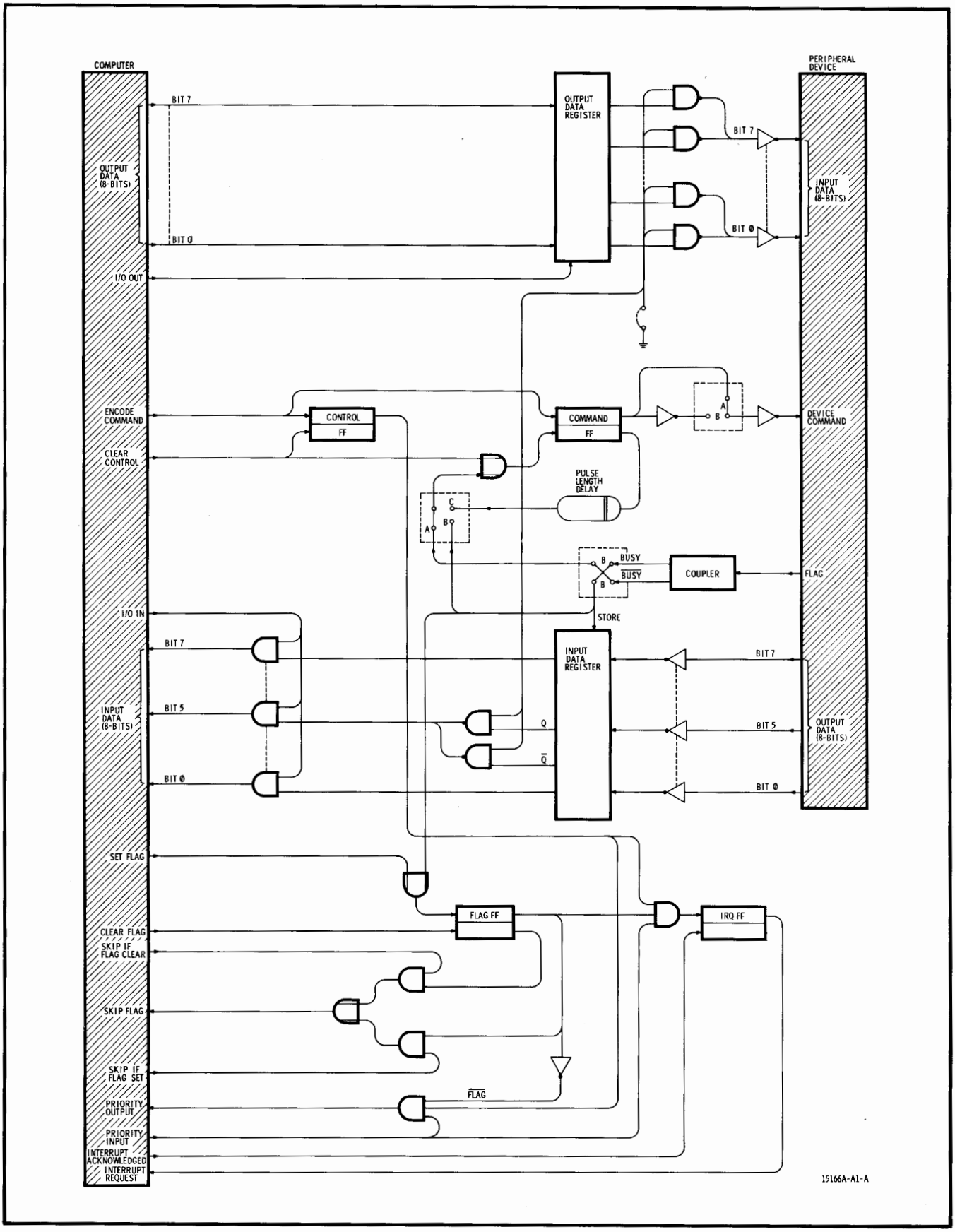


Figure 3–1. Simplified Block Diagram for 15166A Interface Card

3–14 The set or reset condition of the Flag flip-flop may also be tested with an SFS or an SFC instruction to determine the readiness of the I/O device to accept data from the Computer. When using this method, the Interrupt System Enable flip-flop on the I/O Control Card must be reset by a CLF instruction with a Select Code of 00 (octal).

3–15 DETAILED THEORY OF OPERATION

3–16 General

3–17 Figures 5–2 and 5–3 depict the logic diagrams for the standard positive-in/positive-out 8–Bit Duplex Register Card. For lead-wire connections between the interface card and applicable I/O device, refer to Figures 5–2 and 5–3 and to Table 2–1. Figure 5–1 depicts the parts location diagram for the card.

3–18 Logic diagram reference designations preceded by MC are identified by part number in Section IV, and the logic diagram for each Microcircuit Package is shown in Figure A–1.

3–19 Computer Power On

3–20 When power is initially applied by the POWER switch, on the front panel of the Computer, the POPIO and CRS signals are received simultaneously by the interface card from the Computer. These signals establish initial conditions for operation of the interface card. The POPIO signal sets the Flag Buffer flip-flop through "nand" gate MC27C (the input to the flip-flop is inverted). At time T2, the ENF signal from the I/O Control card enables "nand" gate MC57C resetting the IRQ flip-flop. The output of gate MC57C is also transferred through "nand" gate MC57D and with the output of the Flag Buffer flip-flops sets the Flag flip-flop. The POPIO signal is also transferred through "nand" gate MC66A strobing the Output Storage Register. The IOBO Ø through 7 lines are at logic 0, therefore the register is set to logic 0. This means that the Output Storage Register is at logic 0 after Power turn-on. The Control Reset (CRS) signal is received at pin 13 and inverted by "nand" gate MC37B. The output from this gate resets the Control and Command flip-flops.

3–21 Flag and Control Logic

3–22 A programmed STC instruction with the Select Code of the 8–Bit Duplex Register Card initiates the output operation. This provides STC, LSCL, LSCM, and IOG signals to the Duplex Register Card. The STC signal is applied as one true input to "nand" gate MC37C. The LSCL, LSCM, and IOG signals are applied to "nand" gate MC36D, transferred through "nand" gate MC56A providing the second true input to gate MC37C. The false output of gate MC37C sets the Control and Command flip-flops. The set-side output of the Control flip-flop is applied as one true input to "nand" gate MC15A. The other inputs to this gate are the true IEN signal (generated by the set Interrupt System Enable flip-flop on the I/O Control Card) and the true output of the set-side of the Flag flip-flop. The output of "nand" gate MC15A is applied to "nand" gate MC25C and "and" gate MC47A. Gate MC47A will have a true output after the Flag flip-flop is reset and a device of higher priority has not requested an interrupt. Gate MC35A will have a false output at time T5 (SIR), when a device of higher priority has not requested an interrupt (PRH true), the Flag flip-flop is set (true), and the Flag Buffer flip-flop is set (true). The output of "nand" gate MC35A is inverted setting the Interrupt Request flip-flop (IRQ). This flip-flop is reset at the next time T2 (ENF) to prevent further interrupts from this board. The set-side output of the IRQ flip-flop provides the FLGL (lower priority flag) and the IRQL (lower priority interrupt request) signals to the HP Computer. The Interrupt Acknowledge (IAK) signal from the I/O Control Card and the set-side output of the IRQ flip-flop is applied to "nand" gate MC17D. The output of this "nand" gate or the output of "nand" gate MC37A resets the Flag Buffer flip-flop to prevent further interrupt requests.

3–23 Device Command

3–24 The true set-side output of the Command flip-flop may be transferred through jumper W3 which puts a positive voltage on the base of transistor Q17. This turns Q17 on which transfers a negative going Device Encode signal to pin AA of the 48-pin connector. To change the negative going Device Encode signal to a positive-going Device signal, disconnect jumper W3 and connect jumper W8. This transfers the true set-side output of the Command flip-flop to the input of "nand" gate MC46A. The false output of this gate is transferred through jumper W8 which puts a negative potential, developed across resistor R117, on the base of transistor Q17. This turns Q17 off which transfers a positive going Device Encode signal to pin AA of the 48-pin connector. The Command flip-flop is cleared by the Device Flag signal through "nand" gate MC86A, or by a CLC instruction or by a CRS signal.

3–25 Device Flag

3–26 The Device Flag signal is received from the I/O device, at pin 23, and responds to either a positive going or a negative going signal. Jumper W1 sets up the condition that sets the Flag Buffer flip-flop. Jumper W2 also allows data to be strobed, through jumper W4, to the Input Storage Register. Figure 3–2 depicts the timing diagram for the Device Flag circuit.

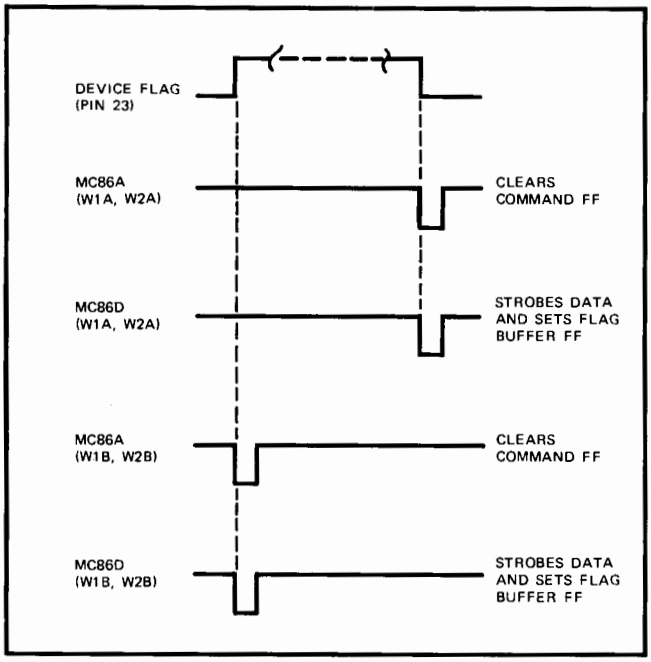


Figure 3–2. Device Flag Timing Diagram

3–27 DEVICE FLAG POSITIVE BOARD. When a negative going (positive voltage to ground) Device Flag signal is received at pin 23, transistor Q18 is turned off. A positive output from the collector of Q18 is applied to "nand" gate MC105A. The output from MC105A (ground) is transferred through the delay network consisting of R26, R27 and C19 to "nand" gate MC105C. This causes the output of MC105C to go positive and the output of MC105D to go to ground. This ground signal is transferred through speed-up resistor R28 and applied to MC105C. This Schmitt Trigger action helps speed up the signal applied at MC105D. The ground output from MC105D is transferred to the B position of jumpers W1 and W2 and also inverted by "nand" gate MC105B and applied to the A position of jumpers W1 and W2. Therefore, for a negative going Device Flag signal, position A of jumper W1 clears the Command flip-flop and position A of jumper W2 sets the Flag Buffer flip-flop and strobes data into the Input Storage Register.

3–28 The two pulse generator circuits MC86B and MC86A, MC86C, and MC86D respond only to a signal which is at ground and goes positive. Capacitor C20 and resistor R30 or capacitor C21 and resistor R31 determine the pulse width of the output pulse which is approximately 300 nanoseconds. Therefore, for a negative going input Device Flag signal (+ voltage to ground) jumper W1 and W2 must be in A position. When the signal is transferred through W1A the Command flip-flop is cleared and when the signal is transferred through W2A, the Flag Buffer flip-flop is set and data is strobed into the Input Storage Register through jumper W4.

3–29 When a positive going (ground to positive voltage) Device Flag signal is received at pin 23, transistor Q18 is turned on. A negative output from the collector of Q18 is applied to "nand" gate MC105A. The output from MC105A (positive) is transferred through the Delay network consisting of R26, R27 and C19 to "nand" gate MC105C. This causes a ground output from MC105C and the output from MC105D to go positive. This positive signal is transferred through speed-up resistor R28 and applied to MC105C. This Schmitt Trigger action helps to speed up the signal applied at MC105D. The positive output from MC105D is transferred to the B position of jumpers W1 and W2, and also inverted by "nand" gate MC105B and applied to the A position of W1 and W2 as a ground output. Therefore, for a positive going Device Flag signal, position B of jumper W1 clears the Command flip-flop and position B of jumper W2 sets the Flag Buffer flip-flop and strobes data into the Input Storage Register.

3–30 Jumpers W1 and W2 do not have to be set for the same polarity signal. These jumpers may be set in either position. Example: An input Device Flag signal (pin 23) can clear the Command flip-flop on the positive edge and on the negative edge set the Flag Buffer flip-flop and strobe the input data into the Input Storage Register.

3–31 DEVICE FLAG NEGATIVE BOARD. With negative going Device Flag signal (ground to negative) applied at pin 23, the output of "nand" gates MC105A and MC105D go to ground and jumpers W1A and W2A should be used. With a positive going Device Flag signal (negative to ground) applied at pin 23, the output of "nand" gates MC105A and MC105B go positive and jumpers W1B and W2B should be used.

3–32 The Status Enable Line, pin 21, enables the user to input data to the card without gating it from a Device Flag signal. A ground is required on pin 21 to enable the Input Storage Register.

3–33 Positive-In/Positive-Out Storage Registers

3–34 OUTPUT REGISTER. Output logic levels to the external I/O device are as follows in the standard version without W13 in the circuit: Logic "1" = + voltage, Logic "0" = ground.

3–35 When IOBO signals are transferred from the Computer (via backplane wiring) to the Output Storage Register, - 0.5 volts (logic 0) or + 2.5 volts (logic 1) is received at the input to the storage register. Since all IOBO circuits are identical, only IOBO Ø will be explained.

3–36 A logic 1 from the Computer, received through connector pin 35, will set the Bit Ø flip-flop, MC44A when IOO + POPIO signal is transferred from the Computer to pin 4 of MC44A. This latches the data into the flip-flop

where the positive voltage (logic 1) is output on pin 16 of the Bit Ø flip-flop. This positive voltage is transferred to the base of transistor Q9, through MC24A/C, turning the transistor off. With transistor Q9 in the off-state, a logic 0 is transferred to the I/O device through pin A of the 48-pin connector as a positive voltage.

3–37 A logic 0 from the Computer, received through connector pin 35, resets the Bit 0 flip-flop MC44A during IOO. The Bit Ø flip-flop is latched when IOO goes false. The set-side output of this flip-flop is at ground and is applied to the base of transistor Q9, through MC24A/C, turning the transistor on, and data (ground) is transferred to the I/O device through pin A of the 48-pin connector. This signal is capable of sinking 12 milli-amperes from an external positive source.

3–38 INPUT REGISTER. Input logic levels from the external I/O device are as follows in the standard version without jumper W13 in circuit:

Logic "1" = ground; Logic "0" = + voltage,

EXCEPT Bit 5 which has logic levels as follows:

Logic "1" = + voltage; Logic "0" = ground.

3–39 When Bit Ø through Bit 7 signals are transferred from the I/O device to the Input Storage Register, a ground potential (external transistor on) or positive voltage (external transistor off) is received at the input to the register. Since the Bit Ø through Bit 7 circuits are identical, only Bit Ø will be explained.

3–40 A ground potential capable of sinking at least 12 milliamperes is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 is cut off which applies a positive voltage to pin 2 of the Bit Ø flip-flop MC14A. A Device Flag signal is transferred from the I/O device through the Device Flag circuit, jumper W4 and "nand" gate MC66B to pin 4 of MC14A. This strobes the data through the flip-flop where the positive voltage output at pin 16 is transferred as one true input to pin 14 of "and" gate MC45A. The other true signal is the IOI · [LSCM · LSCL · IOG] signal. This enables "and" gate MC45A, and data (positive voltage) is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBIØ signal (logic 1).

3–41 A positive voltage or open circuit is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 conducts which applies a ground potential to pin 2 of the Bit Ø flip-flop MC14A. When the Device Flag signal occurs, data is stored. Therefore, the set-side output of MC14A is at a ground level which is transferred to pin 14 of "and" gate MC45A. With this false input to "and" gate MC45A, the output (pin 13) is also ground which is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBIØ signal (logic 0).

3–42 Negative-In/Negative-Out Storage Registers

3–43 OUTPUT REGISTER. Output logic levels to the external I/O device are as follows in the Option 01 card without jumper W13 in circuit:

Logic "1" = ground; Logic "0" = - voltage.

3–44 When IOBO signals are transferred from the Computer (via backplane wiring) to the Output Storage Register, - 0.5 volts (logic 0) or + 2.5 volts (logic 1) is received at the input to the storage register. Since all IOBO circuits are identical, only IOBOØ will be explained.

3–45 A logic 1 from the Computer, received through connector pin 35, will set the Bit Ø flip-flop MC44A, when IOO + POPIO signal is input, from the Computer to pin 4 of MC44A. This latches the data into the flip-flop, and the positive voltage (logic 1) is output on pin 16 of the Bit Ø flip-flop. This positive voltage is transferred to the base of transistor Q9, through MC24A/C, turning the transistor on. With transistor Q9 in the on-state, a ground potential is transferred to the I/O device, through pin A of the 48-pin connector. This signal is capable of sinking 12 milli-amperes from an external negative source.

3–46 A logic 0 from the Computer, received through connector pin 35, resets the Bit Ø flip-flop MC44A during IOO. The Bit Ø flip-flop is latched when IOO goes false. The set-side output of this flip-flop is at ground and is applied to the base of transistor Q9 through MC24A/C, turning the transistor off. With Q9 in the off-state, a negative voltage is transferred to the I/O device through pin A of the 48-pin connector.

3–47 INPUT REGISTER. Input logic levels from the external I/O device are as follows in the Option 01 card without jumper W13 in circuit:

Logic "1" = - voltage; Logic "0" = ground.

EXCEPT Bit 5 which has logic levels as follows:

Logic "1" = ground; Logic "0" = - voltage.

3–48 When Bit Ø through Bit 7 signals are transferred from the I/O device to the Input Storage Register, a ground potential (external transistor on) or negative voltage (external transistor off) is received at the input to the register. Since the Bit Ø through Bit 7 circuits are identical, only Bit Ø will be explained.

3–49 A negative voltage or open circuit is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 is cut off which applies a logic 1 (positive voltage) to pin 2 of the Bit Ø flip-flop MC14A. A Device Flag signal is input from the I/O device through the Device Flag circuit jumper W4 and "nand" gate MC66B to pin 4 of MC14A. This strobes the data through the flip-flop where a positive potential is output on pin 16 and transferred to pin 14 of

"and" gate MC45A. The other true signal is the IOI · [LSCM · LSCL · IOG] signal. This enables "and" gate MC45A, and data (logic 1) is transferred to the Computer through pin 26 of the 86-pin connector, as an IOBIØ signal (logic 1).

3–50 A ground potential capable of sinking at least 12 milliamperes is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 conducts, which applies a ground potential to pin 2 of the Bit Ø flip-flop MC14A. Therefore, the set-side of MC14A is at a false level, which is transferred to pin 14 of "and" gate MC45A. When the Device Flag signal occurs, data is stored. With this false input to "and" gate MC45A, the output (pin 13) is also at a ground potential which is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBIØ signal (logic 0).

3–51 With jumper W13 in position in the circuit, all data bits (Ø through 7) transferred to the I/O Device from the computer are negated before transfer. The negation is achieved by gates MC24, 34, 54, and 74, and control of these gates is achieved by jumper W13 through MC93A and MC93B.

3–52 Jumper W13 also causes the negation of bit 5 transferred to the computer from the I/O Device. Bit 5 is negated through gates MC93C and MC93D, and control of this negation is achieved through the jumper W13 and gates MC93A and MC93B.

SECTION IV

REPLACEABLE PARTS

4–1 INTRODUCTION

4–2 This section contains information for ordering replacement parts for the 15166A Interface Card. Refer to Table 4–1 for a list of replaceable parts in alpha-numerical order of their reference designations, with a description and HP part number for each part.

4–3 ORDERING INFORMATION

4–4 To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the rear of this manual for field-office addresses.

4–5 Specify the following information for each part when ordering:

a. Hewlett-Packard part number.

b. Circuit reference designation

c. Description.

4–6 To order a part not listed in Table 4–1, give a complete description of the part and include its function and location.

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	P	= plug	V	= vacuum tube, neon bulb, photocell, etc.
B	= motor	FL	= filter	Q	= transistor		
BT	= battery	HR	= heater	R	= resistor	VR	= voltage regulator
C	= capacitor	J	= jack	RT	= thermistor	W	= cable
CP	= coupler	K	= relay	S	= switch	X	= socket
CR	= diode	L	= inductor	T	= transformer	Y	= crystal
DL	= delay line	M	= meter	TB	= terminal board		
DS	= lamp	MC	= micro-circuit	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	NPN	= negative-positive-negative	S-B	= slow-blow
AFC	= automatic frequency control	HEX	= hexagonal	NRFR	= not recommended for field replacement	SCHEM.	= schematic
AGC	= automatic gain control	Hg	= mercury	NSR	= not separately replaceable	Se	= selenium
BFO	= beat frequency oscillator					SECT	= section(s)
BeCu	= beryllium copper	IF	= intermediate freq.			SEMICON	= semiconductor
BH	= binder head	IMPG	= impregnated			Si	= silicon
BP	= bandpass	INCD	= incandescent	OBD	= order by description	SIL	= silver
BRS	= brass	INCL	= include(s)	OH	= oval head	SL	= slide
BWO	= backward wave oscillator	INS	= insulation(ed)	OX	= oxide	SPG	= spring
		INT	= internal			SPL	= special
ccw	= counter-clockwise			P	= peak	SST	= stainless steel
CER	= ceramic	k	= kilo = 10^3	PC	= printed circuit	SR	= split ring
CMO	= cabinet mount only			pF	= picofarads = 10^{-12} farads	STL	= steel
COEF	= coefficient	LH	= left hand			Ta	= tantalum
COM	= common	LIN	= linear taper	PH BRZ	= phosphor bronze	TD	= time delay
COMP	= composition	LK WASH	= lock washer	PHL	= Philips	TGL	= toggle
COMPL	= complete	LOG	= logarithmic taper	PIV	= peak inverse voltage	THD	= thread
CONN	= connector	LPF	= low pass filter	PNP	= positive-negative-positive	Ti	= titanium
CP	= cadmium plate					TOL	= tolerance
CRT	= cathode-ray tube	m	= milli = 10^{-3}	P/O	= part of	TQ	= total quantity
cw	= clockwise	M	= meg = 10^6	POLY	= polystyrene	TRIM	= trimmer
		MET FLM	= metal film	PORC	= porcelain	TWT	= traveling wave tube
DEPC	= deposited carbon	MET OX	= metallic oxide	POS	= position(s)		
DR	= drive	MFR	= manufacturer	POT	= potentiometer	VAR	= variable
		MINAT	= miniature	PP	= peak-to-peak	VDCW	= dc working volts
ELECT	= electrolytic	MOM	= momentary	PT	= point		
ENCAP	= encapsulated	MTG	= mounting	PWV	= peak working voltage		
EXT	= external	MY	= "mylar"			W	= watts
				RECT	= rectifier	WIV	= working inverse voltage
F	= farads	n	= nano (10^{-9})	RF	= radio frequency		
FH	= flat head	N/C	= normally closed	RH	= round head or right hand	WW	= wirewound
FIL H	= fillister head	Ne	= neon			W/O	= without
FXD	= fixed	Ni PL	= nickel plate	RMO	= rack mount only	μ	= micro = 10^{-6}
		N/O	= normally open	RMS	= root-mean square	*	= optimum value selected at factory, average value shown (part may be omitted)
		NPO	= negative positive zero (zero temperature coefficient)	RS	= recommended spares		
Ge	= germanium			RWV	= reverse working voltage		
GRD	= ground(ed)						

Table 4–1. Reference Designation Index

REFERENCE DESIGNATION	STOCK NO.	DESCRIPTION
	15166–26501	BOARD: BLANK PC
C1 thru C8	0140–0198	C FXD MICA 200 PF 5% 300VDCW
C9 thru C16	0140–0191	C FXD MICA 56 PF 5% 300VDCW
C17	0140–0192	C FXD MICA 68 PF 5% 300VDCW
C18	0140–0198	C FXD MICA 200 PF 5% 300VDCW
C19	0160–0153	C FXD MYLAR 1000PF 10% 200VDCW
C20 and C21	0160–0154	C FXD MYLAR 2200 PF 10% 200VDCW
C22	0160–0153	C FXD MYLAR 1000 PF 10% 200VDCW
C23 thru C33	0180–0197	C FXD TA ELECT 2.2 UF 10% 20VDCW
CR1 thru CR8		NOT ASSIGNED
CR9 thru CR17 *	1901–0040	DIODE SILICON 30PIV 30 MA
MC14	1820–0301	INTEGRATED CIR QUAD LATCH BUFFER STORAGE
MC15	1820–0068	INTEGRATED CIR TRIPLE 3 INPUT NAND GATE
MC16	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC17	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC24	1820–0327	INTEGRATED CIR QUAD 2 INPUT OPEN COLLECTOR
MC25	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC26	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC27	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC34	1820–0327	INTEGRATED CIR QUAD 2 INPUT OPEN COLLECTOR
MC35	1820–0069	INTEGRATED CIR DUAL 4 INPUT NAND GATE
MC36	1820–0068	INTEGRATED CIR TRIPLE 3 INPUT NAND GATE
MC37	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC44	1820–0301	INTEGRATED CIR QUAD LATCH BUFFER STORAGE
MC45	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC46	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC47	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC54	1820–0327	INTEGRATED CIR QUAD 2 INPUT NAND OPEN COLLECTOR
MC55	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC56	1820–0071	INTEGRATED CIR DUAL 4 INPUT NAND BUFFER
MC57	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC64	1820–0301	INTEGRATED CIR QUAD LATCH BUFFER STORAGE
MC65	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC66	1820–0071	INTEGRATED CIR DUAL 4 INPUT NAND BUFFER

See introduction to this section for abbreviation details

Table 4–1. Reference Designation Index (cont'd)

REFERENCE DESIGNATION	STOCK NO.	DESCRIPTION
MC74	1820–0327	INTEGRATED CIR QUAD 2 INPUT NAND OPEN COLLECTOR
MC75	1820–0956	INTEGRATED CIR DUAL 2 INPUT BUFFER
MC84	1820–0301	INTEGRATED CIR QUAD LATCH BUFFER STORAGE
MC86	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
MC93	1820–0327	INTEGRATED CIR QUAD 2 INPUT NAND OPEN COLLECTOR
MC105	1820–0054	INTEGRATED CIR QUAD 2 INPUT NAND GATE
Q1 thru Q8	1854–0307	TRANSISTOR SI NPN
Q9 thru Q17	1854–0307	TRANSISTOR SI NPN
Q9 thru Q17 **	1853–0036	TRANSISTOR SI PNP
Q18	1854–0307	TRANSISTOR SI NPN
R1 thru R8	0757–0417	R FXD MET FLM 562 OHM 1% 1/8W
R9 thru R17	0698–3151	R FXD MET FLM 2870 OHM 1% 1/8W
R18	0757–0417	R FXD MET FLM 562 OHM 1% 1/8W
R19	0698–3445	R FXD MET FLM 348 OHM 1% 1/8W
R20	0698–3440	R FXD MET FLM 196 OHM 1% 1/8W
R21	0698–0082	R FXD MET FLM 464 OHM 1% 1/8W
R22	0698–3445	R FXD MET FLM 348 OHM 1% 1/8W
R23	0698–3445	R FXD MET FLM 348 OHM 1% 1/8W
R24	0757–0280	R FXD MET FLM 1000 OHM 1% 1/8W
R25	0757–0280	R FXD MET FLM 1000 OHM 1% 1/8W
R26 and R27	0757–0401	R FXD MET FLM 100 OHM 1% 1/8W
R28	0757–0280	R FXD MET FLM 1000 OHM 1% 1/8W
R29	0757–1094	R FXD MET FLM 1470 OHM 1% 1/8W
R30 and R31	0698–3440	R FXD MET FLM 196 OHM 1% 1/8W
R32	0698–3445	R FXD MET FLM 348 OHM 1% 1/8W
R33 thru R36	0698–0084	R FXD MET FLM 2150 OHM 1% 1/8W
R37 thru R100		NOT ASSIGNED
R101	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R101 ***	1810–0022	RESISTOR NETWORK MET FLM (4.3K 1.8K 1K X2)
R102		NOT ASSIGNED
R103	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R103 ***	1810–0022	RESISTOR NETWORK MET FLM (4.3K 1.8K 1K X2)
R104		NOT ASSIGNED

See introduction to this section for abbreviation details

Table 4–1. Reference Designation Index (cont'd)

REFERENCE DESIGNATION	STOCK NO.	DESCRIPTION
R105	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R105 ***	1810–0022	RESISTOR NETWORK MET FLM (4.3K 1.8K 1K X2)
R106		NOT ASSIGNED
R107	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R107 ***	1810–0022	RESISTOR NETWORK MET FLM (4.3K 1.8K 1K X2)
R108		NOT ASSIGNED
R109 ****	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R110		NOT ASSIGNED
R111 ****	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R112		NOT ASSIGNED
R113 ****	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R114		NOT ASSIGNED
R115 ****	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R116		NOT ASSIGNED
R117 ****	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R118	1810–0008	RESISTOR NETWORK MET FLM (1K 2K 10K X2)
R119 thru R122	1810–0020	RESISTOR NETWORK MET FLM (1.5K X7)
W1 thru W21 *****		JUMPER WIRE (CAN BE SELF FABRICATED)

* CR9 THRU CR17 ARE IN THE REVERSE POSITION IN 15166A OPT 01 CARD (SEE SCHEMATIC)

** APPLIES ONLY TO 15166A OPT 01 CARD (SEE ALSO SCHEMATIC)

*** APPLIES ONLY TO 15166A OPT 01 CARD (SEE ALSO SCHEMATIC)

**** R109 B/E, R111B/E, R113 B/E, R115 B/E NOT SHORTED OUT IN 15166A OPT 01 CARD (SEE SCHEMATIC)

***** JUMPERS W14 THRU W21 ARE REMOVED ONLY ON THE 15166A OPT 01 CARD

See introduction to this section for abbreviation details

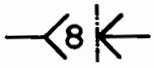
SECTION V

SCHEMATIC DIAGRAMS

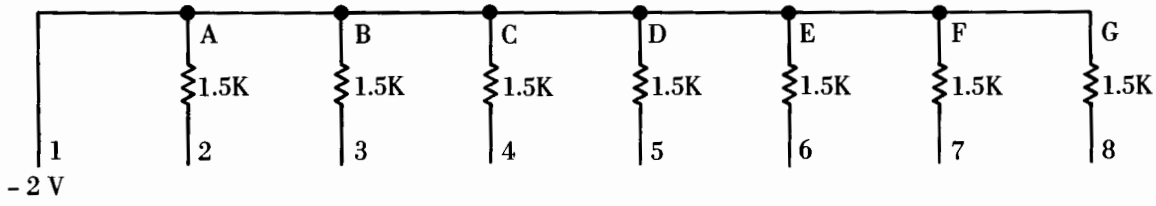
5–1 INTRODUCTION

5–2 This section contains the circuit diagrams and component location drawings necessary for the maintenance of the Model 15163A. Table 5–1 lists notes which apply to the schematic diagrams.

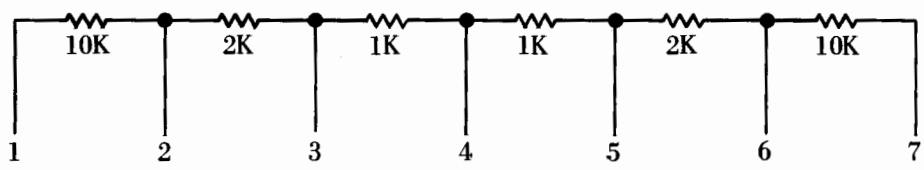
Table 5–1. Schematic Diagram Notes

③	=	Number of circuit diagram referred to
P/O	=	Part of
	=	Assembly board connection with pin number
*	=	Signal from/to external device via 48-Pin connector.
		All other signals are from/to computer via 86-Pin connector

Schematic Diagram for Resistor Networks R110 through R114 (1810–0020)



Schematic Diagram for Resistor Networks R115 through R121 (1810–0008)



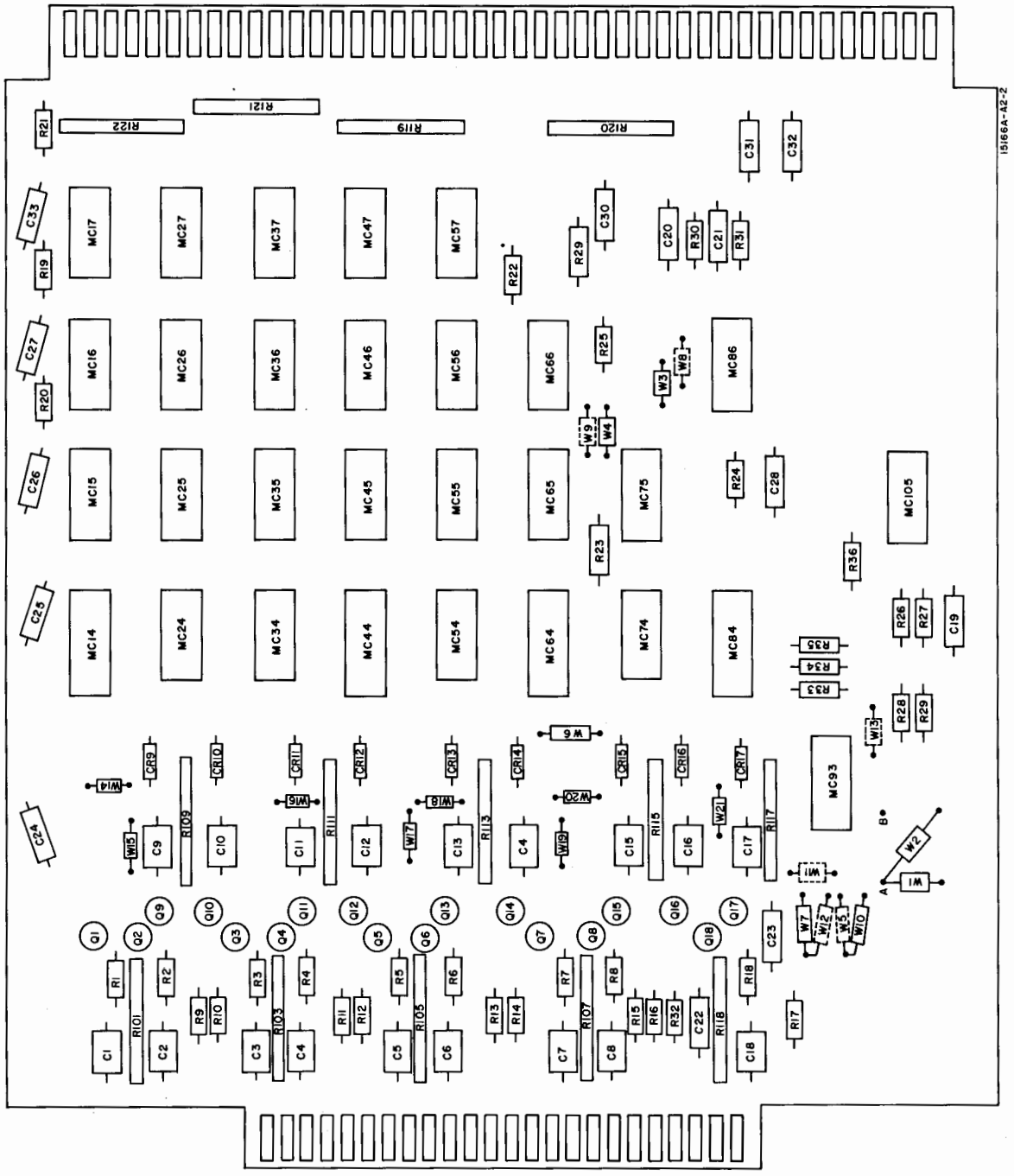


Figure 5–1. 15166A Component Locations

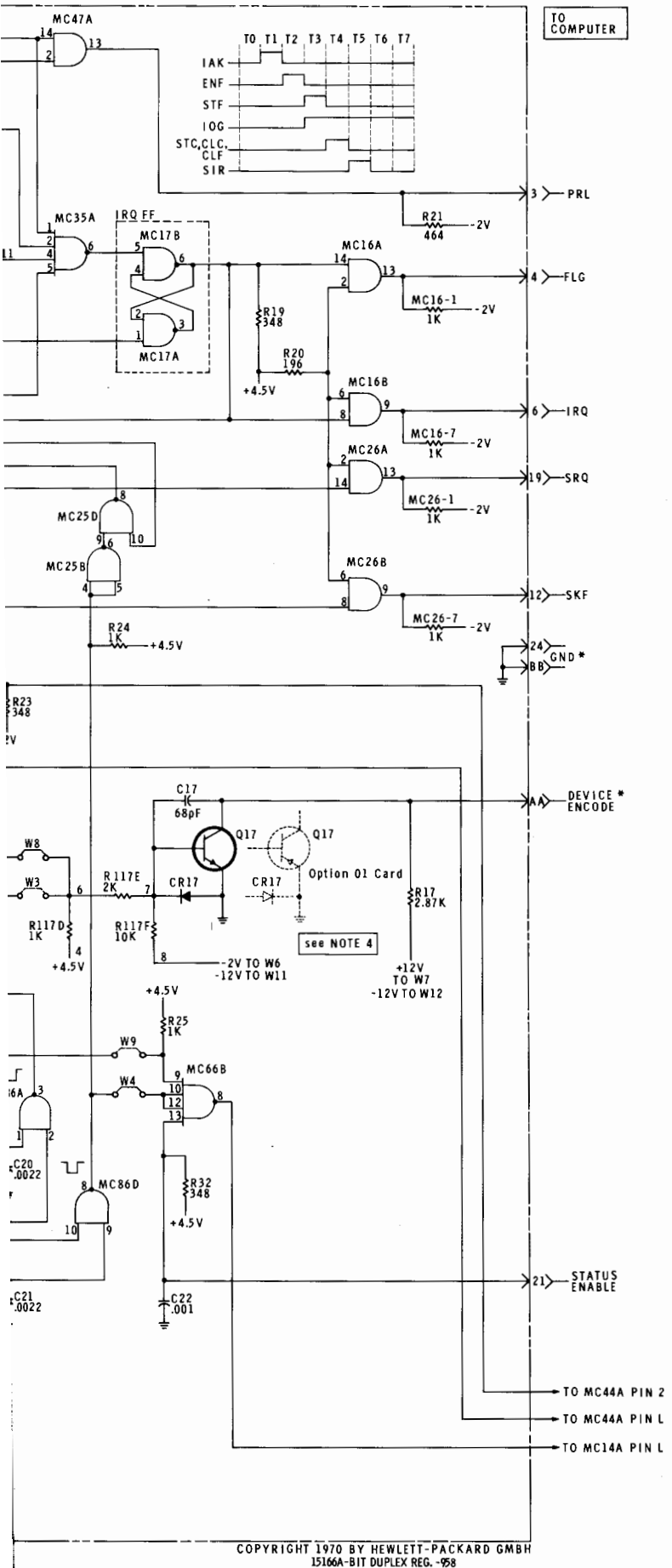
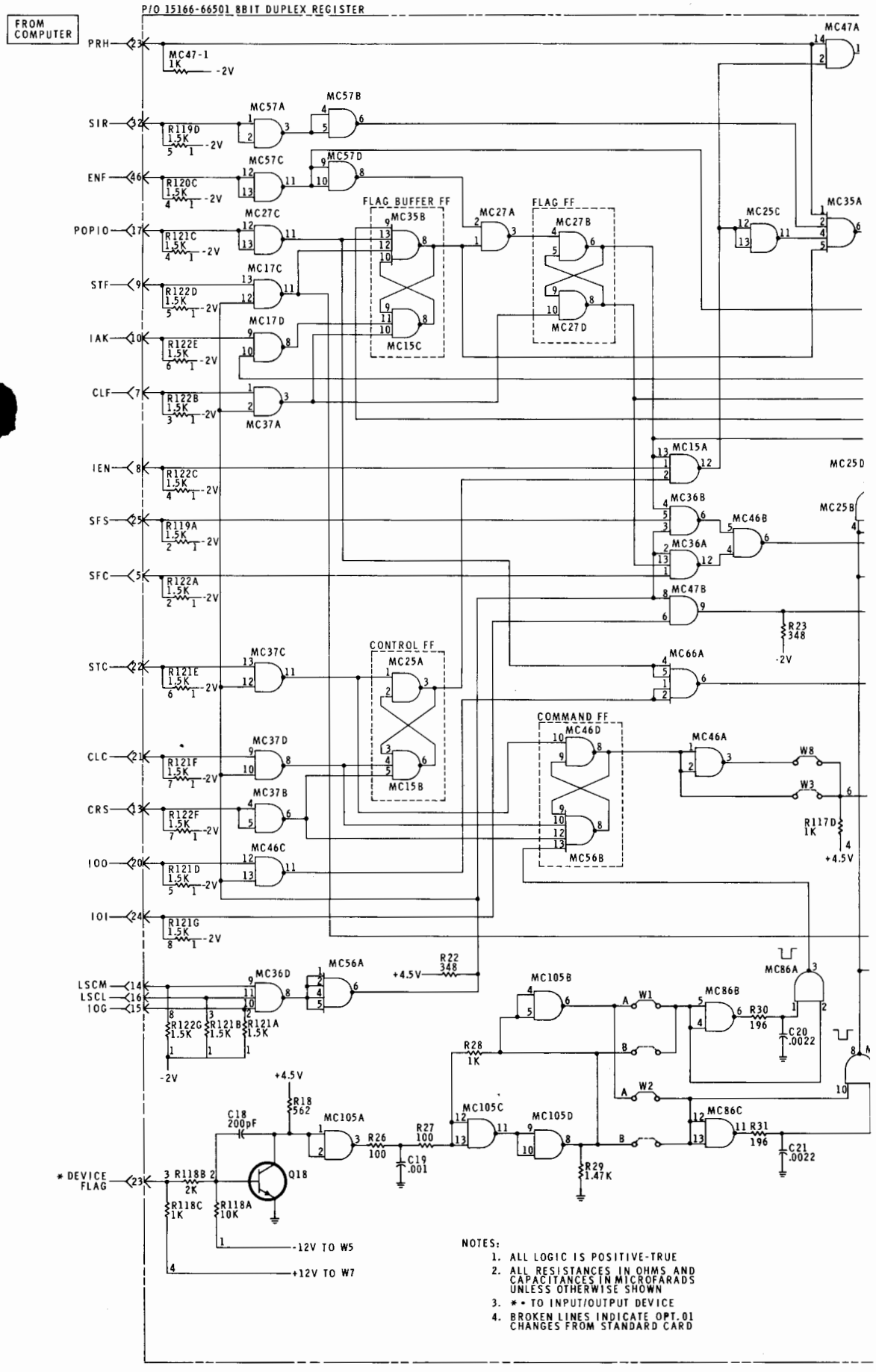


Figure 5–2. 15166A Input/Output Logic Diagram


P/O 15166-66501 8BIT DUPLEX REGISTER
FROM COMPUTER
PRH
SIR
ENF
POPIO
STF
IAK
CLF
IEN
SFS
SFC
STC
CLC
CRS
IOO
IOI
LSCM
LSCL
IOG
* DEVICE FLAG
MC47-1
1K
-2V
MC57A
MC57B
MC57C
MC57D
FLAG BUFFER FF
MC35B
MC15C
MC27A
FLAG FF
MC27B
MC27D
MC27C
MC17C
MC17D
MC37A
MC47A
MC25C
MC35A
MC15A
MC25D
MC36B
MC46B
MC36A
MC25B
MC47B
MC66A
R23
348
CONTROL FF
MC25A
MC15B
MC37C
MC37D
MC37B
MC46C
COMMAND FF
MC46D
MC56B
MC46A
W8
W3
R117D
1K
+4.5V
MC36D
MC56A
R22
348
R122G
R121B
R121A
MC105B
MC86A
MC86B
R30
196
C20
.0022
R28
1K
W1
W2
MC105C
MC105D
MC86C
R31
196
C21
.0022
C18
200pF
R18
562
MC105A
R27
100
R26
100
C19
.001
R29
1.47K
Q18
R118B
2K
R118C
1K
R118A
10K
-12V TO W5
+12V TO W7
NOTES:
1. ALL LOGIC IS POSITIVE-TRUE
2. ALL RESISTANCES IN OHMS AND CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SHOWN
3. * TO INPUT/OUTPUT DEVICE
4. BROKEN LINES INDICATE OPT.01 CHANGES FROM STANDARD CARD

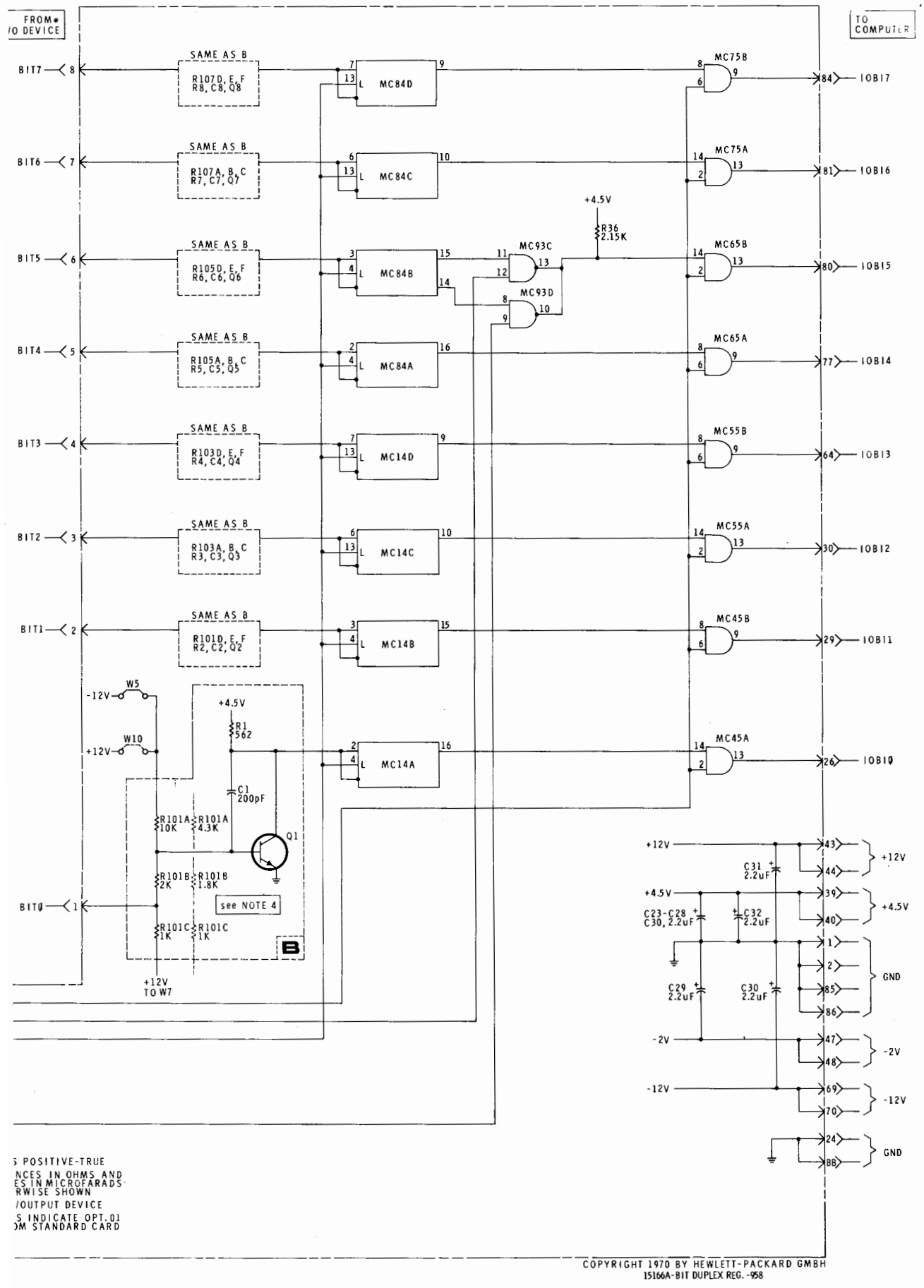
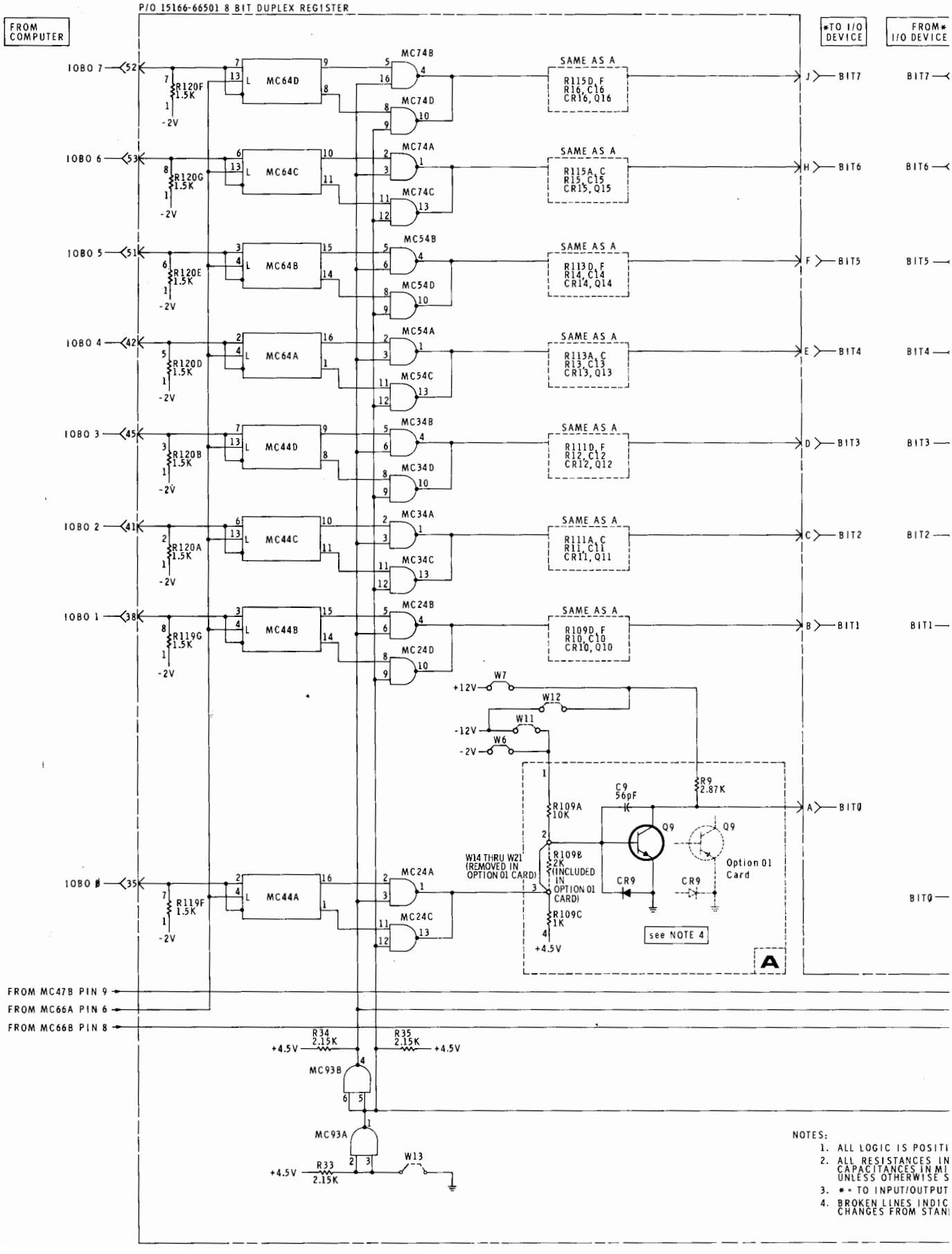


Figure 5–3. 15166A Input/Output Storage Registers


P/O 15166-66501 8 BIT DUPLEX REGISTER
FROM COMPUTER
*TO I/O DEVICE
FROM* I/O DEVICE
IOBO 7
IOBO 6
IOBO 5
IOBO 4
IOBO 3
IOBO 2
IOBO 1
IOBO 0
MC64D
MC64C
MC64B
MC64A
MC44D
MC44C
MC44B
MC44A
MC74B
MC74D
MC74A
MC74C
MC54B
MC54D
MC54A
MC54C
MC34B
MC34D
MC34A
MC34C
MC24B
MC24D
MC24A
MC24C
R120F 1.5K
R120G 1.5K
R120E 1.5K
R120D 1.5K
R120B 1.5K
R120A 1.5K
R119G 1.5K
R119F 1.5K
-2V
SAME AS A
R115D, F R16, C16 CR16, Q16
R115A, C R15, C15 CR15, Q15
R113D, F R14, C14 CR14, Q14
R113A, C R13, C13 CR13, Q13
R111D, F R12, C12 CR12, Q12
R111A, C R11, C11 CR11, Q11
R109D, F R10, C10 CR10, Q10
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
BIT0
W7
W12
W11
W6
+12V
-12V
-2V
R109A 10K
C9 56pF
R9 2.87K
R109B 2K (INCLUDED IN OPTION 01 CARD)
R109C 1K
+4.5V
W14 THRU W21 (REMOVED IN OPTION 01 CARD)
Q9
CR9
Option 01 Card
see NOTE 4
A
FROM MC47B PIN 9
FROM MC66A PIN 6
FROM MC66B PIN 8
R34 2.15K
R35 2.15K
MC93B
MC93A
R33 2.15K
W13
NOTES:
1. ALL LOGIC IS POSITI
2. ALL RESISTANCES IN
CAPACITANCES IN MI
UNLESS OTHERWISE S
3. * = TO INPUT/OUTPUT
4. BROKEN LINES INDIC
CHANGES FROM STAN

SECTION VI

DIAGNOSTIC OPERATING PROCEDURE

6–1 INTRODUCTION

6–2 The objective of this program is to check the 8-Bit Duplex Register Board (HP 15166–66501).

6–3 PROGRAM DESCRIPTION

6–4 The program consists of a background control program and three task routines. The background program obtains information via the Teletype and the Switch Register, and it controls message printout and directs task performance according to the information. The first task routine inserts the address of the Duplex Register into all Input/Output instructions. The second task checks the flag, control, and interrupt circuitry on the board. The third task routine checks the data buffers and associated discrete circuitry by outputting all possible combinations of 8 bits.

6–5 ENVIRONMENT

6–6 Hardware requirements are as follows:

a. HP Computer with 4K memory.

b. Teleprinter (HP 2752A or HP 2754A) and associated interface register.

c. Standard 8-Bit Duplex Register Card (15166–66501) and a 24-pin connector to short all output pins to the adjacent input pins (12597–6002).

d. An input device to enter the diagnostic into memory.

6–7 Software requirements are as follows:

a. This diagnostic.

b. System Input/Output Teleprinter driver.

6–8 DIAGNOSTIC TEST PROCEDURE

a. Duplex Register

(1) Short all output pins to the adjacent input pins with a 24-pin connector.

(2) Place register (with connector) in an Input/Output slot such that every slot of higher priority has either another I/O board or a priority jumper board in it.

(3) Change: Jumper W8 to W3.

(4) Insert: Jumper W13.

b. Teleprinter

(1) Put the Teleprinter Register in any I/O slot.

(2) Connect it to the Teleprinter.

c. Teleprinter Driver

(1) Read the SIO Teleprinter driver into memory.

(2) Put 000002 into the Switch Register.

(3) Push LOAD ADDRESS.

(4) Put the Teleprinter Register address into the Switch Register.

(5) Push RUN.

d. Duplex Register Diagnostic

(1) Read the diagnostic into memory.

(2) Put 000100 into the Switch Register.

(3) Push LOAD ADDRESS.

(4) Push RUN.

e. Program Operation

(1) The program will print: 16 BIT DUPLEX REGISTER DIAGNOSTIC.

(2) The program will print: I/O CHANNEL?

(3) The operator must print (using Teleprinter keyboard) the address of the Duplex Register, followed by a line termination (RETURN, LINE FEED).

(4) The program will print: SET SW. REG. FOR DATA BITS TO BE TESTED.

(5) The program will halt with M and P REGS. = 203 and A, B, and T REGS. = 102002.

Section VII

8–BIT DUPLEX REGISTER

Binary Tape

Source Listing

NOTE

This diagnostic listing is identical to the 16–Bit Duplex Register diagnostic listing

0001 ASMB,A,L
** NO ERRORS*

```
0001*
0002*
0003*
0004*  16 BIT DUPLEX REGISTER DIAGNOSTIC
0005*
0006*
0007*
0008*  STARTING OCTAL ADDRESS = 100
0009*
0010*
0011*  THE FOLLOWING SWITCH REGISTER SETTINGS
0012*  ARE USED FOR PROGRAM CONTROL
0013*
0014******
0015*  BIT 0 = 1 -> HALT AT BEGINNING OF PROGRAM
0016*  BIT 1 = 1 -> HALT AT BEGINNING OF BASIC TEST
0017*  BIT 2 = 1 -> SUPPRESS SUPERFLUOUS MESSAGES
0018*  BIT 3 = 1 -> PERFORM BASIC TEST
0019*  BIT 4 = 1 -> PERFORM DATA BUFFER TEST
0020******
0021*
0022*
0023*  MAIN PROGRAM
0024*
0025*
0026  00100                ORG 100B
0027  00100 024110         JMP 110B
0028  02042                ORG 1058
0029  02042 001322         DEF X
0030  00110                ORG 110B        FIRST AVAIL MEMORY
0031  00110 107700         CLC 0,C         INTERRUPT OFF
0032  00111 014466         JSB EOL         LINE FEED
0033  00112 060311         LDA ML1         PRINT
0034  00113 064267         LDB MAD1        FIRST
0035  00114 114102         JSB 102B,I      MESSAGE
0036  00115 014466         JSB EOL         LINE FEED
0037  00116 024122         JMP *+4
0038  00117 060121  P1     LDA *+2         HALT AT
0039  00120 064121         LDB *+1         BEGINNING
0040  00121 102000         HLT 0           OF PROGRAM
0041  00122 064462         LDB M67         PREPARE
0042  00123 060457         LDA HIS         TRAP
0043  00124 070126         STA *+2         FOR
0044  00125 060460         LDA HI          ILLEGAL
0045  00126 070010         STA 10B         INTERRUPT
0046  00127 034126         ISZ *-1         FROM
0047  00130 002004         INA             ANY
0048  00131 006006         INB,SZB
0049  00132 024126         JMP *-4
0050  00133 014466  P2     JSB EOL         LINE FEED
0051  00134 060321         LDA ML2         PRINT
0052  00135 064312         LDB MAD2        SECOND
0053  00136 114102         JSB 102B,I      MESSAGE
0054  00137 014466         JSB EOL         LINE FEED
0055  00140 060456         LDA RL1
0056  00141 064454         LDB RAD1        FIRST
0057  00142 114150         JSB 104,I       REPLY
0058  00143 060455         LDA REP1        CHECK FIRST CHARACTER
```

```
0059  00144 010463          AND MSK1       FOR VALIDITY
0060  00145 050465          CPA C1        VALID?
0061  00146 024150          JMP *+2        YES.
0062  00147 024133          JMP P2         NO.
0063  00150 060455          LDA REP1       CHECK SECOND
0064  00151 001727          ALF,ALF        CHARACTER
0065  00152 010463          AND MSK1       FOR VALIDITY
0066  00153 050465          CPA C1         VALID?
0067  00154 024156          JMP *+2        YES.
0068  00155 024133          JMP P2         NO.
0069  00156 002400          CLA            GENERATE
0070  00157 060455          LDA REP1       DUPLEX
0071  00160 010464          AND MSK2       REGISTER
0072  00161 070613          STA ADDR       ADDRESS
0073  00162 060455          LDA REP1
0074  00163 001727          ALF,ALF
0075  00164 010464          AND MSK2
0076  00165 001721          ALF,ARS
0077  00166 030613          IOR ADDR
0078  00167 070613          STA ADDR       ADDRESS COMPLETE
0079  00170 014530          JSB ADIN
0080  00171 060461          LDA IBAD       ILLEGAL INTERRUPT
0081  00172 070000  STA1    STA 0          TRAP
0082  00173 014466          JSB EOL
0083  00174 060347          LDA ML3
0084  00175 064322          LDB MAD3       THIRD
0085  00176 114102          JSB 102B,I     MESSAGE
0086  00177 014466          JSB EOL
0087  00200 060202          LDA *+2        HALT
0088  00201 064202          LDB *+1        TO SET
0089  00202 102002          HLT 2          SW. REG.
0090  00203 102501          LIA 1          LOAD MASK FOR
0091  00204 071242          STA DAMSK      DATA TESTING
0092  00205 060375          LDA ML4        SET SW. REG.
0093  00206 064350          LDB MAD4       FOR DESIRED
0094  00207 114102          JSB 102B,I     PROGRAM OPTIONS
0095  00210 014466          JSB EOL
0096  00211 060213  P3      LDA *+2        HALT AT
0097  00212 064213          LDB *+1        BEGINNING
0098  00213 102001          HLT 1          OF BASIC TEST
0099  00214 014501  P4      JSB MODE       CHECK SW. REG.
0100  00215 060526          LDA BIT3       PERFORM
0101  00216 002011          SLA,RSS        BASIC TEST?
0102  00217 024241          JMP P5         NO.
0103  00220 060525          LDA BIT2       YES. SUPPRESS
0104  00221 000010          SLA            MESSAGES?
0105  00222 024230          JMP *+6        YES.
0106  00223 014466          JSB EOL        NO.
0107  00224 060407          LDA ML5        PRINT FIRST
0108  00225 064376          LDB MAD5      BASIC TEST
0109  00226 114102          JSB 102B,I     MESSAGE
0110  00227 014466          JSB EOL
0111  00230 014614          JSB BAT        PERFORM BASIC TEST
0112  00231 060525          LDA BIT2       SUPPRESS
0113  00232 000010          SLA            MESSAGES?
0114  00233 024241          JMP *+6        YES.
0115  00234 014466          JSB EOL        NO.
0116  00235 060421          LDA ML6        PRINT SECOND
```

```
0117  00236 064410          LDB MAD6       BASIC TEST
0118  00237 114102          JSB 102B,I     MESSAGE
0119  00240 014466          JSB EOL
0120  00241 014501  P5      JSB MODE       CHECK SW. REG.
0121  00242 060527          LDA BIT4       PERFORM DATA
0122  00243 002011          SLA,RSS        BUFFER TEST?
0123  00244 024214          JMP P4         PERFORM DATA
0124  00245 060525          LDA BIT2       YES.  SUPPRESS
0125  00246 000010          SLA            MESSAGES?
0126  00247 024255          JMP *+6         YES.
0127  00250 014466          JSB EOL        NO.
0128  00251 060436          LDA ML7        PRINT FIRST
0129  00252 064422          LDB MAD7       DATA TEST
0130  00253 114102          JSB 102B,I      MESSAGE
0131  00254 014466          JSB EOL
0132  00255 015110          JSB DAT        PERFORM DATA BUFFER TEST
0133  00256 060525          LDA BIT2       SUPPRESS
0134  00257 000010          SLA            MESSAGES?
0135  00260 024214          JMP P4         YES.
0136  00261 014466          JSB EOL        NO.
0137  00262 060453          LDA ML8        PRINT SECOND
0138  00263 064437          LDB MAD8       DATA TEST
0139  00264 114102          JSB 102B,I     MESSAGE
0140  00265 014466          JSB EOL
0141  00266 024214          JMP P4
0142*
0143*
0144  00267 000270  MAD1    DEF *+1
0145  00270 030466  MES1    ASC 17,16 BIT DUPLEX REGISTER DIAGNOSTIC
      00271 020102
      00272 044524
      00273 020104
      00274 052520
      00275 046105
      00276 054040
      00277 051105
      00300 043511
      00301 051524
      00302 042522
      00303 020104
      00304 044501
      00305 043516
      00306 047523
      00307 052111
      00310 041440
0146  00311 000042  ML1     DEC 34
0147*
0148  00312 000313  MAD2    DEF *+1
0149  00313 044457  MES2    ASC 6,I/O CHANNEL?
      00314 047440
      00315 041510
      00316 040516
      00317 047105
      00320 046077
0150  00321 000014  ML2     DEC 12
0151*
0152  00322 000323  MAD3    DEF *+1
0153  00323 051505  MES3    ASC 20,SET SW. REG. FOR DATA BITS TO BE TESTED
```

```
       00324 052040
       00325 051527
       00326 027040
       00327 051105
       00330 043456
       00331 020106
       00332 047522
       00333 020104
       00334 040524
       00335 040440
       00336 041111
       00337 052123
       00340 020124
       00341 047440
       00342 041105
       00343 020124
       00344 042523
       00345 052105
       00346 042040
0154   00347 000050   ML3    DEC 40
0155   00350 000351   MAD4   DEF *+1
0156   00351 051505   MES4   ASC 20,SET SW. REG. FOR DESIRED PROGRAM OPTION
       00352 052040
       00353 051527
       00354 027040
       00355 051105
       00356 043456
       00357 020106
       00360 047522
       00361 020104
       00362 042523
       00363 044522
       00364 042504
       00365 020120
       00366 051117
       00367 043522
       00370 040515
       00371 020117
       00372 050124
       00373 044517
       00374 047040
0157   00375 000050   ML4    DEC 40
0158   00376 000377   MAD5   DEF *+1
0159   00377 041105   MES5   ASC 8,BEGIN BASIC TEST
       00400 043511
       00401 047040
       00402 041101
       00403 051511
       00404 041440
       00405 052105
       00406 051524
0160   00407 000020   ML5    DEC 16
0161*
0162   00410 000411   MAD6   DEF *+1
0163   00411 042516   MES6   ASC 8,END BASIC TEST
       00412 042040
       00413 041101
       00414 051511
```

```
       00415 041440
       00416 052105
       00417 051524
       00420 020040
0164   00421 000020  ML6    DEC 16
0165*
0166   00422 000423  MAD7   DEF *+1
0167   00423 041105  MES7   ASC 11,BEGIN DATA BUFFER TEST
       00424 043511
       00425 047040
       00426 042101
       00427 052101
       00430 020102
       00431 052506
       00432 043105
       00433 051040
       00434 052105
       00435 051524
0168   00436 000026  ML7    DEC 22
0169*
0170   00437 000440  MAD8   DEF *+1
0171   00440 042516  MES8 ASC 11,END  DATA BUFFER TEST
       00441 042040
       00442 020104
       00443 040524
       00444 040440
       00445 041125
       00446 043106
       00447 042522
       00450 020124
       00451 042523
       00452 052040
0172   00453 000026  ML8    DEC 22
0173*
0174   00454 000455  RAD1   DEF *+1
0175   00455 000000  REP1   OCT 0
0176   00456 000002  RL1    OCT 2
0177*
0178   00457 070010  HIS    STA 10B
0179   00460 102010  HI     HLT 10B
0180   00461 015041  IBAD   JSB ILINT
0181   00462 177711  M67    OCT 177711
0182   00463 000170  MSK1   OCT 170
0183   00464 000007  MSK2   OCT 7
0184   00465 000060  C1     OCT 60
0185*
0186*  LINE FEED, CARRIAGE RETURN
0187*
0188   00466 000000  EOL    NOP            ENTER SUBROUTINE
0189   00467 070477         STA AS1        STORE
0190   00470 074500         STB BS1        A & B
0191   00471 002400         CLA            LINE
0192   00472 006400         CLB            FEED
0193   00473 114102         JSB 102B,I
0194   00474 060477         LDA AS1        RESTORE
0195   00475 064500         LDB BS1        A & B
0196   00476 124466         JMP EOL,I      EXIT SUBROUTINE
0197   00477 000000  AS1    OCT 0
```

```
0198  00500 000000  BS1   OCT 0
0199*
0200*  MODE SUBROUTINE
0201*
0202  00501 000000  MODE  NOP            ENTER SUBROUTINE
0203  00502 070522       STA AS2         STORE A
0204  00503 102501       LIA 1           EACH BIT
0205  00504 070523       STA BIT0        FROM THE
0206  00505 001300       RAR             SWITCH REGISTER
0207  00506 070524       STA BIT1        IS ROTATED
0208  00507 001300       RAR             INTO THE
0209  00510 070525       STA BIT2        LEAST SIGNIFICANT
0210  00511 001300       RAR            POSITION AND
0211  00512 070526       STA BIT3        STORED IN THE
0212  00513 001300       RAR             STORAGE LOCATION
0213  00514 070527       STA BIT4        BEARING ITS NAME
0214  00515 060523       LDA BIT0        HALT AT
0215  00516 000010       SLA             BEGINNING OG BASIC TEST?
0216  00517 024211       JMP P3          YES
0217  00520 060522       LDA AS2         NO.   RESTORE A
0218  00521 124501       JMP MODE,I      EXIT SUBROUTINE
0219  00522 000000  AS2   OCT 0
0220  00523 000000  BIT0  OCT 0
0221  00524 000000  BIT1  OCT 0
0222  00525 000000  BIT2  OCT 0
0223  00526 000000  BIT3  OCT 0
0224  00527 000000  BIT4  OCT 0
0225*
0226*
0227*  ADDRESS INCLUSION ROUTINE
0228*
0229*
0230  00530 000000  ADIN  NOP            ENTER ROUTINE
0231  00531 107700       CLC 0,C         INTERRUPT SUSTEM OFF
0232  00532 014606       JSB INCLU       PUT CUPLEX REG. ADDR.
0233  00533 070000       STA 0           INTO STA INSTRUCTIONS
0234  00534 070172       STA STA1
0235  00535 070714       STA STA2
0236  00536 070723       STA STA3
0237  00537 014606       JSB INCLU       SAME FOR STC XX,C
0238  00540 103700       STC 0,C
0239  00541 070616       STA STCC1
0240  00542 070673       STA STCC2
0241  00543 071164       STA STCC3
0242  00544 014606       JSB INCLU      SAME FOR SFS XX
0243  00545 102300       SFS 0
0244  00546 070643       STA SFS1
0245  00547 070653       STA SFS2
0246  00550 070663       STA SFS3
0247  00551 070677       STA SFS4
0248  00552 070724       STA SFS5
0249  00553 071170       STA SFS6
0250  00554 014606       JSB INCLU      SABE FOR SFC XX
0251  00555 102200       SFC 0
0252  00556 070647       STA SFC1
0253  00557 070656       STA SFC2
0254  00560 070667       STA SFC3
0255  00561 070702       STA SFC4
```

```
0256  00562 070727          STA SFC5
0257  00563 014606          JSB INCLU     SAME FOR STF XX
0258  00564 102100          STF 0
0259  00565 070652          STA STF1
0260  00566 070707          STA STF2
0261  00567 071112          STA STF3
0262  00570 014606          JSB INCLU     SAME FOR CLC XX
0263  00571 106700          CLC 0
0264  00572 070706          STA CLC1
0265  00573 071154          STA CLC2
0266  00574 014606          JSB INCLU     SAME FOR STC XX
0267  00575 102700          STC 0
0268  00576 070715          STA STC1
0269  00577 014606          JSB INCLU     SAME FOR OTA XX
0270  00600 102600          OTA 0
0271  00601 071152          STA OTA1
0272  00602 014606          JSB INCLU     SAME FOR LIB XX
0273  00603 106500          LIB 0
0274  00604 071172          STA LIB1
0275  00605 124530          JMP ADIN,I    EXIT ROUTINE
0276*
0277*  INCLUSION SUBROUTINE
0278*
0279  00606 000000  INCLU   NOP           ENTER SUBROUTINE
0280  00607 160606          LDA INCLU,I   PUT ADDRESS
0281  00610 030613          IOR ADDR      INTO INSTRUCTION
0282  00611 034606          ISZ INCLU     EXIT
0283  00612 124606          JMP INCLU,I   SUBROUTINE
0284  00613 000000  ADDR    OCT 0         ADDRESS STORAGE
0285*
0286*
0287*  BASIC TEST ROUTINE
0288*
0289*
0290  00614 000000  BAT     NOP           ENTER ROUTINE
0291  00615 107700          CLC 0,C
0292  00616 103700  STCC1   STC 0,C
0293  00617 060775          LDA C2
0294  00620 002006          INA,SZA
0295  00621 024620          JMP *-1
0296  00622 107700          CLC 0,C
0297  00623 103100  CLF1    CLF 0
0298  00624 102100          STF 0         INTERRUPT SYSTEM ON
0299  00625 006400          CLB           INITIALIZE
0300  00626 074760          STB  E1       ERROR
0301  00627 074761          STB E2        BUFFER
0302  00630 074762          STB E3
0303  00631 074763          STB E4
0304  00632 074764          STB E5
0305  00633 074765          STB E6
0306  00634 074766          STB E7
0307  00635 074767          STB E10
0308  00636 074770          STB E11
0309  00637 074771          STB E12
0310  00640 074772          STB E13
0311  00641 074774          STB E14
0312  00642 006004          INB
0313  00643 102300  SFS1    SFS 0         FLAG SET?
```

```
0314  00644 024646          JMP *+2        NO.
0315  00645 074760          STB E1         YES.   ERROR 1
0316  00646 006004          INB            INCREMENT ERROR CODE
0317  00647 102200  SFC1    SFC 0          FLAG CLEAR?
0318  00650 074761          STB E2         NO.  ERROR 2
0319  00651 006004          INB            YES.
0320  00652 102100  STF1    STF 0           SET FLAG
0321  00653 102300  SFS2    SFS 0          FLAG SET?
0322  00654 074762          STB E3          NO.  ERROR 3
0323  00655 006004          INB            YES.
0324  00656 102200  SFC2    SFC 0          CLEAR FLAG
0325  00657 024661          JMP *+2        NO.
0326  00660 074763          STB E4         YES.  ERROR 4
0327  00661 006004          INB
0328  00662 103100  CLF2    CLF 0          CLEAR FLAG
0329  00663 102300  SFS3    SFS 0          FLAG SET?
0330  00664 024666          JMP *+2        NO.
0331  00665 074764          STB E5         YES.  ERROR 5
0332  00666 006004          INB
0333  00667 102200  SFC3    SFC 0          FLAG CLEAR?
0334  00670 074765          STB E6         NO.  ERROR 6
0335  00671 006004          INB             YES.
0336  00672 107700          CLC 0,C        INTERRUPT SYSTEM OFF
0337  00673 103700  STCC2   STC 0,C        ENCODE
0338  00674 060775          LDA C2         WAIT
0339  00675 002006          INA,SZA        FOR
0340  00676 024675          JMP *-1        FLAG
0341  00677 102300  SFS4    SFS 0          FLAG SET?
0342  00700 074766          STB E7         NO.  ERROR 7
0343  00701 006004          INB            YES.
0344  00702 102200  SFC4    SFC 0          FLAG CLEAR?
0345  00703 024705          JMP *+2        NO.
0346  00704 074767          STB E10        YES.  ERROR 10
0347  00705 006004          INB
0348  00706 106700  CLC1    CLC 0          CLEAR CONTROL
0349  00707 102100  STF2    STF 0          SET FLAG
0350  00710 102100          STF 0          INTERRUPT SYSTEM ON
0351  00711 000000          NOP
0352  00712 000000          NOP
0353  00713 060776          LDA IOK
0354  00714 070000  STA2    STA 0
0355  00715 102700  STC1    STC 0          TEST
0356  00716 000000          NOP
0357  00717 000000          NOP            INTERRUPT CIRCUITRY
0358  00720 074770          STB E11        ERROR 11 - FAILURE TO INTERRUPT
0359  00721 006004  P6      INB
0360  00722 060461          LDA IBAD
0361  00723 070000  STA3    STA 0
0362  00724 102300  SFS5    SFS 0          FLAG SET?
0363  00725 074771          STB E12        NO.  ERROR 12
0364  00726 006004          INB            YES.
0365  00727 102200  SFC5    SFC 0          FLAG CLEAR?
0366  00730 024732          JMP *+2        NO.
0367  00731 074772          STB E13        YES.  ERROR 13
0368  00732 006004          INB
0369  00733 107700          CLC 0,C        INTERRUPT SYSTEM OFF
0370  00734 060757          LDA ERBUF      CHECK ERROR BUFFER
0371  00735 164000  P7      LDB 0,I
```

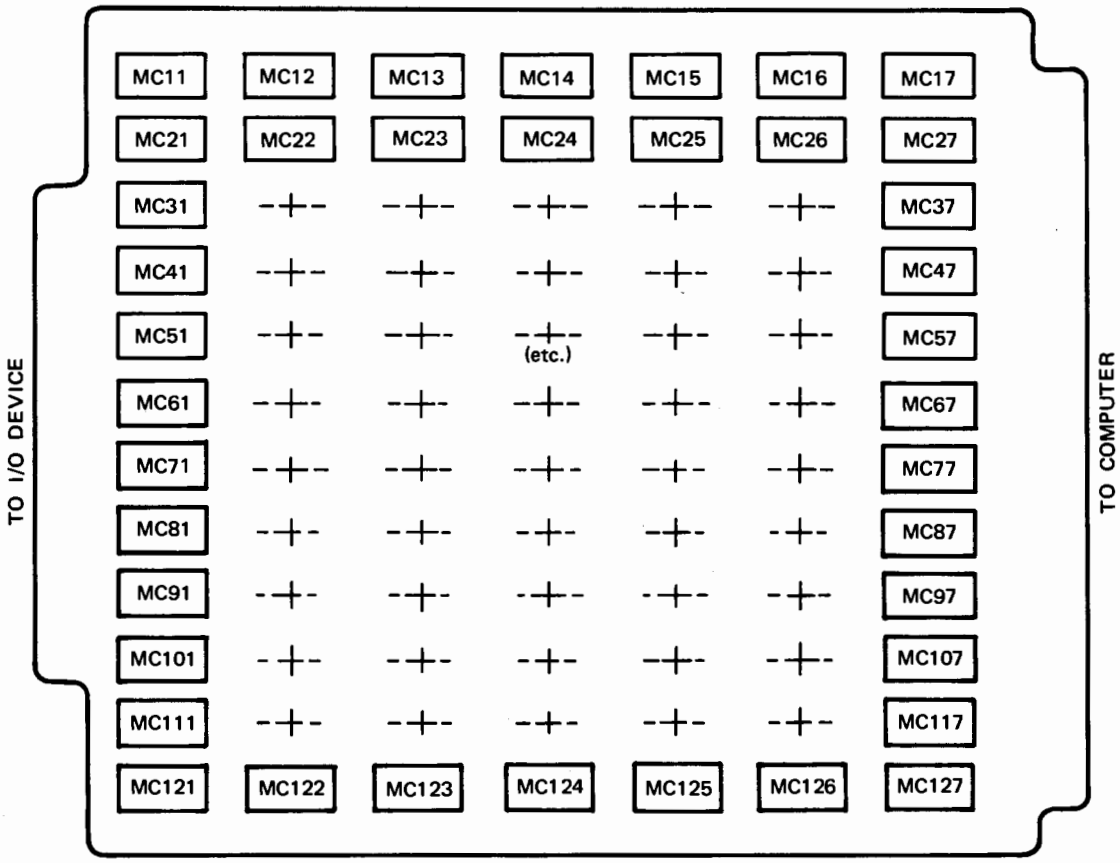
```
0372  00736 006003          SZB,RSS        ERROR?
0373  00737 024746          JMP *+7        NO.
0374  00740 006007          INB,SZB,RSS    END OF ERROR BUFFER?
0375  00741 024750          JMP *+7        YES.
0376  00742 164000          LDB 0,I        NO.
0377  00743 071240          STA AS5        PRINT
0378  00744 014777          JSB ERR        OUT
0379  00745 061240          LDA AS5        ERROR
0380  00746 002004          INA            CODE
0381  00747 024735          JMP P7
0382  00750 060774          LDA E14        INTERRUPT
0383  00751 002003          SZA,RSS        ERROR?
0384  00752 024756          JMP *+4        NO.
0385  00753 061107          LDA ML10       PRINT
0386  00754 065066          LDB MAD10      OUT
0387  00755 114102          JSB 102B,I     MESSAGE
0388  00756 124614          JMP BAT,I      EXIT ROUTINE
0389*
0390  00757 000760  ERBUF DEF *+1         ERROR BUFFER
0391  00760 000000  E1     OCT 0          SFS  TRUE AFTER CLF
0392  00761 000000  E2     OCT 0          SFC FALSE AFTER CLF
0393  00762 000000  E3     OCT 0          SFS FALSE AFER STF
0394  00763 000000  E4     OCT 0          SFC  TRUE AFTER STF
0395  00764 000000  E5     OCT 0          SFS  TRUE AFTER CLF
0396  00765 000000  E6     OCT 0          SFC FALSE AFTER CLF
0397  00766 000000  E7     OCT 0          SFS FALSE AFTER STC  ,C
0398  00767 000000  E10    OCT 0          SFC  TRUE AFTER STC  ,C
0399  00770 000000  E11    OCT 0          FAILURE TO INTERRUPT
0400  00771 000000  E12    OCT 0          SFS FALSE AFTER INTERUPT TEST
0401  00772 000000  E13    OCT 0          SFC  TRUE AFTER INTERRUPT TEST
0402  00773 177777         OCT 177777     ERROR BUFFER TERMINATION
0403  00774 000000  E14    OCT 0          ILLEGAL INTERRUPT
0404*
0405  00775 177774  C2     OCT 177774
0406  00776 024721  IOK    JMP P6
0407*
0408*  BASIC TEST ERROR PRINTOUT WUBROUTINE
0409*
0410  00777 000000  ERR    NOP            ENTER SUBROUTINE
0411  01000 075011         STB BS2        STORE B
0412  01001 060001         LDA 1
0413  01002 015016         JSB .2NUM      PACK 2 NUMBERS
0414  01003 075014         STB MES9+1     PRINT
0415  01004 061015         LDA ML9        OUT
0416  01005 065012         LDB MAD9       ERROR
0417  01006 114102         JSB 102B,I     MESSAGE
0418  01007 065011         LDB BS2        RESTORE B
0419  01010 124777         JMP ERR,I      EXIT SUBROUTINE
0420  01011 000000  BS2    OCT 0
0421  01012 001013  MAD9   DEF *+1
0422  01013 042440  MES9   ASC 1,E
0423  01014 000000         OCT 0
0424  01015 000004  ML9    DEC 4
0425*
0426*  PACK TWO ASCII NUMBERS SUBROUTINE
0427*
0428  01016 000000  .2NUM NOP            ENTER SUBROUTINE
0429  01017 071040         STA AS3        STORE A
```

```
0430  01020 001323          RAR,RAR       FORMAT
0431  01021 001300          RAR           FIRST
0432  01022 010464          AND MSK2      NUMBER
0433  01023 030465          IOR C1
0434  01024 001727          ALF,ALF
0435  01025 070001          STA 1         STORE IT
0436  01026 061040          LDA AS3       FORMAT
0437  01027 010464          AND MSK2      SECOND
0438  01030 030465          IOR C1
0439  01031 001727          ALF,ALF
0440  01032 070001          STA 1         STORE IT
0441  01033 061040          LDA AS3       FORMAT
0442  01034 030001          IOR 1         PACK THEM
0443  01035 070001          STA 1         INTO B
0444  01036 061040          LDA AS3       RESTORE A
0445  01037 125016          JMP .2NUM,I   EXIT SUBROUTINE
0446  01040 000000  AS3     OCT 0
0447*
0448*  ILLEGAL DUPLEX REGISTER INTERRUPT SUBROUTINE
0449*
0450  01041 000000  ILINT   NOP           ENTER SUBROUTINE
0451  01042 071063          STA AS4       STORE
0452  01043 075064          STB BS3       A & B
0453  01044 061041          LDA ILINT     PACK
0454  01045 001700          ALF           FIRST
0455  01046 011065          AND MSK3      TWO
0456  01047 015016          JSB .2NUM     NUMBERS
0457  01050 075104          STB IA        STORE THEM
0458  01051 061041          LDA ILINT     PACK
0459  01052 001727          ALF,ALF       SECOND
0460  01053 001222          RAL,RAL       TWO
0461  01054 015016          JSB .2NUM     NUMBERS
0462  01055 075106          STB IA+2      STORE THEM
0463  01056 002404          CLA,INA
0464  01057 070774          STA E14
0465  01060 061063          LDA AS4       RESTORE
0466  01061 065064          LDB BS3       A & B
0467  01062 125041          JMP ILINT,I   EXIT SUBROUTINE
0468  01063 000000  AS4     OCT 0
0469  01064 000000  BS3     OCT 0
0470  01065 000017  MSK3    OCT 17
0471  01066 001067  MAD10   DEF *+1
0472  01067 042440  MES10   ASC 13,E 14   PROGRAM ADDRESS =
      01070 030464
      01071 020040
      01072 020120
      01073 051117
      01074 043522
      01075 040515
      01076 020101
      01077 042104
      01100 051105
      01101 051523
      01102 020075
      01103 020040
0473  01104 000000  IA      OCT 0,0,0
      01105 000000
      01106 000000
```

```
0474  01107 000040  ML10  DEC 32
0475*
0476*
0477*  DATA BUFFER TEST ROUTINE
0478*
0479*
0480  01110 000000  DAT   NOP           ENTER ROUTINE
0481  01111 107700        CLC 0,C       INTERRUPT SUSTEM OFF
0482  01112 102100  STF3  STF 0
0483  01113 002400        CLA
0484  01114 015150  P8    JSB DOIC      OUTPUT A CHARACTER
0485  01115 003000        CMA           OUTPUT ITS
0486  01116 015150        JSB DOIC      COMPLEMENT
0487  01117 003000        CMA           OUTPUT THE
0488  01120 015150        JSB DOIC      CHARACTER AGAIN
0489  01121 002006        INA,SZA       INCREMENT CHARACTER.   = 0?
0490  01122 025114        JMP P8        NO.
0491  01123 102500        LIA 0         YES.  CHECK IOBI DRIVERS
0492  01124 002003        SZA,RSS       ANY ERRORS?
0493  01125 125110        JMP DAT,I     NO.  EXIT ROUTINE
0494  01126 071241        STA AS6       YES.
0495  01127 015016        JSB .2NUM     PACK
0496  01130 075320        STB MES13+9   A REG.
0497  01131 061241        LDA AS6       AND
0498  01132 001700        ALF           STORE
0499  01133 071241        STA AS6       IT IN THE
0500  01134 011065        AND MSK3      ERROR
0501  01135 015016        JSB .2NUM     MESSAGE
0502  01136 075316        STB MES13+7
0503  01137 061241        LDA AS6
0504  01140 001700        ALF
0505  01141 001222        RAL,RAL
0506  01142 015016        JSB .2NUM
0507  01143 075317        STB MES13+8
0508  01144 061321        LDA ML13      OUTPUT
0509  01145 065306        LDB MAD13     ERROR
0510  01146 114102        JSB 102B,I    MESSAGE
0511  01147 125110        JMP DAT,I     EXIT ROUTINE
0512*
0513*  DATA OUT, IN, AND COMPARE SUBROUTINE
0514*
0515  01150 000000  DOIC  NOP           ENTER SUBROUTINE
0516  01151 071240        STA AS5       STORE A
0517  01152 102600  OTA1  OTA 0         OUTPUT A
0518  01153 025160        JMP *+5
0519  01154 106700  CLC2  CLC 0
0520  01155 061261        LDA ML11      LOSS
0521  01156 065243        LDB MAD11     OF FLAG
0522  01157 114102        JSB 102B,I    MESSAGE
0523  01160 014501        JSB MODE      CHECK SW. REG.
0524  01161 060527        LDA BIT4      EXIT DAT
0525  01162 002011        SLA,RSS       ROUTINE?
0526  01163 125110        JMP DAT,I     YES.
0527  01164 103700  STCC3 STC 0,C       NO.  ENCODE
0528  01165 060775        LDA C2        WAIT
0529  01166 002006        INA,SZA       FOR
0530  01167 025166        JMP *-1       FLAG
0531  01170 102300  SFS6  SFS 0         FLAG SET?
```

```
0532  01171 025154         JMP CLC2       NO.  REPEAT ENCODING
0533  01172 106500  LIB1   LIB 0          YES.  READ DATA
0534  01173 060001         LDA 1          MASK OFF
0535  01174 011242         AND DAMSK      UNWANTED BITS
0536  01175 070001         STA 1          MASK OFF
0537  01176 011242         AND DAMSK      UNWANTED BITS
0538  01177 050001         CPA 1          OUTPUT = INPUT ?
0539  01200 025235         JMP P9         YES.
0540  01201 075237         STB BS4        NO.
0541  01202 071241         STA AS6
0542  01203 001700         ALF            PACK
0543  01204 011065         AND MSK3       OUTPUT
0544  01205 015016         JSB .2NUM      WORD
0545  01206 075270         STB MES12+5     AND
0546  01207 061241         LDA AS6        STORE
0547  01210 001727         ALF,ALF        IT IN THE
0548  01211 001222         RAL,RAL        ERROR
0549  01212 015016         JSB .2NUM      MESSAGE
0550  01213 075272         STB MES12+7
0551  01214 061237         LDA BS4        PACK
0552  01215 001700         ALF            INPUT
0553  01216 011065         AND MSK3       WORD
0554  01217 015016         JSB .2NUM      AND
0555  01220 075302         STB MES12+15    STORE
0556  01221 061237         LDA BS4        IT IN THE
0557  01222 001727         ALF,ALF        ERROR
0558  01223 001222         RAL,RAL      MESSAGE
0559  01224 015016         JSB .2NUM
0560  01225 075303         STB MES12+16
0561  01226 001700         ALF
0562  01227 001222         RAL,RAL
0563  01230 015016         JSB .2NUM
0564  01231 075304         STB MES12+17
0565  01232 061305         LDA ML12       OUTPUT
0566  01233 065262         LDB MAD12      ERROR
0567  01234 114102         JSB 102B,I     MESSAGE
0568  01235 061240  P9     LDA AS5        RESTORE A
0569  01236 125150         JMP DOIC,I     EXIT SUBROUTINE
0570  01237 000000  BS4    OCT 0
0571  01240 000000  AS5    OCT 0
0572  01241 000000  AS6    OCT 0
0573  01242 000000  DAMSK  OCT 0          DATA MASK STORAGE
0574*
0575  01243 001244  MAD11  DEF *+1
0576  01244 043114  MES11  ASC 13,FLAG FAILURE IN DATA TEST
      01245 040507
      01246 020106
      01247 040511
      01250 046125
      01251 051105
      01252 020111
      01253 047040
      01254 042101
      01255 052101
      01256 020124
      01257 042523
      01260 052040
0577  01261 000032  ML11   DEC 26
```

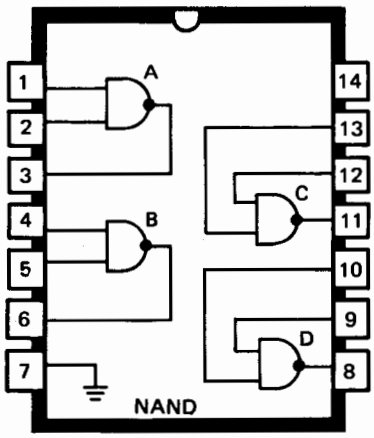
APPENDIX A



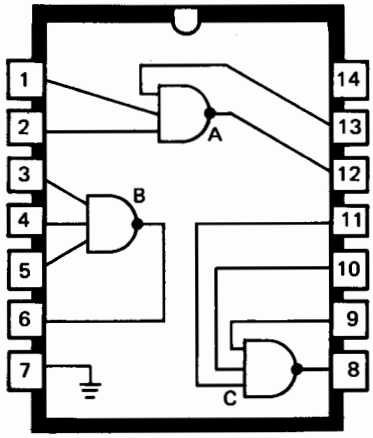
NOTE: A Microcircuit Package always assumes the reference designation assigned to its location on the card as illustrated in this figure.

Figure A–1. Microcircuit Package Locations

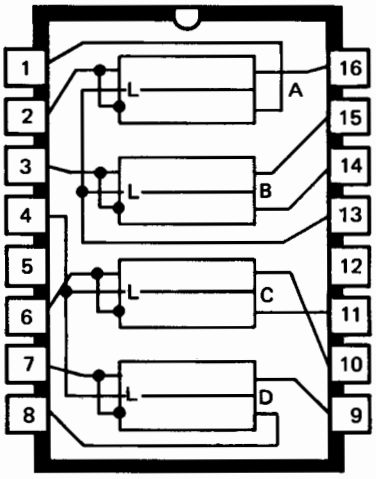
1820–0054



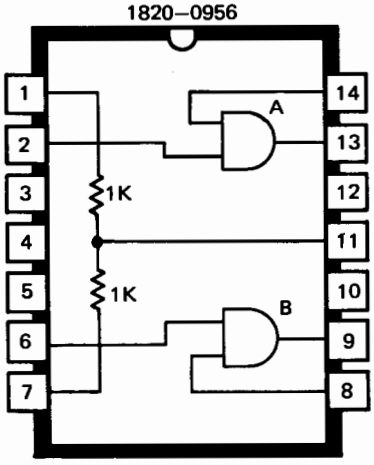
1820–0068



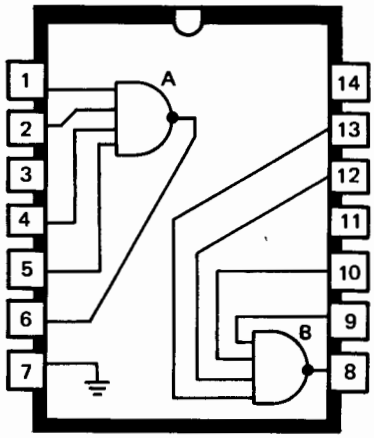
1820–0301



1820–0974
1820–0956



1820–0348
1820–0069
1820–0071



1820–0327

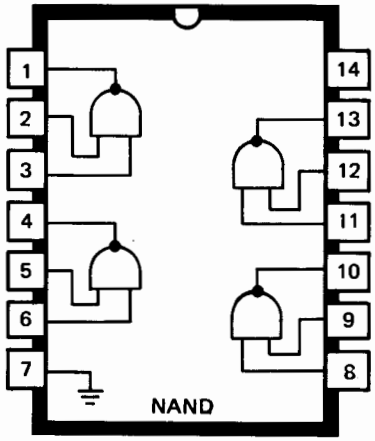


Figure A–2. Microcircuit Packages, Top View

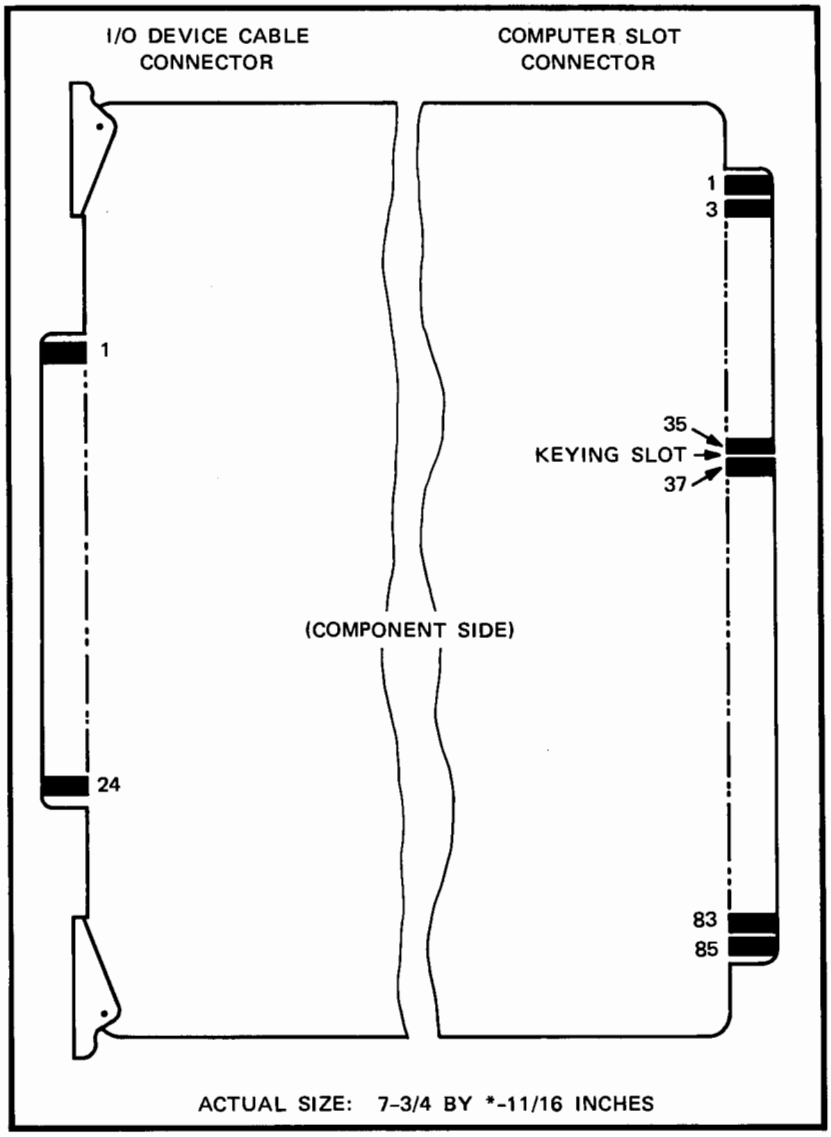


Figure A–3. Orientation of Connector Pins