HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

13210A

DISC DRIVE INTERFACE KIT

(FOR THE 2100 SERIES COMPUTERS)

Printed-Circuit Assemblies

13210-60000, Series 1211, 1249, 1438, 1446
13210-60004, Series 1211, 1232

Note

This manual is directly applicable to interface kits with serial prefixes shown above and can also be made applicable to interface kits with serial prefixes 1135 and 1138 by incorporating the appropriate changes listed in the appendix at the back of this manual.

13210-90003

HEWLETT-PACKARD COMPANY
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PRINTED: MAY 1975

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ILLUSTRATIONS

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HEWLETT PACKARD

13210A
DISC DRIVE INTERFACE KIT
OPERATING AND SERVICE MANUAL

UPDATING SUPPLEMENT

28 NOV 1977

MANUAL IDENTIFICATION

Manual Serial No. Prefix: 1211, 1232, 1249, 1438, 1446
Manual Printed: MAY 1975
Manual Part No.: 13210-90003
Microfiche Part No.: 13210-90008

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to equipment containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left. For any given instrument serial number prefix, all change steps noted for prior serial number prefixes must be incorporated in addition to those for the given prefix.

INSTRUMENT CHANGES

Serial No. Prefix	Change

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Series	Changes
NA	Disc Interface 1 PCA	13210-60004	1626	1 thru 4
NA	Disc Interface 1 PCA	13210-60004	1710	5 thru 7
NA	Disc Interface 1 PCA	13210-60004	1715	8 thru 10

Changes 1 thru 4 dated 17 March 1977.
Changes 5 thru 7 dated 22 April 1977.
Changes 8 thru 10 dated 28 November 1977.

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Printed in U.S.A.

CHANGE	DESCRIPTION
1	Title page. Change series code for 13210-60004 to 1626.
2	Page 5-2, table 5-2. Change as follows: a. Delete "63" from REFERENCE DESIGNATION column for entry beginning with U35. b. Change "U73, 82" entry in REFERENCE DESIGNATION column to read "U82". c. Add entries for U63 and U73 as follows: U63; 1820-1367; INTEGRATED CIRCUIT TTL; 01295; SN74S08N U73; 1820-1449; INTEGRATED CIRCUIT TTL; 01295; SN74S32N
3	Page 5-3, figure 5-1. Change PCA series number to "1626".
4	Page 5-5, figure 5-2. Change as follows: a. Zone A2. Add "1626" to series numbers. b. Zone B3. For IOO(B) signal, change "(E3)" to "(E3, F6)". c. Zone A3. At top of U77, connect pins 1, 2, 11, and 23 to signal ground. d. Zone C5. At right side of U102, change pin "6" to "9" and pin "9" to "6". e. Zone C7. At pin 4 of U21, change "$\overline{\text{CRS}}$ (B17)" to read "$\overline{\text{XFER CYL}}$ (B12)". f. Zone B11. At U35B, pin 6, show a signal line labeled "IOI(B)(F6)". g. Zone C11. Change zone designation under signal $\overline{\text{DEN}}$ from "(E5)" to "(F7)". h. Zone F14. Change "U66F" to read "U66E". i. Zone B17, 18. Delete zone designation "C7" from beneath signal $\overline{\text{CRS}}$. j. Zone F5, 6, 7. At U33B, pin 8, add the circuit shown in figure US-1. k. Zone B12. Change input connections to U35D and U52A as shown in figure US-2.
5	Title page. Change series code for 13210-60004 to 1710.
6	Page 5-3, figure 5-1. Change PCA series number to 1710.
7	Page 5-5, figure 5-2. Change as follows: a. Zone A2. Add "1710" to series numbers. b. Zone F5, 6, 7. Change U22B to U35D and change pin numbers and inputs as shown in figure US-3. c. Zone B12. Change U35D to U22B, add "$\overline{\text{CRS}}$" input connection, and change pin numbers as shown in figure US-4.
8	Title page. Change series code for 13210-60004 to 1715.

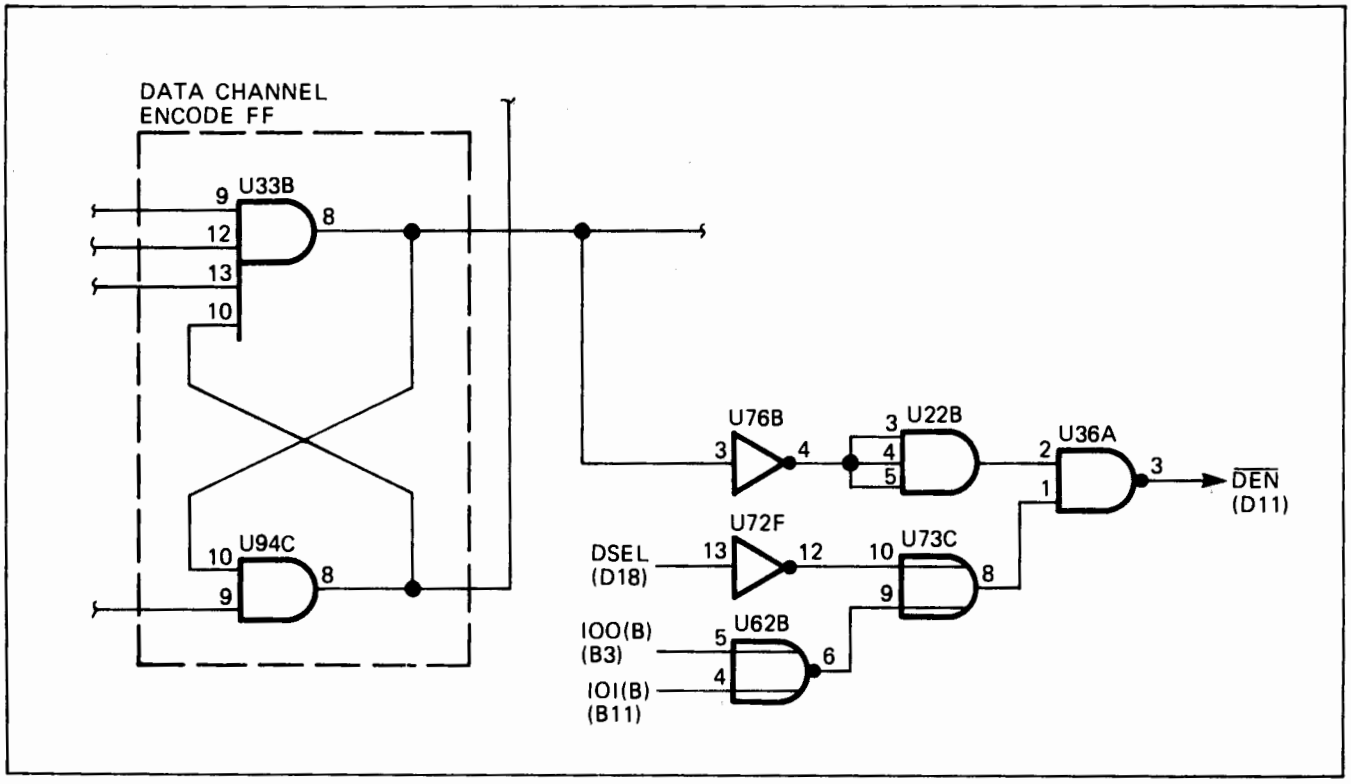


Figure US-1. Addition to Figure 5-2 at Zone F5, 6, 7

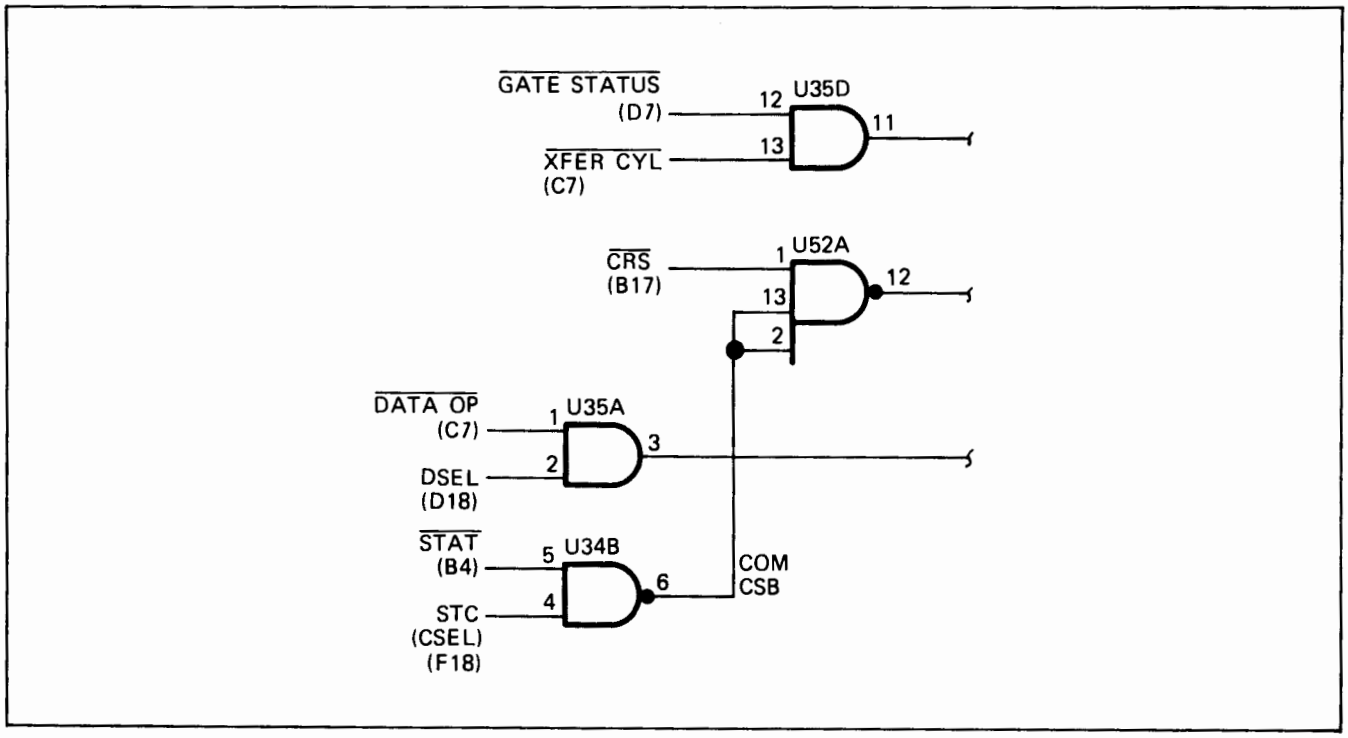


Figure US-2. Change to Figure 5-2 at Zone B12

CHANGE	DESCRIPTION
9	Page 5-2, table 5-2. Change as follows: a. For first capacitor entry, change REFERENCE DESIGNATION column entry to read "C1 thru C12, C15 thru C20". Change HP PART NO. to "0160-2055", MFR CODE to "56289", and MFR PART NO. to "C023F101F103ZS22-CDH". b. Add entries for C21 and C22 as follows: C21: 0180-1746; CAPACITOR, fxd, Ta, 15 μF, ±10%, 20 VDCW; 56289; 150D156X9020B2 C22: 0180-0309; CAPACITOR, fxd, Ta, 4.7 μF, ±20%, 10 VDCW; 56289; 150D475X0010A2
10	Page 5-3, figure 5-1. Change as follows: a. Change PCA series number to "1715". b. Add "C19" between U102 and U92. c. Add "C20" adjacent to upper right corner of U11. d. Add "C21" to right of R6. e. Add "C22" between U77 and R13.

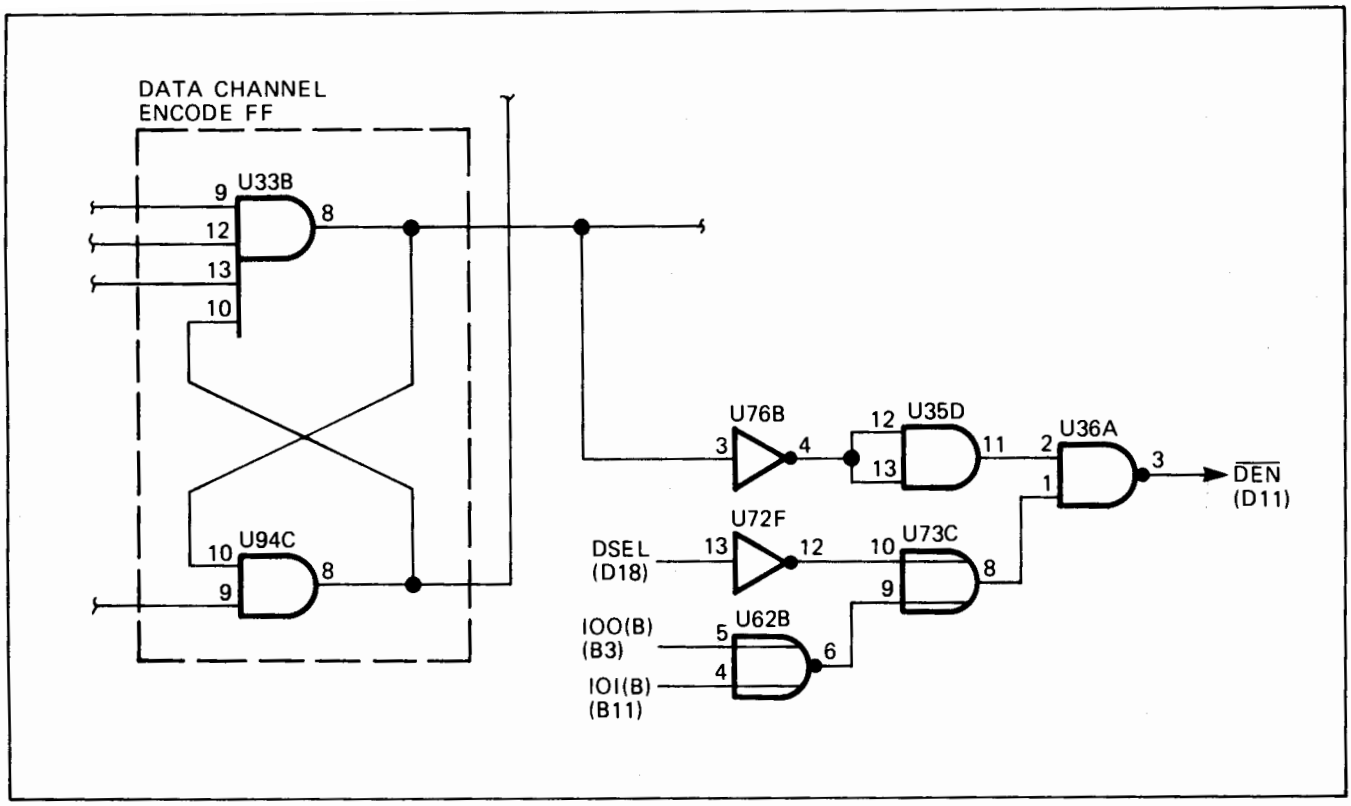


Figure US-3. Change to Figure 5-2 at Zone F5, 6, 7

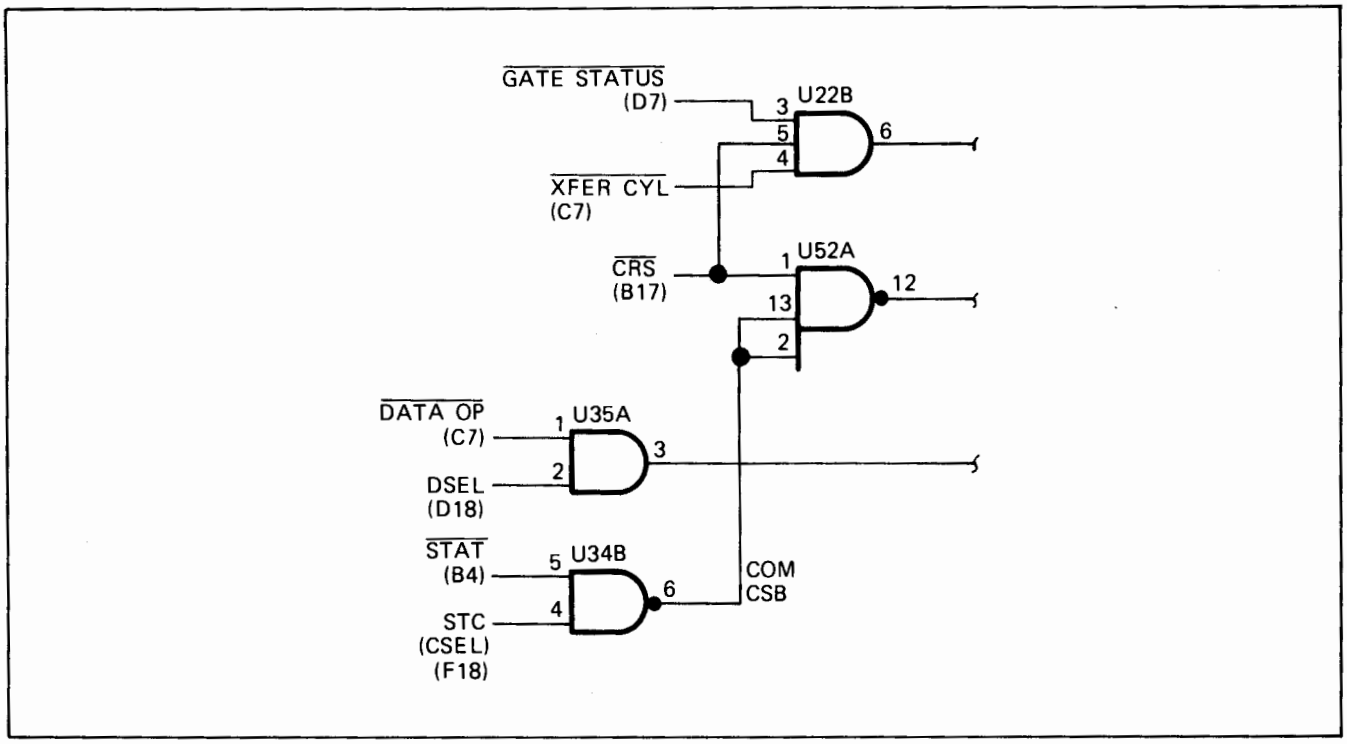


Figure US-4. Change to Figure 5-2 at Zone B12

TABLES

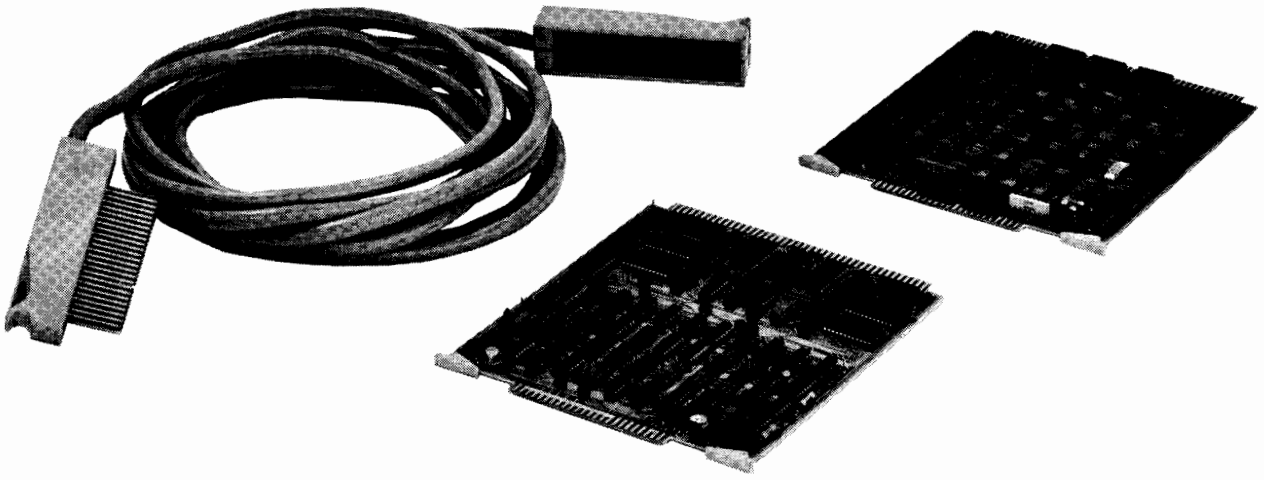


Figure 1-1. HP 13210A Disc Drive Interface Kit

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides general information, installation, programming, theory of operation, maintenance, and replaceable parts information for the HP 13210A Disc Drive Interface Kit. (See figure 1-1.)

1-3. GENERAL DESCRIPTION.

1-4. The kit includes the control circuits and cable for connecting the HP 7900 Series Disc Drives to the HP 2100 Series Computers with Direct Memory Access (DMA)* capability. The control circuits are on two plug-in printed-circuit assemblies (PCA's) which install in the I/O portion of the computer card cage. The cable connects the PCA's to the disc drive.

Note

The plug-in PCA's should only be installed in HP computers with DMA* capability. The PCA's should not be installed in the HP 2150A or 2150B Input/Output and Memory Extender, or in the HP 2151A Input/Output Extender. The extenders do not have the DMA capability necessary to operate the disc drive.

1-5. INTERFACE KIT CONTENTS.

1-6. The interface kit contains the following:

a. Disc Interface 1 printed-circuit assembly (part no. 13210-60004).

b. Disc Interface 2 printed-circuit assembly (part no. 13210-60000).

c. Interconnecting Cable, 20 feet long (part no. 13210-60003).

d. Operating and Service Manual (part no. 13210-90003).

1-7. IDENTIFICATION.

1-8. Hewlett-Packard uses five digits and a letter (00000A) to identify standard interface kits. If the designation of the kit received does not agree with the designation on the title page of this manual, there are differences between the kit received and the kit described in this manual. These differences are explained in manual supplements available at HP Sales and Service Offices. (Addresses of these offices are listed at the back of this manual.)

1-9. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the PCA. The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the positions of the components. The two-digit division code identifies the division of Hewlett-Packard that manufactured the PCA. If the series code numbers do not correspond exactly with the code numbers on the title page of this manual, the PCA's differ from those described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office.

1-10. The interface cable is identified by a part number, marked on one of the plugs attached to the cable.

1-11. The manual and manual supplements are identified by title, part number, and publication date, marked on the title page of the document.

1-12. SPECIFICATIONS.

1-13. Specifications for the interface kit components are listed in table 1-1.

Table 1-1. HP 13210A Disc Drive Interface Kit Specifications

Data Rate to/from HP 7900 Series Disc Drive:	2,500,000 bits/second*
Data Rate to/from HP Computers:	156,250 words/second*
Computer Power Supply Requirements:	+5V: 4A -2V: 140 mA +12V: 60 mA -12V: 100 mA

*The high data rate requires that the computer have at least one DMA channel.

*Dual Channel Port Controller (DCPC) in HP 21MX Series Computers.

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides information for unpacking, initial inspection, and installation for the HP 13210A Disc Drive Interface Kit. The computer, disc drive, and disc drive power supply should be installed and prepared for operation before installing the interface kit.

2-3. UNPACKING AND INITIAL INSPECTION.

2-4. If the disc drive interface kit is received separately from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the box rattles, request that the carrier's agent be present when the carton is opened.

2-5. Inspect each component of the kit as the parts are unpacked. If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-6. INSTALLATION.

2-7. Install the disc drive interface kit as follows:

a. Set POWER switch on disc drive power supply to OFF.

b. Set computer POWER switch to OFF.

c. Open the computer for access to I/O card slots and install the 13210-60004 Disc Interface 1 PCA into the card slot corresponding to the desired I/O select code.

d. Install the 13210-60000 Disc Interface 2 PCA into the next lower priority slot.

e. Connect the double-connector end of the interface cable to the PCA's so that the DISC INTERFACE 1 portion of the connector fits onto the disc interface 1 PCA and the DISC INTERFACE 2 portion fits onto the disc interface 2 PCA.

f. Connect the single-connector end of the interface cable to the I/O connector at the back of the disc drive with the "cable-end" of the connector routed across the back of the disc drive.

SECTION III
PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains programming considerations for systems employing the HP 13210A Disc Drive Interface Kit. Included are disc drive characteristics, command and status descriptions, programming recommendations, and a typical assembly language program.

3-3. DISC DRIVE CHARACTERISTICS.

3-4. The interface kit will interface an HP 2100 Series Computer to as many as four HP 7900 Series Disc Drives using discs with the following characteristics.

a. Each disc stores 203 cylinders of information.

b. Each cylinder contains 96 addressable sectors, 24 on the top surface of each disc and 24 on the bottom surface of each disc.

c. Each sector contains a sector address field and a data field. The address field contains cylinder, head, and sector numbers of the sector, and indicators for defective and protected cylinder; the data field contains as many as 128 sixteen-bit data words.

3-5. The interface kit requires two adjacent computer I/O addresses: a data channel and a command channel address. The data channel is assigned the higher priority (lower number) I/O address.

3-6. COMMAND DESCRIPTIONS.

3-7. All commands are transferred through the computer A- or B-register by an OTA/B instruction addressed to the command channel. Commands are then stored by the interface. An STC,C instruction will set the command channel Control FF and the Encode FF which will cause the interface to execute the command. When multiple OTA/B instructions are received before the STC,C instruction, the interface will execute the last OTA/B instruction issued. When the command issued is Status Check, Seek Record, or Address Record, the interface will accept another command as soon as the required data transfer through the data channel has been completed. For all other commands, new commands must not be issued until the command channel Flag FF is set to indicate completion of the current operation.

Note

Because the interface will only respond to a positive-going Encode signal, during multiple Seek Record operations the command channel Control FF must be cleared (CLC) before a subsequent STC,C instruction will be recognized.

3-8. The command word consists of a four-bit command code and a two-bit drive select. (An additional two bits are used with the Initialize Data command.) The command word format is shown in figure 3-1. The four-bit command code contains the binary code of the command to be executed. Table 3-1 lists the commands to which the interface will respond. Commands other than those listed will cause improper operation. The two-bit drive select contains the binary code of the disc drive that is to execute the command.

Table 3-1. Computer to Interface Commands

COMMAND	BITS			
	15	14	13	12
Status Check	0	0	0	0
Write Data	0	0	0	1
Read Data	0	0	1	0
Seek Record	0	0	1	1
Refine Sector	0	1	0	1
Check Data	0	1	1	0
Initialize Data	1	0	0	1
Address Record	1	0	1	1

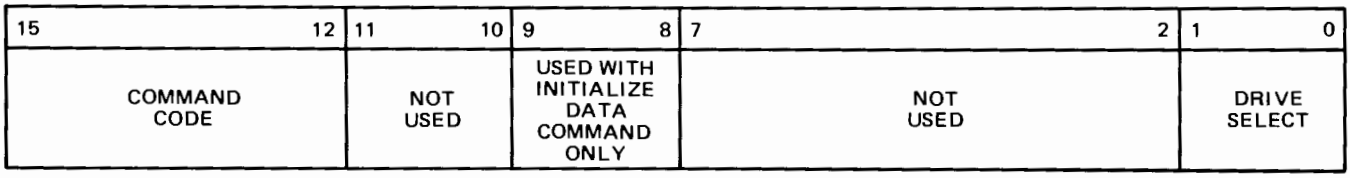


Figure 3-1. Command Word Format

3-9. Commands, addresses, and status are transferred to and from the interface by an OTA/B or LIA/B instruction addressed to the data channel. Data records are transferred to and from the interface under DMA control. The data channel Encode FF must be set for data transfer to take place between the interface and disc drive. The data channel Flag FF will be set by the interface to indicate that data transfer may take place.

3-10. Drive attention status bits are transferred to the computer by an LIA/B or MIA/B instruction addressed to the command channel. Only the four lowest order bits of the data word are used. Each bit position represents a disc drive address; bit position 0 corresponds to disc drive 0, etc. Valid attention status bits are set between the setting of the command channel Flag FF and the next STC instruction to indicate that the disc drive has become ready or is completing a Seek operation.

3-11. STATUS CHECK.

3-12. The Status Check command causes the interface to assemble the status word of the desired disc drive and transfer the word to the computer through the data channel. Command execution is completed when the computer accepts the status word from the data channel; the command channel Flag FF is not set for this operation. A Status Check operation should be performed to verify proper execution of preceding operations. Status word bit definitions are given in paragraph 3-38. Status is changed only with a non-status operation.

3-13. WRITE DATA.

3-14. The Write Data command causes the interface to write data on a disc. The desired head and sector addresses must be present in the interface record address register (RAR) and the heads must be positioned over the correct cylinder before the Write Data command is issued. When the addressed sector comes into position under the head, the interface will examine the cylinder condition indicators and address information in the address field and cyclic check the entire sector. If the cylinder is not protected or defective and the address compares with the address in the RAR, the interface will increment the sector address in the RAR and initiate writing in the next sector.

3-15. The interface will write the address field and then write the data from the data channel. If the computer sends less than 128 data words, the interface will write zeros in the remainder of the sector before setting the command channel Flag FF. If the computer sends more than 128 data words, the interface will increment the sector address in the RAR and continue to write in the next sector. (Data transfer will be suspended while the interface writes the address field.) Writing will continue in this manner until the computer ends data transfer or until the interface detects an end-of-cylinder (EOC) signal or error condition, at which time the command channel Flag FF will be set. (When writing begins on the upper disc surface writing will continue in all sectors of the addressed cylinder on the bottom surface before EOC will be detected.)

3-16. If, during the examination of the address field, the defective cylinder indicator (DCI) is set, if the protected cylinder indicator (PCI) is set and the disc drive OVERRIDE switch is set to PROTECT, or if the disc drive DATA PROTECT switch for the addressed head is on, the command channel Flag FF will be set and no writing or data transfer will take place. A Status Check command should be issued to determine the cause of the termination.

3-17. READ DATA.

3-18. The Read Data command causes the interface to read the addressed record and transfer the data field to the computer. The record address must be present in the interface record address register (RAR) and the heads must be positioned over the correct cylinder before the Read Data command is issued. When the command is issued, the interface will increment the sector address in the RAR and, when the addressed sector comes into position, examine the address field for the defective cylinder indicator. The interface then compares the sector address to the address in the RAR before initiating data transfer to the computer. If the computer accepts less than 128 data words, the interface will cyclic check the remainder of the data field before setting the command channel Flag FF. If the computer will accept more than 128 data words, the interface will increment the sector address in the RAR and continue to read the next sector. (Data transfer will be suspended while the interface examines the address field.) Reading will continue until the computer stops accepting data or until the interface detects an end-of-cylinder (EOC) signal or error condition, at which time the command channel Flag FF will be set.

3-19. If, during the examination of the address field, the defective cylinder indicator (DCI) is set or the sector address does not compare with the address in the RAR, reading will continue to the end of the current sector before data transfer is halted and the command channel Flag FF is set. A Status Check operation should be performed to determine the exact cause for termination. A Status Check operation after normal termination will determine if the protected cylinder indicator was set or if the disc drive DATA PROTECT switch for the addressed head was on.

3-20. SEEK RECORD.

3-21. The Seek Record command causes the interface to execute a head-positioning operation in the addressed disc drive. When the command is issued, the interface will select the addressed disc drive and accept two 16-bit words of address information (addressed to the data channel) that are required for the head-positioning operation. When a cylinder address word has been transferred to the interface, the interface will set the data channel Flag FF to indicate acceptance of the address. The first word should contain the cylinder to which the heads should move. The second word should contain the head and sector addresses. Address word formats are shown in figure 3-2.

15 8	7 0
NOT USED	CYLINDER ADDRESS

15 10	9 8	7 5	4 0
NOT USED	HEAD ADDRESS	NOT USED	SECTOR ADDRESS

Figure 3-2. Address Word Formats for Seek Record Command

3-22. The two address words will be stored as a new record address in the interface RAR. The interface will then transfer the record address to the disc drive and initiate the head-positioning operation. Although the command channel Flag FF is not set until head positioning is complete, the interface will be free to perform other operations as soon as the second word of address information is accepted. As a result, simultaneous operations with parallel-connected disc drives are possible.

3-23. If the addressed disc drive has a head-positioning operation in progress when a new Seek Record command is issued, the heads will be positioned over the former addressed cylinder, but the latter addressed head and sector will be selected. Seek check status will be set. Seek check status will also be set if the cylinder address is greater than 202, or if the sector address is greater than 23.

3-24. REFINE SECTOR.

3-25. The Refine Sector command causes the interface to straddle-erase the addressed record as an attempt to improve the magnetic characteristics of the record. The command should only be used after retry procedures fail to recover the data. The record address must be present in the interface record address register (RAR) before the Refine Sector command is issued.

3-26. When the command is issued, the interface will increment the sector address in the RAR and straddle-erase the addressed sector; no writing or reading will take place. No examination of the address field for defective or protected cylinders or address comparison will take place. The command channel Flag FF will be set when the end of the addressed sector is reached.

3-27. CHECK DATA.

3-28. The Check Data command causes the interface to cyclic check data records of a specific number of sectors to verify recoverability of the data. The Check Data operation is similar to a Read Data operation except that no data transfer takes place. The beginning address of the cyclic check must be in the interface record address register (RAR), and the heads must be positioned over the correct cylinder before the Check Data command is issued.

3-29. When the command is issued, the interface will select the addressed disc drive and accept one 16-bit word of sector count information addressed to the data channel. The word format is shown in figure 3-3. The interface will increment the RAR and, when the addressed sector comes into position, examine the address field for the defective cylinder indicator, compare the sector address to the address in the RAR, and cyclic check the entire sector. The interface will then subtract one from the sector count and repeat the operation in the next sector until the sector count reaches zero or until the interface detects an end-of-cylinder signal or error condition, at which time the command channel Flag FF will be set.

3-30. If, during the examination of the address field, the defective cylinder indicator (DCI) is set or the sector address does not compare with the address in the RAR, the interface will halt the operation at the end of the current sector and set the command channel Flag FF. A Status Check operation should be performed to determine the exact cause for early termination. A Status Check operation after normal termination will determine if the protected cylinder indicator was set or if the disc drive DATA PROTECT switch for the addressed head was on.

15 6	5 0
NOT USED	SECTOR COUNT

Figure 3-3. Sector Count Word Format for Check Data Command

3-31. INITIALIZE DATA.

3-32. The Initialize Data command causes the interface to initialize unwritten cylinders and to generate the defective- and protected-cylinder indicators. The command will be accepted only when the disc drive OVERRIDE switch is set to ACCESS and the DATA PROTECT switch for the selected head is off. If the OVERRIDE switch is set to PROTECT or the DATA PROTECT switch is on, the command channel Flag FF will be set and no attempt will be made to execute the command. The Initialize Data operation is similar to a Write Data operation except that the interface does not examine the first sector address field for cylinder condition indicators or address information. The desired head and sector addresses must be present in the RAR and the heads must be positioned over the correct cylinder before the Initialize Data command is issued.

3-33. When the command is issued the interface will select the addressed disc drive and increment the RAR. When the addressed sector comes into position, the interface will assemble and write the address field. The address information is that in the RAR; the cylinder condition indicator information is contained in bits 8 and 9 of the command word. If bit 8 is set, the defective cylinder indicator will be set and an incorrect address will be written in the address field; if bit 9 is set, the protected cylinder indicator will be set; if both bits 8 and 9 are set, only the defective cylinder indicator is set.

3-34. Data transfer from the computer will begin with the first data word. If the computer sends less than 128 sixteen-bit words, the interface will write zeros in the remainder of the data field. If the computer sends more than 128 data words, the interface will increment the sector address in the RAR and continue to write in the next sector. (Data transfer will be suspended while the interface writes the address field.) Writing will continue in this manner until the computer ends data transfer or until the interface detects an end-of-cylinder signal or error condition, at which time the command channel Flag FF will be set.

3-35. ADDRESS RECORD.

3-36. The Address Record command causes the interface to alter the contents of the record address register. The Address Record operation is similar to a Seek Record operation except that no operation is performed by the disc drive.

3-37. When the command is issued, the interface accepts two words of address information addressed to the data channel. The first word should contain the cylinder number to which the heads should move; the second word should contain the head and sector addresses. Address word formats are shown in figure 3-2. When the second address word has been accepted, the command channel Flag FF will be set.

3-38. STATUS DESCRIPTIONS.

3-39. Status information is transferred to the computer A- or B-register by either an LIA/B or MIA/B instruction addressed to the data channel. The status word may be transferred any time the disc drive is selected. Individual status bits are listed in table 3-2.

3-40. ANY ERROR.

3-41. Any-error status (bit 0) is set when any of the other status bits are set, except flagged cylinder status (bit 3) or data protect status (bit 10). Any-error status is set when flagged cylinder status is set as a result of an attempt to write on a protected cylinder or initialize a cylinder with the disc drive OVERRIDE switch set to PROTECT. Any-error status is also set with flagged cylinder status when attempting to write, read, or check data on a defective cylinder (because the defective cylinder will set address error status). However, any-error status will not be set with flagged cylinder status when attempting to read or check data on a protected cylinder or attempting to write on a protected cylinder with the OVERRIDE switch set to ACCESS.

3-42. DATA ERROR.

3-43. Data error status (bit 1) is set if any of the following conditions exist:

a. During Read Data, Check Data, or Write Data if the interface fails to synchronize the data clock with the serial datum bits or if the interface detects an error when cyclic checking.

b. During Write Data, Read Data, Refine Sector, Check Data or Initialize Data if the disc drive becomes not-ready during data handling.

Data error status is cleared with execution of the Status Check command.

Table 3-2. Status Word Bits

BIT	STATUS
0	Any Error
1	Data Error
2	Drive Busy
3	Flagged Cylinder
4	Address Error
5	End of Cylinder
6	Not Ready
7	Not Used
8	Seek Check
9	Not Used
10	Data Protect
11	Drive Unsafe
12	Not Used
13	Overrun
14	First Status
15	Not Used

3-44. DRIVE BUSY.

3-45. Drive busy status (bit 2) is set when the disc drive is executing a Seek Record command (from the time the last address word is accepted until head-positioning is complete).

3-46. FLAGGED CYLINDER.

3-47. Flagged cylinder status (bit 3) is set if any of the following conditions exist:

a. During Initialize Data if the OVERRIDE switch on the disc drive is set to PROTECT.

b. During Initialize Data or Write Data if the disc drive DATA PROTECT switch for the addressed head is on.

c. During Read Data, Check Data, or Write Data if the interface detects a protected or defective cylinder indicator. If a defective cylinder is detected, address error status is also set. (Flagged cylinder status will not be set if an actual address errorr is detected in the same sector.)

Flagged cylinder status is cleared with the execution of the Status Check command.

3-48. ADDRESS ERROR.

3-49. Address error status (bit 4) is set during Read Data, Check Data, or the first-sector checking phase of Write Data if the sector address read does not compare with the address in the RAR or if the defective cylinder indicator is set (set with flagged cylinder status bit). Address error status is cleared with the execution of the Status Check command.

3-50. END OF CYLINDER.

3-51. End-of-cylinder status (bit 5) is set if any of the following conditions exist:

a. During the data transfer portion of Write Data, Read Data, or Initialize Data if the interface has reached the end of the data field for sector 23, head 1 or 3, and the computer signals for continuation of data transfer into the next sector.

b. During the cyclic check portion of Check Data if the interface has reached the end of the data field for sector 23, head address 1 or 3, anytime the cyclic check sector count is not zero.

End-of-cylinder status is cleared with execution of the Status Check command.

3-52. NOT READY.

3-53. Not ready status (bit 6) is set if the selected disc drive is not attached to the interface, if the disc is not up to speed or the heads are not loaded, or if the disc drive is in an unsafe condition, in which case drive unsafe status (bit 11) will also be set. Operator intervention may be required to bring the disc drive to the ready state.

3-54. SEEK CHECK.

3-55. Seek check status (bit 8) is set if a Seek Record command has been issued and one of the following conditions exist:

a. The cylinder addressed is greater than 202.

b. The sector addressed is greater than 23.

c. A head-positioning operation is still in progress.

Seek check status is cleared by the next proper Seek Record command issued to the selected disc drive.

3-56. DATA PROTECT.

3-57. Data protect status (bit 10) is set if the disc drive DATA PROTECT switch for the addressed head is on. Write Data and Initialize Data commands will not be accepted. (Any-error and flagged cylinder status will also be set if either of these commands is issued.)

3-58. DRIVE UNSAFE.

3-59. Drive unsafe status (bit 11) is set if the disc drive checking circuits detect an unsafe condition in the disc drive access system or read/write electronics. Not ready status will also be set.

3-60. OVERRUN.

3-61. Overrun status (bit 13) is set if either of the following conditions exist:

a. During the data transfer portion of Write Data, Read Data, or Initialize Data if the computer attempts to transfer data after the maximum response time but before the interface sets the command channel Flag FF to signal operation completion. The computer DMA must respond to a data channel Flag FF signal within 5.9 microseconds.

b. During Write Data, Read Data, Check Data, or Initialize Data if a sector pulse is detected before the end of the data field of the current sector is detected.

Overrun status is cleared with the execution of a Status Check command.

3-62. FIRST STATUS.

3-63. First status (bit 14) is set when the selected disc drive goes from not-ready to ready status. First status is cleared with the execution of a Status Check command.

3-64. PROGRAMMING CONSIDERATIONS.

3-65. WRITE CHECKING.

3-66. When records are written, a program check should be performed to ensure that the record in memory was written on the disc without error and that the data can be recovered from the disc without error. When data integrity is crucial, each record should be read after being written and compared, a word at a time, with the original record in memory. This technique provides a check of both the parallel transfer between computer and interface, and serial data transfer between interface and disc drive. When data integrity is less crucial, issuance of a Check Data command will check just the serial data transfer between interface and disc drive.

3-67. DISC INITIALIZATION.

3-68. Prior to use in system, new, unwritten discs should be processed with a disc initialization program. The program should write the address field for all sectors, and should execute additional data testing to help isolate defects that may have developed after manufacture.

3-69. The additional data testing should include the following routine executed six times on each cylinder:

a. Write a fixed data pattern in all data fields of the cylinder. On each of the six passes a different data pattern should be used. The six recommended patterns are listed below in octal notation:

(1)	0	0	0	0	0	0
(2)	1	7	7	7	7	7
(3)	1	2	5	2	5	2
(4)	0	5	2	5	2	5
(5)	1	6	2	7	4	5
(6)	1	7	0	3	6	0

b. Execute a Check Data command 10 times on all data fields of the cylinder. If a data error occurs more than once in executing the routine on a cylinder, the cylinder should be flagged defective.

3-70. ERROR RECOVERY PROCEDURES.

3-71. Errors which occur in the storage system are often correctable by using retry procedures. Programs should include retry procedures to reduce the number of errors that will affect system operation. Paragraphs 3-72 through 3-76 list specific correctable error conditions and recommended retry procedures.

3-72. DATA ERROR DURING READ DATA. When a data error occurs during a Read Data operation, issue the following retry procedure.

a. Read the record 16 times.

b. If the error persists, issue a Seek Record command to cylinder zero, then to cylinder 202, and return to the failing cylinder.

c. Read the record 16 times.

d. If the error persists, issue a Refine Data command and read the record 16 times.

e. If the error persists, terminate the retry procedure.

3-73. DATA ERROR DURING WRITE DATA OR INITIALIZE DATA. When a data error occurs during a Write Data or Initialize Data operation, re-issue the command once and if the error persists, terminate the retry procedure.

3-74. ERRORS DURING WRITE CHECKING ROUTINES. When a data error occurs during the Read Data or Check Data portion of a write-checking routine (refer to paragraph 3-65), the complete write and write-checking routine should be tried 16 times. If the error persists, terminate the retry procedure. If an error is detected during the memory/record comparison, the write and write-checking routine should be retried once.

3-75. ADDRESS ERRORS. When an address error occurs, the interface will automatically return the heads to cylinder zero. Re-issue the Seek Record command to the failing cylinder and if the error persists, terminate the retry procedure.

3-76. OVERRUNS. If an overrun occurs, retry the operation once and if the error persists, terminate the retry procedure.

3-77. TYPICAL PROGRAM.

3-78. Table 3-3 is a typical assembly language program that will transfer data to and from the disc drive under DMA control and check status.

Table 3-3. Typical Assembly Language Program

```
                                READ PROGRAM (NON INTERRUPT)

CW1A    OCT     1 2 0 0 U U     DMA PROGRAM CONTROL WORD, UU IS DATA CHANNEL SELECT CODE
CW2B    OCT     1 A A A A A     DMA STARTING ADDRESS; DATA INTO MEMORY (MAX. ADDR. = 77777B)
CW3A    OCT     -0 B B B B B    DMA WORD COUNT (MAX. COUNT - 06144B, 2's COMPLEMENT i.e., 171634B)
RDCMD   OCT     0 2 0 0 0 0     READ COMMAND WORD
DN      NOP                     DRIVE NUMBER (0 THROUGH 3)

        JSB     SEEK            MOVE HEAD TO DESIRED CYLINDER
        CLC     DC              INSURE CONTROL SIGNALS ARE RESET ON
        CLC     CC              DATA AND COMMAND CHANNELS
        LDA     CW1A            GET FIRST DMA CONTROL WORD
        OTA     6               OUTPUT TO DMA CHANNEL
        CLC     2               PREPARE DMA FOR DMA CONTROL WORD 2
        LDA     CW2B            GET DMA CONTROL WORD 2
        OTA     2               OUTPUT TO DMA CHANNEL
        STC     2               PREPARE DMA FOR DMA CONTROL WORD 3
        LDA     CW3A            GET DMA CONTROL WORD 3
        OTA     2               OUTPUT TO DMA CHANNEL
        LDA     RDCMD           GET INTERFACE READ COMMAND WORD
        IOR     DN
        OTA     CC              OUTPUT TO COMMAND CHANNEL
        STC     DC,C            PREPARE DATA CHANNEL FOR READ OPERATION
        STC     6,C             ACTIVATE DMA
        STC     CC,C            INITIATE READ OPERATION
        SFS     CC              IS READ OPERATION COMPLETE
        JMP     *-1             NO. WAIT.
        JSB     STATS           YES. GO CHECK STATUS

                                WRITE PROGRAM (NON INTERRUPT)

CW1A    OCT     1 2 0 0 U U     DMA PROGRAM CONTROL WORD, UU IS DATA CHANNEL SELECT CODE
CW2A    OCT     0 A A A A A     DMA STARTING ADDRESS; DATA OUT OF MEMORY (MAX. ADDR. = 77777B)
CW3A    OCT     -0 B B B B B    DMA WORD COUNT (MAX. COUNT = 06144B, 2's COMPLEMENT i.e., 171634B)
WRCMD   OCT     0 1 0 0 0 0     WRITE COMMAND WORD
DC      EQU     UU              UU IS DATA CHANNEL SELECT CODE
CC      EQU     VV              VV IS COMMAND CHANNEL SELECT CODE
DN      NOP                     DRIVE NUMBER (0 THROUGH 3)

        JSB     SEEK            MOVE HEAD TO DESIRED CYLINDER
        CLC     DC              INSURE CONTROL SIGNALS ARE RESET
        CLC     CC              ON DATA AND COMMAND CHANNELS.
        LDA     CW1A            GET FIRST DMA CONTROL WORD
        OTA     6               OUTPUT TO DMA CHANNEL
        CLC     2               PREPARE DMA FOR DMA CONTROL WORD 2
        LDA     CW2A            GET SECOND DMA CONTROL WORD
        OTA     2               OUTPUT TO DMA CHANNEL
        STC     2               PREPARE DMA FOR DMA CONTROL WORD 3
        LDA     CW3A            GET THIRD DMA CONTROL WORD
        OTA     2               OUTPUT TO DMA CHANNEL
        STC     DC
        STF     DC              ENABLE DMA TO DATA CHANNEL DATA TRANSFER
        STC     6,C             ACTIVATE DMA
        LDA     WRCMD           GET INTERFACE WRITE COMMAND WORD
        IOR     DN
```

Table 3-3. Typical Assembly Language Program (Continued)

```
                        WRITE PROGRAM (NON INTERRUPT) (Continued)

         OTA    CC          OUTPUT COMMAND WORD TO COMMAND CHANNEL
         STC    CC,C        INITIATE WRITE COMMAND
         SFS    CC          IS WRITE OPERATION COMPLETE?
         JMP    *-1         NO. WAIT
         JSB    STATS       YES. GO CHECK STATUS.

                        SEEK SUBROUTINE (NON INTERRUPT)

DC       EQU    UU          UU IS DATA CHANNEL SELECT CODE
CC       EQU    VV          VV IS COMMAND CHANNEL SELECT CODE
CYLNO    OCT    0 0 W W W   WWW IS CYLINDER NUMBER
HDSEC    OCT    0 0 X X X X XXXX IS FORMATTED HEAD AND SECTOR NUMBER
SKCMD    OCT    0 3 0 0 0 0 SEEK COMMAND WORD
DN       NOP                DRIVE NUMBER (0 – 3)

SEEK     NOP                SUBROUTINE ENTRY POINT
         CLC    DC          INSURE CONTROL SIGNALS ARE RESET
         CLC    CC          ON DATA AND COMMAND CHANNELS
         LDA    CYLNO       GET DESIRED CYLINDER ADDRESS
         OTA    DC
         STC    DC,C        OUTPUT CYLINDER ADDRESS TO DATA CHANNEL
         LDA    SKCMD       GET SEEK COMMAND WORD
         IOR    DN
         OTA    CC          OUTPUT SEEK COMMAND TO COMMAND CHANNEL
         STC    CC,C        INITIATE SEEK COMMAND
         SFS    DC          FIRST ADDRESS WORD ACCEPTED?
         JMP    *-1         NO. WAIT.
         LDA    HDSEC       YES. GET HEAD/SECTOR ADDRESS WORD.
         OTA    DC
         STC    DC,C        OUTPUT HEAD/SECTOR ADDRESS TO DATA CHANNEL
         SFS    CC          SEEK OPERATION COMPLETE?
         JMP    *-1         NO. WAIT
         JSB    STATS       YES. GO CHECK STATUS
         JMP    SEEK, I     RETURN TO CALLING PROGRAM

                           STATUS CHECK SUBROUTINE

DC       EQU    UU          UU IS DATA CHANNEL SELECT CODE
CC       EQU    VV          VV IS COMMAND CHANNEL SELECT CODE
STCMD    OCT    0 0 0 0 0 0 STATUS CHECK COMMAND WORD
DN       NOP                DRIVE NUMBER (0 THROUGH 3)

STATS    NOP                ENTRY POINT
         CLC    DC          INSURE CONTROL SIGNALS ARE
         CLC    CC          RESET ON COMMAND AND DATA CHANNELS
         LDA    STCMD       GET STATUS CHECK COMMAND WORD
         IOR    DN
         OTA    CC          OUTPUT TO COMMAND CHANNEL
         STC    CC,C        INITIATE STATUS CHECK COMMAND
         SFS    DC          IS STATUS WORD READY?
         JMP    *-1         NO. WAIT
         LIA    DC          LOAD STATUS WORD
         SLA                IS ANY ERROR BIT SET?
         JMP    ERROR       YES. GO TO ERROR ROUTINE.
         JMP    STATS, I    NO. RETURN TO CALLING PROGRAM
```

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains theory of operation and operational flow diagrams for the 13210A Disc Drive Interface Kit. Block diagrams for the two interface PCA's are shown in figures 4-3 and 4-4. Operation is shown in figures 4-5 through 4-7.

4-3. FUNCTIONAL DESCRIPTION.

4-4. POWER ON.

4-5. When power is initially applied to the computer, the POPIO and CRS signals are received simultaneously from the computer's I/O control PCA. The signals establish initial operating conditions for the interface PCA's. The POPIO signal sets both the command channel and data channel Flag FF's. The CRS signal clears the command channel Control FF and the data channel Encode FF, clears the Attention register, and transfers cylinder address 000 to the disc drive.

4-6. Once the computer sends the PON signal to the disc interface 1 PCA, the disc interface 1 PCA issues a Control signal to the disc drive. The Control signal indicates to the disc drive that the computer dc power supplies have stabilized.

4-7. COMMAND EXECUTION.

4-8. For the disc drive(s) to perform any operation commanded by the computer the interface must execute numerous internal operations. These internal operations, and the associated decision-making, are synchronously performed by a state decoder that is activated by a read-only memory (ROM) and a state register. Synchronous operation is provided by a 2.5-MHz Control Clock signal that is generated by a 10-MHz crystal oscillator and divider. See figure 4-3.

4-9. Each four-bit command word is applied to the ROM as part of an eight-bit address. Each addressed ROM memory location contains a unique four-bit word that is synchronously loaded into the state register. The state register output is decoded by the state decoder, whose outputs serve as internal "instructions" for the interface. By monitoring the ROM output, disc drive status, and other interface signals, a qualifier encoder alters the ROM address, and the state decoder issues sequential instructions for the interface at the appropriate times.

4-10. In this manner, the interface controls the execution of computer commands that require multiple steps. For example, when a Seek Record command is received, the interface will control the transfer timing of the two-word record address between the computer and disc drive. The interface will then wait, if necessary, for the disc drive to move the heads over the addressed record, and will only signal the computer for additional commands when the disc drive has completed execution of the command. Commands requiring less complex internal operations (e.g. Read) are decoded directly by a command decoder and re-issued as a single-line command to the disc drive at the appropriate time. Although re-issuance of such a command is more direct, the ROM-state decoder circuitry described above is still required for the execution of these commands. When a Read command is received, for example, the ROM-state decoder circuits will control the actual reading of data from the disc drive and execute the transfer of read data to the computer.

4-11. DATA TRANSFER EXECUTION.

4-12. The execution of commands requiring data transfer also requires the interface to perform numerous internal operations. When data supplied by the computer is to be written by the disc drive, the interface control of the write operation includes: transferring record addresses, drive addresses, etc.; checking for correct address response by the disc drive; ensuring proper sector format (which includes an address field and a data field); adding clock information to the data being written; performing parallel-to-serial conversion of data words; generating check characters; and continuously monitoring the write operation until completed. When data is to be transferred to the computer, the interface control of the read operation includes: transferring record addresses, drive addresses, etc.; checking for correct address response by the disc drive; separating clock information from the data; performing serial-to-parallel conversion of data words; checking for data errors; and continuously monitoring the read operation until completed. See figure 4-4.

4-13. WRITE OPERATIONS. The format in which address fields and data fields are written on the disc is controlled by a sector formatter; clock information is added to the data by a write formatter. A detected sector pulse activates the formatter. By counting bits and 16-bit words and enabling data to be written at prescribed times, each sector is written in the format shown in figure 4-1. (The 2.5-MHz clock signal is generated by the 10-MHz crystal oscillator and divider mentioned above.)

4-14. Data words and address words are transferred from the computer through an output buffer register. Bits of the buffer register output that contain the address information

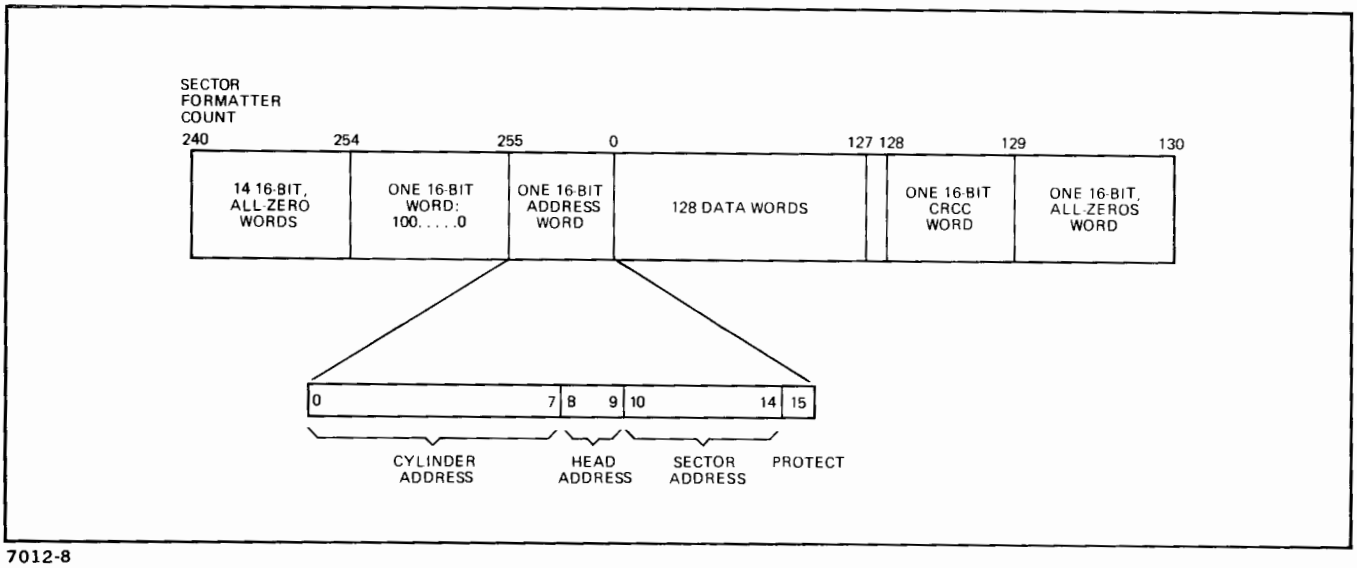


Figure 4-1. Sector Write Format

in an address word (all 16 bits are not used) are parallel-connected to a record address register (RAR). The outputs of both the buffer register and the RAR are applied to a multiplexer that transfers only one of the outputs at a time to a parallel-to-serial/serial-to-parallel converter. The sector formatter, described above, determines when the address field is to be written and strobes the RAR contents to the converter. When the sector formatter determines that the data field is to be written, the contents of the output buffer register are strobed to the converter. The serial output of the converter is routed through the sector formatter and write formatter described above.

4-15. Serial data from the output of the sector formatter is parallel-fed to a cyclic redundancy check character (CRCC) generator. The bit pattern of the 16-bit CRCC word is a function of the data field bit pattern and the Boolean equation of the CRCC generator. The CRCC word, when read at the end of a subsequent read operation, aids in determining if any read data errors occurred.

4-16. READ OPERATIONS. Serial data read from the disc drive is applied to a phase-lock loop in the read data decoder. Because variations in the rotational speed of disc drives causes the frequency of the clock information contained in the read data to vary, the phase-lock loop includes a voltage-controlled oscillator that provides the frequency flexibility required to compensate for these variations. The phase-lock loop produces a nominal output of 2.5 MHz, the precise frequency of the data when written. The combination of the phase-lock loop output and the read data input is used to separate the data from the clock information. Separated data is routed to the serial-to-parallel converter and to the CRCC generator. At the appropriate time (every 16th bit), the sector formatter loads the contents of the converter into the read buffer register. The read buffer register contents are strobed into the input buffer register for subsequent transfer to the computer. The CRCC generator monitors the read data, compares it with the CRCC word that is read at the end of each data field and sets the appropriate bit in the interface status register when a data error is detected.

4-17. DETAILED CIRCUIT DESCRIPTION.

4-18. COMMAND EXECUTION.

4-19. The four most significant bits of the words are loaded into the command output register U77 by an OTA/B instruction addressed to the command channel. The register contents are decoded by command decoder U83 and are routed to the read-only memory (ROM) U93 as part of an eight-bit address. The command decoder converts the four bits of command from the computer to single-line commands for transfer to the disc drive. The four-bit ROM outputs are translated by the state decoder U21, which issues additional "internal" instructions that are required to execute the computer command.

4-20. The qualifier encoder U103 provides one bit of the eight-bit ROM address. The level of the qualifier bit is determined by comparison of the current ROM state (in the state register) with various status signals from other interface circuits and the disc drive. As a result, the sequence of state decoder outputs is determined by the command issued and the current status of the interface and disc drive.

4-21. DATA TRANSFER OPERATIONS.

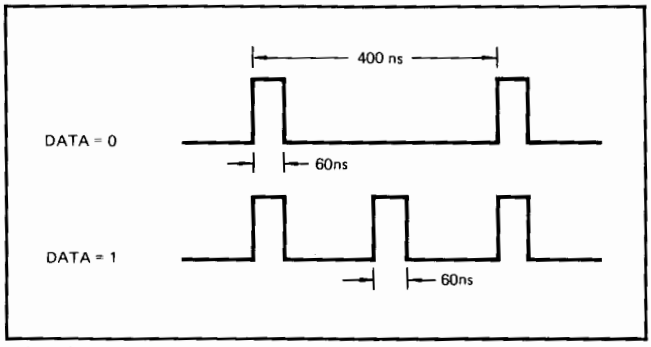
4-22. Record addresses and data from the computer are transferred through the output buffer register (U57 and U87). The register contents are parallel-connected to the record address register (RAR) (U56, U66, and U67) and the multiplexer (U47, U46, U97, and U96). The multiplexer strobes the contents of the RAR or the output buffer register into the parallel-to-serial/serial-to-parallel converter (U25 and U105) at the appropriate time.

4-23. During write operations, the contents of the RAR are loaded when the address field of the sector is being written; the contents of the output buffer register are loaded when the data field is being written. Control of the format in which the sectors are written is maintained by the sector formatter described in paragraphs 4-26 through 4-28.

4-24. During read operations, serial data is stacked by the converter and, at the appropriate time, 16-bit words are loaded into the read buffer register (U26 and U106). The contents of the read buffer register are also present in the input buffer register (U27, U28, U107, and U108). Data is transferred from the input buffer register to the computer by an LIA/B or MIA/B instruction addressed to the data channel.

4-25. WRITE OPERATIONS.

4-26. Write data is presented serially to the disc drive by the write formatter (U41A and U41B). The write formatter combines the 2.5-MHz clock signal and the data to be written in the format shown in figure 4-2. (During refine sector operations, line driver U81 is inhibited so that no data is actually written; in all other respects the operation is identical to writing.) The format in which sector address fields and data fields are written is controlled by the sector formatter which controls the application of data to the write formatter. The sector formatter establishes the format by passing data to the write formatter only at precise points in bit- and word-count that is initiated at the beginning of each sector.



7012-12

Figure 4-2. Data Bit Cell

4-27. When the addressed sector comes into position under the disc drive heads, the bit and word counter in the sector formatter is enabled by "and" gate U33D(C6). Subsequent Data Clock pulses from "and" gate U82B(B4) clock the bit counter (U43). Every 16 bits the bit counter clocks the word counter (U63 and U113). At appropriate word counts, the sector formatter enables "and" gate U52B which passes data to the write formatter.

4-28. READ OPERATIONS.

4-29. Serial data from the disc drive is routed to the Sync Phase FF U11A in the phase-lock loop and to the One's Catcher FF U112B. The serial data toggles the Sync Phase FF to provide one input to the voltage-controlled oscillator (VCO)(U101). The VCO output signal toggles the VCO Phase FF (U111B) to provide a second input to the VCO. The VCO phase-compares the two inputs and adjusts its output frequency until synchronized with the read data frequency. The synchronized output is routed through "exclusive-or" gate U23C to clock the Sync One Detector FF (U102B) and Data Buffer FF (U112A), which, along with the Ones Catcher FF, separate the data from the clock information. The serial output of the Data Buffer FF is routed to the serial-to-parallel converter for stacking into 16-bit words.

4-30. The word counter in the sector formatter is preset to count 240 when the data transfer operation commences (i.e. $\overline{\text{Control}}$ goes low). Once the read gate (U71D) is enabled, Data Clock pulses clock the bit counter in the sector formatter, which, in turn, clocks the word counter. When the word counter reaches count 246, the Lock-up Delay FF (U102A) is set. The Lock-up Delay FF enables the Sync One Detector FF and also presets the bit counter to count 15 and the word counter to count 253. As a result, the very next data pulse, which will be the "1" bit in the sector sync word, sets the Sync One Detector FF and thus enables the Data Buffer FF. (The word counter is clocked to count 254 so that address and data words can be counted precisely.) Subsequent data pulses toggle the Data Buffer FF which provides a serial data output in the conventional non-return-to-zero (NRZ) format as shown in figure 4-8.

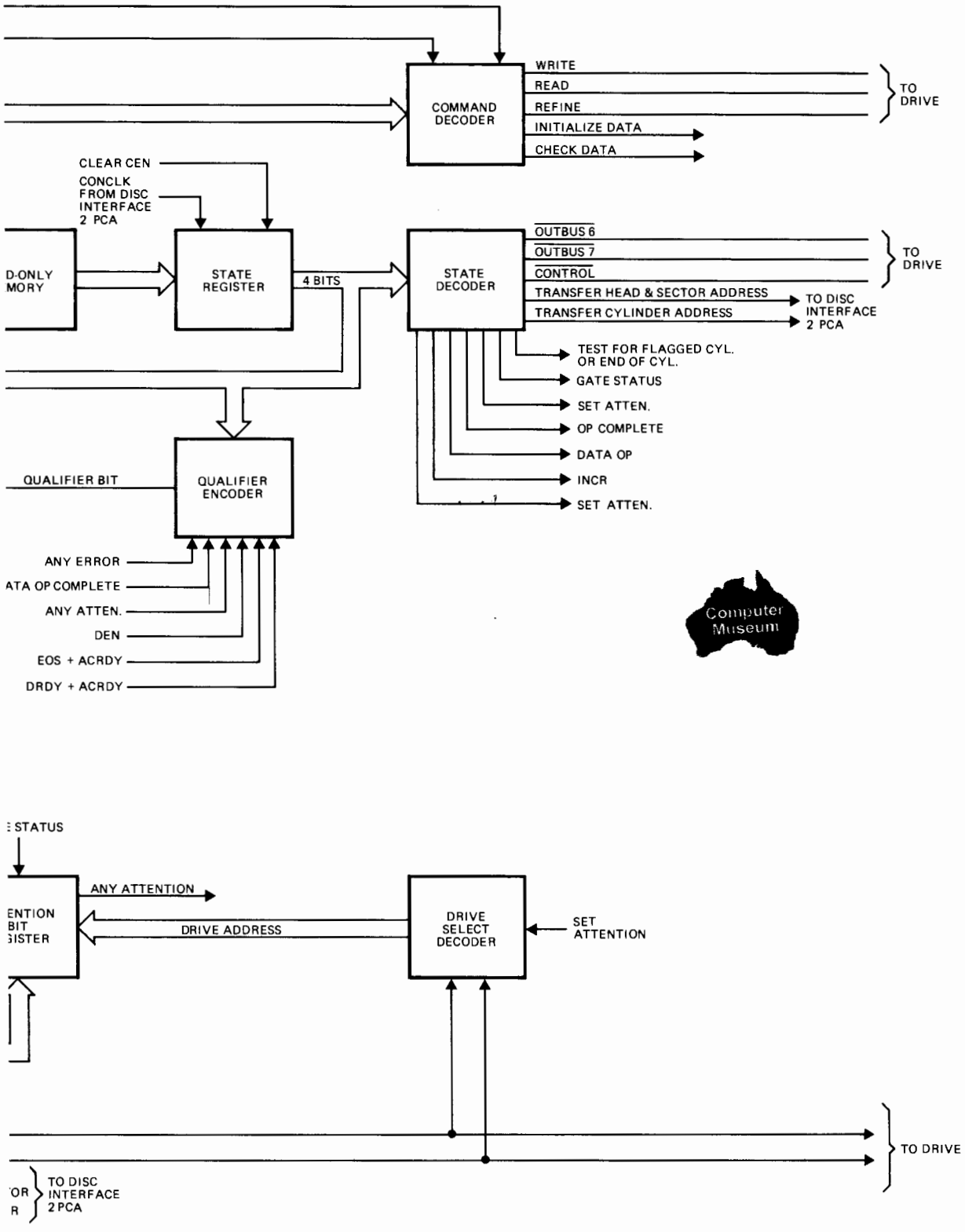
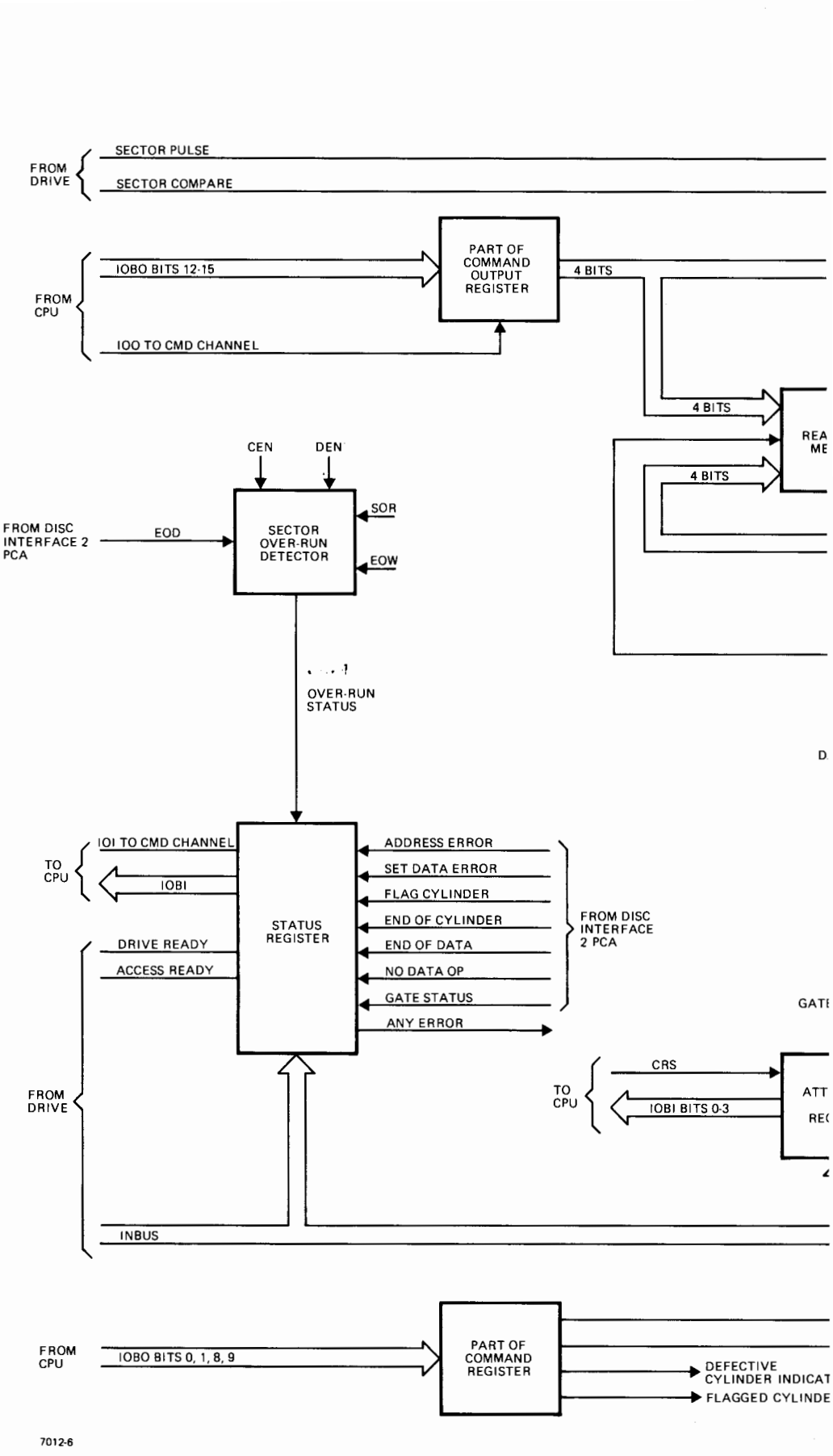


Figure 4-3. Disc Interface 1 PCA Block Diagram


FROM DRIVE
SECTOR PULSE
SECTOR COMPARE
FROM CPU
IOBO BITS 12-15
IOO TO CMD CHANNEL
PART OF COMMAND OUTPUT REGISTER
4 BITS
4 BITS
4 BITS
CEN
DEN
FROM DISC INTERFACE 2 PCA
EOD
SECTOR OVER-RUN DETECTOR
SOR
EOW
OVER-RUN STATUS
TO CPU
IOI TO CMD CHANNEL
IOBI
STATUS REGISTER
DRIVE READY
ACCESS READY
ADDRESS ERROR
SET DATA ERROR
FLAG CYLINDER
END OF CYLINDER
END OF DATA
NO DATA OP
GATE STATUS
ANY ERROR
FROM DISC INTERFACE 2 PCA
FROM DRIVE
TO CPU
CRS
IOBI BITS 0-3
INBUS
FROM CPU
IOBO BITS 0, 1, 8, 9
PART OF COMMAND REGISTER
DEFECTIVE CYLINDER INDICAT
FLAGGED CYLINDE
7012-6

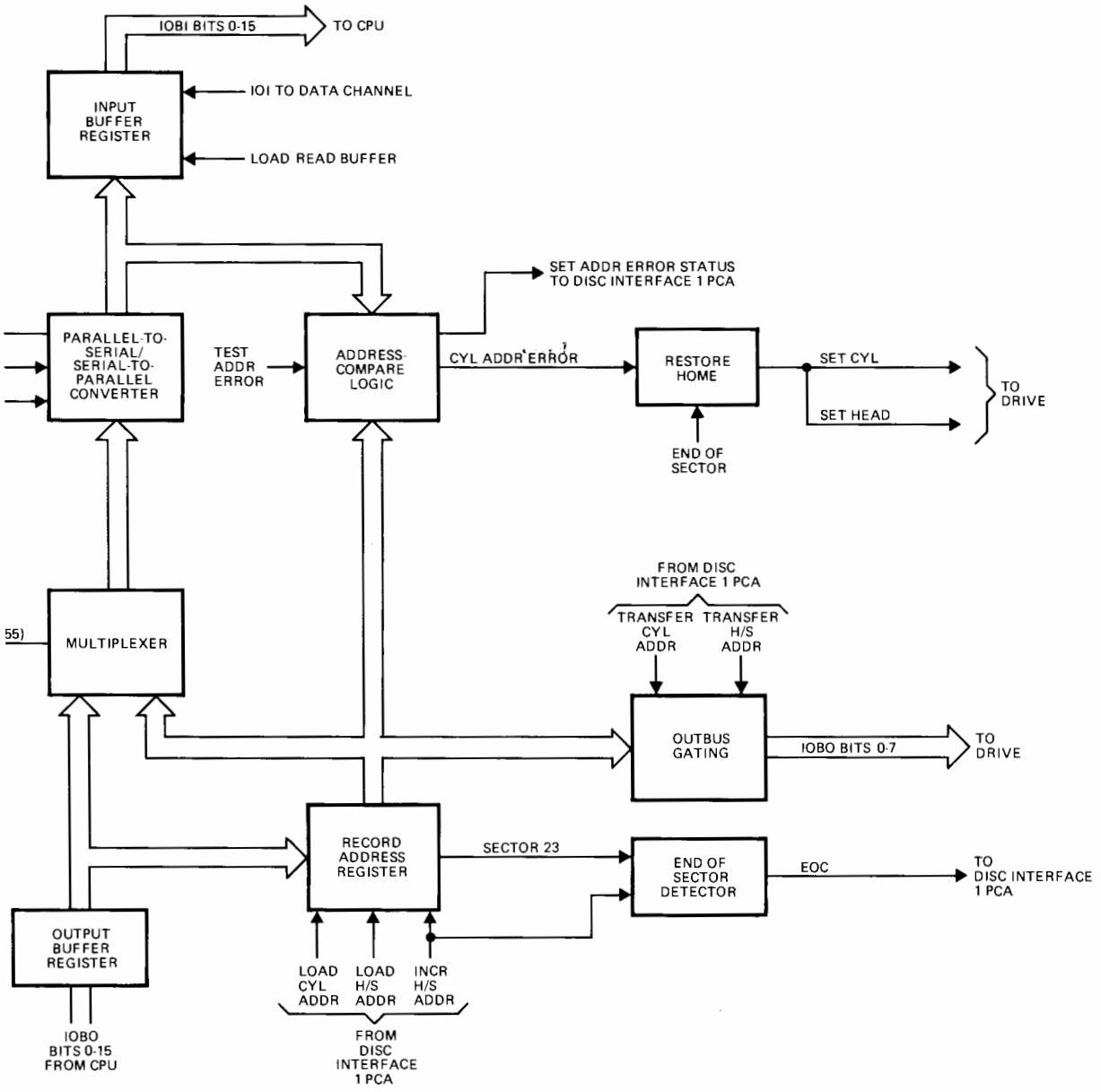
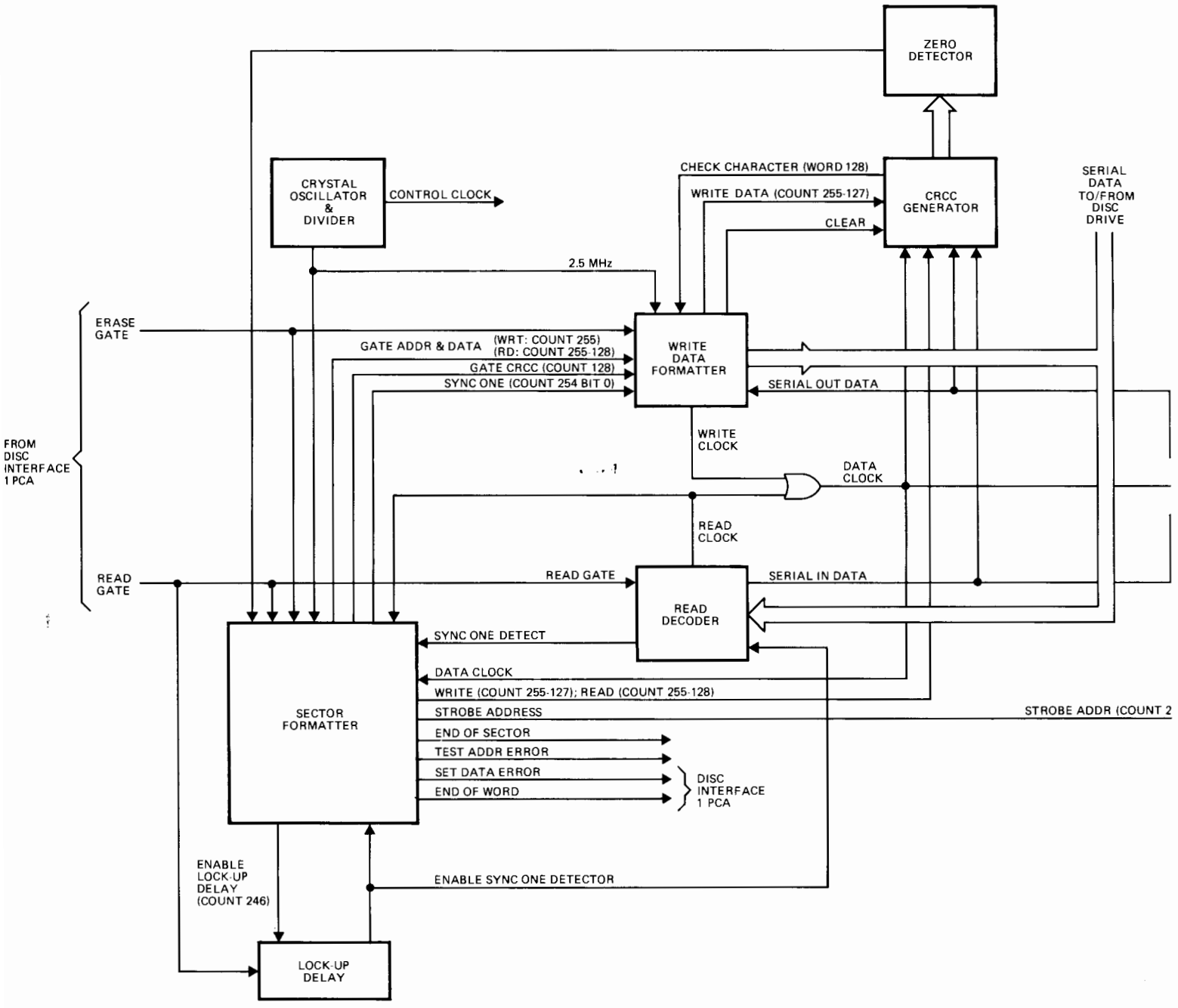


Figure 4-4. Disc Interface 2 PCA Block Diagram


ZERO DETECTOR
CRYSTAL OSCILLATOR & DIVIDER
CONTROL CLOCK
CHECK CHARACTER (WORD 128)
WRITE DATA (COUNT 255-127)
CLEAR
CRCC GENERATOR
SERIAL DATA TO/FROM DISC DRIVE
2.5 MHz
ERASE GATE
GATE ADDR & DATA
(WRT: COUNT 255)
(RD: COUNT 255-128)
GATE CRCC (COUNT 128)
SYNC ONE (COUNT 254 BIT 0)
WRITE DATA FORMATTER
SERIAL OUT DATA
FROM DISC INTERFACE 1 PCA
WRITE CLOCK
DATA CLOCK
READ CLOCK
READ GATE
READ GATE
SERIAL IN DATA
READ DECODER
SYNC ONE DETECT
DATA CLOCK
WRITE (COUNT 255-127); READ (COUNT 255-128)
STROBE ADDRESS
STROBE ADDR (COUNT 2
SECTOR FORMATTER
END OF SECTOR
TEST ADDR ERROR
SET DATA ERROR
END OF WORD
DISC INTERFACE 1 PCA
ENABLE LOCK-UP DELAY (COUNT 246)
ENABLE SYNC ONE DETECTOR
LOCK-UP DELAY

7012-7

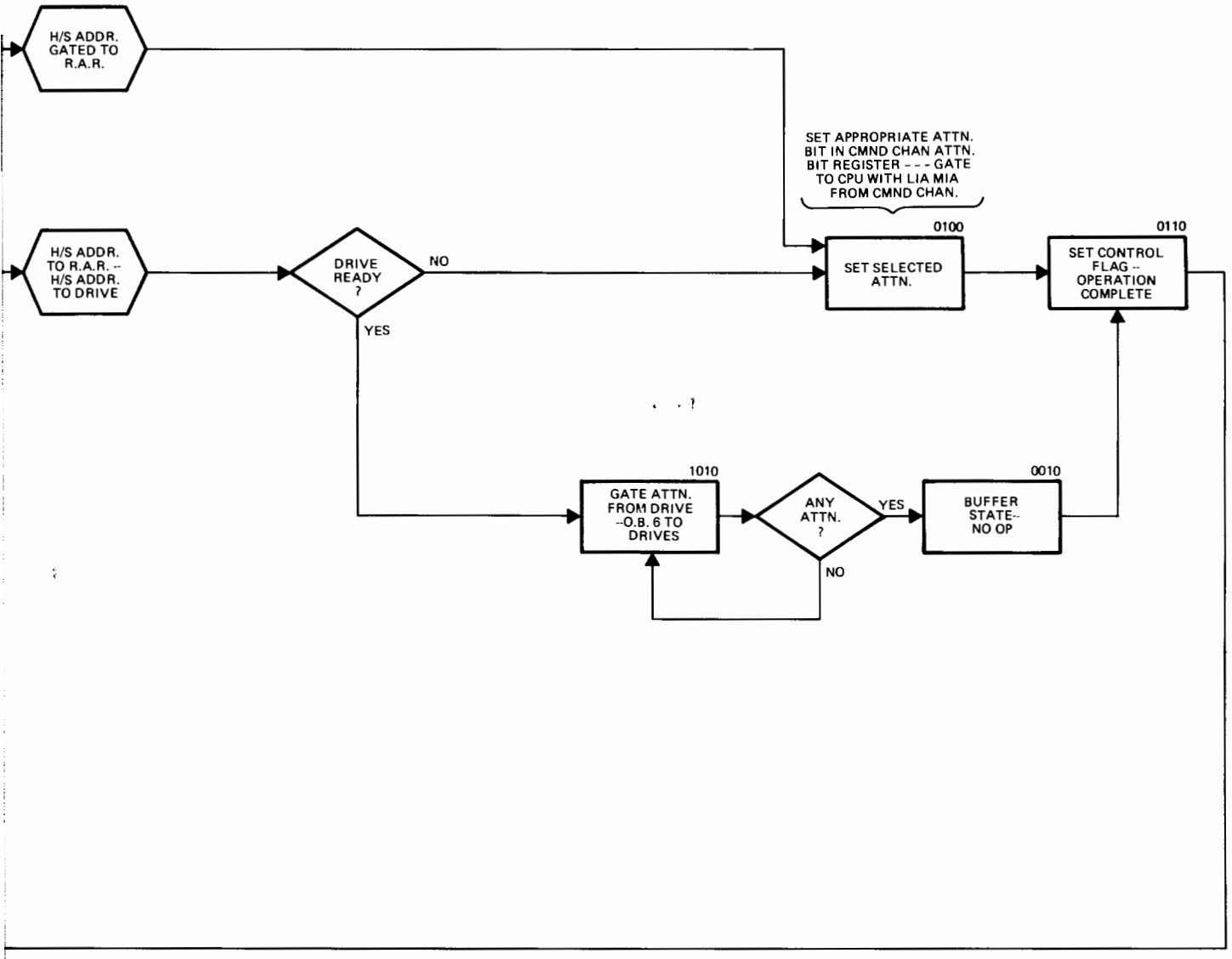
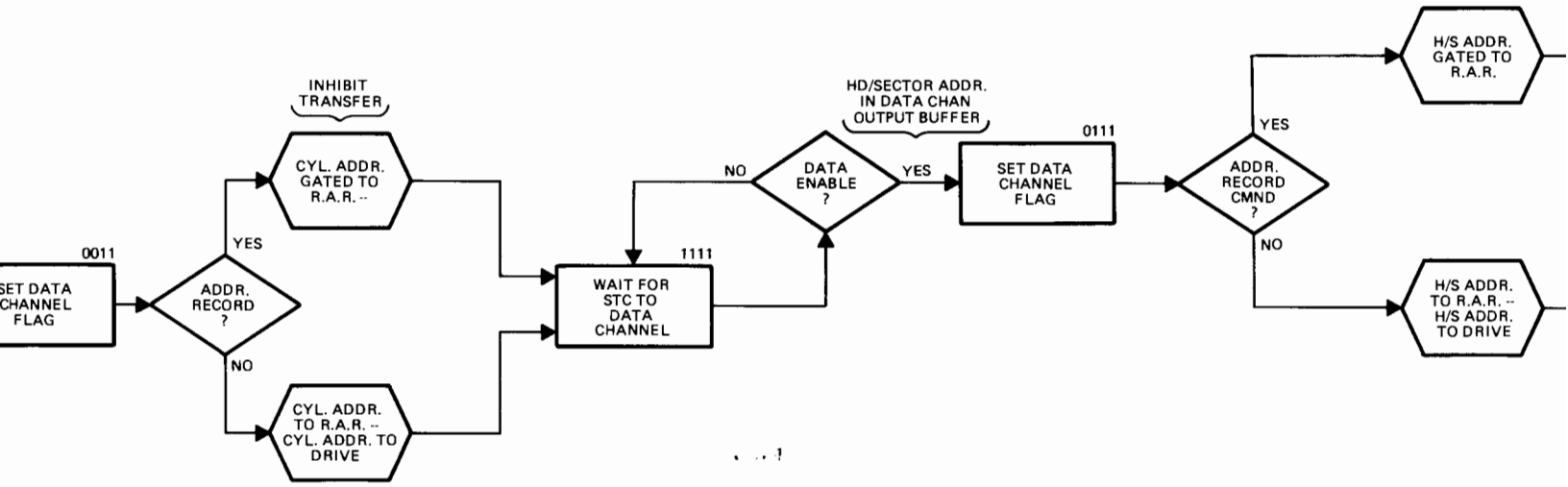
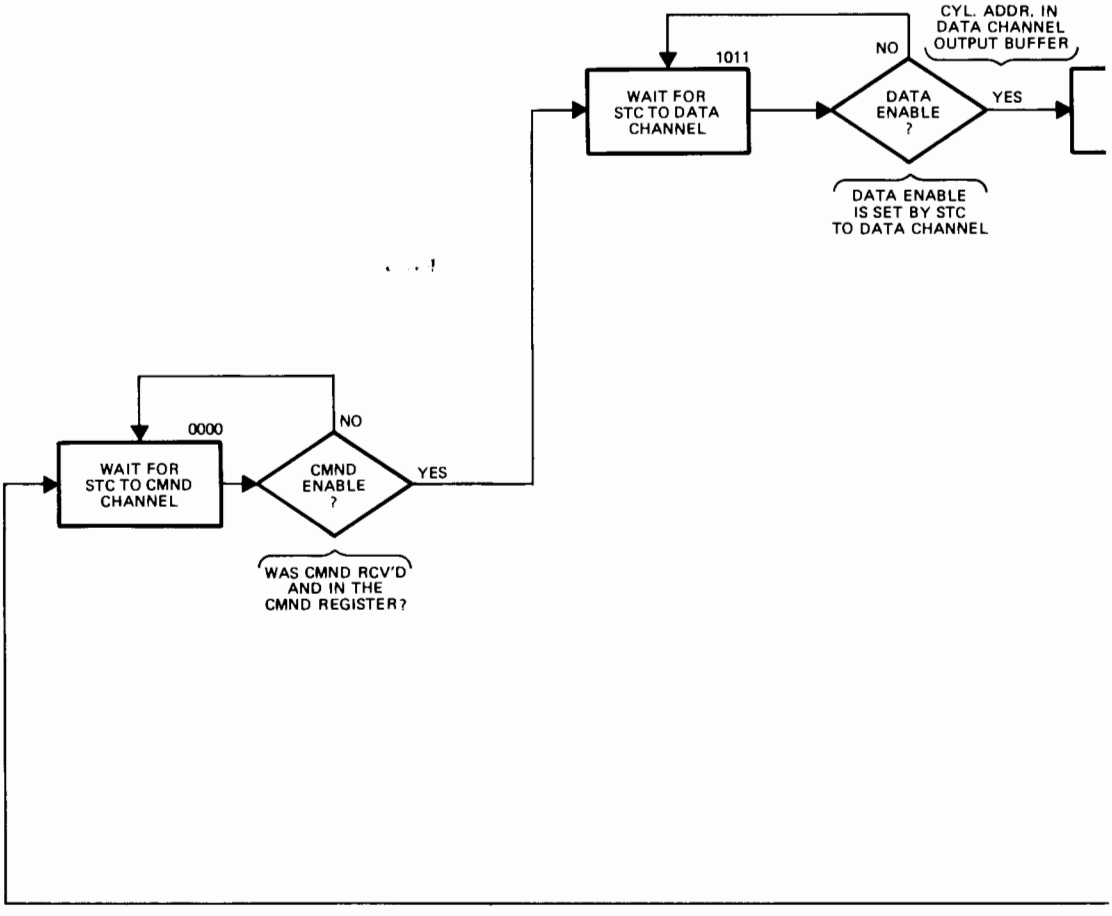


Figure 4-5. Seek Record and Address Record Operations Flow Diagram


INHIBIT TRANSFER
HD/SECTOR ADDR. IN DATA CHAN OUTPUT BUFFER
0011
SET DATA CHANNEL FLAG
ADDR. RECORD ?
YES
NO
CYL. ADDR. GATED TO R.A.R. --
CYL. ADDR. TO R.A.R. -- CYL. ADDR. TO DRIVE
1111
WAIT FOR STC TO DATA CHANNEL
DATA ENABLE ?
NO
YES
0111
SET DATA CHANNEL FLAG
ADDR. RECORD CMND ?
YES
NO
H/S ADDR. GATED TO R.A.R.
H/S ADDR. TO R.A.R. -- H/S ADDR. TO DRIVE


0000
WAIT FOR STC TO CMND CHANNEL
NO
CMND ENABLE ?
YES
WAS CMND RCV'D AND IN THE CMND REGISTER?
1011
WAIT FOR STC TO DATA CHANNEL
NO
DATA ENABLE ?
YES
CYL. ADDR. IN DATA CHANNEL OUTPUT BUFFER
DATA ENABLE IS SET BY STC TO DATA CHANNEL

7012-9A

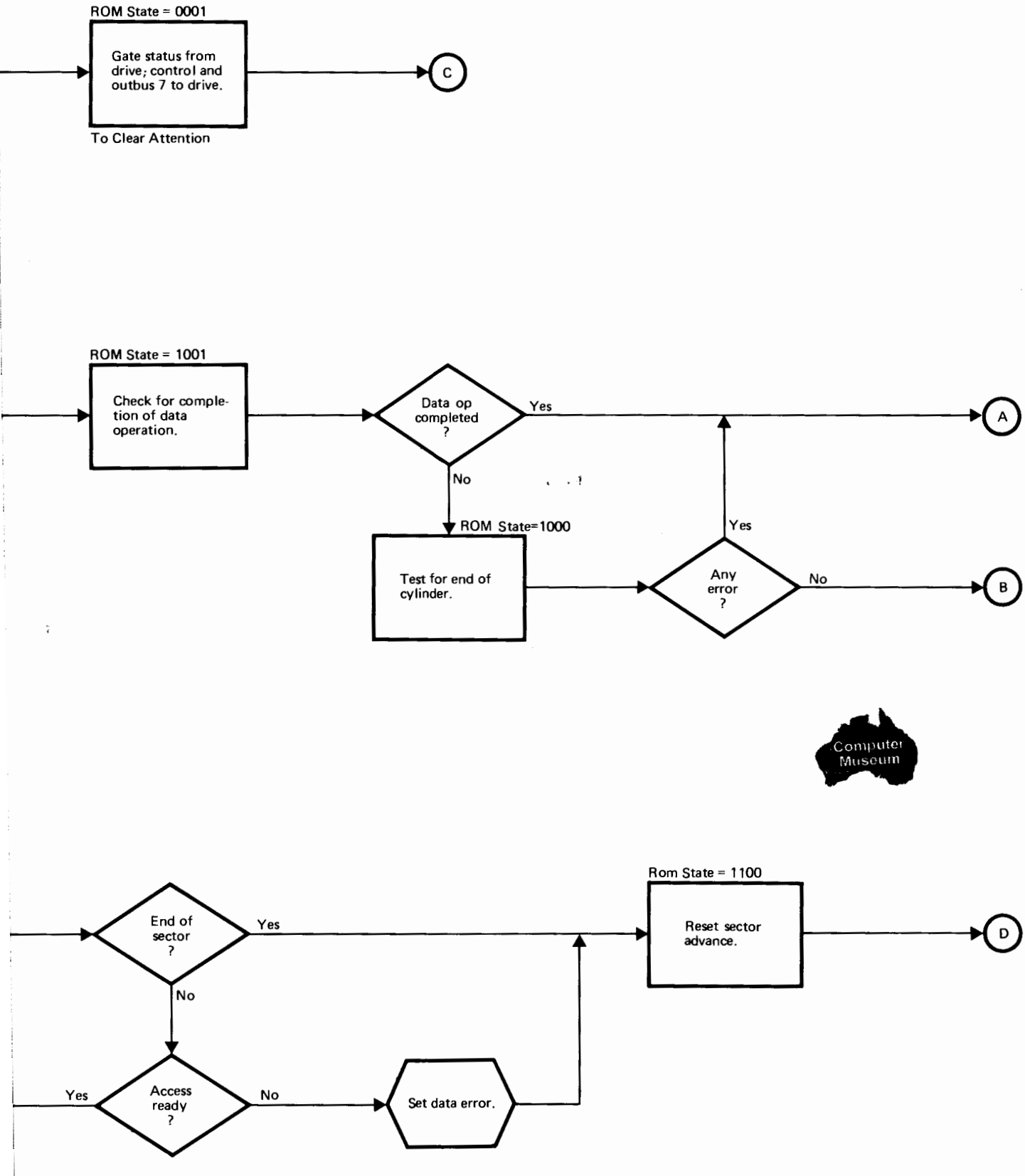
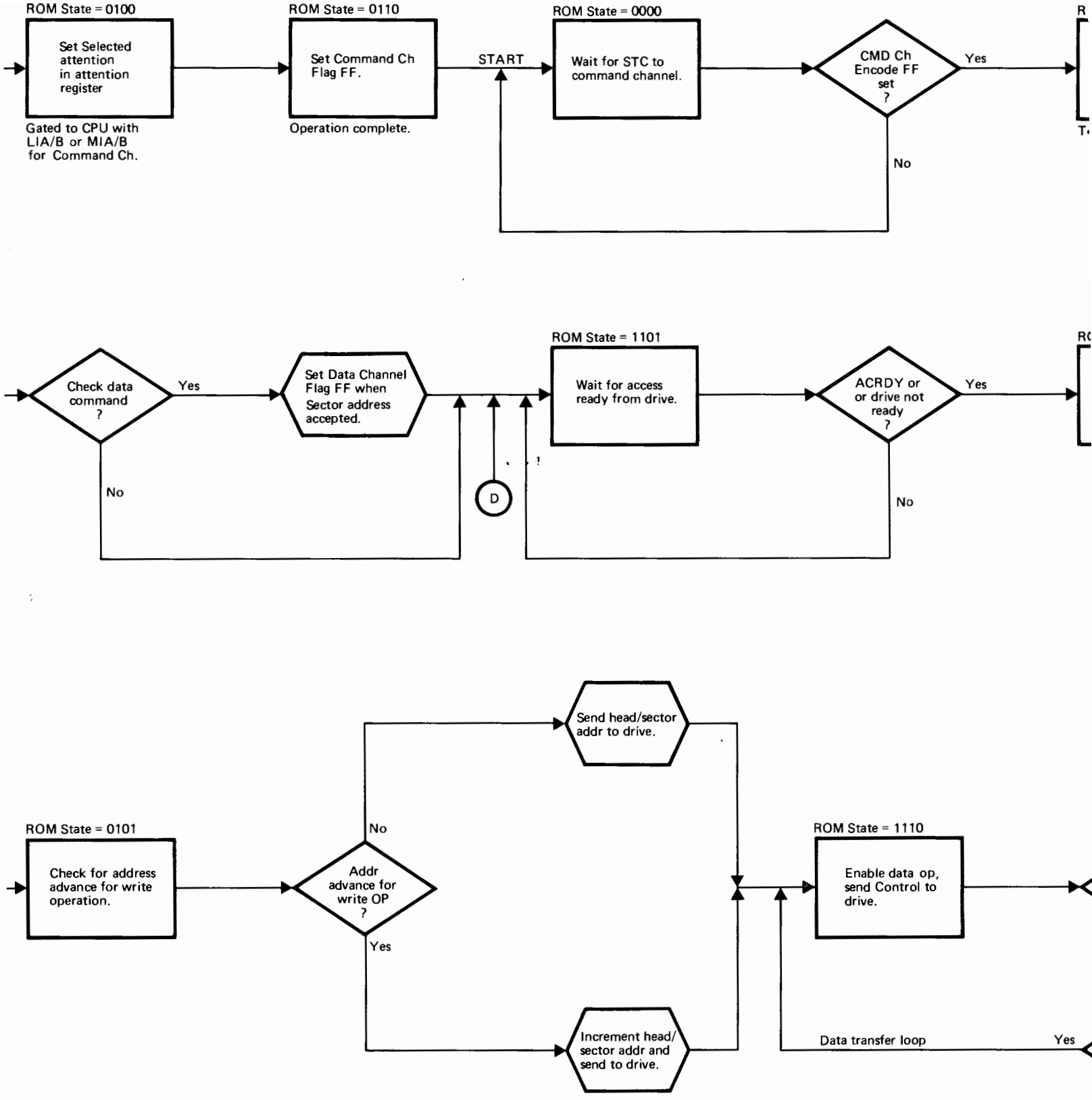
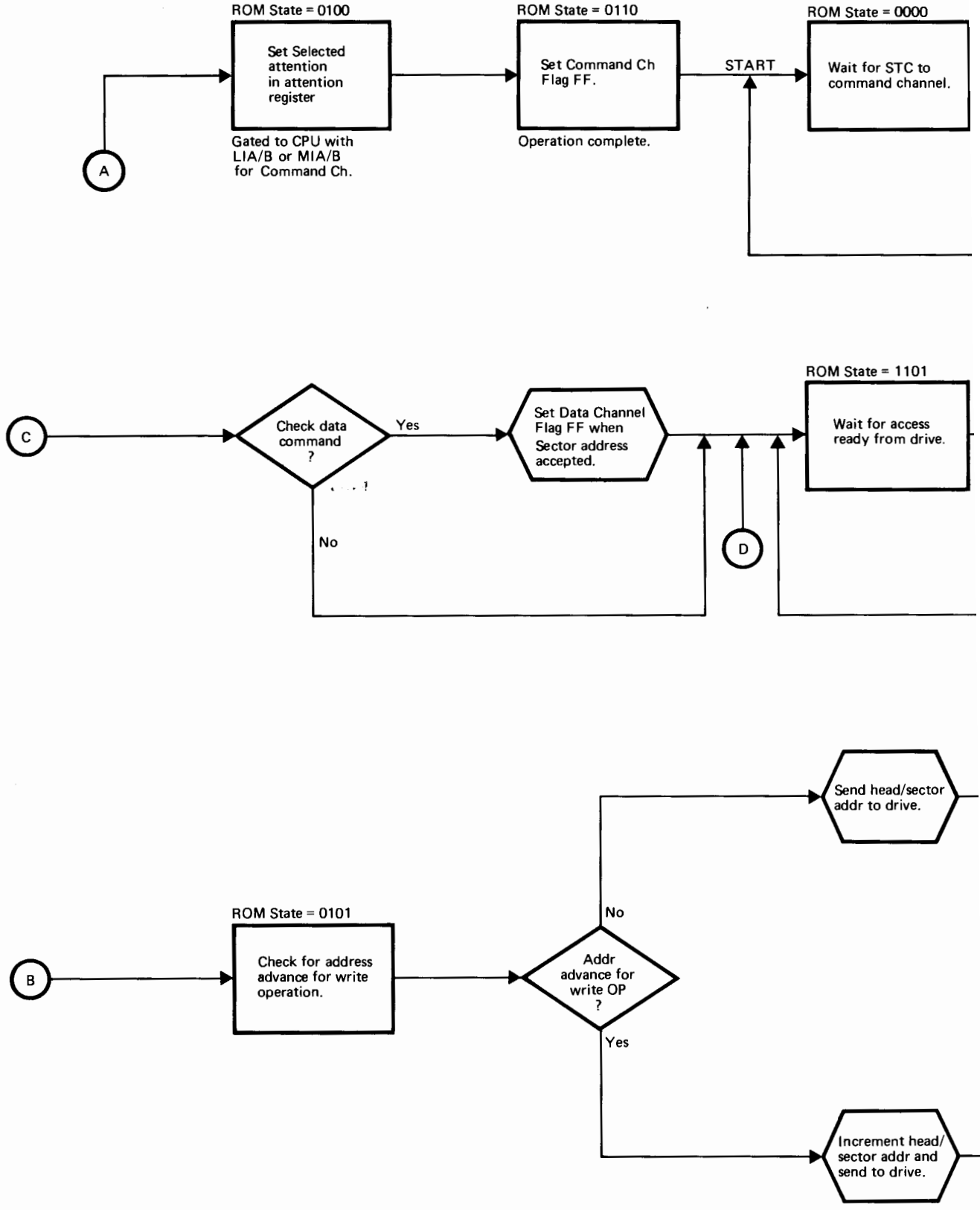


Figure 4-6. Write, Read, Check Data, and Initialize Data Operations Flow Diagram


ROM State = 0100
Set Selected attention in attention register
Gated to CPU with LIA/B or MIA/B for Command Ch.
ROM State = 0110
Set Command Ch Flag FF.
Operation complete.
START
ROM State = 0000
Wait for STC to command channel.
CMD Ch Encode FF set ?
Yes
No
Check data command ?
Yes
No
Set Data Channel Flag FF when Sector address accepted.
D
ROM State = 1101
Wait for access ready from drive.
ACRDY or or drive not ready ?
Yes
No
ROM State = 0101
Check for address advance for write operation.
Addr advance for write OP ?
No
Yes
Send head/sector addr to drive.
Increment head/ sector addr and send to drive.
ROM State = 1110
Enable data op, send Control to drive.
Data transfer loop
Yes


ROM State = 0100
Set Selected attention in attention register
Gated to CPU with LIA/B or MIA/B for Command Ch.
ROM State = 0110
Set Command Ch Flag FF.
Operation complete.
START
ROM State = 0000
Wait for STC to command channel.
A
C
Check data command ?
Yes
No
Set Data Channel Flag FF when Sector address accepted.
ROM State = 1101
Wait for access ready from drive.
D
B
ROM State = 0101
Check for address advance for write operation.
Addr advance for write OP ?
No
Yes
Send head/sector addr to drive.
Increment head/ sector addr and send to drive.

7012-10 A

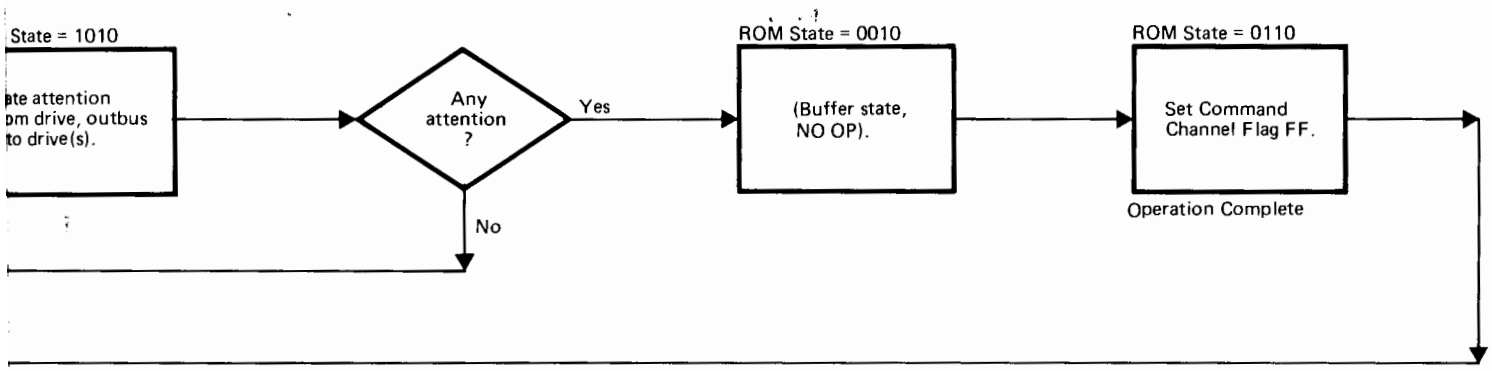
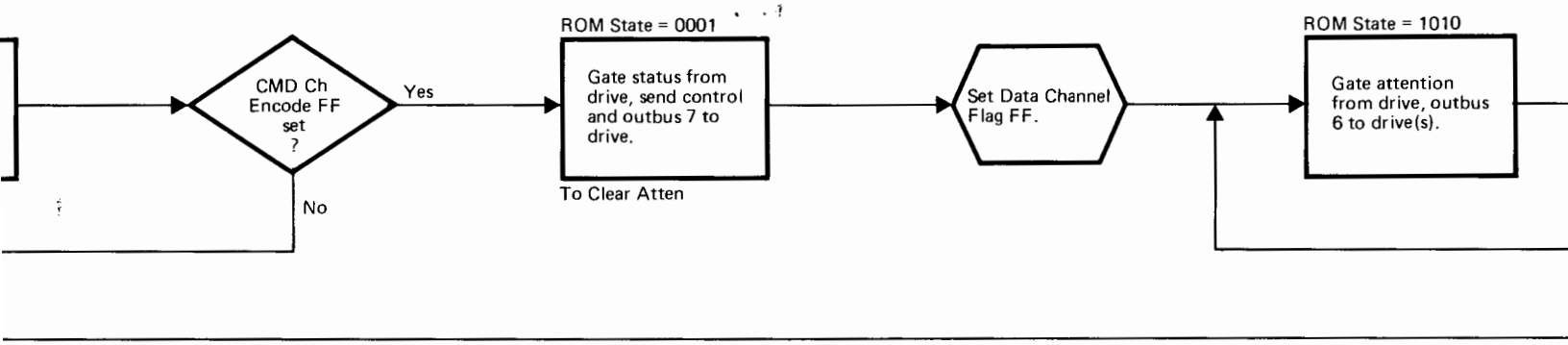
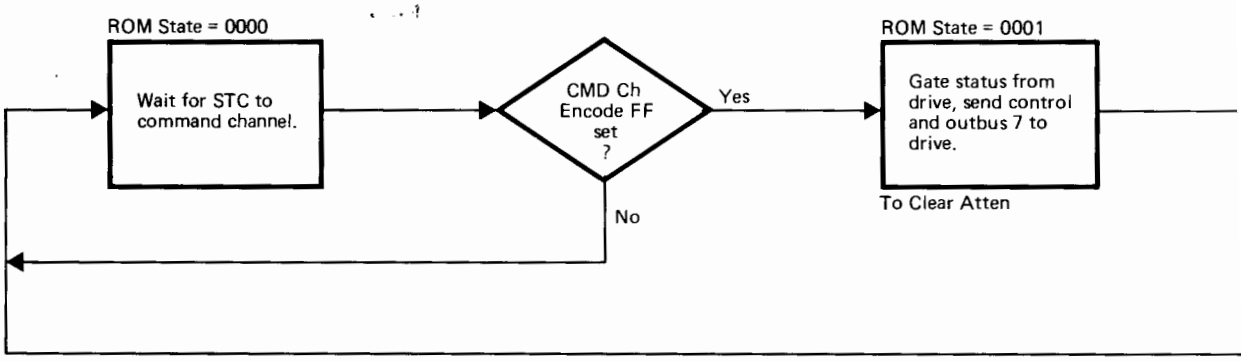
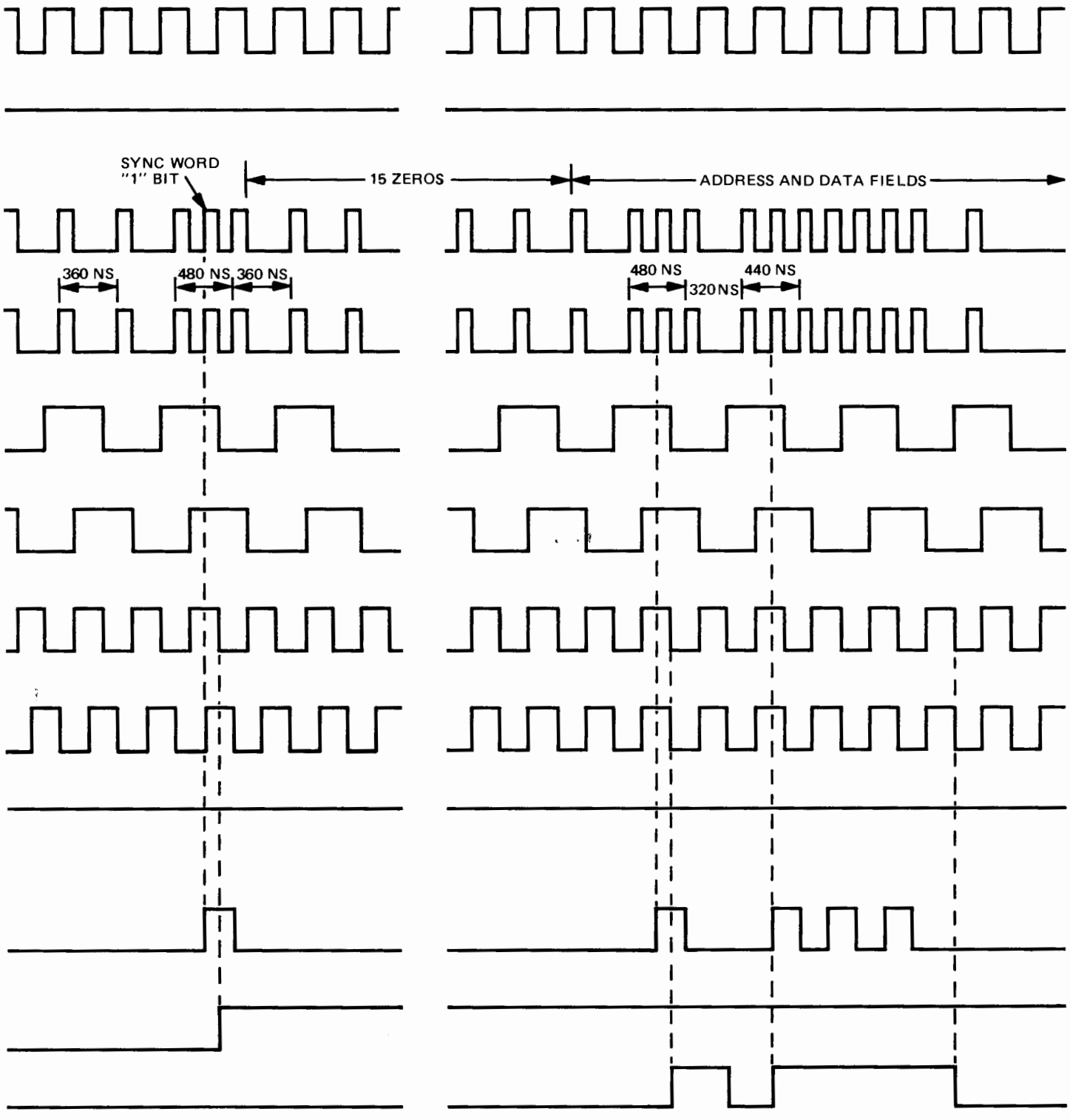


Figure 4-7. Status Operation Flow Diagram


CMD Ch Encode FF set ?
Yes
No
ROM State = 0001
Gate status from drive, send control and outbus 7 to drive.
To Clear Atten
Set Data Channel Flag FF.
ROM State = 1010
Gate attention from drive, outbus 6 to drive(s).


ROM State = 0000
Wait for STC to command channel.
CMD Ch Encode FF set ?
Yes
No
ROM State = 0001
Gate status from drive, send control and outbus 7 to drive.
To Clear Atten

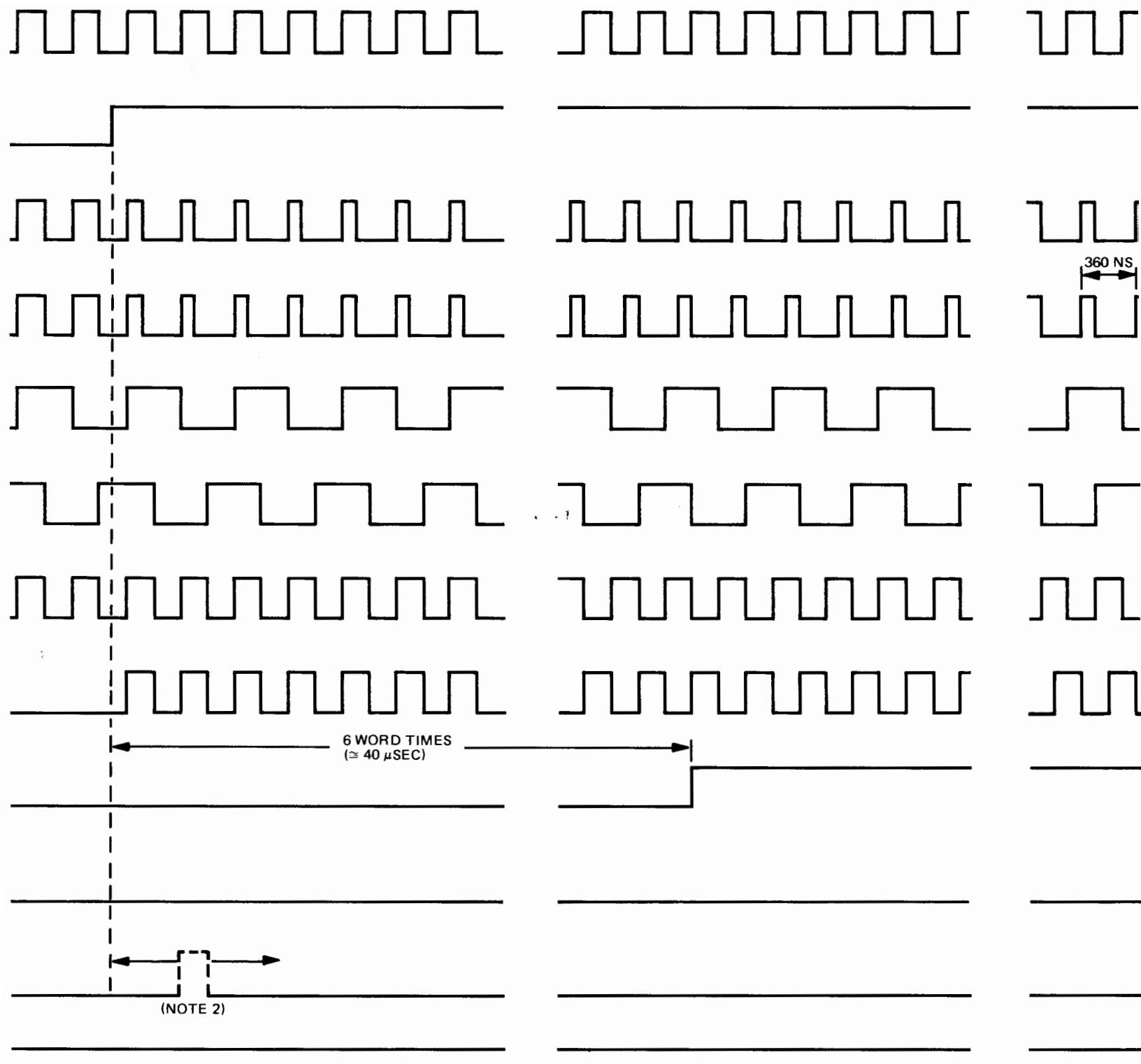
7012-11

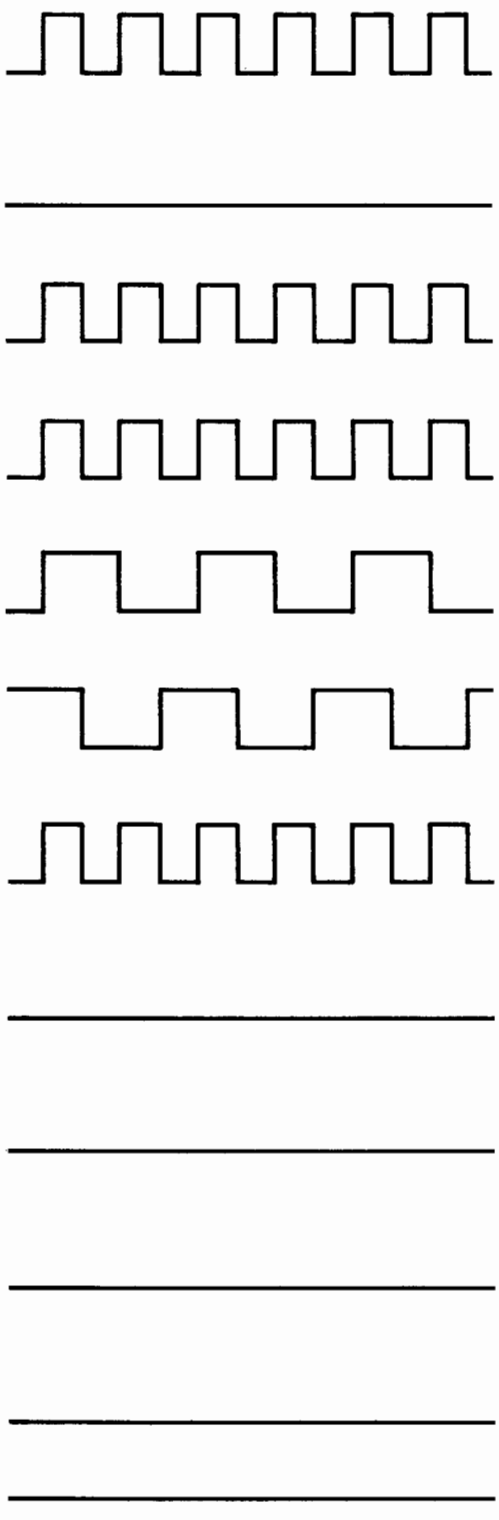


NOTES:

1. ALL SIGNAL LOCATIONS ON DISC INTERFACE 2 PCA (13210-60000).
2. ONE'S CATCHER FF MAY BE SET ANYTIME AFTER READ GATE ENABLED BUT NO "1" BITS ARE PASSED UNTIL AFTER LOCK-UP DELAY FF IS SET.

Figure 4-8. Read Data Separation Timing Diagram


360 NS
6 WORD TIMES
(≅ 40 μSEC)
(NOTE 2)


2.5 MHZ FROM CRYSTAL OSCILLATOR (U11 PIN 9)
READ GATE: CONTROL •READ (U71D PIN 11)
READ DATA (U91 PIN 4)
READ DATA• 2.5 MHZ (U92D PIN 11)
SYNC PHASE FF (U111A PIN 9)
VCO PHASE FF (U111B PIN 12)
DATA WINDOW: SYNC PHASE FF = VCO PHASE FF (U61C PIN 6)
DATA CLOCK: READ GATE • VCO OUTPUT (U82D PIN 11)
LOCK-UP DELAY FF (U102A PIN 5)
ONE'S CATCHER FF (U112B PIN 9)
SYNC ONE DETECTOR FF (U102B PIN 9)
DATA BUFFER FF (U112A PIN 5)

13210-13

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section provides maintenance information for the HP 13210A Disc Drive Interface Kit. Included are preventive maintenance and corrective maintenance instructions, mnemonic definitions, parts location views, and schematic diagrams.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in the computer documentation. There are no separate preventive maintenance procedures to be performed on the interface kit.

5-5. CALIBRATION.

5-6. The disc interface 2 PCA (13210-60000) contains a voltage-controlled oscillator (VCO) within the phase-lock loop integrated circuit U101 that may require adjustment following replacement of U101, C17, or C18. Adjustment may also be required periodically if data errors occur.

5-7. The VCO can be checked and adjusted, if necessary, as follows:

a. After at least 5 minutes warm-up time, connect TP2 (U111A, pin 2) to ground and connect digital frequency counter to TP1 (U61B, pin 4).

b. Frequency counter should read between 2.495 and 2.505 MHz.

c. If required, adjust C18 to obtain a counter reading between 2.495 and 2.505 MHz.

5-8. TROUBLESHOOTING.

5-9. Troubleshooting the interface kit is accomplished by performing the appropriate diagnostic program procedures and analyzing the error halts that occur as the test is being run. Figures 5-1 through 5-4 contain the schematic and parts location diagrams for the kit. Tables 5-1 and 5-2 list the replaceable parts for the disc interface 1 and disc interface 2 PCA's. Table 5-3 lists the interconnecting cable plug-to-plug connections.

Table 5-1. Mnemonic Definitions

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
ACRDY	Access Ready	HAD	Head Address
ADDR ERR; AE	Address Error	ID	Initialize Data
CD	Check Data	IINCR	Inhibit Increment
CDC 0	Check Data Character 0	INCR	Increment
CEN	Command (Channel) Enabled	IOO COM REG	IOO (to Command Register)
CMCH CON FF	Command Channel Control FF	IXSFER	Inhibit Transfer
CMCH FLG FF	Command Channel Flag FF	LRB	Load Read Buffer
CONCLK	Control Clock	PM	Parallel Mode
CSEL	Command Channel Selected	RDGT(B)	Read Gate (Buffered)
CYLAD	Cylinder Address	SAD	Sector Address
DATA OP	Data Operation	SADDR	Strobe Address
DCH FLG FF	Data Channel Flag FF	SEC ADV FF	Sector Advance FF
DCLK	Data Clock	SID	Serial-in Data
DEN	Data (Channel) Enabled	SK SET D FLAG	Seek Set Data Flag FF
DR; DRDY	Drive Ready	SOD	Serial-out Data
DSEL	Data Channel Selected	SOR	Sector Overrun
EOC	End of Cylinder	S6 (etc)	State Register, State 6 (etc)
EOD	End of Data	TAE	Test Address Error
EOS	End of Sector	WC	Write Clock
EOW	End of Word	WRT	Write
ERSGT	Erase Gate	XADDR	Transfer Address
FBS	Flagged Bit Status	XCYL; XFER CYL	Transfer Cylinder
FC; FLG CYL	Flagged Cylinder	XFER H/S(B)	Transfer Head/Sector (Buffered)
FLG BFR RST	Flag Buffer FF Reset		

Table 5-2. Disc Interface 1 PCA (13210-60004) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	13210-60004	DISC INTERFACE 1 PCA	28480	13210-60004
C1 thru 12, 15 thru 18	0150-0093	CAPACITOR, fxd, cer, 0.01 μF, +80-20%, 100 VDCW	72982	801-K800011
C13	0160-3455	CAPACITOR, fxd, cer, 470 pF, 10%, 1000 VDCW	56289	C067F102F471KS22
C14*	0160-2145	CAPACITOR, fxd, cer disc, 0.005 μF, 10%, 500 VDCW	91418	TA
Q1, 2, 3	1854-0477	TRANSISTOR	80131	2N2222A
R1, 2, 3, 5, 6, 8, 13	1810-0075	RESISTOR ARRAY, 750 ohms, 5%, 0.15W each	28480	1810-0075
R4, 7	1810-0127	RESISTOR ARRAY, 240/560 ohms, 5%, 0.15W each	28480	1810-0127
R9 thru 12, 19, 20 21, 23	0683-1025	RESISTOR, fxd, comp, 1000 ohms, 5%, 1/4W	01121	CB 1025
R14	1810-0030	RESISTOR ARRAY, 1k, 5%, 0.15W each	28480	1810-0030
R15, 16	0683-7515	RESISTOR, fxd, comp, 750 ohms, 5%, 1/4W	01121	CB 7515
R17, 18, 22	0683-1015	RESISTOR, fxd, comp, 100 ohms, 5%, 1/4W	01121	CB 1015
U11	1820-0626	INTEGRATED CIRCUIT, TTL	07263	U7B931459X
U12, 15, 24, 26, 34, 36, 42, 51, 92, 94, 95, 96	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7400N
U13, 33	1820-0069	INTEGRATED CIRCUIT, TTL	01295	SN7420N
U16, 22	1820-0372	INTEGRATED CIRCUIT, TTL	28480	1820-0372
U17	1820-0758	INTEGRATED CIRCUIT	28480	1820-0758
U21	1820-0495	INTEGRATED CIRCUIT, TTL	01295	SN74154N
U23, 32, 52, 84	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U25, 43, 72, 74, 76, 86	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U27, 28, 57, 97, 98	1820-0758	INTEGRATED CIRCUIT	28480	1820-0758
U35, 63, 75, 104	1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P
U44, 62, 85	1820-0239	INTEGRATED CIRCUIT, TTL	28480	1820-0239
U45	1820-0250	INTEGRATED CIRCUIT, TTL	28480	1820-0250
U46, 56, 102, 105, 106	1820-0437	INTEGRATED CIRCUIT, TTL	04713	MC4015P
U53	1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN7473N
U54	1820-0727	INTEGRATED CIRCUIT, TTL	07263	U7B932159X
U55, 65	1820-0233	INTEGRATED CIRCUIT, TTL	01295	SN74193N
U61, 64	1820-0077	INTEGRATED CIRCUIT, TTL	01295	SN7474N
U66, 101	1820-0577	INTEGRATED CIRCUIT, TTL	01295	SN7416N
U71	1820-0537	INTEGRATED CIRCUIT, TTL	28480	1820-0537
U73, 82	1820-0205	INTEGRATED CIRCUIT, TTL	28480	1820-0205
U77	1820-0726	INTEGRATED CIRCUIT, TTL	01295	SN74199
U81	1820-0621	INTEGRATED CIRCUIT, TTL	01295	SN7438N
U83	1820-0111	INTEGRATED CIRCUIT, TTL	07263	U6B930159X
U93	1816-0005	INTEGRATED CIRCUIT	28480	1816-0005
U103	1820-0615	INTEGRATED CIRCUIT, TTL	04713	FAIR 9312
U107	1820-0238	INTEGRATED CIRCUIT, DTL	04713	MC 1810P
*C14 (below series 1232)	0160-3457	CAPACITOR, fxd, cer disc, 0.002 μF, 10%, 500 VDCW	56289	C067F501F681KS22-CDH

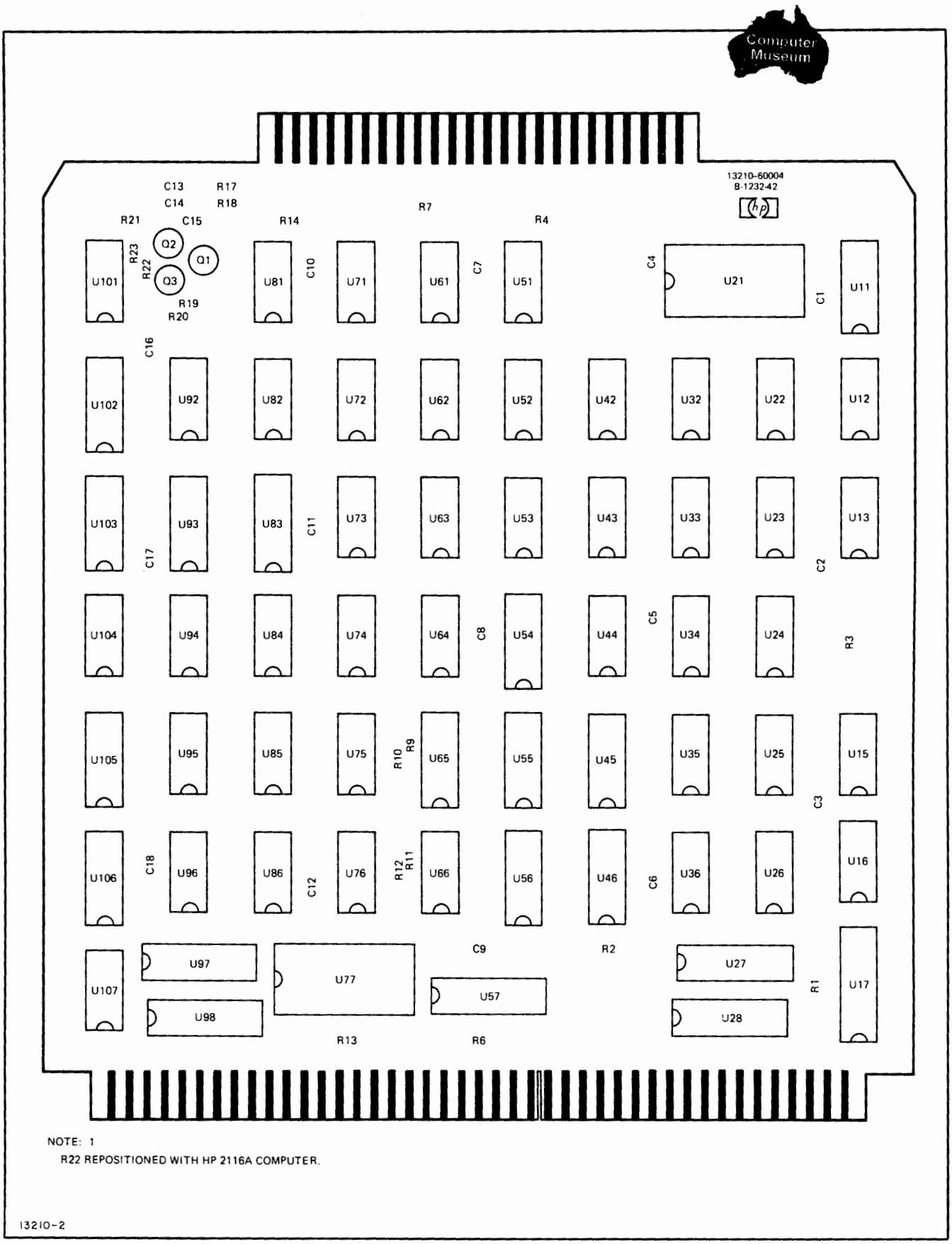


Figure 5-1. Disc Interface 1 PCA Parts Location Diagram

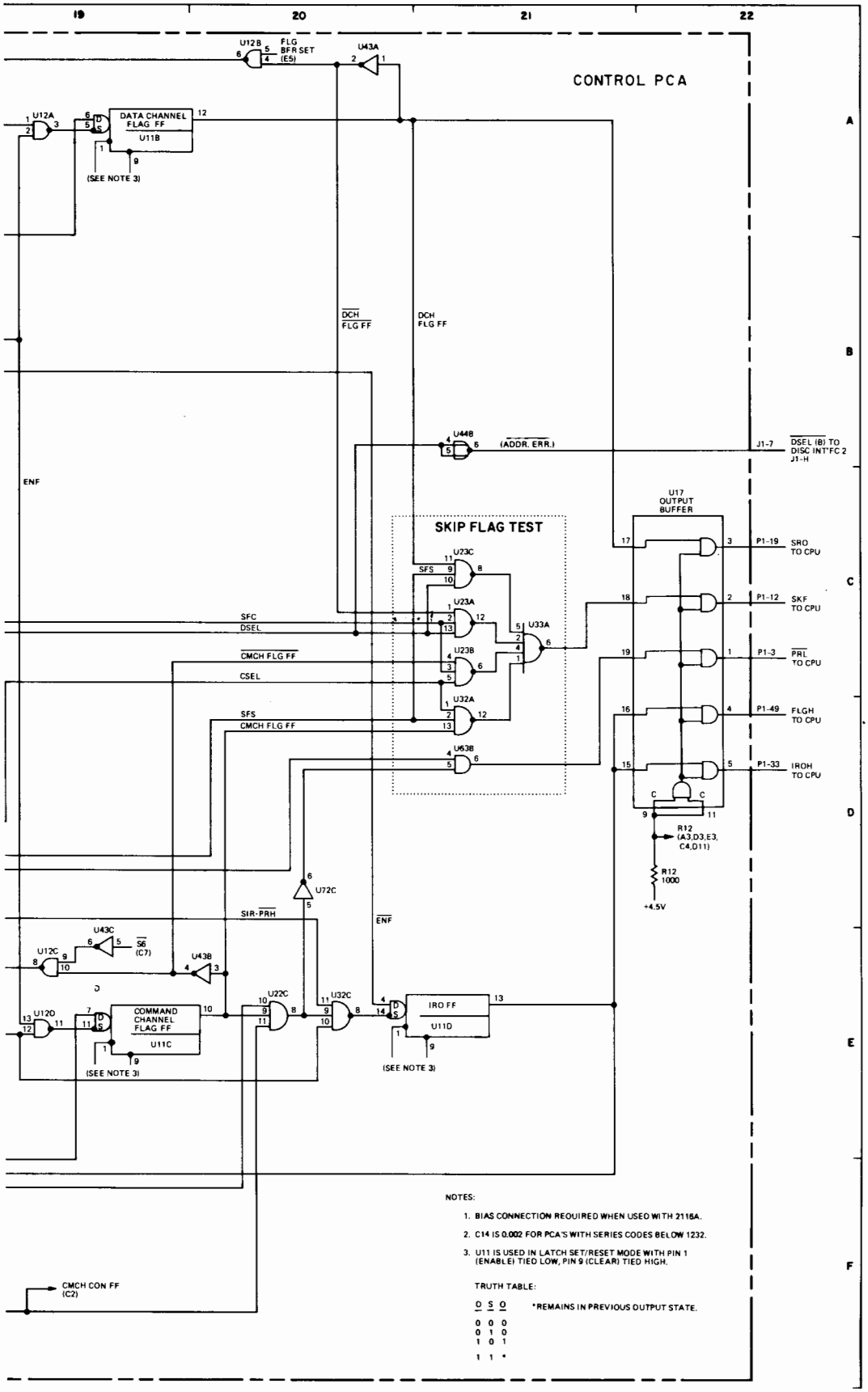
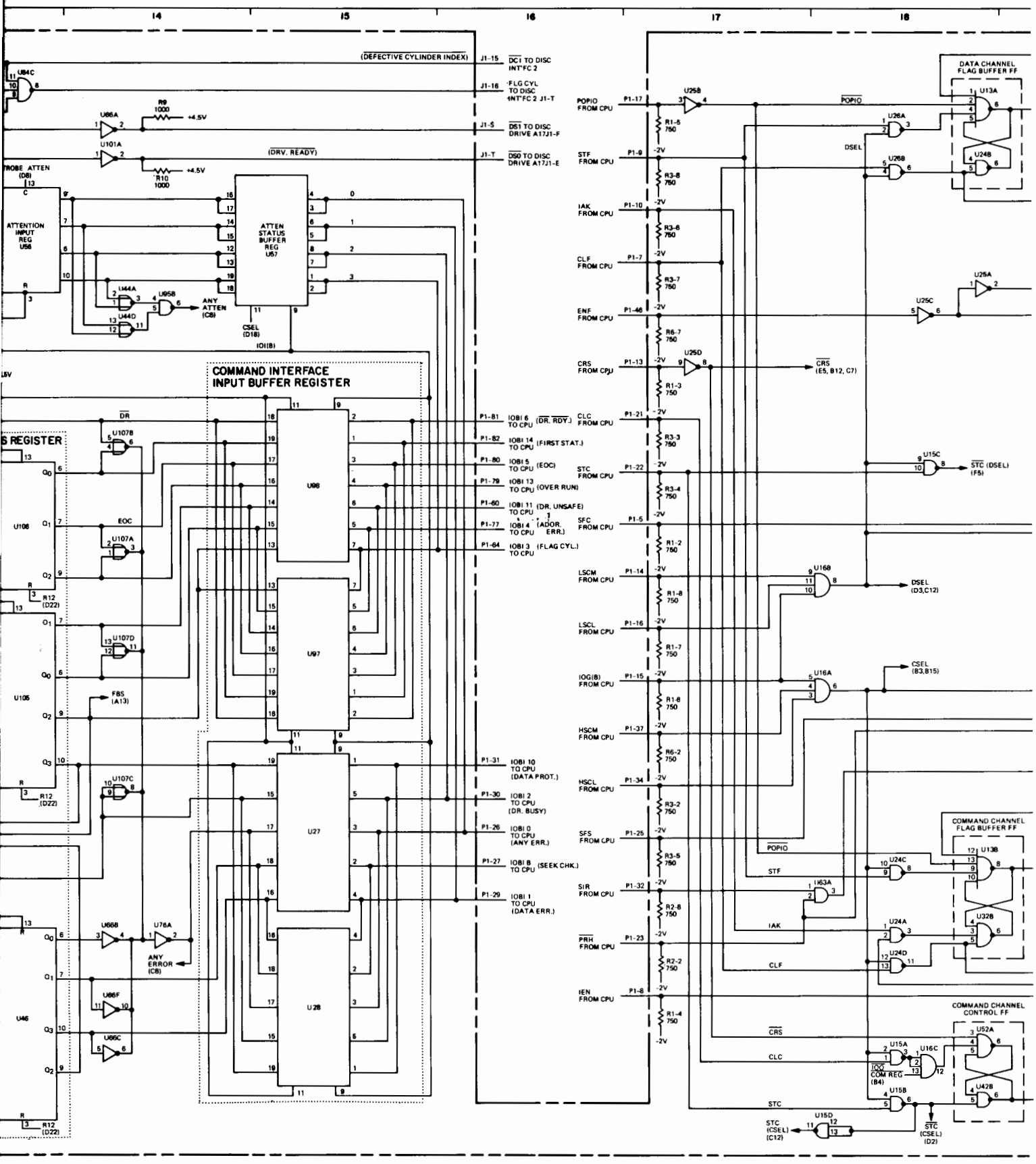
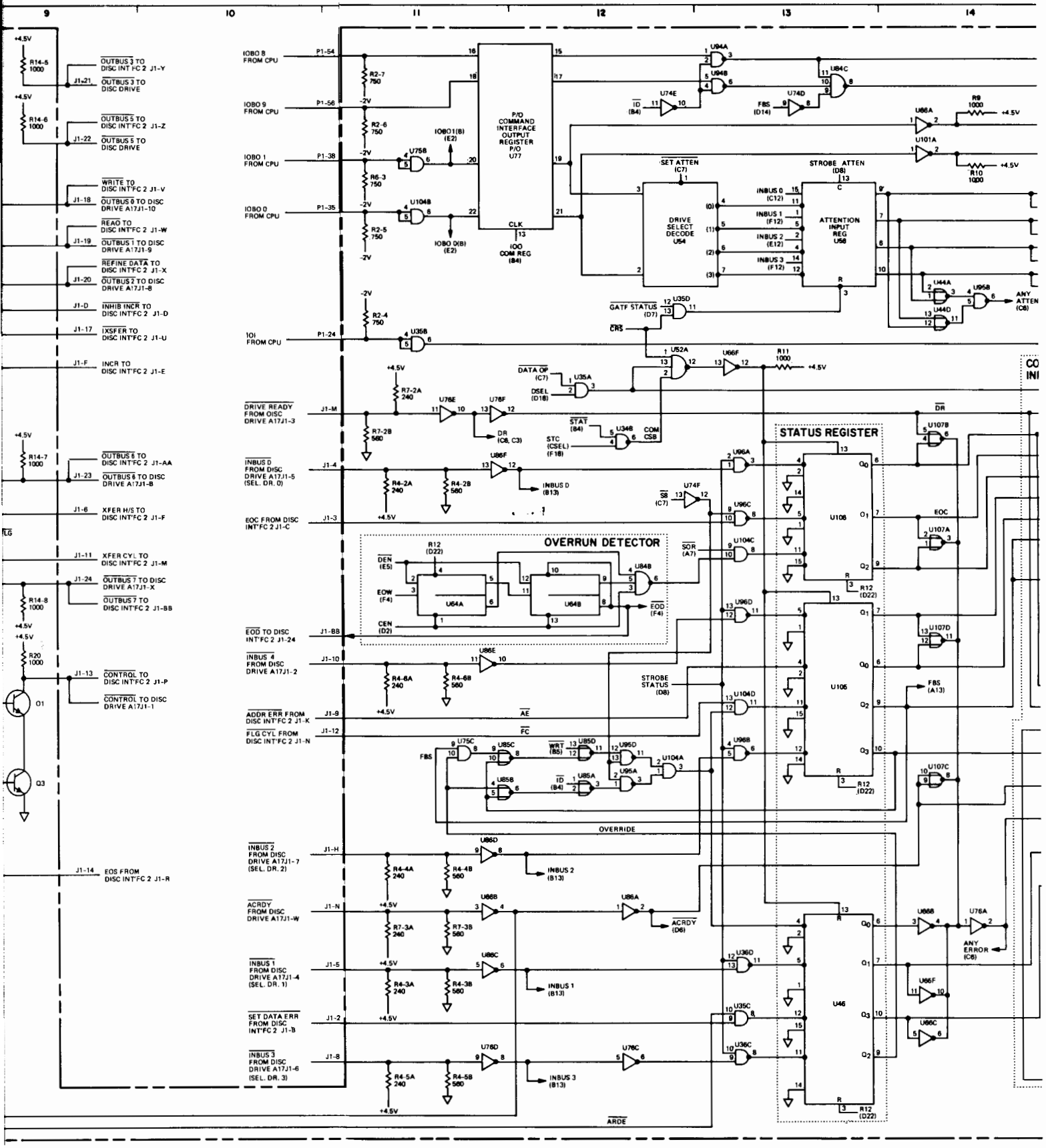
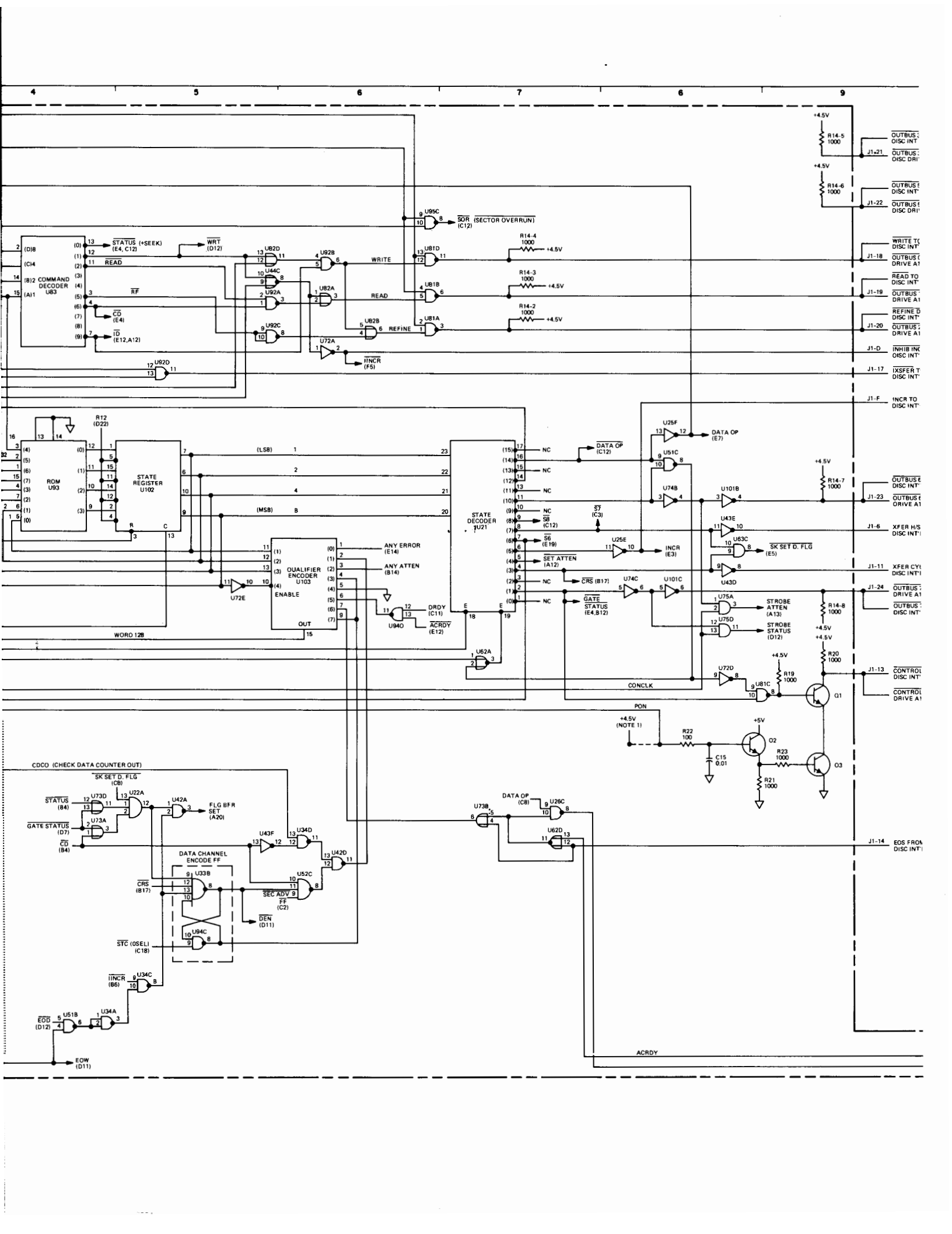


Figure 5-2. Disc Interface 1 PCA Schematic Diagram


14
15
16
17
18
(DEFECTIVE CYLINDER INDEX)
J1-15 DCI TO DISC INT'FC 2
J1-16 FLG CYL TO DISC INT'FC 2 J1-T
J1-5 DSI TO DISC DRIVE A17J1-F
J1-T DSO TO DISC DRIVE A17J1-E
(DRV. READY)
U84C
U66A
U101A
R9 1000
R10 1000
+4.5V
PROBE ATTEN (D8)
ATTENTION INPUT REG U56
ATTEN STATUS BUFFER REG U57
U44A
U44D
U95B
ANY ATTEN (C8)
CSEL (D18)
IOI(8)
COMMAND INTERFACE INPUT BUFFER REGISTER
S REGISTER
U108
U105
U46
U98
U97
U27
U28
DR
EOC
FBS (A13)
R12 (D22)
U107A
U107B
U107C
U107D
U66B
U66C
U66F
U76A
ANY ERROR (C8)
P1-81 IOBI 6 TO CPU (DR. RDY.)
P1-82 IOBI 14 TO CPU (FIRST STAT.)
P1-80 IOBI 5 TO CPU (EOC)
P1-79 IOBI 13 TO CPU (OVER RUN)
P1-60 IOBI 11 TO CPU (DR. UNSAFE)
P1-77 IOBI 4 TO CPU (ADDR. ERR.)
P1-64 IOBI 3 TO CPU (FLAG CYL.)
P1-31 IOBI 10 TO CPU (DATA PROT.)
P1-30 IOBI 2 TO CPU (DR. BUSY)
P1-26 IOBI 0 TO CPU (ANY ERR.)
P1-27 IOBI 8 TO CPU (SEEK CHK.)
P1-29 IOBI 1 TO CPU (DATA ERR.)
POPIO FROM CPU P1-17
STF FROM CPU P1-9
IAK FROM CPU P1-10
CLF FROM CPU P1-7
ENF FROM CPU P1-46
CRS FROM CPU P1-13
CLC FROM CPU P1-21
STC FROM CPU P1-22
SFC FROM CPU P1-5
LSCM FROM CPU P1-14
LSCL FROM CPU P1-16
IOG(8) FROM CPU P1-15
HSCM FROM CPU P1-37
HSCL FROM CPU P1-34
SFS FROM CPU P1-25
SIR FROM CPU P1-32
PRH FROM CPU P1-23
IEN FROM CPU P1-8
U25B
R1-5 750
R3-8 750
R3-7 750
R6-7 750
R1-3 750
R3-3 750
R3-4 750
R1-2 750
R1-8 750
R1-7 750
R6-2 750
R3-2 750
R3-5 750
R2-8 750
R2-2 750
R1-4 750
-2V
DATA CHANNEL FLAG BUFFER FF
U13A
U26A
U26B
U24B
DSEL
U25A
U25C
U25D
CRS (E5, B12, C7)
U15C
STC (DSEL) (F5)
U16B
DSEL (D3,C12)
U16A
CSEL (B3,B15)
COMMAND CHANNEL FLAG BUFFER FF
U13B
U24C
U24A
U24D
U32B
U16D
U63A
STF
IAK
CLF
COMMAND CHANNEL CONTROL FF
U52A
U15A
U16C
U42B
U15B
U15D
CLC
STC
CRS
IOG COM REG (B4)
STC (CSEL) (C12)
STC (CSEL) (D2)


9
10
11
12
13
14
STATUS REGISTER
OVERRUN DETECTOR
DRIVE SELECT DECODE U54
ATTENTION INPUT REG U58
P/O COMMAND INTERFACE OUTPUT REGISTER P/O U77
IOBO 8 FROM CPU
IOBO 9 FROM CPU
IOBO 1 FROM CPU
IOBO 0 FROM CPU
IOI FROM CPU
OUTBUS 3 TO DISC INT'FC 2 J1-Y
OUTBUS 3 TO DISC DRIVE
OUTBUS 5 TO DISC INT'FC 2 J1-Z
OUTBUS 5 TO DISC DRIVE
WRITE TO DISC INT'FC 2 J1-V
OUTBUS 0 TO DISC DRIVE A17J1-10
READ TO DISC INT'FC 2 J1-W
OUTBUS 1 TO DISC DRIVE A17J1-9
REFINE DATA TO DISC INT'FC 2 J1-X
OUTBUS 2 TO DISC DRIVE A17J1-8
INHIB INCR TO DISC INT'FC 2 J1-D
XSFER TO DISC INT'FC 2 J1-U
INCR TO DISC INT'FC 2 J1-E
OUTBUS 6 TO DISC INT'FC 2 J1-AA
OUTBUS 6 TO DISC DRIVE A17J1-B
XFER H/S TO DISC INT'FC 2 J1-F
XFER CYL TO DISC INT'FC 2 J1-M
OUTBUS 7 TO DISC DRIVE A17J1-X
OUTBUS 7 TO DISC INT'FC 2 J1-BB
CONTROL TO DISC INT'FC 2 J1-P
CONTROL TO DISC DRIVE A17J1-1
EOS FROM DISC INT'FC 2 J1-R
DRIVE READY FROM DISC DRIVE A17J1-3
INBUS 0 FROM DISC DRIVE A17J1-5 (SEL. DR. 0)
EOC FROM DISC INT'FC 2 J1-C
EOD TO DISC INT'FC 2 J1-24
INBUS 4 FROM DISC DRIVE A17J1-2
ADDR ERR FROM DISC INT'FC 2 J1-K
FLG CYL FROM DISC INT'FC 2 J1-N
INBUS 2 FROM DISC DRIVE A17J1-7 (SEL. DR. 2)
ACRDY FROM DISC DRIVE A17J1-W
INBUS 1 FROM DISC DRIVE A17J1-4 (SEL. DR. 1)
SET DATA ERR FROM DISC INT'FC 2 J1-B
INBUS 3 FROM DISC DRIVE A17J1-6 (SEL. DR. 3)
OVERRIDE
ARDE
ANY ATTEN (C8)
ANY ERROR (C6)
EOC
FBS (A13)
ACRDY (D6)
INBUS 0 (B13)
INBUS 1 (B13)
INBUS 2 (B13)
INBUS 3 (B13)
EOD (F4)
DR (C8, C3)


4
5
6
7
6
9
COMMAND DECODER U83
STATUS (+SEEK) (E4, C12)
WRT (D12)
READ
RF
CD (E4)
ID (E12,A12)
U95C
SOR (SECTOR OVERRUN) (C12)
U82D
U92B
WRITE
U81D
R14-4 1000 +4.5V
U44C
U92A
U82A
READ
U81B
R14-3 1000 +4.5V
U82B
REFINE
U81A
R14-2 1000 +4.5V
U72A
INCR (F5)
U92D
+4.5V
R14-5 1000
R14-6 1000
J1-21
J1-22
J1-18
J1-19
J1-20
J1-D
J1-17
J1-F
INHIB INC DISC INT'
IXSFER T DISC INT'
INCR TO DISC INT'
R12 (D22)
ROM U93
STATE REGISTER U102
(LSB) 1
2
4
(MSB) 8
STATE DECODER U21
NC
DATA OP (C12)
U25F
DATA OP (E7)
U51C
U74B
U101B
R14-7 1000
J1-23
J1-6
J1-11
J1-24
S7 (C3)
SB (C12)
S6 (E19)
U25E
INCR (E3)
SET ATTEN (A12)
CRS (B17)
GATE STATUS (E4,B12)
U43E
U63C
SK SET D. FLG (E5)
U43D
U74C
U101C
U75A
STROBE ATTEN (A13)
U75D
STROBE STATUS (D12)
R14-8 1000
QUALIFIER ENCODER U103
ENABLE
OUT
ANY ERROR (E14)
ANY ATTEN (B14)
U72E
U940
DRDY (C11)
ACRDY (E12)
WORD 128
U62A
CONCLK
U72D
U81C
R19 1000
R20 1000
Q1
J1-13
PON
+4.5V (NOTE 1)
R22 100
C15 0.01
+5V
Q2
R23 1000
R21 1000
Q3
CDCO (CHECK DATA COUNTER OUT)
SK SET D. FLG (C8)
STATUS (84)
U73D
U22A
U42A
FLG BFR SET (A20)
GATE STATUS (D7)
U73A
CD (B4)
U43F
U34D
U42D
DATA CHANNEL ENCODE FF
U33B
CRS (B17)
U52C
SEC ADV FF (C2)
DEN (D11)
STC (OSEL) (C18)
U94C
IINCR (B6)
U34C
EOD (D12)
U51B
U34A
EOW (D11)
U73B
DATA OP (C8)
U26C
U62D
J1-14
ACRDY

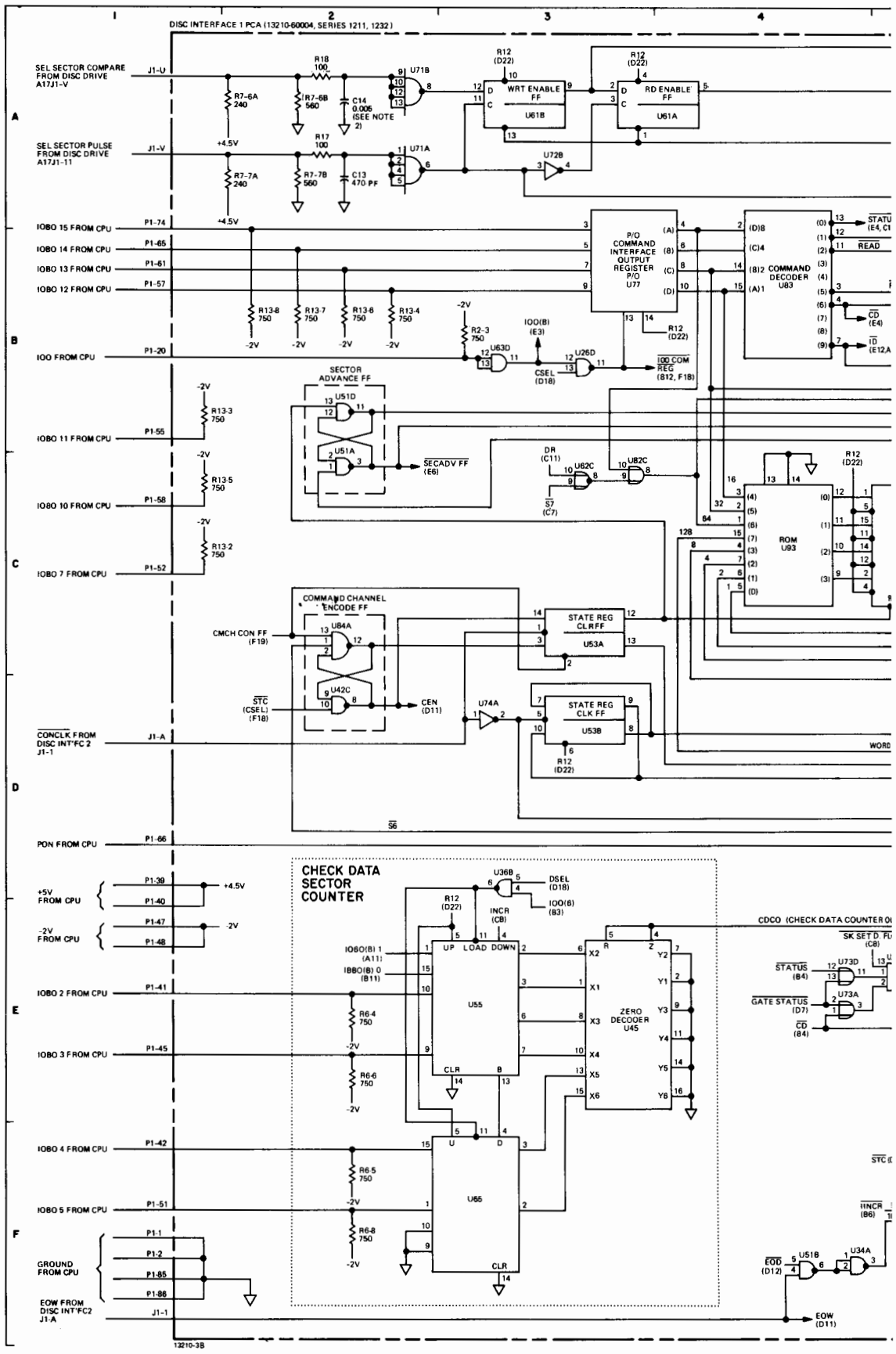

DISC INTERFACE 1 PCA (13210-60004, SERIES 1211, 1232)
SEL SECTOR COMPARE FROM DISC DRIVE A17J1-V
SEL SECTOR PULSE FROM DISC DRIVE A17J1-11
IOBO 15 FROM CPU
IOBO 14 FROM CPU
IOBO 13 FROM CPU
IOBO 12 FROM CPU
IOO FROM CPU
IOBO 11 FROM CPU
IOBO 10 FROM CPU
IOBO 7 FROM CPU
CONCLK FROM DISC INT'FC 2 J1-1
PON FROM CPU
+5V FROM CPU
-2V FROM CPU
IOBO 2 FROM CPU
IOBO 3 FROM CPU
IOBO 4 FROM CPU
IOBO 5 FROM CPU
GROUND FROM CPU
EOW FROM DISC INT'FC2 J1-A
WRT ENABLE FF
RD ENABLE FF
P/O COMMAND INTERFACE OUTPUT REGISTER P/O U77
COMMAND DECODER U83
SECTOR ADVANCE FF
COMMAND CHANNEL ENCODE FF
STATE REG CLR FF
STATE REG CLK FF
ROM U93
CHECK DATA SECTOR COUNTER
ZERO DECODER U45
SECADV FF (E6)
CEN (D11)
EOW (D11)
13210-3B

Table 5-3. Disc Interface 2 PCA (13210-60000) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
	13210-60000	DISC INTERFACE 2 PCA	28480	13210-60000
C1	0140-0198	CAPACITOR, fxd, mica, 200 pF, 5%	72136	RDM15F201J3C
C2 thru C14, 16, 20, 24, 25, 32 thru 34	0160-2055	CAPACITOR, fxd, cer, 0.01 μF, +80 -20%, 100 VDCW	56289	C023F101F103 ZS22-CDH
C15, 19, 21, 22	0150-0121	CAPACITOR, fxd, cer, 0.1 μF, +80 -20%, 50 VDCW	56289	5C50BIS-CML
C26 thru C29*	0160-3277	CAPACITOR, fxd, cer, 0.01 μF, 20%, 50 VDCW	96733	G504BX103M
C17 (below series 1438)	0160-2204	CAPACITOR, fxd, mica, 100 pF, 5%	72136	RDM15F111J3C
C17 (series 1438 & above)	0160-2202	CAPACITOR, fxd, mica, 75 pF, 5%, 300 VDCW	28480	0160-2202
C18 (below series 1446)	0121-0046	CAPACITOR, vari, cer, 9-35 pF	28480	0121-0046
C18 (series 1446 & above)	0121-0178	CAPACITOR, vari, cer, 15-60 pF	72982	538-011F15-60
C23	0160-3456	CAPACITOR, fxd, cer, 0.001 μF, 10%, 250 VDCW	56289	C067F251F102
C30, 31	0160-0161	CAPACITOR, fxd, My, 0.01 μF, 10%, 200 VDCW	56289	192P10392-PTS
CR1	1902-0041	DIODE, breakdown, 5.11V, 5%	04713	SZ10939-98
CR2	1902-0049	DIODE, breakdown, 6.19V	04713	SZ10939-122
Q1	1854-0045	TRANSISTOR	04713	2N956
R1, 3, 5, 6, 14 thru 18, 20, 23	0683-1025	RESISTOR, fxd, comp, 1000 ohms, 5%, 1/4W	01121	CB 1025
R2, 4	0683-1825	RESISTOR, fxd, comp, 1800 ohms, 5%, 1/4W	01121	CB 1825
R7, 8	0757-0417	RESISTOR fxd, met flm, 562 ohms, 1%, 1/8W	28480	0757-0417
R9, 10	0757-0398	RESISTOR, fxd, met flm, 75 ohms, 1%, 1/8W	28480	0757-0398
R11, 13	0683-5625	RESISTOR, fxd, comp, 5.6k, 5%, 1/4W	01121	CB 5625
R12	0757-0279	RESISTOR, fxd, met flm, 3.16k, 1%, 1/8W	28480	0757-0279
R19	0683-3915	RESISTOR, fxd, comp, 390 ohms, 5%, 1/4W	01121	CB 3915
R21, 22	0698-3446	RESISTOR, fxd, met flm, 383 ohms, 1%, 1/8W	28480	0698-3446
R24	0811-0988	RESISTOR, fxd, ww, 82 ohms, 3%, 3W	28480	0811-0988
R25	0686-1215	RESISTOR, fxd, comp, 120 ohms, 1/2W	19701	MF7C, T-O
R26 thru R29**	0698-7236	RESISTOR, fxd, flm, 1k, 2%, 1/8W	28480	0698-7236
U11	1820-0099	INTEGRATED CIRCUIT, TTL	01295	SN7493N
U12	1820-0070	INTEGRATED CIRCUIT, TTL	01295	SN7430N
U13, 14, 32, 53	1820-0239	INTEGRATED CIRCUIT, TTL	28480	1820-0239
U15, 16, 25, 26, 57 67, 87, 105, 106	1820-0726	INTEGRATED CIRCUIT, TTL	01295	SN74199
U21, 61	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U22, 33, 51, 64, 72, 82, 85, 86, 92	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7400N
U23	1820-0282	INTEGRATED CIRCUIT, TTL	01295	SN7486N
U24, 34, 42, 62, 71	1820-0141	INTEGRATED CIRCUIT, TTL	04713	MC3001P
U27, 28, 107, 108	1820-0758	INTEGRATED CIRCUIT	28480	1820-0758
U31, 52	1820-0068	INTEGRATED CIRCUIT, TTL	12040	SN7410N
U41, 55	1820-0544	INTEGRATED CIRCUIT, TTL	01295	SN74H103N
U43, 63, 113	1820-0233	INTEGRATED CIRCUIT, TTL	01295	SN74193N
U44	1820-0374	INTEGRATED CIRCUIT, TTL	01295	SN74H21N
U45, 95	1820-0250	INTEGRATED CIRCUIT, TTL	28480	1820-0250
U46, 47, 96, 97	1820-0616	INTEGRATED CIRCUIT, TTL	07263	U78932259X
U54, 75	1820-0128	INTEGRATED CIRCUIT, DTL	04713	MC837P
U56, 66	1820-0455	INTEGRATED CIRCUIT, TTL	18324	N8288A
U65	1820-0418	INTEGRATED CIRCUIT, DTL	28480	1820-0418
U73, 103	1820-0727	INTEGRATED CIRCUIT, TTL	07263	U7B932159X
U74, 84, 94, 104, 114	1820-0621	INTEGRATED CIRCUIT, TTL	01295	SN7438N
U81	1820-0722	INTEGRATED CIRCUIT, TTL	01295	SN75109N
U83, 93	1820-0637	INTEGRATED CIRCUIT, TTL	18324	N8875A
U91	1820-0723	INTEGRATED CIRCUIT, TTL	01295	SN75107N
U101	1826-0047	INTEGRATED CIRCUIT	18324	NE562B
U102, 112	1820-0077	INTEGRATED CIRCUIT, TTL	01295	SN7474N
U111	1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN7473N
Y1	0410-0436	CRYSTAL, quartz, 10 MHz	28480	0410-0436
*C26 thru C29 (below series 1249)	0150-0121	CAPACITOR, fxd, cer, 0.1 μF, +80 -20%, 50 VDCW	56289	5C50BIS-CML
**R26 thru R29 (below series 1249)	–	Not Used		

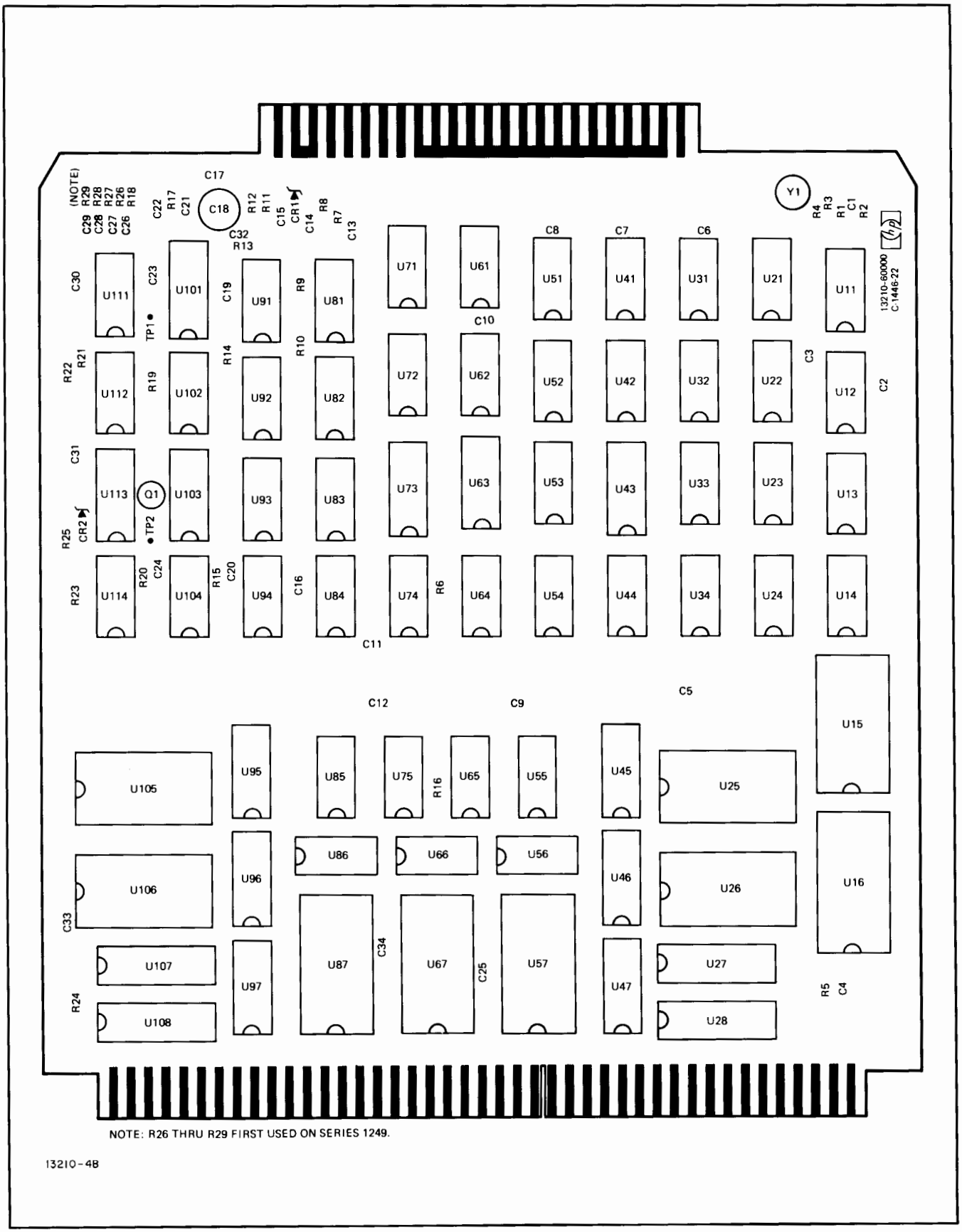


Figure 5-3. Disc Interface 2 PCA Parts Location Diagram

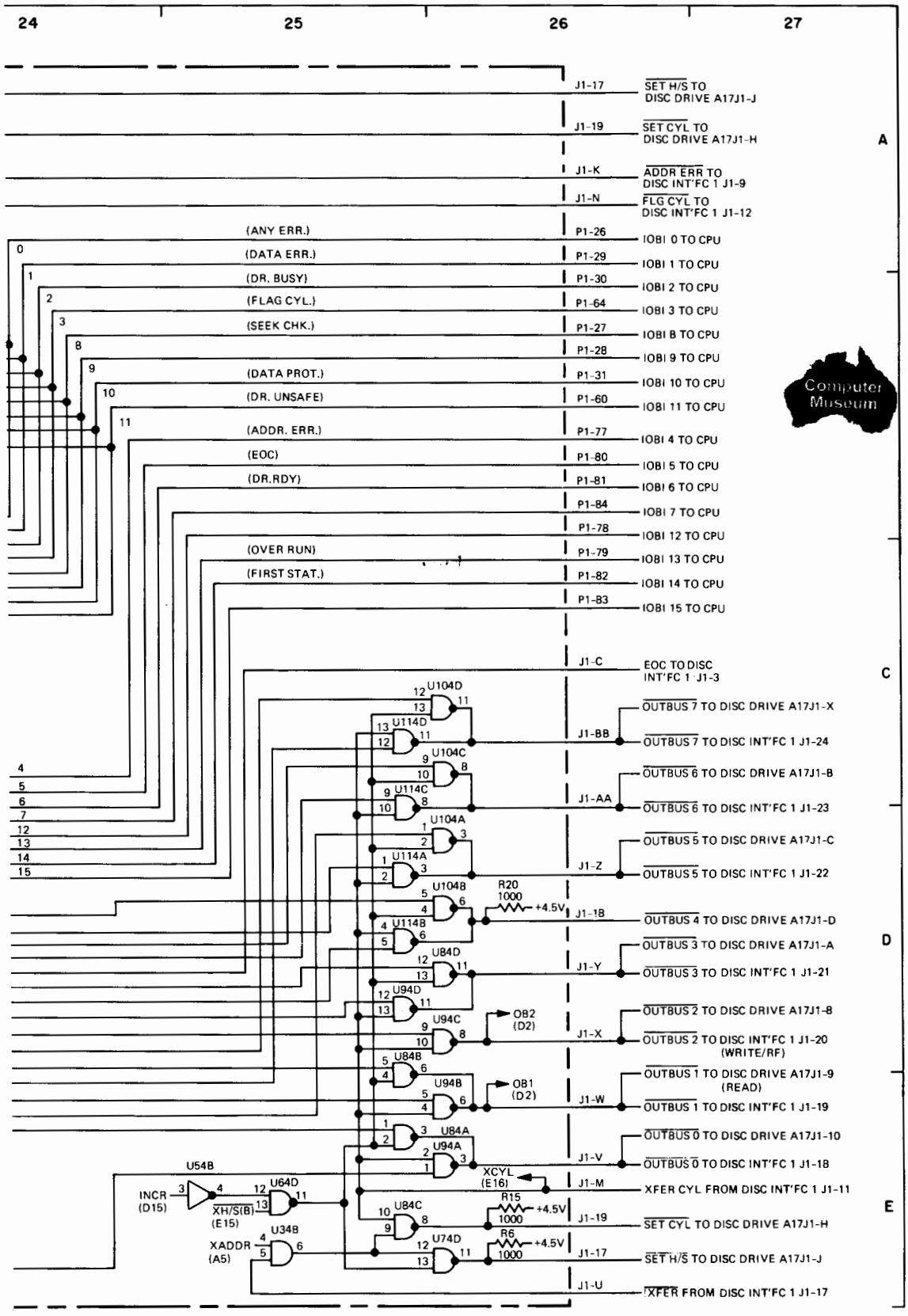
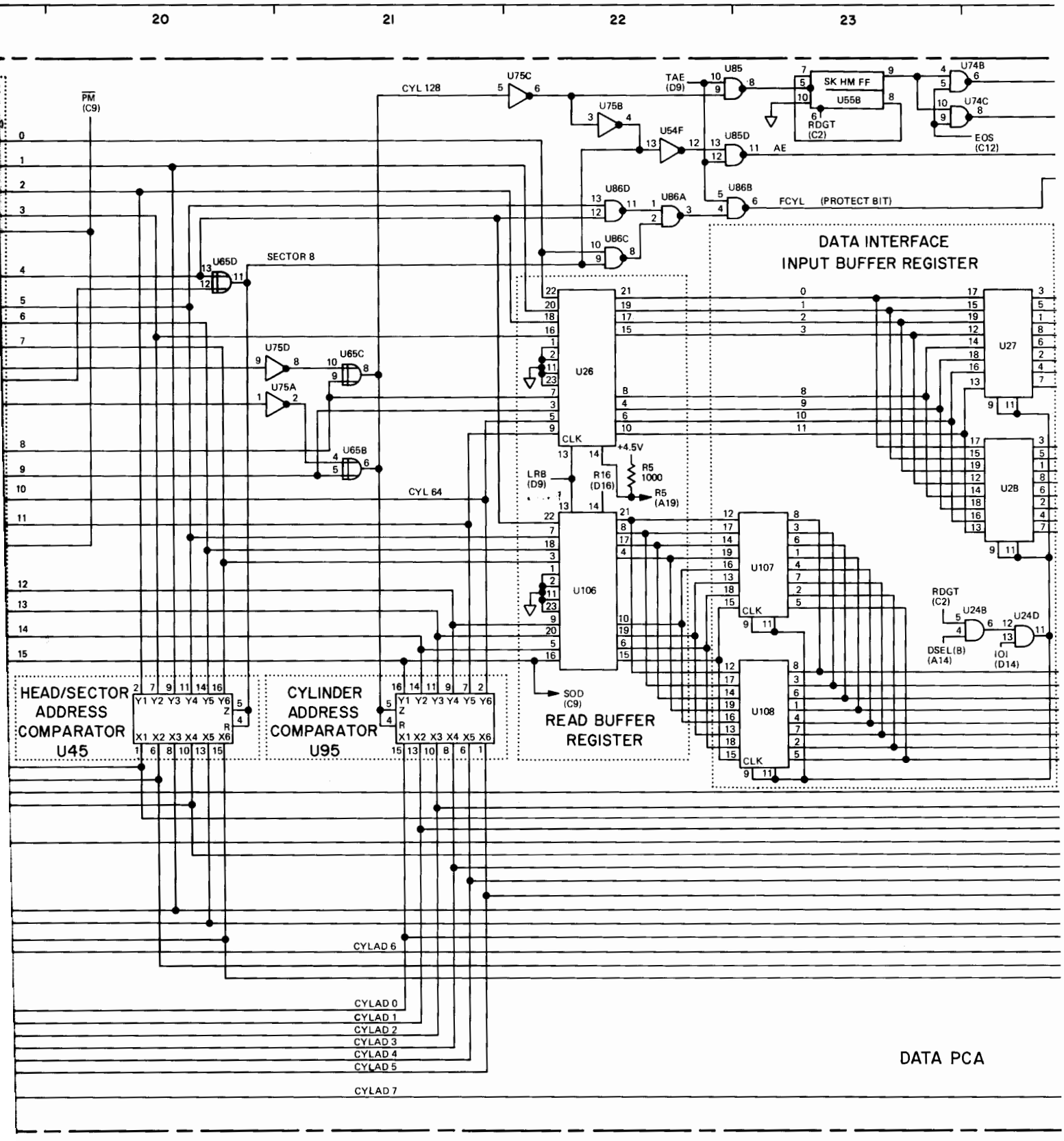
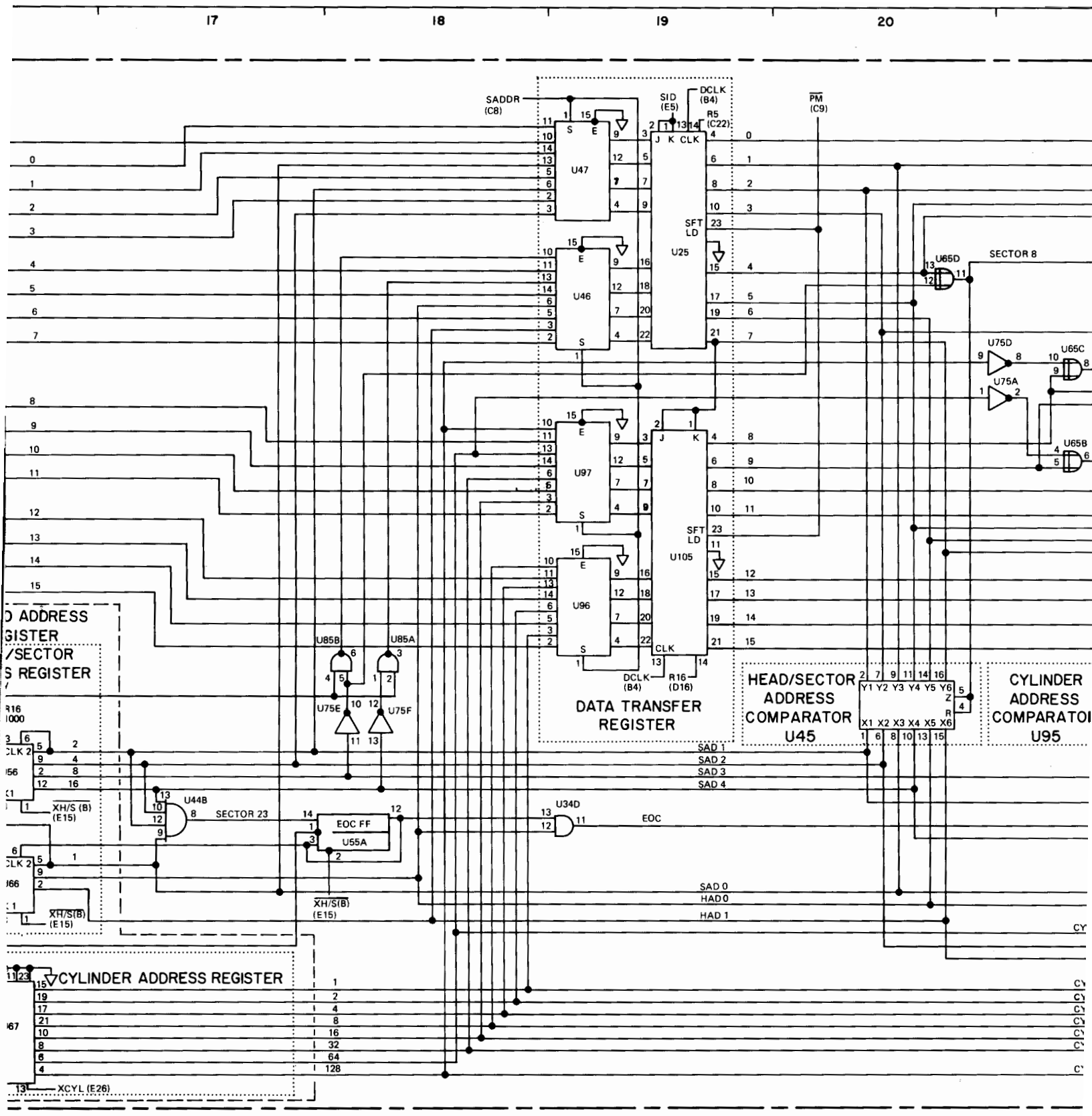
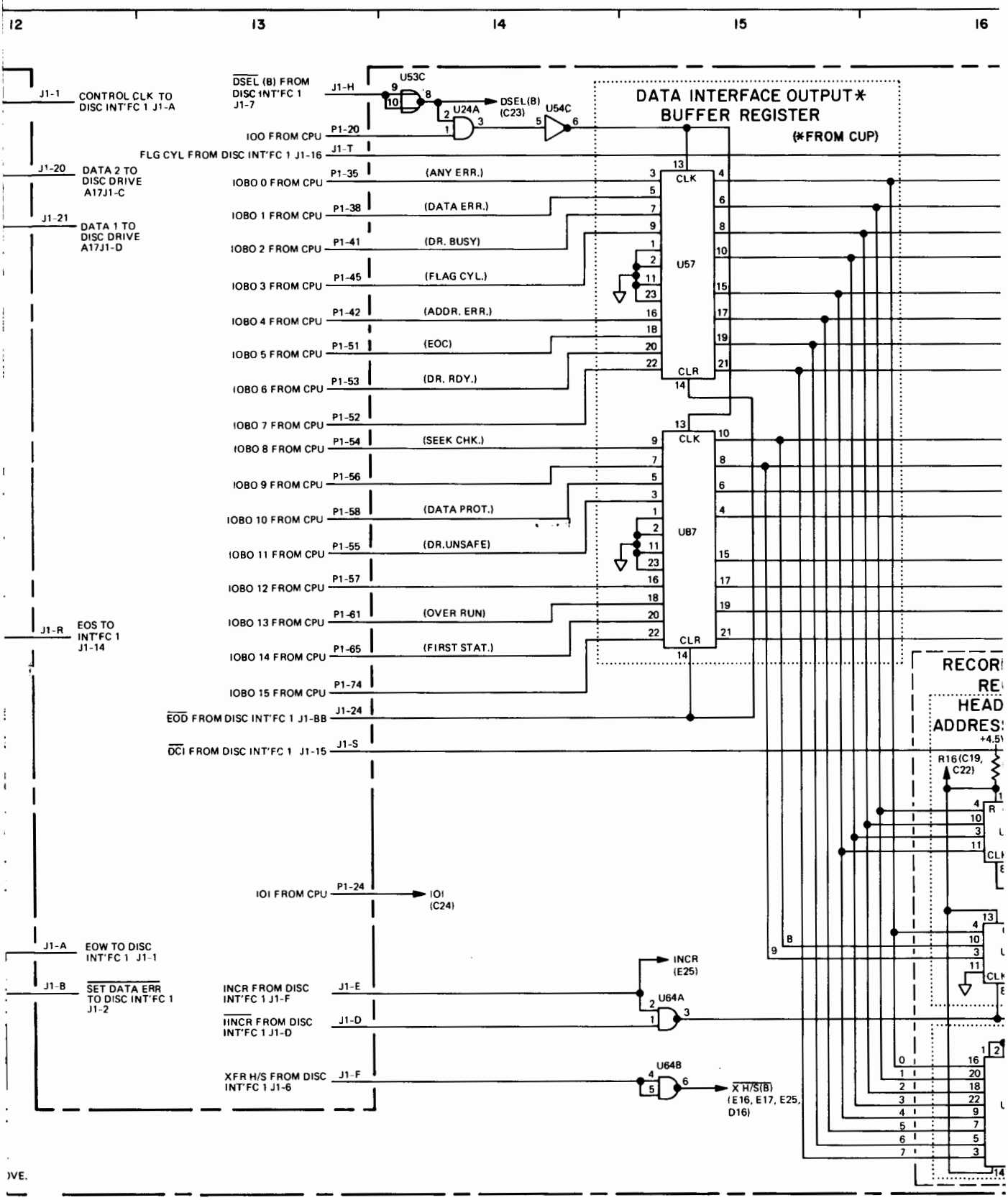
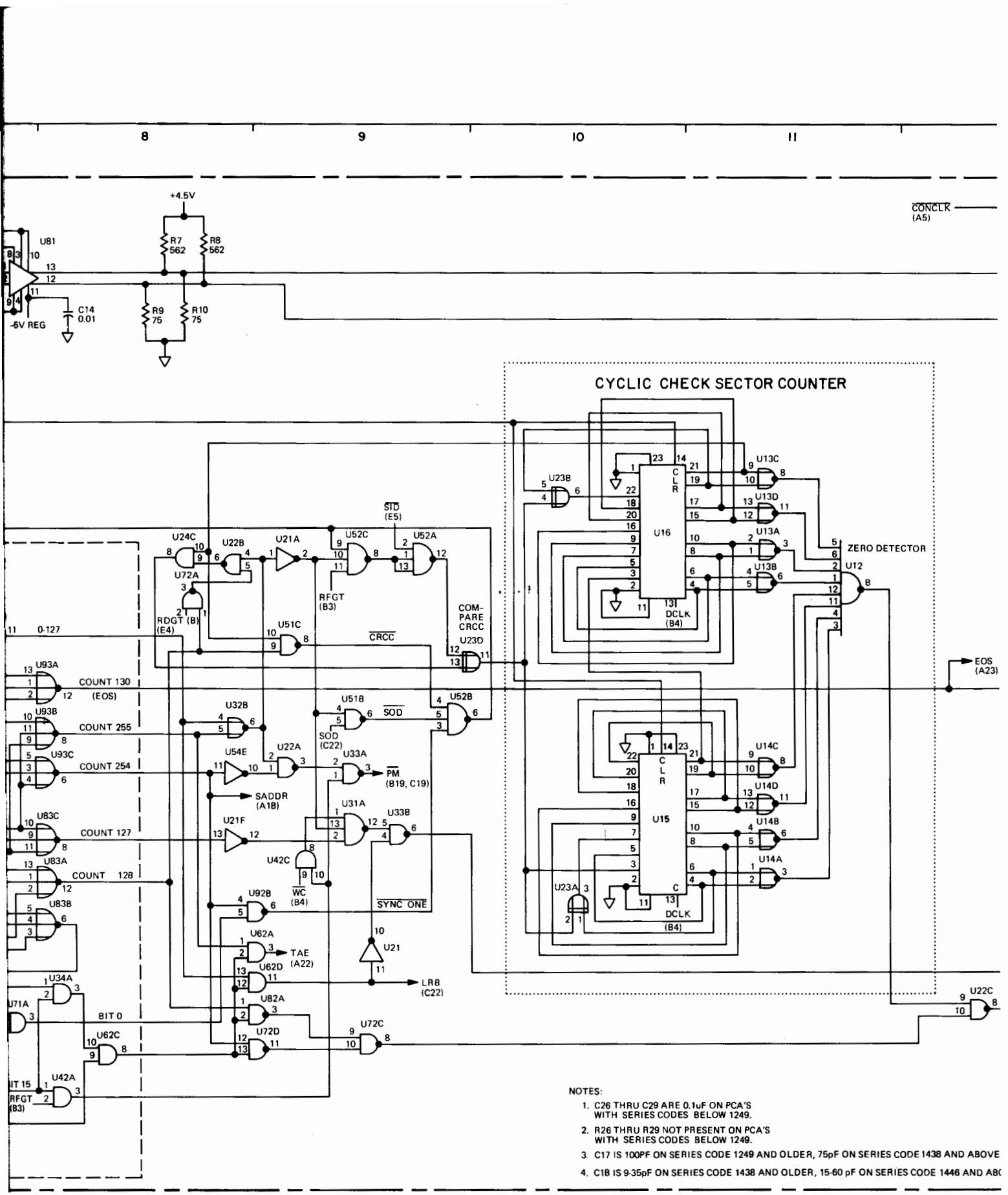


Figure 5-4. Disc Interface 2 PCA Schematic Diagram


20
21
22
23
PM (C9)
CYL 128
U75C
TAE (D9)
U85
U75B
U54F
U85D
AE
SK HM FF
U55B
RDGT (C2)
U74B
U74C
EOS (C12)
U86D
U86A
U86B
FCYL (PROTECT BIT)
U86C
DATA INTERFACE
INPUT BUFFER REGISTER
U65D
SECTOR 8
U75D
U65C
U75A
U65B
U26
CLK
+4.5V
R5 1000
LRB (D9)
R16 (D16)
R5 (A19)
CYL 64
U106
U107
U108
U27
U2B
RDGT (C2)
U24B
U24D
DSEL(B) (A14)
IOI (D14)
SOD (C9)
READ BUFFER REGISTER
HEAD/SECTOR ADDRESS COMPARATOR U45
CYLINDER ADDRESS COMPARATOR U95
CYLAD 6
CYLAD 0
CYLAD 1
CYLAD 2
CYLAD 3
CYLAD 4
CYLAD 5
CYLAD 7
DATA PCA

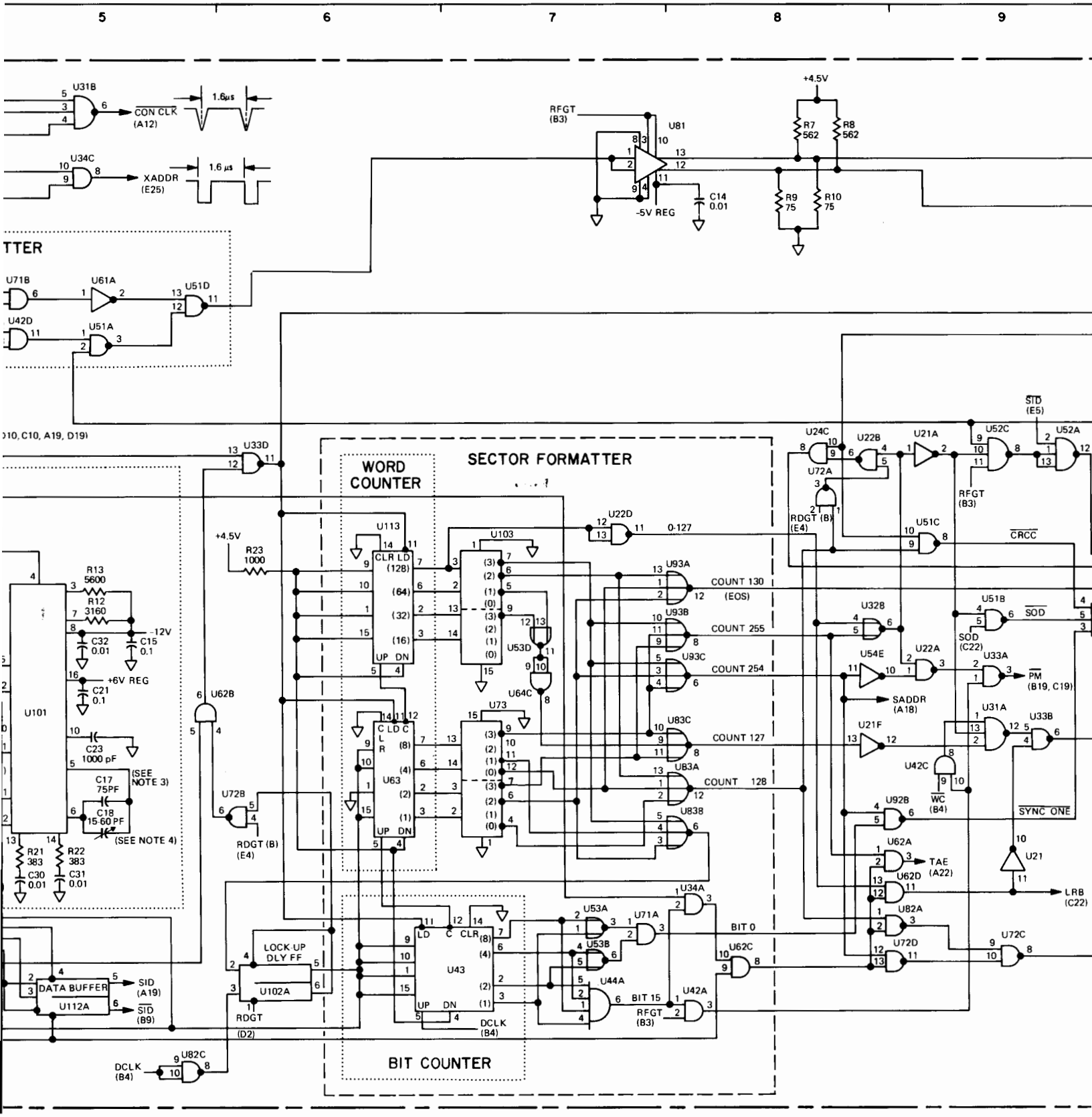

17
18
19
20
SADDR (C8)
SID (E5)
DCLK (B4)
R5 (C22)
PM (C9)
U47
U46
U97
U96
U25
U105
SFT LD
DATA TRANSFER REGISTER
U65D
SECTOR 8
U75D
U65C
U75A
U65B
U85B
U85A
U75E
U75F
HEAD/SECTOR ADDRESS COMPARATOR U45
CYLINDER ADDRESS COMPARATOR U95
SAD 1
SAD 2
SAD 3
SAD 4
U44B
SECTOR 23
EOC FF
U55A
U34D
EOC
SAD 0
HAD 0
HAD 1
XH/S (B) (E15)
XH/S(B) (E15)
CYLINDER ADDRESS REGISTER
XCYL (E26)


12
13
14
15
16
DATA INTERFACE OUTPUT* BUFFER REGISTER
(*FROM CUP)
J1-1 CONTROL CLK TO DISC INT'FC 1 J1-A
DSEL (B) FROM DISC INT'FC 1 J1-7
J1-H
U53C
U24A
DSEL(B) (C23)
U54C
IOO FROM CPU P1-20
FLG CYL FROM DISC INT'FC 1 J1-16 J1-T
J1-20 DATA 2 TO DISC DRIVE A17J1-C
J1-21 DATA 1 TO DISC DRIVE A17J1-D
IOBO 0 FROM CPU P1-35 (ANY ERR.)
IOBO 1 FROM CPU P1-38 (DATA ERR.)
IOBO 2 FROM CPU P1-41 (DR. BUSY)
IOBO 3 FROM CPU P1-45 (FLAG CYL.)
IOBO 4 FROM CPU P1-42 (ADDR. ERR.)
IOBO 5 FROM CPU P1-51 (EOC)
IOBO 6 FROM CPU P1-53 (DR. RDY.)
IOBO 7 FROM CPU P1-52
IOBO 8 FROM CPU P1-54 (SEEK CHK.)
IOBO 9 FROM CPU P1-56
IOBO 10 FROM CPU P1-58 (DATA PROT.)
IOBO 11 FROM CPU P1-55 (DR.UNSAFE)
IOBO 12 FROM CPU P1-57
IOBO 13 FROM CPU P1-61 (OVER RUN)
IOBO 14 FROM CPU P1-65 (FIRST STAT.)
IOBO 15 FROM CPU P1-74
U57
U87
CLK
CLR
J1-R EOS TO INT'FC 1 J1-14
EOD FROM DISC INT'FC 1 J1-BB J1-24
DCI FROM DISC INT'FC 1 J1-15 J1-S
IOI FROM CPU P1-24
IOI (C24)
J1-A EOW TO DISC INT'FC 1 J1-1
J1-B SET DATA ERR TO DISC INT'FC 1 J1-2
INCR FROM DISC INT'FC 1 J1-F J1-E
IINCR FROM DISC INT'FC 1 J1-D J1-D
XFR H/S FROM DISC INT'FC 1 J1-6 J1-F
INCR (E25)
U64A
U64B
X H/S(B) (E16, E17, E25, D16)
RECOR
RE
HEAD
ADDRES
+4.5V
R16(C19, C22)
)VE.



NOTES:

1. C26 THRU C29 ARE 0.1uF ON PCA'S WITH SERIES CODES BELOW 1249.
2. R26 THRU R29 NOT PRESENT ON PCA'S WITH SERIES CODES BELOW 1249.
3. C17 IS 100PF ON SERIES CODE 1249 AND OLDER, 75pF ON SERIES CODE 1438 AND ABOVE
4. C18 IS 9-35pF ON SERIES CODE 1438 AND OLDER, 15-60 pF ON SERIES CODE 1446 AND AB(


5
6
7
8
9
U31B
CON CLK
(A12)
1.6µs
U34C
XADDR
(E25)
1.6 µs
RFGT
(B3)
U81
+4.5V
R7
562
R8
562
R9
75
R10
75
C14
0.01
-5V REG
TTER
U71B
U61A
U51D
U42D
U51A
U33D
WORD
COUNTER
SECTOR FORMATTER
U113
U103
U22D
0-127
+4.5V
R23
1000
U93A
COUNT 130
(EOS)
U93B
COUNT 255
U93C
COUNT 254
U83C
COUNT 127
U83A
COUNT 128
U838
U53D
U64C
U73
U63
U62B
U72B
RDGT (B)
(E4)
U24C
U22B
U21A
U52C
U52A
U72A
RDGT (B)
(E4)
RFGT
(B3)
STD
(E5)
U51C
CRCC
U328
U51B
SOD
SOD
(C22)
U54E
U22A
U33A
PM
(B19, C19)
SADDR
(A18)
U31A
U21F
U33B
U42C
WC
(B4)
SYNC ONE
U92B
U62A
TAE
(A22)
U21
U62D
LRB
(C22)
U82A
U72D
U72C
U62C
BIT 0
U34A
U53A
U71A
U53B
U44A
BIT 15
U42A
RFGT
(B3)
U43
LOCK-UP
DLY FF
U102A
RDGT
(D2)
DCLK
(B4)
U82C
DCLK
(B4)
DATA BUFFER
U112A
SID
(A19)
SID
(B9)
BIT COUNTER
U101
R13
5600
R12
3160
-12V
C32
0.01
C15
0.1
+6V REG
C21
0.1
C23
1000 pF
C17
75PF
(SEE
NOTE 3)
C18
15-60 PF
(SEE NOTE 4)
R21
383
C30
0.01
R22
383
C31
0.01
)10, C10, A19, D19)

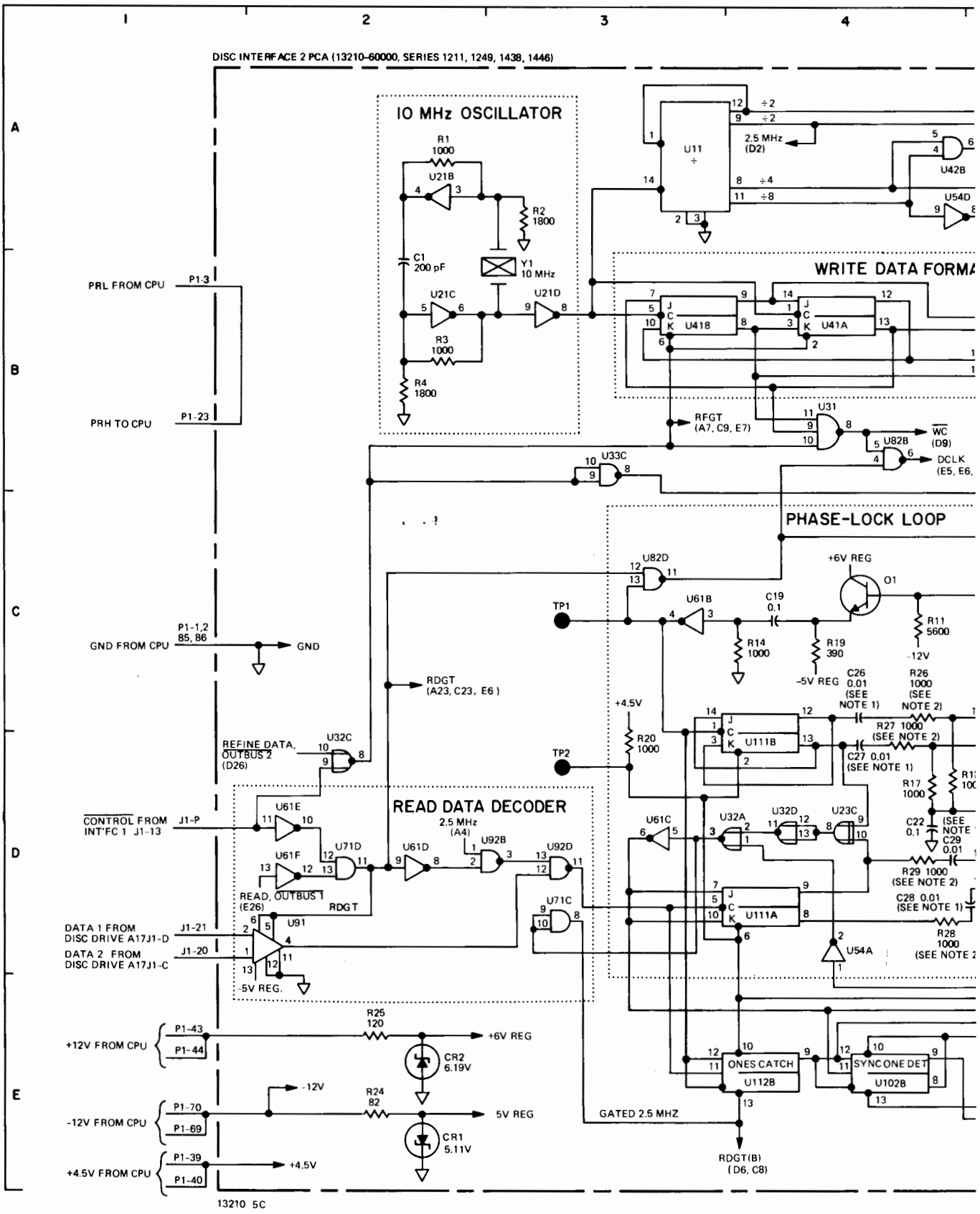

DISC INTERFACE 2 PCA (13210-60000, SERIES 1211, 1249, 1438, 1446)
10 MHz OSCILLATOR
READ DATA DECODER
PHASE-LOCK LOOP
WRITE DATA FORMA
PRL FROM CPU
P1-3
PRH TO CPU
P1-23
GND FROM CPU
P1-1,2
85, 86
GND
CONTROL FROM INT'FC 1 J1-13
J1-P
DATA 1 FROM DISC DRIVE A17J1-D
J1-21
DATA 2 FROM DISC DRIVE A17J1-C
J1-20
+12V FROM CPU
P1-43
P1-44
-12V FROM CPU
P1-70
P1-69
+4.5V FROM CPU
P1-39
P1-40
13210 5C
R1 1000
R2 1800
R3 1000
R4 1800
C1 200 pF
Y1 10 MHz
U21B
U21C
U21D
U11
2.5 MHz (D2)
U42B
U54D
U418
U41A
RFGT (A7, C9, E7)
U31
WC (D9)
U82B
DCLK (E5, E6,
U33C
U82D
+6V REG
Q1
TP1
U61B
C19 0.1
R11 5600
-12V
R14 1000
R19 390
-5V REG
C26 0.01 (SEE NOTE 1)
R26 1000 (SEE NOTE 2)
RDGT (A23, C23, E6)
+4.5V
R20 1000
TP2
U111B
R27 1000 (SEE NOTE 2)
C27 0.01 (SEE NOTE 1)
REFINE DATA, OUTBUS 2 (D26)
U32C
U61E
U61F
U71D
U61D
U92B
U92D
U71C
U91
READ, OUTBUS 1 (E26)
RDGT
2.5 MHz (A4)
-5V REG.
U61C
U32A
U32D
U23C
R17 1000
C22 0.1
C29 0.01
R29 1000 (SEE NOTE 2)
C28 0.01 (SEE NOTE 1)
U111A
R28 1000
U54A
R25 120
+6V REG
CR2 6.19V
R24 82
-12V
5V REG
CR1 5.11V
+4.5V
ONES CATCH U112B
SYNC ONE DET U102B
GATED 2.5 MHZ
RDGT(B) (D6, C8)

Table 5-4. Interconnecting Cable Plug-to-Plug Connections

DISC INTERFACE 1 (P1) PIN	CONNECTS TO	DISC INTERFACE 2 (P2) PIN	CONNECTS TO	DISC DRIVE (P3) PIN	CONNECTS TO
1	P2-A	1	P1-A	1	P1-13, P2-P
2	P2-B	2	Common	2	P1-18, P2-V
3	P2-C	3	Common	3	P1-21, P2-Y
4	P3-V	4	Common	4	Common
5	P3-W	5	Common	5	Common
6	P2-F	6	Common	6	Common
7	P2-H	7	Common	7	Common
8	P3-U	8	Common	8	Common
9	P2-K	9	Common	9	Common
10	P3-R	10	Common	10	Common
11	P2-M	11	Common	11	Common
12	P2-N	12	Common	12	Common
13	P2-P, P3-1	13	Common	13	Common
14	P2-R	14	Common	14	Common
15	P2-S	15	Common	15	Common
16	P2-T	16	Common	16	Common
17	P2-U	17	P3-B	17	Common
18	P2-V, P3-2	18	P3-H	18	Common
19	P2-W, P3-A	19	P3-C	19	Common
20	P2-X, P3-S	20	P3-Z, P3-22	20	Common
21	P2-Y, P3-3	21	P3-Y	21	Common
22	P2-Z, P3-J	22	NC	22	P3-Z
23	P2-AA, P3-K	23	NC	23	NC
24	P2-BB, P3-D	24	P1-BB	24	Shield
A	P2-1	A	P1-1	A	P1-19, P2-W
B	NC	B	P1-2	B	P2-17
C	NC	C	P1-3	C	P2-19
D	P2-D	D	P1-D	D	P1-BB, P2-24
E	NC	E	P1-F	E	P1-S
F	P2-E	F	P1-6	F	P1-T
H	P3-T	H	P1-7	H	P2-18
J	P3-U	J	NC	J	P1-22, P2-Z
K	NC	K	P1-9	K	P1-23, P2-AA
L	NC	L	NC	L	NC
M	P3-X	M	P1-11	M	P1-V
N	P3-P	N	P1-12	N	P1-U
P	NC	P	P1-13	P	P1-N
R	NC	R	P1-14	R	P1-10
S	P3-E	S	P1-15	S	P1-20, P2-X
T	P3-F	T	P1-16	T	P1-H
U	P3-N	U	P1-17	U	P1-8
V	P3-M	V	P1-18, P3-2	V	P1-4
W	NC	W	P1-19, P3-A	W	P1-5
X	NC	X	P1-20, P3-S	X	P1-M
Y	NC	Y	P1-21, P3-3	Y	P2-21
Z	NC	Z	P1-22, P3-J	Z	P2-20, P3-22
AA	NC	AA	P1-23, P3-K	AA	NC
BB	P2-24	BB	P1-24, P3-D	BB	Shield

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section provides information for ordering replacement parts for the disc drive interface kit. Separate parts lists and parts location diagrams are provided for each printed-circuit assembly in section V of this manual. Parts are listed in these tables in alphanumeric order by reference designation. Table 6-1 is a complete parts list for the disc drive interface kit.

6-3. Table 6-1 lists the following information for each part:

a. Hewlett-Packard part number.

b. Description of the part. (Refer to table 6-2 for an explanation of abbreviations used in the DESCRIPTIONS column.)

c. Typical manufacturer of the part as a five-digit code. (Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.)

d. Manufacturer's part number.

6-4. ORDERING INFORMATION.

6-5. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Kit model number.

b. HP stock number for each part.

c. Description of each part.

Table 6-1. HP 13210A Disc Drive Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
13210-60000	DISC INTERFACE 2 PCA (Refer to table 5-3.)	28480	13210-60000	1
13210-60003	INTERFACE CABLE	28480	13210-60003	1
13210-60004	DISC INTERFACE 1 PCA (Refer to table 5-2.)	28480	13210-60004	1
13210-90003	OPERATING AND SERVICE MANUAL	28480	13210-90003	1

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or microcircuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= cable, jumper
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
ad	= anode			ph	= Phillips head
Al	= aluminum	H	= henries	pk	= peak
AR	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	PIV	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
B	= base	hex	= hexagon, hexagonal	PWV	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rmo	= rack mount only
Be Cu	= beryllium copper	insul	= insulation, insulated	rms	= root-mean-square
		impgrg	= impregnated	RWV	= reverse working voltage
C	= collector	incand	= incandescent	rect	= rectifier
cw	= clockwise	ips	= inches per second	r/min	= revolutions per minute
ccw	= counterclockwise			RTL	= resistor-transistor logic
cer	= ceramic	k	= kilo (10^3), kilohm		
cmo	= cabinet mount only			s	= second
com	= common	lp	= low pass	SB, TT	= slow blow
crt	= cathode-ray tube			Se	= selenium
CTL	= complementary-transistor logic	m	= milli (10^{-3})	Si	= silicon
		M	= mega (10^6), megohm	scr	= silicon controlled rectifier
cath	= cathode	My	= Mylar	sil	= silver
cd pl	= cadmium plate	mfr	= manufacturer	sst	= stainless steel
comp	= composition	mom	= momentary	stl	= steel
conn	= connector	mtg	= mounting	spcl	= special
compl	= complete	misc	= miscellaneous	spdt	= single-pole, double-throw
		Met Ox	= metal oxide	spst	= single-pole, single-throw
dc	= direct current	mintr	= miniature	semicond	= semiconductor
dr	= drive				
DTL	= diode-transistor logic	n	= nano (10^{-9})	Ta	= tantalum
depc	= deposited carbon	n.c.	= normally closed or no connection	td	= time delay
dpdt	= double-pole, double-throw			Ti	= titanium
dpst	= double-pole, single-throw	Ne	= neon	tgl	= toggle
		no.	= number	thd	= thread
E	= emitter	n.o.	= normally open	tol	= tolerance
ECL	= emitter-coupled logic	np.	= nickel plated	TTL	= transistor transistor logic
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	U(μ)	= micro (10^{-6})
elctlt	= electrolytic				
		NSR	= not separately replaceable	V	= volt(s)
F	= farads	NRFR	= not recommended for field replacement	var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head	OD	= outside diameter	VDCW	= direct current working volts
Flm	= film	OBD	= order by description		
Fxd	= fixed	orn	= orange	W	= watts
filh	= fillister head	ovh	= oval head	ww	= wirewound
		oxd	= oxide	wht	= white
G	= giga (10^9)			WIV	= working inverse voltage
Ge	= germanium	p	= pico (10^{-12})		
gl	= glass	PC	= printed circuit	yel	= yellow
gnd	= ground(ed)				

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wisconsin
01295	Texas Instruments Inc. Semiconductor Components Div.	Dallas, Texas
04713	Motorola Semiconductor Prod. Inc.	Phoenix, Arizona
07263	Fairchild Camera & Inst. Corp. Semiconductor Div.	Mountain View, California
12040	National Semiconductor Corp.	Danbury, Connecticut
18324	Signetics Corp.	Sunnyvale, California
19701	Mepco/Electra Inc. Electra Div.	Mineral Wells, Texas
28480	Hewlett-Packard Company	Palo Alto, California
56289	Sprague Electric Co.	N. Adams, Massachusetts
72136	Electro Motive Mfg. Co. Inc.	Willimantic, Connecticut
72982	Erie Technological Prod. Inc.	Erie, Pennsylvania
80131	Electronic Industries Association	Washington D.C.
91418	Radio Materials Co.	Chicago, Illinois
96733	San Fernando Electric Mfg. Co.	San Francisco, California

CHANGE	DESCRIPTION
1	Pages 5-4 and 5-7; table 5-2 and figure 5-4. Change C17 from 100 pF, part no. 0160-2204 to 110 pF, part no. 0140-0194.
2	Page 5-7, figure 5-4. a. Add connection between U112B pin 12 and U61C pin 5; delete the connection between U112B pin 12 and U61B pin 4. b. Delete U54A from the circuit and connect U32A pin 1 to U32A pin 2.
3	Page 5-4, table 5-2; page 5-7, figure 5-4. Change R11 and R13 from 5.6k, part no. 0683-5625 to 12k, part no. 0683-1235.
4	Page 5-3, figure 5-2. Add connection between U35D pin 13 and U52A pin 1. Delete $\overline{\text{CRS}}$ signal connection from State Decoder, U21 pin 4.
5	Page 5-3, figure 5-2. Delete connection between U52A pin 13 and pin 2. Add connection between U36A pin 3 (near IOI input) and U52A pin 13.

MANUAL PART NO. 13210-90003
MICROFICHE PART NO. 13210-90008

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