Operating and Service Manual HP 13192A and HP 13193A

Write Test and Read Test Accessories

(For The Digital Magnetic Tape Unit)

Printed-Circuit Assemblies:
13192-60010, Series 1037
13192-60020, Series 1028
13192-60030, Series 1028
13193-60010, Series 1405

MANUAL PART NO. 13192-90002

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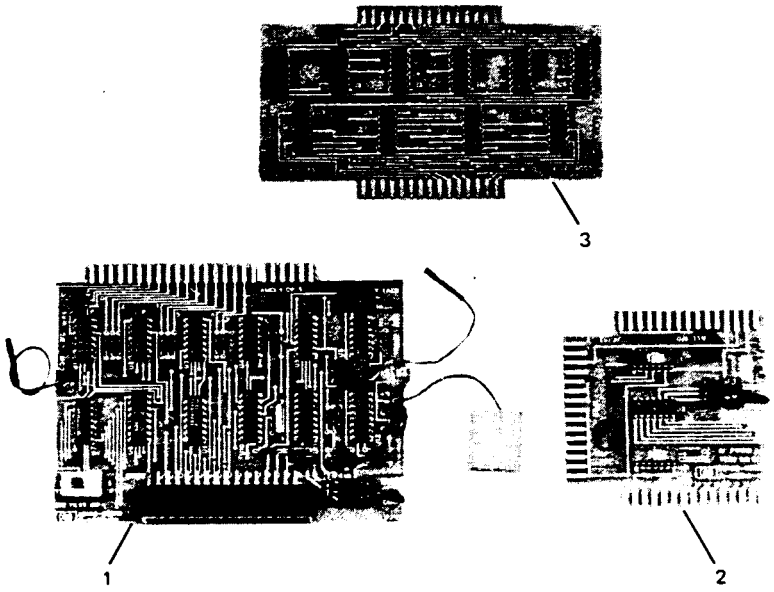

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WRITE TEST ACCESSORY
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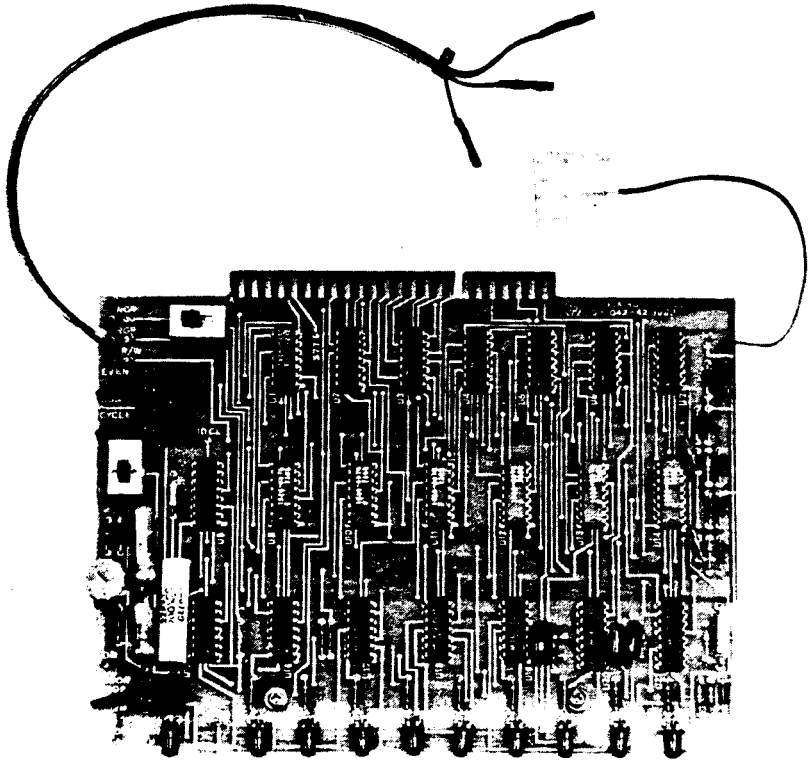
2. WRITE PROGRAM 1 TEST PCA (A2)
3. WRITE PROGRAM 2 TEST PCA (A3)



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READ TEST PCA

Figure 1-1. HP 13192A Write Test Accessory and HP 13193A Read Test Accessory

SECTION I GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual provides general information, installation, operation, theory of operation, and maintenance information for the HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory.

1-3. DESCRIPTION.

1-4. The read test accessory and the write test accessory, in conjunction with related test accessories, provide the means to exercise the write and read capability of HP 7970 Series Digital Magnetic Tape Units that record in non-return-to-zero, inverted (NRZI) format in an off-line environment.

1-5. The HP 13192A Write Test Accessory consists of three printed-circuit assemblies (PCA's) as shown in figure 1-1. The main write test PCA, part no. 13192-60010, plugs directly into a connector on the tape unit write assembly motherboard. Write program 1 and write program 2 PCA's are capable of providing one of five pre-programmed, 10-character write test patterns when plugged into the main write test PCA. There is also a custom-programmed general purpose test PCA, which is available, as an option, to the user who desires his own test pattern.

1-6. In addition to the 10 characters, the write test accessory provides either even or odd parity, initiates a longitudinal redundancy check character (LRCC), and generates a variable-rate write clock (WC). The write clock rate is adjustable to cover magnetic tape recording densities of 200 to 800 bits per inch, (bpi) over a tape speed range of 10-to-45 inches per second (ips). The write test data can be generated in a continuous format for cross-talk (X TALK) checks, or in an interrupted (BLOCK) format. A write status (SW) indicator on the main write test PCA is turned on when write- and erase-head current is established in the tape unit.

1-7. The HP 13193A Read Test Accessory (see figure 1-1) plugs directly into the read assembly motherboard of the tape unit. The read test PCA has several modes of operation to read parity errors when reading data previously written on magnetic tape.

1-8. Both the write test accessory and the read test PCA use TTL and DTL integrated circuits. The write test PCA's derive +5 volts operating power from the tape unit write assembly. The tape unit read assembly also provides 5-volt operating power for the read test PCA.

1-9. RELATED ACCESSORIES.

1-10. There are two related test accessories that are used with the write test accessory and the read test accessory:

a. HP 13191A Control and Status Test Accessory.

b. "Scratch" Tape.

1-11. The control and status test PCA is a requirement for both read and write tests. The "scratch" tape is used when a write, or read-after-write (R/W) test function is being performed.

1-12. RELATED MANUALS.

1-13. The following manuals contain information which is pertinent to the use of the write test accessory and the read test accessory:

a. *HP 13191A Control and Status Test Accessory Operating and Service Manual*, part number 13191-90000.

b. *HP 7970A Digital Magnetic Tape Unit Operating and Service Manual*, part number 07970-90620.

c. *HP 7970B/C Digital Magnetic Tape Unit Operating and Service Manual*, part number 07970-90383.

d. *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*, part number 07970-90765.

1-14. IDENTIFICATION.

1-15. Hewlett-Packard uses five digits and a letter (00000A) for standard accessory identification designations. If the designation of your accessory does not agree with that on the title page of this manual, there are differences between your accessory kit and the kit described in this manual. These differences are described in change sheets and manual supplements that are available at the nearest HP Sales and Service Office. These offices are listed in the back of this manual.

1-16. Printed-circuit assembly revisions are identified by a letter, series code, and a division code stamped on the PCA (e.g. A-1152-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the schematic diagram in this manual, there are differences between the PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements that are available at the nearest HP Sales and Service Office.

1-17. SPECIFICATIONS.

1-18. Specifications for the HP 13192A Write Test Accessory are listed in table 1-1. Specifications for the Read Test Accessory are listed in table 1-2.

Table 1-1. Write Test Accessory Specifications

SIZE

HP 13192-60010 Main Write Test PCA:	5-11/16 by 4-5/16 inches
HP 13192-60020 Write Program 1 Test PCA Board:	3-5/16 by 3-5/16 inches
HP 13192-60030 Write Program 2 Test PCA Board:	5-11/16 by 3-5/16 inches

SHIPPING WEIGHT

4 lbs net

POWER REQUIREMENTS (supplied by tape unit)

+5 volts dc @ 400 ma maximum

LOGIC LEVELS (negative logic)

TTL:

Assertion (Logic 1) is less than, or equal to +0.8V (7.8 ma @ +0.4V)

Negation (Logic 0) is greater than, or equal to +2.0V (1.55 ma @ +2.4V)

DTL:

Assertion (Logic 1) is less than, or equal to +0.4V (33 ma @ +0.4V)

Negation (Logic 0) is greater than, or equal to +2.4V (1.5 ma @ +2.4V)

WRITE DATA:

TAPE DENSITY:	200 to 800 bpi
TAPE SPEED:	10 to 45 ips

Seven- or nine-track tape data test capability

DATA PARITY:	Odd or even
RECORDING FORMATS:	6 Standard write pattern programs
	1 optional custom write pattern program
OPERATING MODES:	Continuous
	Block
EQUIPMENT COMPATIBILITY:	HP 7970A, 7970B/C Digital Magnetic Tape Unit

Table 1-2. Read Test Accessory Specifications

SIZE

5-13/16 by 7-1/2 inches

SHIPPING WEIGHT

3 lbs net

POWER REQUIREMENTS

+5 volts dc @ 300 ma (supplied by tape unit)

LOGIC LEVELS (negative Logic)

TTL:

Assertion (Logic 1) is less than, or equal to +0.8V (7.8 ma @ +0.4V)

Negation (Logic 0) is greater than, or equal to +2.0V (1.55 ma @ +1.4V)

DTL:

Assertion (Logic 1) is less than, or equal to +0.4V (33 ma @ +0.4V)

Negation (Logic 0) is greater than, or equal to +2.4V (1.5 ma @ +2.4V)

READ DATA:

TAPE DENSITY:	200 to 800 bpi
TAPE SPEED:	10 to 45 ips seven- or nine-track tape test capability
PARITY DETECTION:	Odd or even, vertical (lateral) and longitudinal
OPERATING MODES:	Continuous Block Cycle (Alternate forward and reverse tape motion)
EQUIPMENT COMPATIBILITY:	HP 7970A, HP 7970B/C Digital Magnetic Unit

SECTION II INSTALLATION

2-1. INTRODUCTION.

2-2. The HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory are factory-checked to assure performance to the published specifications before being packed for shipment. This section provides information to determine that these test accessories have been received intact. Installation instructions for these test accessories and other associated tape unit accessory connections are included. Initial plug and jumper connections, as well as tape unit compatibility adjustments for the test PCA's are included in this section.

2-3. UNPACKING AND INSPECTION.

2-4. Before unpacking, inspect the shipping carton for damage. If damage to the shipping carton is evident, request that the carrier's shipping agent be present when the accessories are unpacked. After unpacking, inspect the accessories for mechanical damage (cracks, broken parts, etc).

2-5. If any PCA is damaged, and fails to meet the published specification, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (HP Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing materials for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged PCA without waiting for any claims against the carrier to be settled.

2-6. INSTALLATION PREPARATION.

2-7. Turn off power on the tape unit to be tested (the master tape unit in a master-slave multi-unit application) and take the tape unit physically off-line by removing the computer interface connector cables.

2-8. Installation of the HP 13191A Control and Status Test Accessory is required for operating the HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory. The procedure for installing the control and status test PCA is described in the HP 13191A manual. A part of the control and status test accessory operating and installation procedures is repeated in this manual for convenience.

2-9. For performing a write/read test on read-after-write tape units, install a "scratch" tape with a write enable ring inserted. (Inspect the tape pack for damage. Do not use tape that shows signs of abuse.) For testing read-only tape units, install a pre-recorded test tape.

2-10. INSTALLATION.

2-11. Installing the HP 13192A Write Test Accessory, the HP 13193A Read Test Accessory, and the HP 13191A Control and Status Test Accessory consists of plugging these boards into the tape unit write assembly, read assembly, and control and status PCA, respectively. Table 2-1 lists the signal-jumper connections that are required for the six basic test operations performed with these test accessories. Figure 2-1 shows the test PCA's installed. Figure 2-2 provides an overall installation and interconnection diagram. Paragraphs 2-12 through 2-14 describe the individual test PCA installations in detail. The write clock (WC) adjustment indicated in paragraph 2-14 must be performed whenever the write test accessory is used.

2-12. CONTROL AND STATUS TEST PCA INSTALLATION.

2-13. The following steps are always performed when using the control and status PCA. Other connections and switch positions are according to the particular test function.

a. Plug the HP 13191A Control and Status Test PCA (component side forward) into J2A of the tape unit control and status PCA (A16), as shown in figure 2-1. Do not force the PCA, a keying slot prevents installation if the board is being inserted incorrectly.

b. Connect the control and status PCA +5V jumper P2 to the +5V pin of the tape unit control and status PCA (A16) as shown in figure 2-2.

c. Observe the position of the CS (unit address select) jumper on the tape unit A16 PCA. On the control and status test PCA, connect jumper P1 to the CS pin (i.e. OFF, CS0, CS1, CS2, or CS3) that corresponds to the position of the CS jumper on the tape unit A16 PCA. If the optional tape unit front panel unit address select switches are installed, the test PCA and jumper P1 tape unit A16 CS jumper should be in the OFF position.

2-14. MAIN WRITE TEST PCA INSTALLATION.

a. Plug the main write test PCA (component side into WJ11 of the tape unit write assembly motherboard, as shown in figure 2-1.

b. Connect main write test PCA +5V power connector, XA2 to WJ12 of the write assembly motherboard A17, as shown in figure 2-2.

Table 2-1. Test PCA Signal-Jumper Connections

Basic Test Operation	Test PCA Signal-Jumper Connections (See Note)
Write (Block)	(W)CF jumper to (C)WCF pin
Write (Continuous)	No signal jumpers required
Read (Block-CF)	(R)RCF jumper to (C)CF pin
Read (Block-Cycle)	(R)RCF jumper to (C)CF pin (R)RCR jumper to (C)CR pin
Read After Write	(R)RCF jumper to (C)CF pin (W)CF jumper to (C)WCF pin (R)R/W jumper to (C)R/W pin
Read (Continuous)	(R)RCF jumper to C(CF) pin

NOTE: (W) = HP 13191A Main Write Test Accessory
(R) = HP 13193A Read Test Accessory
(C) = HP 13191A Control and Status Test Accessory

c. Connect main write test PCA CF (Forward Command) jumper P1, to the WCF (Write, Forward Command) pin of the control and status test PCA, as shown in figure 2-2.

d. Plug one of the following write test program PCA's into XA1 (component side up) of the main write test board as shown in figure 2-1:

(1) Write program 1 test PCA

(2) Write program 2 test PCA

e. Set the tape unit power switch to ON and perform the following write clock (WC) rate adjustment:

(1) Connect an HP 5245L Electronic Frequency Counter or equivalent to the tape unit write PCA (A17A1) WC test point (see figure 2-2).

(2) On the main write test PCA, connect the HI/LOW jumper (P2), and adjust the clock rate potentiometer (R13) for an 800 bits per inch (bpi) test that corresponds to the speed of the tape unit listed in table 2-2). For any other tape unit recording density or tape speed, use the following formula:

WC Rate = BPI X IPS.

2-15. READ TEST PCA INSTALLATION.

a. Set tape unit power switch to OFF

b. Plug read test PCA (component side up) into RJ11 of A18, the tape unit read assembly motherboard, as shown in figure 2-1. Do not force the PCA. A keying slot prevents installation if the board is being inserted incorrectly.

c. Connect the read test PCA +5V power connector XA1 to RJ12 of the Read Assembly Motherboard.

d. Connect the RCF (Read Command Forward) blue jumper lead on the read test PCA to the CF pin of the control and status test PCA, as shown in figure 2-2.

e. Connect the (read-after-write) R/W black jumper lead on the read test PCA to the R/W pin of the control and status test PCA, as shown in figure 2-2.

f. Connect the RCR (Read Command Reverse) red jumper lead on the read test PCA to the CR pin of the control and status test PCA.

2-16. INSTALLATION CHECK.

2-17. The correct performance of the installed test PCA's should be verified as soon as possible after these PCA's have been received. Paragraph 3-28 (in section III) provides a read-after-write (R/W) check procedure that adequately exercises the write test PCA and the read test PCA. Successful completion of this check indicates that the test PCA's are operating correctly.

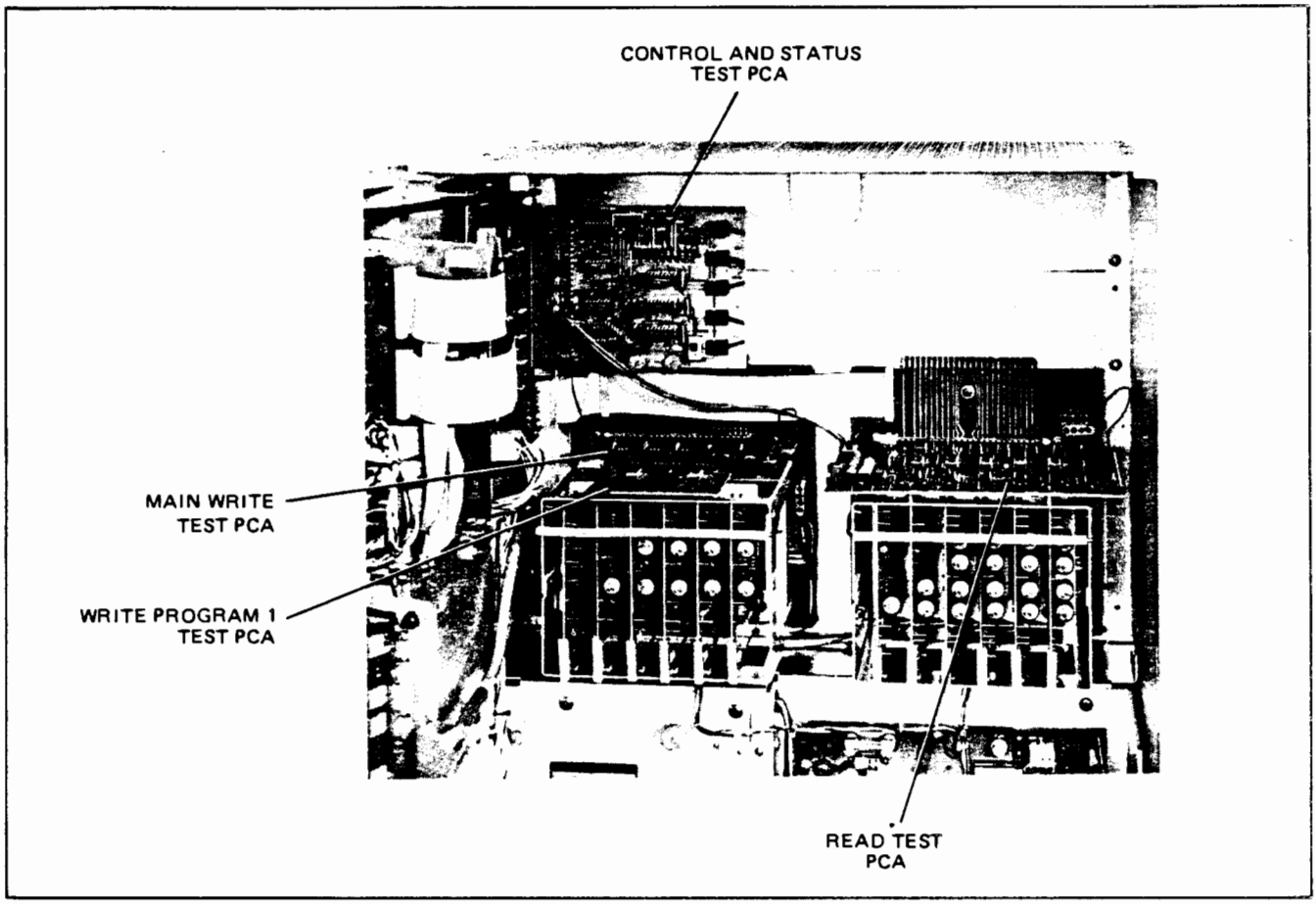

Figure 2-1. Test Accessory Installation

Table 2-2. Main Write Test PCA Clock Rate Adjustment (800 bpi)

Tape Unit Speed, Inches Per Seconds (ips)	Write Test PCS HI/LOW Jumper (P2)	WC Rate (Indicated on frequency counter)
12.5	LO	10 ±0.1 kHz
25	HI	20 ±0.2 kHz
37.5	HI	30 ±0.3 kHz
45	HI	36 ±0.33 kHz

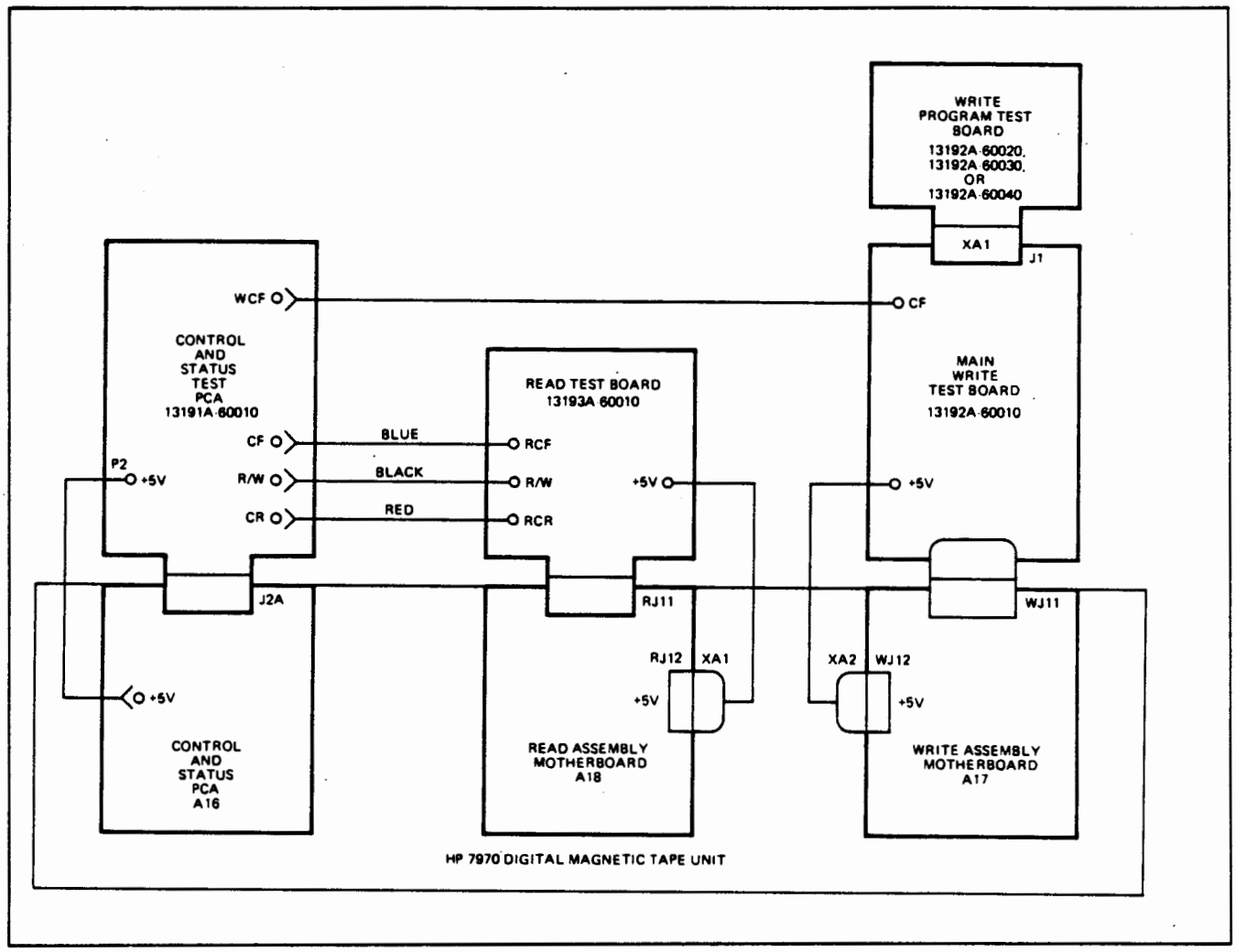

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Figure 2-2. Test Accessory Interconnection Diagram

SECTION III OPERATION

3-1. INTRODUCTION.

3-2. This section contains information required to operate the 13192A Write Test Accessory and the HP 13193A Read Test Accessory. Application information, which lists the various HP 7970 Digital Magnetic Tape Unit tests that are performed with these test boards, is included. References are made to the appropriate tape unit operating and service manual sections where the actual test procedures are described.

3-3. Control and indicator descriptions are included in this section. All controls and indicators on the test PCA's are identified, and the function of each is briefly explained. A discussion of the overall operation, and the interrelated functions of the test boards is also presented.

3-4. Part of this section describes a typical test procedure. This procedure specifies that the test boards were properly installed and the tape unit is configured as described in paragraphs 2-11 through 2-17. Certain operations involving the HP 13191A Control and Status Test Accessory are included in this section to provide continuity of the test procedure.

3-5. APPLICABILITY.

3-6. Table 3-1 lists the various off-line tests and adjustments that can be performed on the HP 7970 Series Digital Magnetic Tape Units when using the HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory. References are made to the sections of the tape unit operating and service manuals, where these tests and adjustment procedures are described. Other test accessory requirements, such as the HP 13191A Control and Status Test Accessory oscilloscopes, or special tapes, are also listed in the table.

3-7. CONTROLS AND INDICATORS.

3-8. Figures 3-1 and 3-2 show the controls and indicators of the write test accessory and the read test accessory. Table 3-2 describes the functions of the controls and indicators shown in figure 3-1. Controls and indicators shown in figure 3-2 are described in table 3-3. Table 3-4 lists test PCA initial switch settings for the basic tests performed by the write test and the read test accessories. Paragraphs 3-9 through 3-19 provide a detailed description of the write test procedures. Paragraphs 3-20 through 3-31 describe the read test procedures.

3-9. WRITE TEST ACCESSORY OPERATION.

3-10. The HP 13192A Write Test Accessory provides the means to simulate write-operation signals and check the write electronic circuits of the tape unit. It is an operational requirement that the HP 13191A Control and Status Test Accessory be installed when performing these write tests. The write test accessory then allows checking of the following performance parameters such as (see table 3-1):

(1) Write-time Assymetry

(2) Write head static skew

(3) Write reset

(4) Erase/write phasing

(5) Write crosstalk

Refer to paragraphs 2-12 and 2-13 for initial test set-up.

3-11. The HP 13192A Write Test Accessory operates in either of two modes: continuous or block (as selected by the XTALK/BLOCK switch). The procedure for writing continuous data patterns is as follows:

a. Set the XTALK/BLOCK switch to the XTALK position.

b. Check and adjust the Write Clock (WC) rate as described in paragraph 2-13, step e.

c. Configure the control and status test PCA for continuous operation by:

(1) Setting the PROG/MAN switch to the MAN position.

(2) Setting the WSW switch up to the WSW position.

(3) Setting the CF switch up to the CF position.

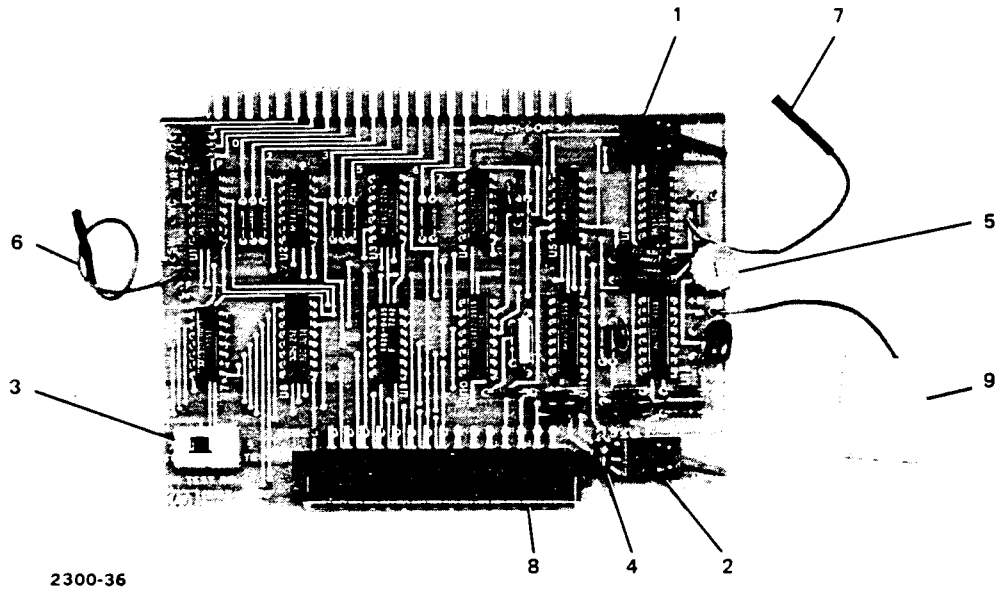
3-12. The procedure for writing a block-type pattern is as follows (the block length, i.e. the number of characters per block is variable and is determined by an adjustment on the control and status test PCA.):

a. Set the XTALK/BLOCK switch to the BLOCK position.

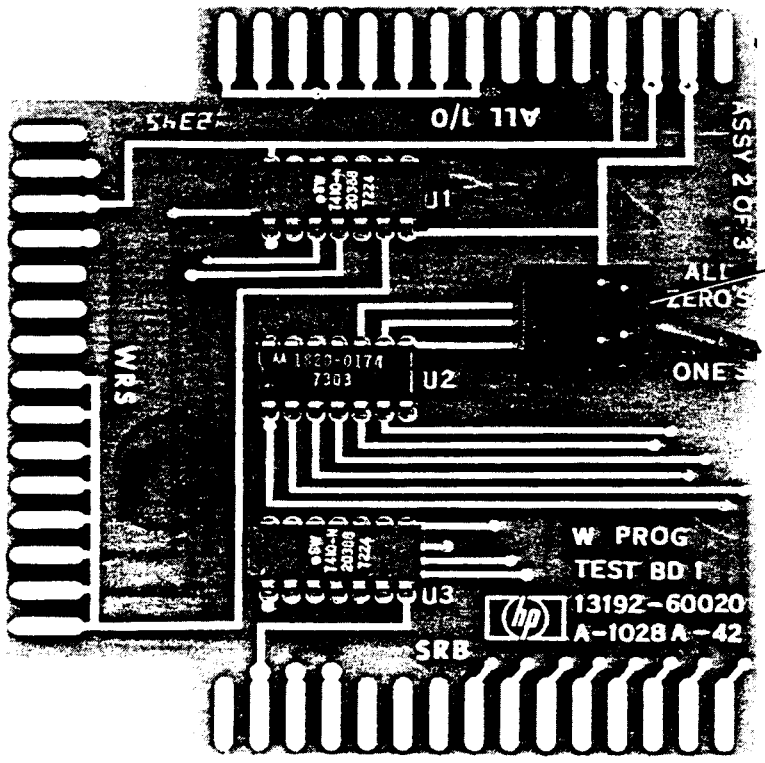
b. Check and adjust the Write Clock (WC) as described in paragraph 2-13, step e.

Table 3-1. Test PCA Applications

TEST OR ADJUSTMENT PROCEDURE	REFERENCE	13192A or 13193A TEST PCA APPLICATION	OTHER TEST ACCESSORIES USED
Write Data Performance Test	7970B/C Operating and Service Manual, Part 1, Section III, Para. 3-49	HP 13192A (with any program test board HP 13193A	HP 13191A and Scratch tape (write enable ring installed)
Read Preamplifier Gain Test	7970B/C Operating and Service Manual, Part 3, Section II, Para. 2-8	HP 13192A-60010 PCA HP 13192A-60020 PCA (ALL I/O Plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Read Character Gate Strobe and Read Clock Test	7970B/C Operating and Service Manual, Part 3, Section II, Para. 2-16	HP 13192A-60010 PCA HP 13192A-60010 (All I/O, and SRB plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Pre-Amplifier Gain Adjustment	HP 7970B/C Operating and Service Manual, Part 3, Section II, Para. 2-21	HP 13192A-60010 PCA HP 13192A-60020 PCA (ALL I/O plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Write Time Assymetry Test	HP 7970B/C Operating and Service Manual, Part 4, Para. 2-11	HP 13192A-60010 PCA HP 13192A-60020 PCA (ALL I/O plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Write/Read Skew Test	HP 7970B/C Operating and Service Manual, Part 4, Section II, Para. 2-13	HP 13192A-60010 PCA HP 13192A-60020 PCA (ALL I/O plug) HP 13193A	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Write/Read Phasing and Write Reset Test	HP 7970B/C Operating and Service Manual, Part 4, Section II, Para. 2-15	HP 13192A-60010 PCA HP 13192A-60020 PCA (WRS plug) HP 13193A	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Erase/Write Phasing Test	HP 7970B/C, Operating and Service Manual, Part 4, Section II, Para. 2-17	HP 13192A-60010 PCA HP 13192A-60020 PCA (ALL I/O plug) HP 13193A	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Write Cross-Talk Test	HP 7970B/C, Operating and Service Manual, Part 4, Section II, Para. 2-19	HP 13192-60010 PCA HP 13192-60030 PCA (DDP Plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)
Internal Write Clock Delay and Pulse Width Test	HP 7970B/C Operating and Service Manual, Part 4, Section II, Para. 2-21	HP 13192-60010 PCA	Oscilloscope
Tape Interchangeability Test	HP 7970B/C Operating and Service Manual, Part 4, Section II, Para. 2-25	HP 13193A	HP 13191A, Oscilloscope, and Tape with random length blocks
Write Skew Delay Adjustment	HP 7970B/C Operating and Service Manual, Part 4, Section II, Para. 2-30	HP 13192-60010 PCA HP 13192-60020 PCA (ALL I/O plug)	HP 13191A, Oscilloscope, and Scratch tape (write enable ring installed)



MAIN WRITE TEST BOARD (A1)



WRITE PROGRAM 1 TEST PCA (A2)

Figure 3-1. Write Test Accessory Controls and Indicator

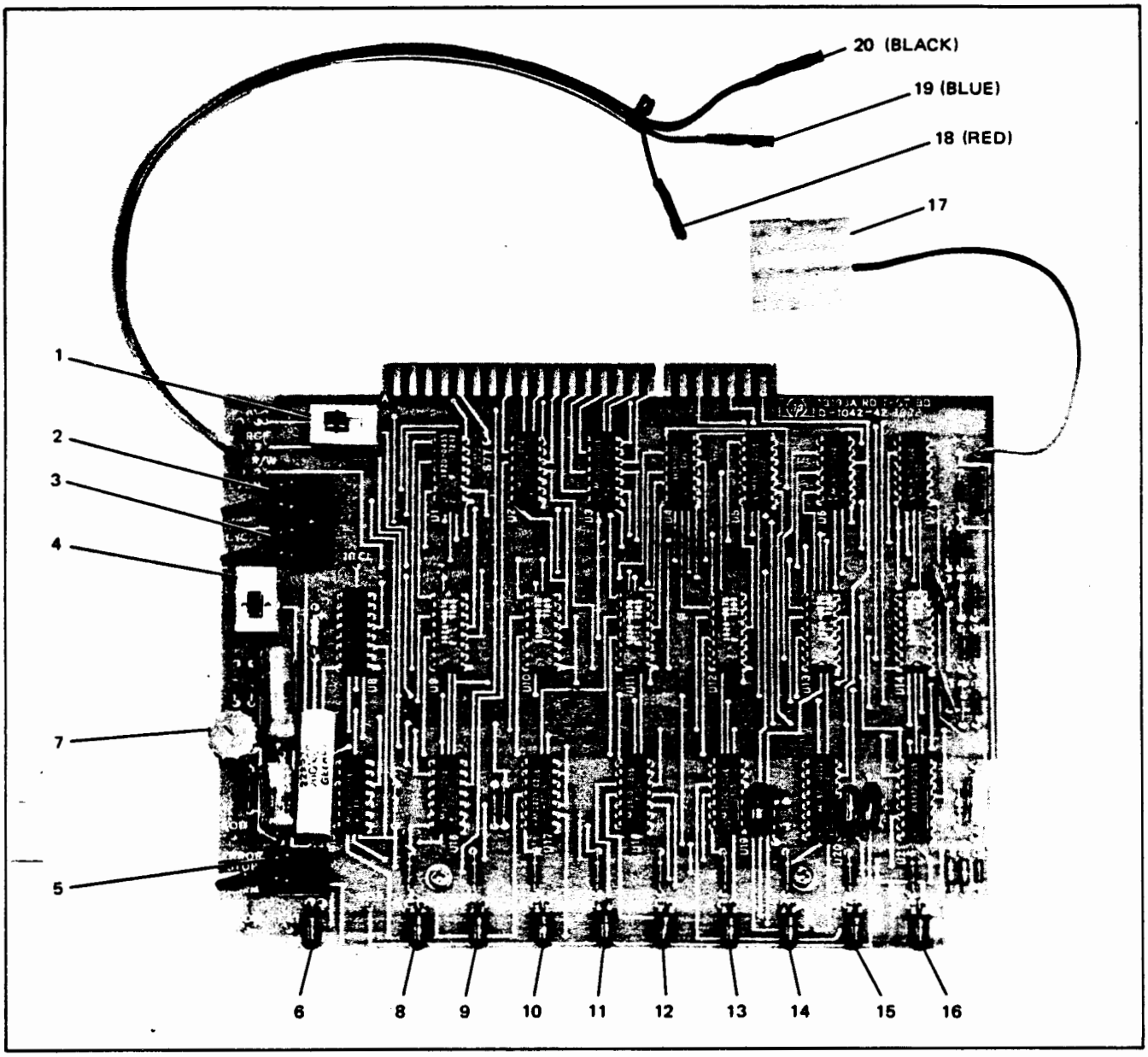


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Figure 3-2. Read Test Accessory Controls and Indicators

c. Configure the HP 13191A Control and Status PCA for programmed operation by:

(1) Setting the PROG/MAN switch to the PROG position.

(2) Setting the SET CRW switch to OFF.

(3) Initially, setting the PCF potentiometer fully counterclockwise, then adjusting block length per paragraph 3-13.

(4) Setting the WSW switch up to the WSW position.

(5) Setting the CF switch up to the CF position.

3-13. In the block mode of operation, the length of the block is determined by the PCF adjustment on the control and status test PCA. This block-length is adjusted as follows (refer to figure 3-3):

a. Connect channel A of a dual-trace oscilloscope to the WC test point (TP2) of the main write test PCA.

b. Connect channel B of the dual-trace oscilloscope to the WCF test point (TP4) of the main write test PCA.

c. Synchronize the oscilloscope to the negative slope of the WCF gate observed on the channel B trace.

Table 3-2. Write Test Accessory Controls and Indicator

FIGURE & INDEX NO.	NAME	REF DESIG	FUNCTION
FIG 3-1			
1	X-TALK/BLOCK switch	A1S1	Selects continuous or block mode of operation
2	EVEN/ODD switch	A1S2	Selects even or odd vertical parity
3	7 TR/9TR switch	A1S3	Selects nine-track or seven-track write test data
4	SW indicator	A1CR3	Indicates whether tape unit is in write mode
5	Clock Adjustment Potentiometer	A1R13	Allows setting the appropriate clock rate for 10-to-45 ips operation at densities of 200, 556, or 800 bpi
6	CF jumper	A1P1	Interfaces with the control and status test PCA for writing block-type data
7	HI/LO jumper	A1P2	Selects the appropriate clock rate range (10-to-25 ips, or 20-to-45 ips)
8	Program PCA connector	A1XA1	Connects input test formats from write program test PCA's
9	+5V connector	A1XA2	Provides operating voltages for the write test accessory PCA's
10	ALL ONE'S/ALL ZERO'S switch	A2S1	Selects a fixed logic "0" or a fixed logic "1" format for the write test program

Table 3-3. Read Test Accessory Controls and Indicators

FIGURE & INDEX NO.	NAME	REF DESIG	FUNCTION
FIG 3-2			
1	RD BL/OFF switch	S1	Selects read block or continuous test function
2	EVEN/ODD switch	S2	Selects even or odd vertical (lateral) parity
3	CYCLE/CF switch	S3	Selects cyclic forward and reverse (CYCLE) or continuous forward (CF) tape motion in read block mode.
4	HI/LO switch	S4	Selects appropriate read clock range for high-speed tape operation (20-to-45 ips) or low-speed operation (10-to-20 ips) in read block mode
5	NORM/ERROR STOP switch	S5	Selects normal, momentary stop for parity error display (NORM) or permanent stop on parity error display (ERROR STOP)
6	LAT P lamp	CR5	Displays vertical (lateral) parity error
7	10 CL ADJ	R10	Sets appropriate internal longitudinal parity evaluation interval in the read block mode
8 thru 16	P, 0 thru 7 lamps	CR6 thru CR14	Displays longitudinal parity error on tracks P, and 0 thru 7
17	+5V jumper	XA1	Provides operating voltage for the read test PCA
18	RCR jumper (red)	W1	Provides the means of issuing the reverse tape motion command to the HP 13191A
19	RCF jumper (blue)	W2	Provides the means of issuing tape forward motion command to the HP 13191A
20	R/W jumper (black)	W3	Provides the means of issuing the read-after-write command to the HP 13191A

Table 3-4. Initial Test Accessory Switch Settings

Test Operation	Write-Block (See Notes 4, 6)	Write-Continuous (See Note 4)	Read Only-Block (See Note 5)	Read Only-Continuous	Read-After-Write (See Notes 4,5,6)
HP 13191A Control and Status Test PCA	1. CF switch on (up) 2. PROG/MAN switch to PROG 3. WSW switch on (up)	1. CF switch on (up) 2. PROG/MAN switch to MAN 3. WSW switch on (up)	1. CF switch on (up) 2. WSW switch off (down)	1. CF switch on (up) 2. WSW switch off (down)	1. CF switch on (up) 2. WSW switch on (up)
HP 13192A Main Write Test PCA	1. BLOCK/X TALK switch to BLOCK	1. BLOCK/X TALK switch to XTALK	Not Used	Not Used	1. BLOCK/X TALK switch to BLOCK
HP 13193A Read Test PCA	Not Used	Not Used	1. RD BL switch to RD BL 2. CF/CYCLE switch to CF 3. NORM/ERROR STOP TO NORM switch	1. RD BL switch to OFF (right) 2. NORM/ERROR STOP switch to NORM	1. RD BL switch to RD BL 2. CYCLE/CF switch to CF 3. NORM/ERROR STOP switch to NORM

NOTE:
1. Parity switches are set as required on main write test PCA and read test PCA.
2. 7-TR/9-TR switch set as required on the main write test PCA.
3. ERROR STOP/NORM switch (on the read test PCA)can be set in the ERROR STOP position as an option for the read tests and R/W test.
4. All write tests require a clock rate adjustment as described in paragraph 2-14e.
5. Read block and R/W tests require adjustment as described in paragraph 3-26.
6. Write Block and R/W Tests require PCF adjustment as described in paragraph 3-26.

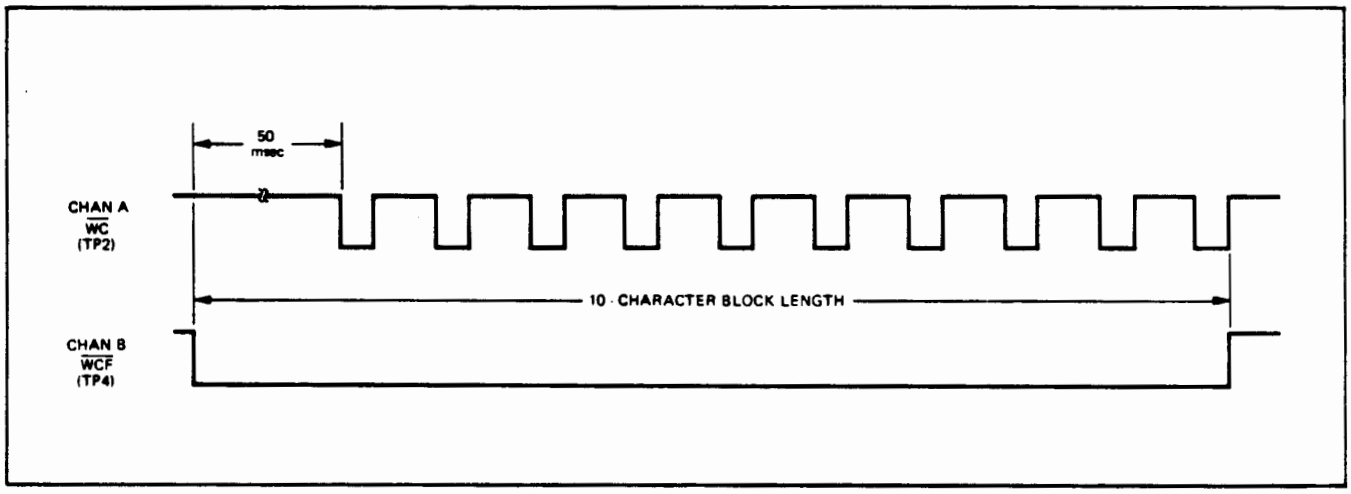


Figure 3-3. Block Length Adjustment Waveforms

d. Adjust the PCF potentiometer on the control and status test PCA so that the gate duration of the WCF signal is equal to 10 WC pulses. The block length is then adjusted to generate ten characters per block. (One character is generated with every WC pulse).

3-14. The block length may be adjusted to accommodate any number of characters within the limits dictated by the recording density and tape speed handling capacity of the tape unit. Caution is advised, however, when making this adjustment. The gate width of the WCF signal should exceed 50 milliseconds. If the gate width is less than 50 milliseconds, the tape will be erased, since the write clocks (WC) and the character output of the write test accessory are delayed 50 milliseconds after the leading edge of the WCF gate.

3-15. TEST PATTERN PROGRAMS.

3-16. Programmed test patterns may be generated using the HP 13192-60020 Write Program 1 Test PCA, or the HP 13192-60030 Write Program 2 Test PCA. Together, these two program PCA's provide as many as six different write data patterns to the user.

3-17. WRITE PROGRAM 1 TEST PCA.

3-18. The write program 1 test PCA has three connectors that can be inserted into the main write test PCA. Each connector is marked with the mnemonic title that identifies the selected data pattern. These four programmed test patterns are shown in chart form in figure 3-4, and the waveforms generated are shown in figures 5-7, 5-8, and 5-9. The mnemonic titles are explained below:

MNEMONIC	FUNCTION
ALL 1/0	Provides a pattern of all one's or all zero's, depending on the position of S1.
SRB	Provides a single-rotating-bit pattern that progresses from track to track, on a character-by-character basis to verify that each data track will generate a read clock.
WRS	Provides a data pattern of three one's, followed by seven zero's on each data channel. A write reset (WRS) pulse will be generated during every seventh character time sequence.

3-19. WRITE PROGRAM 2 TEST PCA.

3-20. The write program 2 test PCA has two connectors that may be inserted into the main write test PCA. The mnemonic titles are marked at each connector to indicate the selected pattern. The two programmed test patterns available are shown in figure 3-5). The mnemonics are explained below:

MNEMONIC	FUNCTION
DDP	Provides a dynamic data pattern to create a maximum combination of flux relationships for verifying total dynamic skew characteristics of the tape unit.
PIO	Provides a pattern of "isolated-one" in combination with "triple-one" sequences for checking isolated and crowded pulses.

3-21. READ TEST ACCESSORY OPERATION.

3-22. The HP 13193A Read Test Accessory reads recorded data, then detects and displays both vertical and longitudinal parity errors. It is a requirement that the HP 13191A Control and Status Test Accessory be used in conjunction with the read test accessory to perform all read tests. The read test accessory may be operated in either of two basic modes: continuous or block mode.

3-23. CONTINUOUS MODE.

3-24. In the continuous mode of operation, even or odd vertical (lateral) parity errors (as selected by the EVEN/ODD parity select switch, S2) are detected and displayed. The first vertical parity error, sensed by the test PCA, is displayed on the LAT P indicator (CR5), which then remains lit until manually cleared. To clear this error indication, the operator should toggle the ERROR STOP/NORM switch S5. The number of vertical parity errors detected may be counted by monitoring the LAT P test point (TP9) with an oscilloscope, during the test interval. During the continuous read test operation, tape motion is continuous, and is exclusively controlled by the control and status test accessory.

3-25. BLOCK MODE.

3-26. In the block mode of operation, the read test accessory evaluates "blocked" or interrupted tape data. Tape motion is interrupted, and controlled jointly by the read and the control and status test accessories. In this mode, the read test accessory provides an error-stop option which halts further tape motion when a parity error is detected. This option is activated by setting the ERROR STOP/NORMAL switch to the ERROR STOP position.

Note: In the read block or the read-after-write modes of operation, the first block read after tape motion begins may light the parity error lamps. This is an erroneous parity fault indication that should be ignored. This applies to the first block only.

ALL I/O

S1 in the ALL ZERO'S position

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7	8	9	10
$\overline{WD0}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD1}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD2}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD3}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD4}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD5}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD6}$	0	0	0	0	0	0	0	0	0	0
$\overline{WD7}$	0	0	0	0	0	0	0	0	0	0

ALL I/O

S1 in the ALL ONE's position

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7	8	9	10
$\overline{WD0}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD1}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD2}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD3}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD4}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD5}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD6}$	1	1	1	1	1	1	1	1	1	1
$\overline{WD7}$	1	1	1	1	1	1	1	1	1	1

WRS

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7*	8	9	10
$\overline{WD0}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD1}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD2}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD3}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD4}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD5}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD6}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD7}$	1	1	1	0	0	0	0	0	0	0

*WRS (Write Reset Pulse) is generated, which enables LRCC signal in tape drive unit.

SRB

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7	8	9	10
$\overline{WD0}$	1	0	0	0	0	0	0	0	0	0
$\overline{WD1}$	0	1	0	0	0	0	0	0	0	0
$\overline{WD2}$	0	0	1	0	0	0	0	0	0	0
$\overline{WD3}$	0	0	0	1	0	0	0	0	0	0
$\overline{WD4}$	0	0	0	0	1	0	0	0	0	0
$\overline{WD5}$	0	0	0	0	0	1	0	0	0	0
$\overline{WD6}$	0	0	0	0	0	0	1	0	0	0
$\overline{WD7}$	0	0	0	0	0	0	0	1	0	0

NOTE:
1 = 0V (approx)
0 = +5V (approx)

2300 16

Figure 3-4. Write Test Accessory Data Program 1 Output Pattern

PIO

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7	8	9	10
$\overline{WD0}$	0	1	0	0	0	0	1	1	1	0
$\overline{WD1}$	0	1	0	0	0	0	0	1	1	1
$\overline{WD2}$	1	1	1	0	0	0	1	0	0	0
$\overline{WD3}$	0	0	1	0	0	1	1	1	0	0
$\overline{WD4}$	0	1	1	1	0	0	0	1	0	0
$\overline{WD5}$	0	1	0	0	1	1	1	0	0	0
$\overline{WD6}$	0	0	1	1	1	0	0	0	1	1
$\overline{WD7}$	0	0	0	1	1	1	0	0	1	0

DDP

TRACK BIT	CHARACTER (TIME SEQUENCE) 1	2	3	4	5	6	7	8	9	10
$\overline{WD0}$	0	1	0	0	0	0	0	0	0	0
$\overline{WD1}$	1	1	0	0	0	0	0	0	0	0
$\overline{WD2}$	1	1	1	0	0	0	0	0	0	0
$\overline{WD3}$	1	1	1	1	0	0	0	0	0	0
$\overline{WD4}$	1	1	1	1	1	0	0	0	0	0
$\overline{WD5}$	1	1	1	1	1	1	0	0	0	0
$\overline{WD6}$	1	1	1	1	1	1	1	0	0	0
$\overline{WD7}$	1	1	1	1	1	1	1	1	0	0

NOTE:
1 = 0V (approx)
0 = +5V (approx)

2300 17

Figure 3-5. Write Test Accessory Data Program 2 Output Pattern

3-27. READ TEST ACCESSORY ADJUSTMENT. To provide the correct longitudinal parity, the tape unit under test generates a longitudinal redundancy check character (LRCC). This LRCC is checked by the read test accessory during the time interval which immediately follows read data time. The "check time interval" (i.e. the interval during which the LRCC and longitudinal parity is evaluated as described in paragraph 4-54 of section IV) is determined by the adjustment of the 10 CL potentiometer, R10. This adjustment is critical to the test operation and, if improperly set, erroneous parity errors are displayed. The adjustment is made while reading an 800-bpi tape, and is accomplished in the following manner:

a. Connect the oscilloscope to the 10 CL test point (TP6) on the read test PCA. Set the oscilloscope to trigger on the negative slope of the waveform shown in figure 3-6.

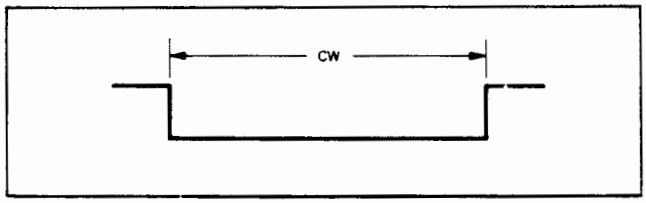


Figure 3-6. 10 CL Gate Signal (TP6)

b. On the read test PCA, set the LO/HI switch as required, and adjust the 10 CL ADJ potentiometer to obtain the 10 Clock Width (CW) that conforms to tape-speed parameters listed in table 3-5.

For any other tape unit density or speed; use the following formula to determine the correct CW:

$$CW = \frac{10}{BPI \times IPS}$$

The read test accessory provides other options such as the cycle test and the read-after-write (R/W) test functions when operating in the block mode of operation.

3-28. CYCLE TEST FUNCTION. The cycle test function is usually initiated by the read test PCA operator when an error halt condition exists (resulting from incorrect parity). Setting the CYCLE/CF switch, S3 to the CYCLE position, causes tape motion to resume. The read test PCA then issue alternate forward and reverse tape motion commands which permits the operator to view a specific data block repeatedly, to identify the incorrect character.

3-29. READ-AFTER-WRITE TEST FUNCTION. When the read-after-write function is employed, the read test accessory, as well as the write test and control and status test accessories combine synchronous operations, to evaluate the read-after-write (R/W) performance of the tape unit.

3-30. The R/W (read-after-write) test is used to detect and display vertical or horizontal parity errors that could occur when the tape unit is in the read-after-write mode of operation. The main write test PCA (HP 13192-60010) is programmed with a write program 2 test PCA (HP 13192-60030) to provide a unique data patter. This data is written on scratch tape which is equipped with a write enable ring. The following test components are required to perform a read-after-write test on the tape unit:

a. Main write test PCA, HP part no. 13192-60010

b. Write program 2 test PCA, HP part no. 13192-60030

c. Control and status test PCA, HP part no. 13191-60010

d. Read test PCA, HP part no. 13193-60010

e. Scratch tape (with write enable ring installed, HP part no. 9162-0025 or 0026

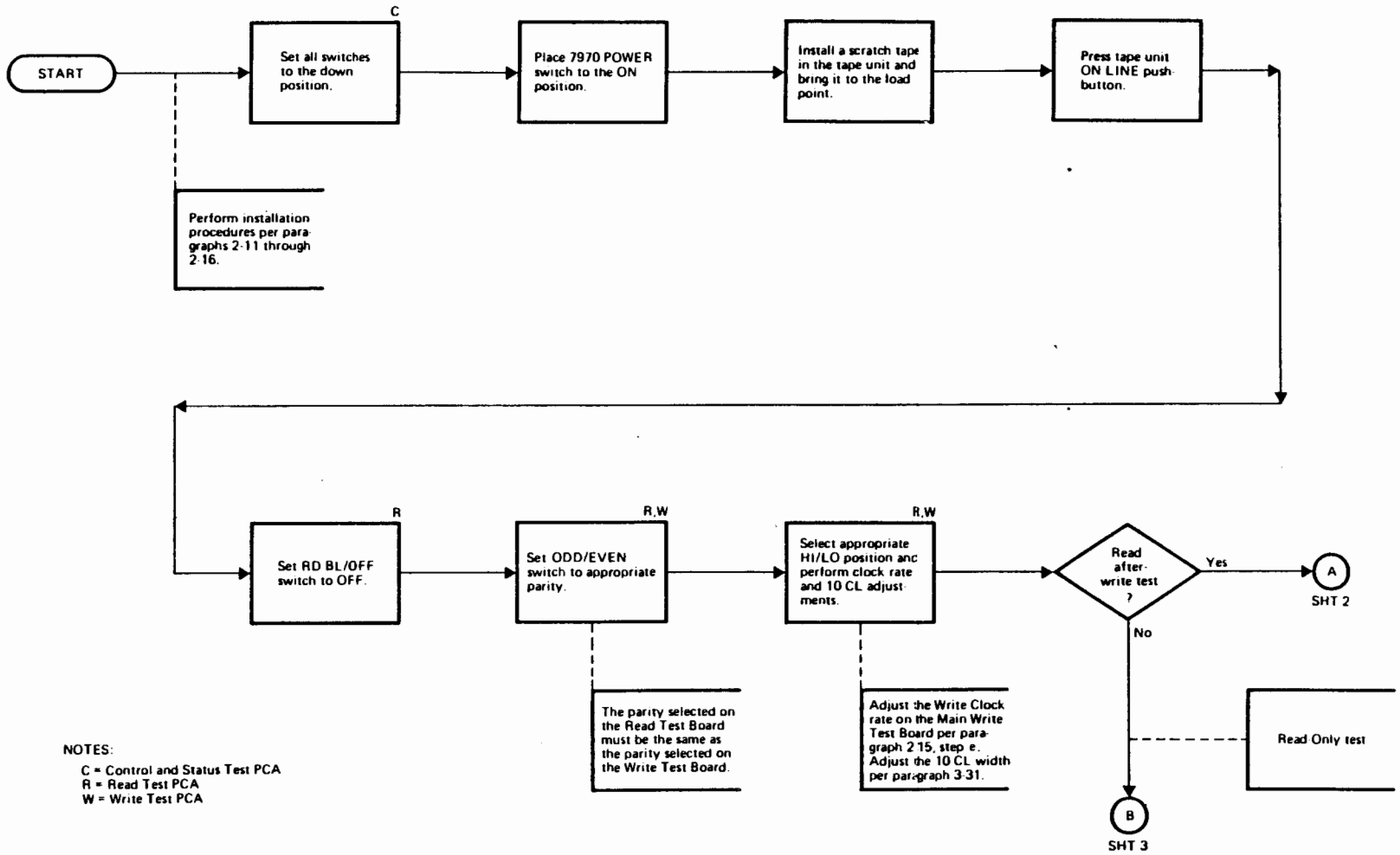
3-31. Figure 3-7 provides a flow diagram which shows the sequence of operations performed on the tape unit and the test components described in paragraph 3-30. Prior to performing this test, install the test PCA's per paragraphs 2-10 through 2-15.

3-32. On the flow diagram (figure 3-7), the letter appearing at the upper right-hand corner of each block denotes the test PCA on which the operation (described by the block) is performed. These letters are explained below:

C = control and status test PCA
W = write test PCA
R = read test PCA

Table 3-5. Read Test PCA 10 Clock Width Adjustment (800 bpi)

Tape Unit Speed; inches per second (ips)	Read Test PCA LO/HI Switch (S4) Position	10 Clock Gate Width CW (in microseconds)
12.5	LO	1000
25	HI	500
37.5	HI	333
45	HI	277



2300 20A (SHT 1)

Figure 3-7. R/W Test Operational Flowchart (Sheet 1 of 4)

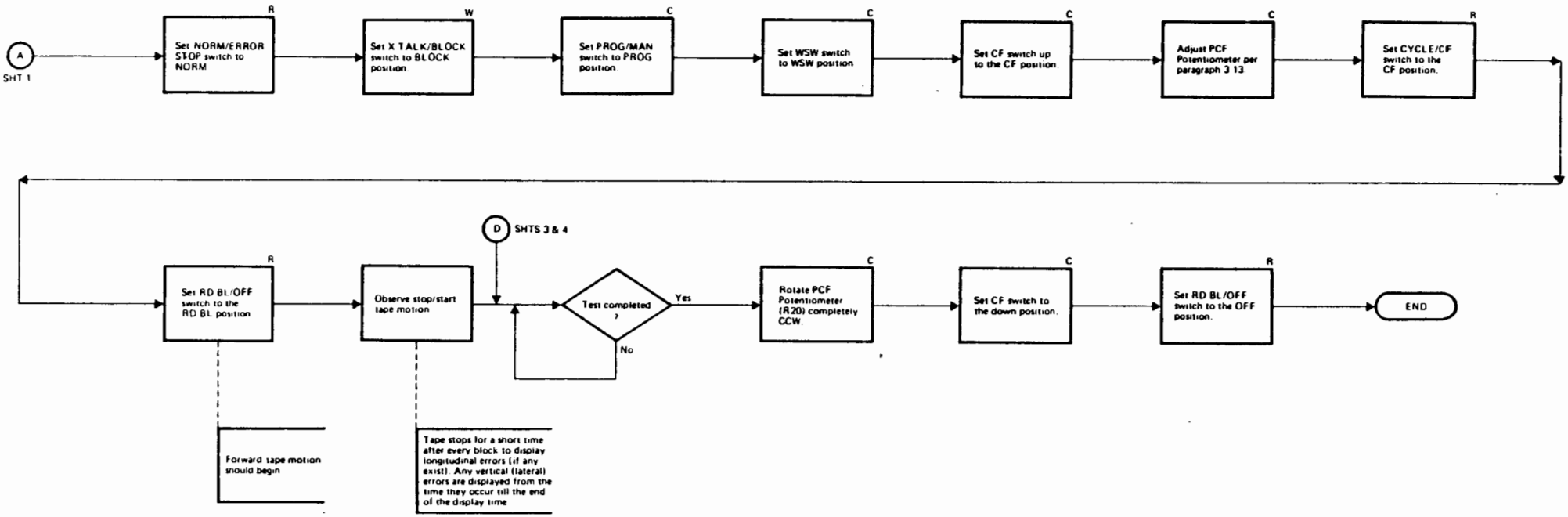


Figure 3-7. R/W Test Operational Flowchart (Sheet 2 of 4)

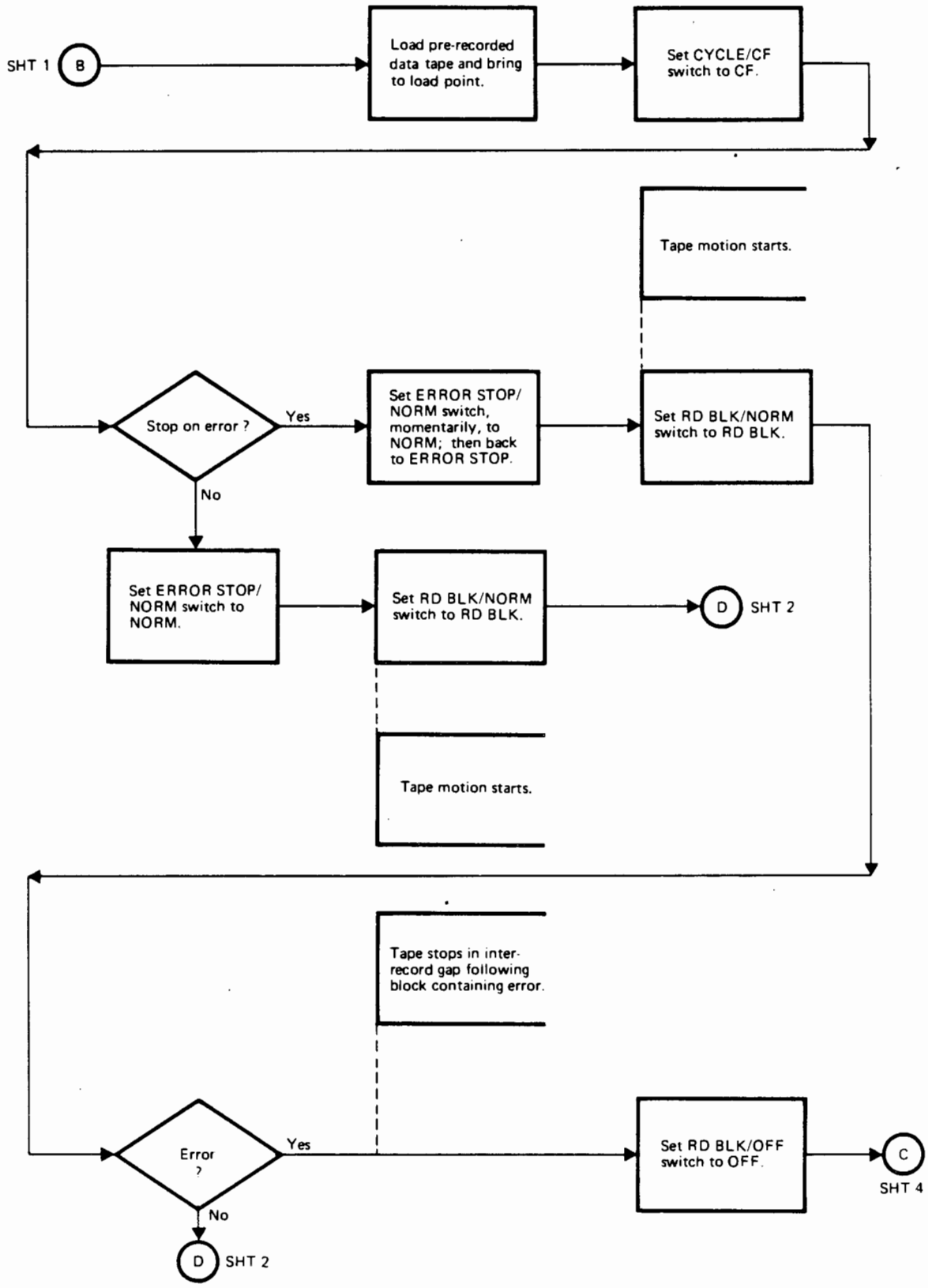


Figure 3-7. R/W Test Operational Flowchart (Sheet 3 of 4)

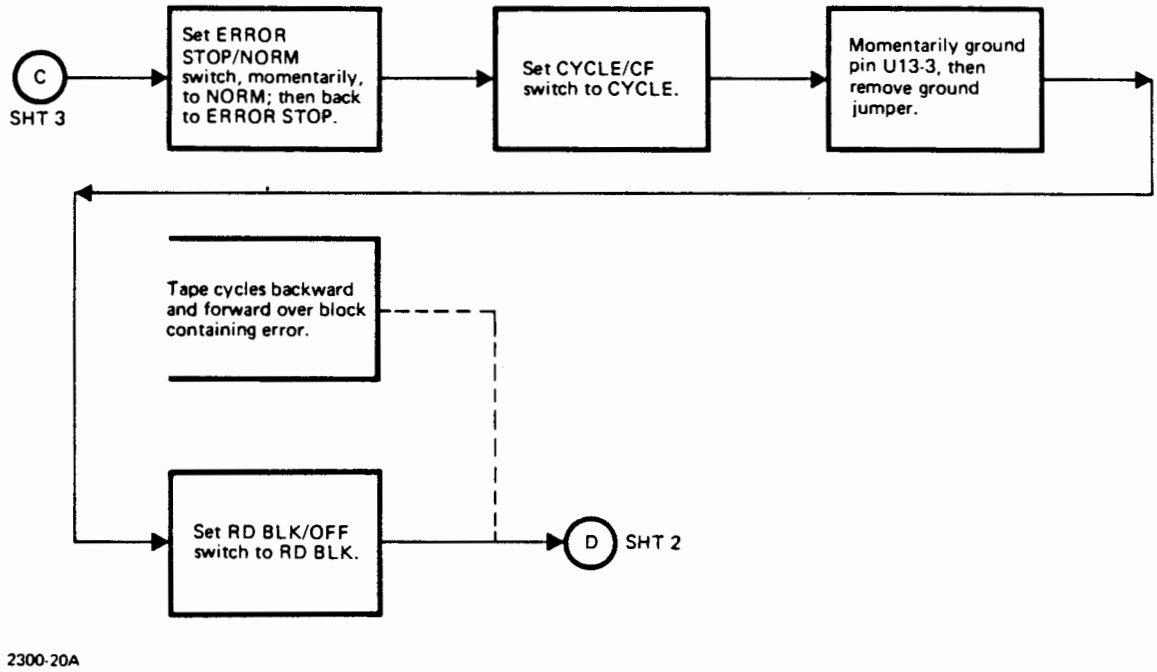


Figure 3-7. R/W Test Operational Flowchart (Sheet 4 of 4)

SECTION IV THEORY OF OPERATION

4-1. INTRODUCTION.

4-2. This section contains general and detailed descriptions of how the HP 13192A Write Test and the HP 13193A Read Test Accessories perform the test operations described in section III. When required, information concerning the HP 13191A Control and Status Test Accessory to provide continuity of the test function theory of operation. If necessary, refer to the HP 13191A Control and Status Test Accessory Operating and Service Manual for more complete circuit theory. The combined operations of the three test PCA's are discussed first in the functional description of the read-after-write (R/W) test. This description relates the test function to the operation of the tape unit-under-test, thereby providing an over-view of the test accessory operation. Next, the pertinent details of the read test accessory and the write test accessory circuit operations are separately described.

4-3. READ-AFTER-WRITE TEST FUNCTIONAL DESCRIPTION.

4-4. The read-after-write test description provides a general overview of the write test accessory and the read test accessory operation. This test, which evaluates the capability of the tape unit to write and read data blocks correctly, can be functionally broken down into four time-sequenced operations (Refer to figures 4-1 and 4-2):

(1) Error-display time

(2) Read-after-write data time

(3) Longitudinal Redundancy Check Character (LRCC) time

(4) Longitudinal Parity error display time

4-5. ERROR-DISPLAY RESET TIME.

4-6. The end of a previous longitudinal error display period initiates another read-after-write data block operation cycle by clearing the parity error display circuits on the read test PCA. The clear signal that accomplishes this also activates the command forward (CF) signal. This signal is applied to the tape unit via the control and status test PCA to initiate forward tape motion.

4-7. READ-AFTER-WRITE DATA TIME.

4-8. Approximately 50 milliseconds after forward tape motion is initiated, the control and status test PCA generates the Write Command Forward (WCF) signal, which is applied to the write test accessory. This signal is a variable-duration negative gate. The gate duration is controlled by R20, the PCF potentiometer on the control and status test PCA. As a result, the PCF potentiometer controls the read-after-write data time duration. The WCF gate signal enables the write test accessory circuits. The enabled circuits then generates data to be written, (WDP, WD0 through WD8), a write reset pulse (WRS) and the write clock (WC). These signals are applied to the tape unit write assembly (A17). When the control and status test PCA WSW switch is in the WSW position, a write enable signal input to the tape unit (control and status PCA A16) allows data to be written on tape. During the same operation, the tape unit read assembly (A18), reads the tape, and responds to the data input by generating read data (RDP, RD0 through RD7), an LRCC, and read clock pulses (RC). These signals are applied to the Read Test PCA, which checks each character of the data block for correct vertical parity. If parity errors are detected during this read-after-write data time interval, the LAT PAR indicator is lit. Data ceases to be written and read when the WCF gate terminates.

4-9. LRCC TIME.

4-10. The tape unit responds to the write test accessory WRS input pulse by generating the LRCC character approximately four write clock periods after the WCF signal ends when a seven-track tape is used. When a nine-track tape is used, the LRCC is delayed eight clock periods after WCF time. Approximately 2-1/2 read clock periods after WCF signal termination, the read test PCA senses an end-of-data condition, and goes into the LRCC-read mode of operation. This mode time is adjusted by the 10 CL potentiometer for an approximate 10 read clock period duration.

4-11. LONGITUDINAL PARITY ERROR DISPLAY TIME.

4-12. The end of LRCC time initiates the longitudinal parity error display time and stops tape motion by terminating the true CF signal. The generated 250-millisecond display period gate signal allows longitudinal parity errors (if any are detected) to be displayed. This negative gate signal is recognized as a true R/W signal by the control and status test PCA. As a result, the WCF gate generator on the control and status test PCA is inhibited and data cannot be written during the display period. When the display period gate signal terminates, both the longitudinal and vertical parity circuits are cleared to the no-error state, and another read-after-write test cycle is started.

4-13. WRITE TEST ACCESSORY.

4-14. The HP 13192A Write Test Accessory consists of a main write test PCA, and two programming PCA's which plug into the main write PCA to provide six different write

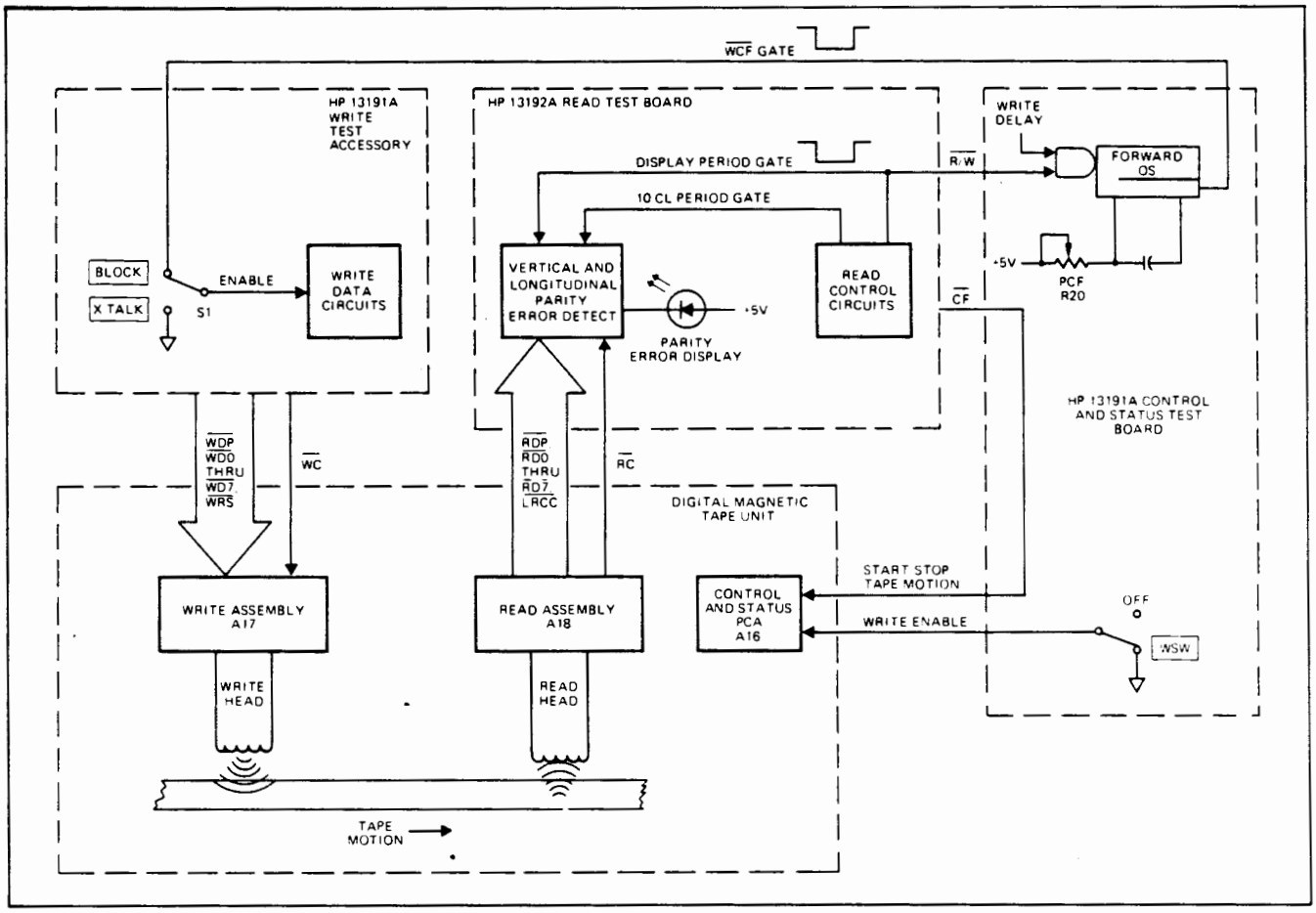


Figure 4-1. R/W Test Functional Diagram

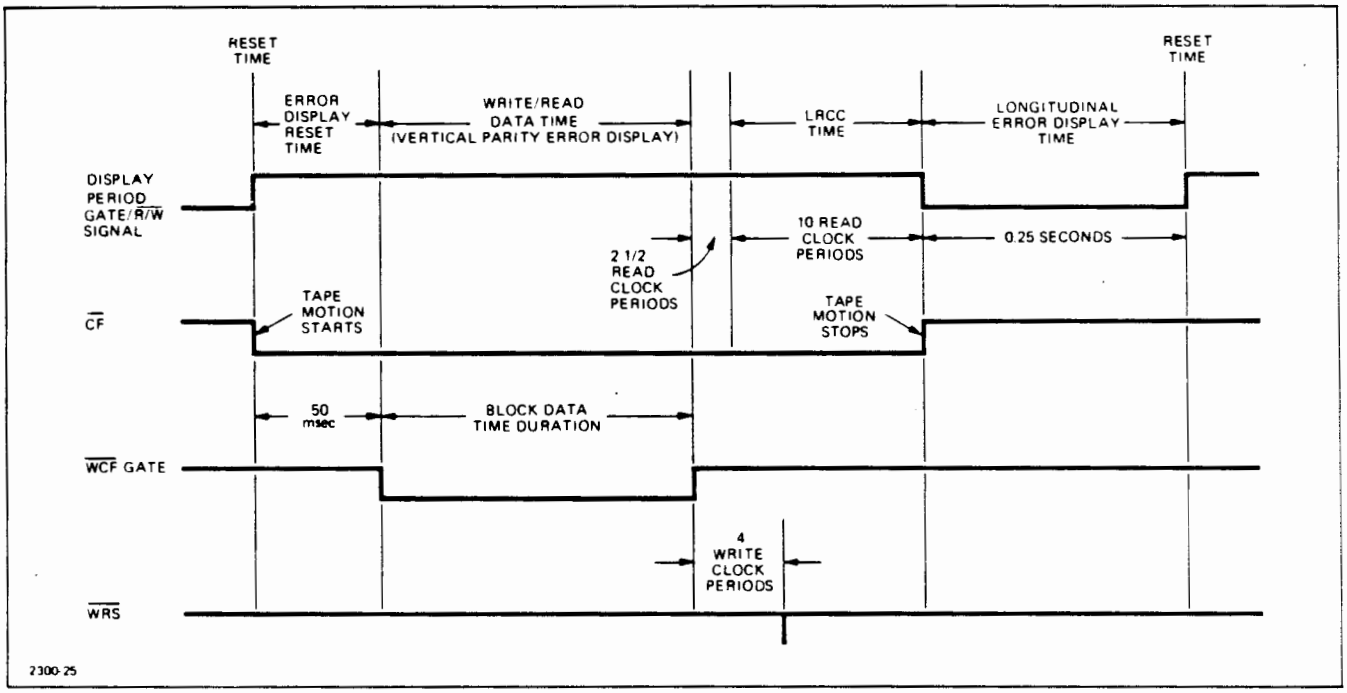


Figure 4-2. R/W Test Timing Diagram

data patterns. These patterns are rotating, ten-character sequences. Each pattern is designed to exercise a particular tape unit write capability. The write tests are generated in a continuous format when the X TALK/BLOCK switch S1 is in the X TALK position, or in a burst or interrupted format when S1 is in the BLOCK position. The duration of the burst write data pattern is determined by settings on the HP 13191A Control and Status Test Accessory. Paragraphs 4-15 through 4-19 provide a functional description of the over-all write test accessory operation. The paragraphs following the functional description provide detailed circuit analysis of the write test accessory cross-talk block operation. Lastly, the write test program PCAs are briefly discussed.

4-15. WRITE TEST ACCESSORY FUNCTIONAL DESCRIPTION

4-16. A simplified write test accessory logic diagram is shown in figure 4-3. The master write clock generates pulses that provide output signals and appropriate output signal timing. This pulse, or clock rate, is adjustable to provide a frequency range of 2 kHz to 16 kHz when LOW is selected, or a range of 16 kHz to 36 kHz when HI is selected. As a result, the write test accessory is capable of writing with tape speeds of 10 to 20 inches per seconds (ips) in LOW, and 20 to 45 ips in the HI range; at recording densities of 200, 556, or 800 bits per inch (bpi).

4-17. The 10-character generator provides a continuous or block write test pattern as determined by the X TALK /BLOCK control circuits. In the block mode of operation, a write command forward (WCF) gate, derived from the control and status test accessory, initiates generation of the write clock and data characters to be written after a 50-millisecond delay. This delay compensates for the time necessary for tape units to reach normal speeds before writing the data patterns. The type of test data pattern to be generated is determined by the selection of one of three available write program test PCA's (see paragraph 3-15).

4-18. The write clock is delayed approximately 400 nanoseconds after the character generator is pulled by the master clock. This delay ensures that the data characters (WDP, WD0 through WD7) are available at the write test accessory output when the write clock is generated.

4-19. The 7-TR/9-TR switch allows formatting of the write test accessory output to accommodate seven-track or nine-track tapes. Write-data tracks 0 and 1 (WD0 and WD1) are not used when the switch is in the 7-TR position. The parity generator samples data in all test modes and provides the appropriate parity bit for either even or odd parity (as selected by the ODD/EVEN switch).

4-20. In the block mode, the write reset (WRS) pulse generator provides a pulse output four clock pulses after the termination of the WCF signal. The WRS pulse causes the tape unit to provide an even number of one bits in each data track (WDP, WD0 through WD7), by generating a longitudinal redundancy check character (LRCC).

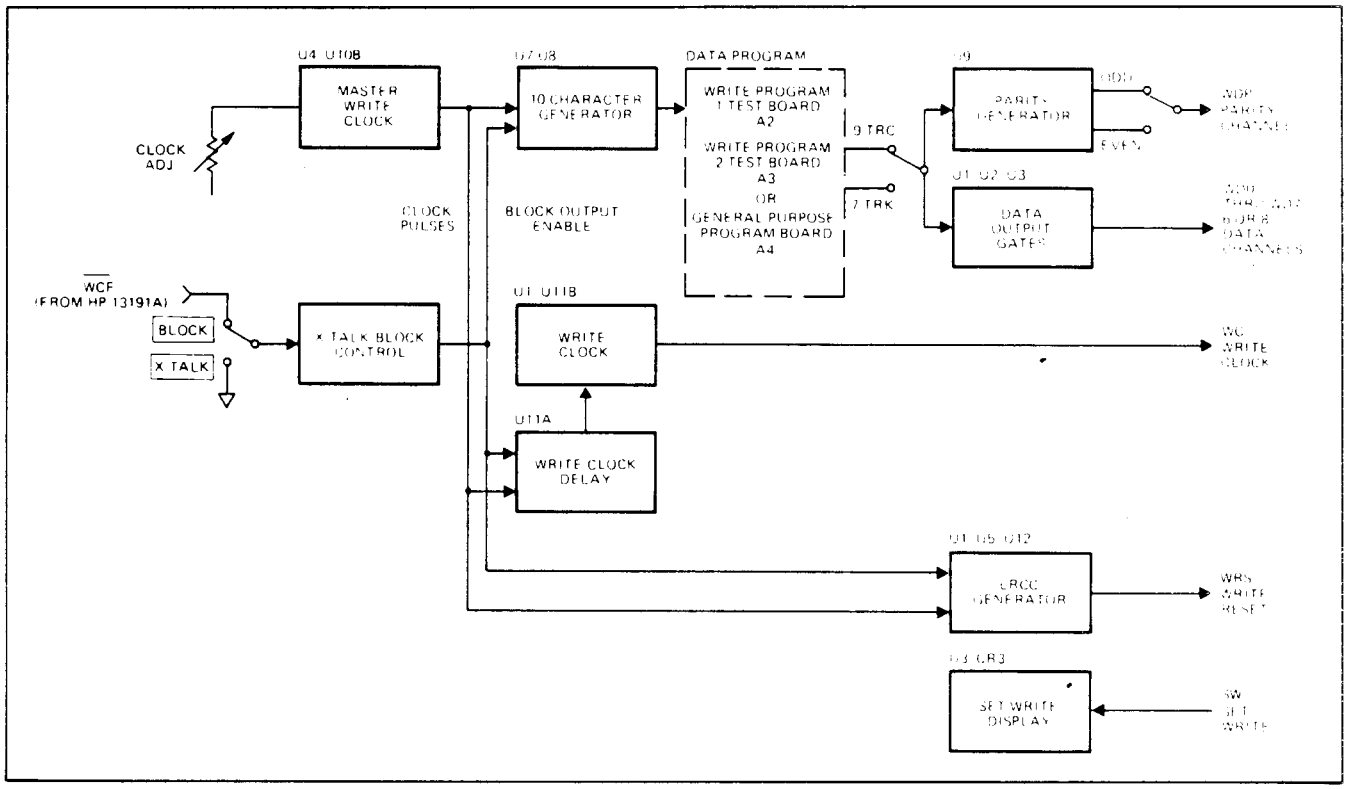


Figure 4-3. Write Test Accessory Simplified Logic Diagram

4-21. MAIN WRITE TEST ACCESSORY CIRCUIT DESCRIPTION.

4-22. The HP 13192A Write Test Accessory schematic diagrams are shown in figures 5-6 through 5-11. On the main write test PCA, the master write clock, consisting of U10B and U4, provides frequency-adjustable clock pulses that trigger decade counter U7, WD Delay one-shot U11A, and WRS Delay one-shot U12B. This clock frequency is adjusted by connecting HI/LOW jumper P2 to either J1 or J2 and adjusting potentiometer R13 for the desired clock rate. Connector XA2 provides +5V operating power which originates from the tape unit write assembly. S1 selects either a continuous data pattern in the X TALK position, or an interrupted data pattern in the BLOCK position.

4-23. CONTINUOUS X TALK MODE. When S1 is in the X TALK position, a continuous data pattern is written. Ground is applied to "nand" gate U5A, Block Delay one-shot U10A, and to the direct-clear input of the WRS generator U12A. Inverter U5A remains high at pin 3 and the clear-side Q output of one-shot U10A stays high as a result of the ground input from S1. These high inputs to "nand" gate U5B causes its output to be low at pin 6. This fixed low on the Block Control line inhibits the Reset-9 (R9) input of the decade counter U7, and disables WRS Delay one-shot U12B. As a result U12B provides a constant low to the direct-clear input of 4-clock Delay flip/flops U6A and U6B, disabling these flip/flops. "Nand" gate U5A responds to the constant-low input by providing a constant-high Block Output Enable signal. This high enables "nor" gates U1A/b, U2A/B/C/C, U3A/B and the WC Delay one-shot U11A.

4-24. The master write clock pulses trigger Decade Counter U7. U7 counts these clock pulses and provides a four-bit binary command output that continuously counts from zero to nine, then back to zero. (See figure 4-4.) These cycling, binary commands are applied to binary-to-decimal converter U8. Table 4-1 shows the command outputs of U7 as they relate to the master clock pulses, and the write character time sequences. U8 responds to the binary command inputs by generating ten, staggered-character output gates (see 10-character generator output in figure 4-4) which are applied to the selected write test program PCA via pins F through S of connector XA1.

4-25. The negative master clock pulses from U10B pin 10 triggers the WC Delay one-shot U11A at pin 4. The one-shot responds to these clock pulse inputs by generating a negative, 400-nanosecond pulse output, which is applied to WC Generator U11B. U11B is a two-microsecond one-shot which is triggered by the positive transition of the input pulse. As a result, the WC generator provides 2-microsecond pulses which are delayed 400 nanoseconds after the master clock pulses. This delay compensates for the transient time of the character generator signal and allows simultaneous generation of the write data pattern and the write clock pulses.

Table 4-1. U7 Binary Command Outputs

Master Clock Pulses		1	2	3	4	5	6	7	8	9	10	11	12
Character Time Sequence		1	2	3	4	5	6	7	8	9	10	1	2
U7	Q_A (Pin 12)	0	1	0	1	0	1	0	1	0	1	0	1
	Q_B (Pin 9)	0	0	1	1	0	0	1	1	0	0	0	0
	Q_C (Pin 9)	0	0	0	0	1	1	1	1	0	0	0	0
	Q_D (Pin 11)	0	0	0	0	0	0	0	0	1	1	0	0

NOTE: 1 = approx +5V, 2 = approx 0V } For U7 Q_A thru Q_D outputs.

4-26. The character-pattern output from the selected write program test PCA is applied back to the main write test PCA via pins 8 through 15 of XA1. These character bits are applied to parity checker/generator U9 and to "nor" gates U1A/B, U2A/b/C/D, and U3A/B. Table 4-2 shows that the Σ-even output of parity generator U9 depends on two conditions: the number of bits that comprise the input character, and the position of EVEN/ODD switch S2.

4-27. Assume, for example, a character consisting of six one-bits is generated by the test program PCA which is plugged into XA1. U9 then detects an even number of input bits (Σ -character one bits = even). If S2 were in the EVEN position, U9 pin 4 would be high, activating the odd parity generation function. As a result, the Σ-even output (U9 pin 5) responds to the six-bit input by generating no more bits (ie remaining low), thereby maintaining an even parity character. Had S2 been in the ODD position, U9 would be in the even parity generation mode, resulting in the generation of another bit (ie. the Σ-even output going high) to obtain odd parity.

4-28. "Nor" gates U1A/B, U2A/B/C/D, and U3A/B are enabled by a constant high on the Block Output Enable line. This allows the output-character pattern (WDP, WD0 through WD7), and the write clock (WC) to be generated by the main write test PCA. Each time the tape unit establishes the set write condition, that is when current flows through the write head, a low SW signal is applied to U3, pins 12 and 13. U3 inverts this input to provide high signal drive that lights the SW indicator, CR3.

4-29. BLOCK MODE. (Refer to figures 5-6 and 4-5). When the main write test PCA BLOCK/X TALK switch A1S1 is in the BLOCK position, the output pattern appears in an interrupted or "burst" form. In the block mode, the low WCF (Write Forward Command), originating in the control and status test PCA, controls the time duration of

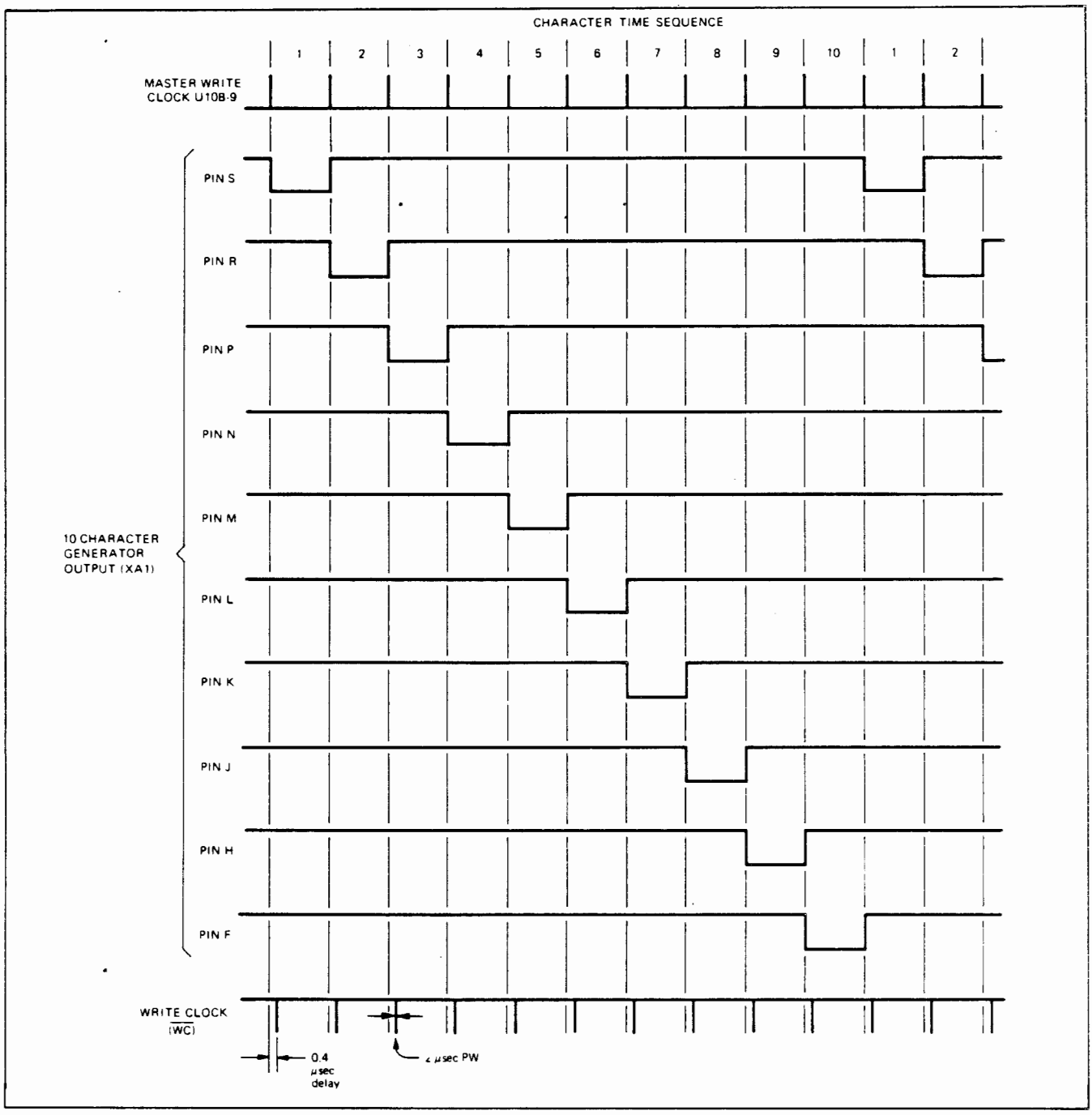


Figure 4-4. Ten-Character Generator and Write Clock (WC) Output in the X TALK (Continuous) Mode

the write test pattern output. This signal also initiates generation of the WRS (Write Reset) pulse. The WCF Gate signal triggers Block Delay one-shot U10A, direct-clears WRS Generator U12A, and is inverted to provide an enabling input to pin 4 of "nand" gate U5B.

4-30. The Block Delay one-shot responds to the negative-going transition of the WCF leading edge by generating a low gate which holds the output of U5B pin 6 high for 50 milliseconds. This high Block Control signal disables decade counter U7 (i.e. the counter is held in the reset-9 state) and inhibits WRS Delay one-shot U12B. U5B inverts this high signal to provide a low signal which inhibits "nor" gates U1A/B, U2A/B/C/D, and U3A/B, and keeps WC Delay one-shot U11A in the reset state. In other words, during the 50-millisecond interval of the Block Delay one-shot output, generation of write test patterns and write clock pulses is inhibited.

Table 4-2. Parity Bit Generation

Σ Character one Bits	S2 Position	U7 Function Activated	*Σ-even Output (U9 pin 5)
EVEN	ODD	Even Parity Generation	1
	EVEN	Odd Parity Generation	0
ODD	ODD	Even Parity Generation	0
	EVEN	Odd Parity Generation	1

* 1 = Positive Parity Bit generated

0 = No Parity Bit generated

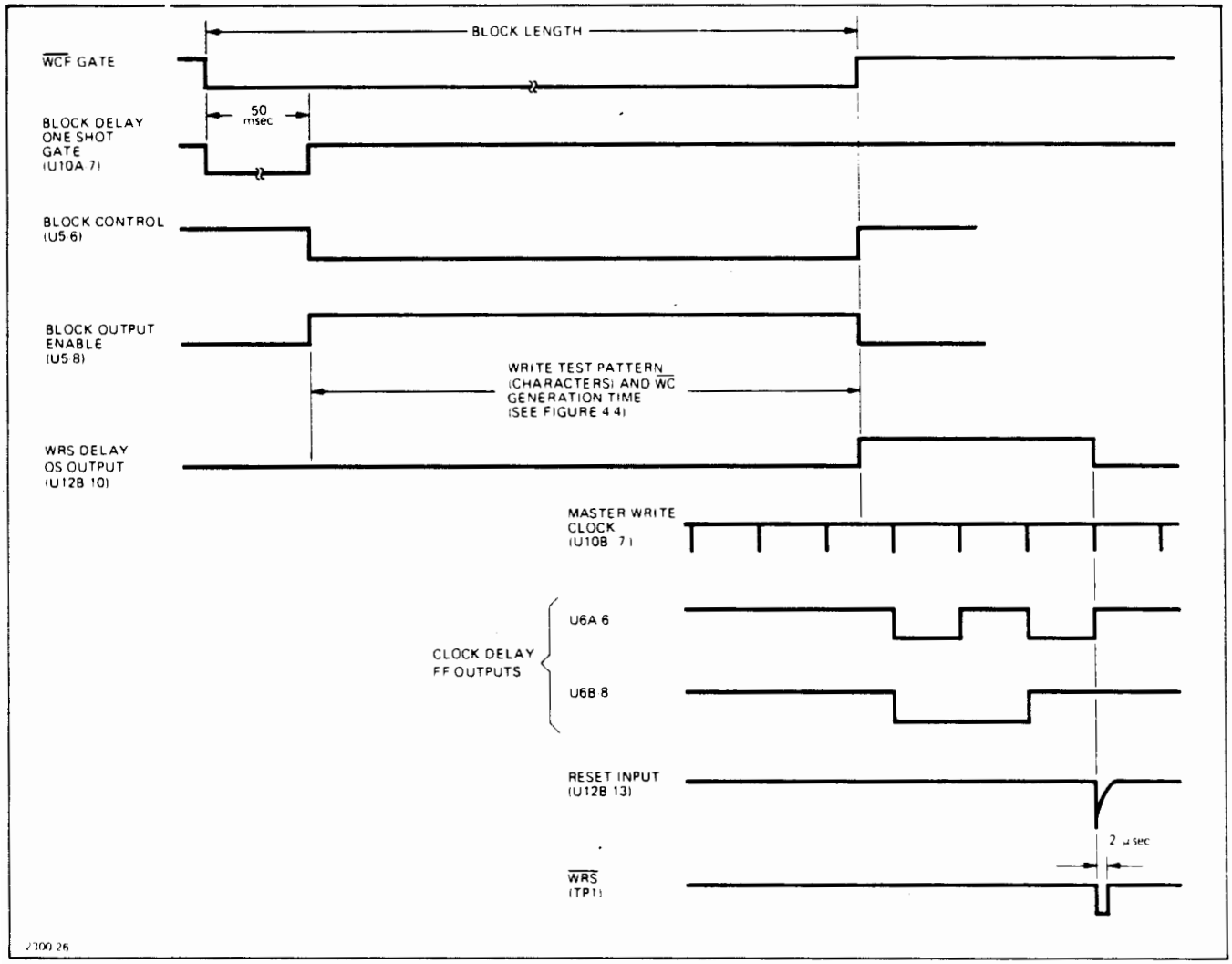


Figure 4-5. Write Test Waveforms (Block Mode)

4-31. When the Block Delay one-shot output terminates, enabled "nand" gate U5B is driven low at pin 6. This low signal enables decade counter U7 (ie U7 is released from the reset-9 state), and is inverted by U5B to provide a high Block Output Enable signal. This high signal permits the WC-generating circuits to operate and enables "nor" gates U1A/B, U2A/B/C/D, and U3A/B. As a result, the write test patterns and write clock pulses are generated for the duration of the WCF gate.

4-32. When the WCF signal terminates, the write clock and character generator are again disabled. The positive-going transition of the WCF gate trailing edge triggers WRS (Write Reset) Delay one-shot U12B. The resulting positive output signalfrom U12B pin 10 enables the Clock Delay flip-flops U6A and U6B. These flip-flops then count four master write clock pulses. When the fourth clock pulse is counted, U6A pin 6 and U6B pin 8 go high. This combination provides an input that drives "nand" gate U4C low at pin 8. The differentiating network, consisting of C5, R14, R15 and R19, transfers this low signal transition, in the form of a negative-going pulse, to the clear input (pin 13) of WRS Delay one-shot U12B. This causes the clear-side output (pin 9) of the one-shot to go high. This high signal transition triggers WRS Generator U12A (at pin 4). U12A, a one-shot, generates a negative, 2-microsecond pulse. This pulse drives U5D high for 2 microseconds. U1C inverts the pulse output from U5D to provide the negative-going, 2-microsecond WRS signal. This WRS signal is applied to the tape unit four clock periods after write test pattern generation time.

4-33. WRITE TEST PROGRAM PCAs.

4-34. The write test accessory includes two PCA's which are plugged into the main write test PCA to provide five pre-programmed test patterns. (Refer to paragraph 3-13). Table 4-3 lists the program test PCA's and the particular test patterns available at each PCA connector. The table also lists figure numbers for PCA schematics and waveform diagrams. These output waveforms are shown with the assumption that the main write test PCA is operating with the X TALK/BLOCK switch in the X TALK (continuous) position and the 7-TR/9-TR switch is in the 9-T position. The ten-character generator output (see waveforms in figure 4-4) drives the program test PCA via pins F through S of connector XA1. Program test PCA power (+5 volts and ground (common) connections are made through respective pins C and B of XA1.

4-35. READ TEST ACCESSORY.

4-36. The HP 13193A Read Test Accessory performs the parity check functions and, in certain operating modes controls tape motion and write format when testing the HP 7970 B/C Digital Magnetic Tape Unit. The vertical (lateral) parity check operation is described in paragraph 4-36 and the longitudinal parity check function is covered in paragraph 4-38. The read-after-write (R/W) test operation, as performed by the read test accessory (in conjunction with the write test PCA and the control and status test PCA), is described in detail after the parity check theory. This R/W

Table 4-3. Write Test Program PCA's

Board	Program (Connector)	Schematic and Waveform Diagram
HP 13192A-60020 Write Program 1 Test PCA's (A2)	ALL 1/0 All one's or all zero's	Figure 5-7
	SRB Single rotating bit	Figure 5-9
	WRS Write reset Pulse	Figure 5-8
HP 13192A-60030 Write Program 2 Test PCA's (A3)	DDP Dynamic data program	Figure 5-11
	PIO Programmed isolated one	Figure 5-10

test is the most complex function which provides maximum circuit description coverage. The read block and read continuous operating modes are briefly discussed next (the read test accessory operates in the read-block mode while performing the R/W test). The cycle mode of operation is discussed last. This mode provides parity checking while the tape alternately moves in a forward and reverse direction.

4-37. VERTICAL PARITY CHECKS.

4-38. Vertical or lateral parity is a character check, to ensure that each nine-bit (or selected seven-bit) character has the appropriate amount of one bits. Parity checker U1, ODD/EVEN Select Switch S2, and inverter U2F comprise the Read Test Board vertical parity check circuits (see figure 5-9). U1 is an eight bit parity checker whose parity-checking capability is extended to nine bits by using the WD0 bit (track) as a device parity selection input. ODD/EVEN switch S2 determines the type of parity test to be performed by the read test PCA. Table 4-4 shows how the parity test function is accomplished. For example, if all nine input bits (RDP, RD0 through RD7) are one's, then the sum of one bits will be odd. The Σ-parity input pins of U1 (pins 1, 2, 8 through 13) however, detect even parity (a one bit at each of the eight inputs). The high RD0 input to U1 pin 3 selects an even parity check function for the parity checker. Since eight bits are counted, the Σ-even output (U1 pin 5) goes high and the Σ-odd output (U1 pin 6) goes low. The read test PCA circuits are configured so that a high output of S2 (ODD/EVEN switch) indicates parity error, and a low output indicates a no-error condition. If S2 were in the EVEN position, a high parity error output would result. This is correct because the original number of one bit inputs is odd though only eight one bits are counted by U1). If S2 is placed in the ODD position, a low, no-error output signal is obtained. Table 4-4 provides information to determine vertical parity error signal levels for any read data input and (S2) parity selection.

4-39. LONGITUDINAL PARITY CHECKS.

4-40. Longitudinal parity is a means of checking the number of one bits on a given blocked data track (ie RDP, RD0 through RD7). If, initially, the total number of one bits per track in a block is odd, then circuits within the tape drive unit generate a unique longitudinal redundancy check character (LRCC), which provides an extra one bit per track for even parity. The read test PCA checks each data block track for the appropriate even longitudinal parity. Figure 4-6 represents two of nine identical circuits that simultaneously perform this parity check on all nine data tracks. As an example figure 4-7 shows time-sequenced waveforms that represent two conditions:

(1) Correct longitudinal parity on the WD0 track.

(2) Incorrect longitudinal parity on the WD1 track.

4-41. The test function begins with a reset pulse that clears the Parity Detect flip-flops. If these flip-flops remain cleared after monitoring a complete data block, then correct longitudinal parity for that block is confirmed. An odd number of data bits within a block leaves the flip-flop in the set condition. The resulting outputs activate the

Table 4-4. Vertical (Lateral) Parity Check Function

	Σ of one's (RDP, RD0 thru RD7 Test PCA Input)	RD0 Test PCA Input Bit	Σ of one's U1 Input	U1 Check Function	Vertical Parity Error Indication	
					S2 = ODD	S2 = EVEN
9 bit Input Data	ODD	1	EVEN	EVEN PARITY	Low	High (Error)
	EVEN	1	ODD	EVEN PARITY	High (Error)	Low
	ODD	0	ODD	ODD PARITY	Low	High (Error)
	EVEN	0	EVEN	ODD PARITY	High (Error)	Low
7 Bit Input Data (Note: RD0 and RD1 are fixed one bits and are not used as data)	ODD	1	EVEN	EVEN PARITY	Low	High (Error)
	EVEN	1	ODD	EVEN PARITY	High (Error)	Low

NOTE: 1 and Low = approx. 0V
0 and High = approx. +5V

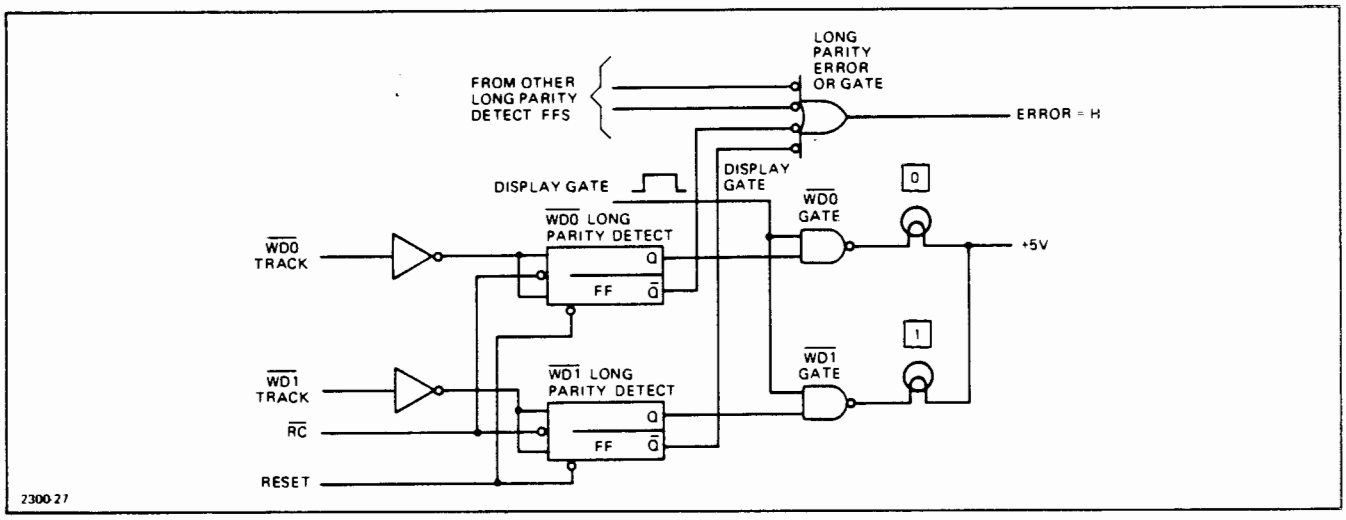


Figure 4-6. Simplified Longitudinal Parity Error Circuits

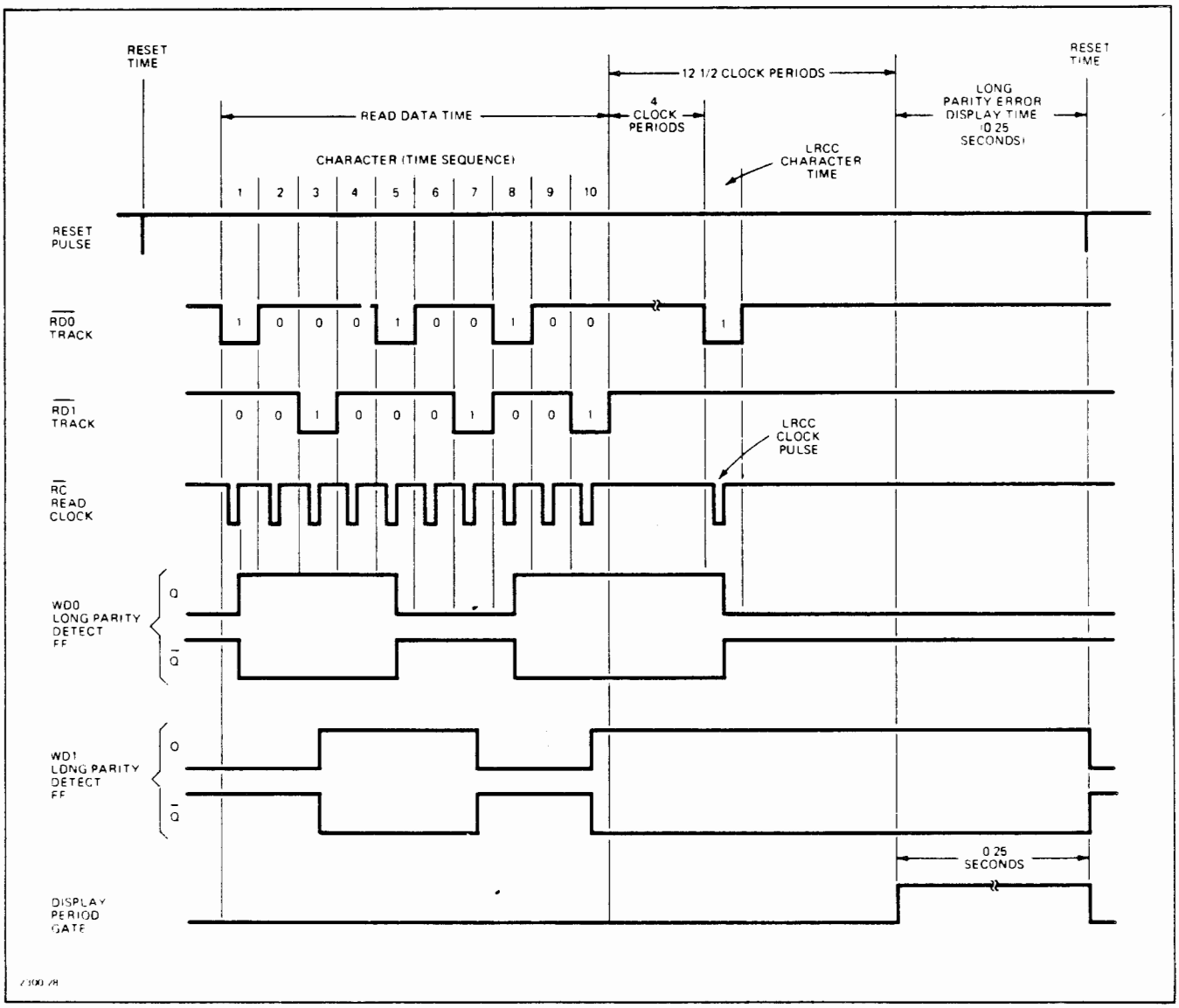


Figure 4-7. Longitudinal Parity Check Waveforms

longitudinal-error indicating circuits. For this example, a ten-character block is being read by the read test PCA. The RD0 track contains an odd number of data one bits. The generated LRCC then supplements this data track by adding another one bit. With a total of four one bits on the track, the WD0 flip-flop is toggled four times from an initially cleared state. As a result, the flip-flop is left in the cleared state when display time occurs. The low set-side output of the flip-flop inhibits the WD0 gate. When the positive Display Period signal is applied, the display gate output remains high, and the "0" (longitudinal) parity error light remains off.

4-42. The WD1 track does not receive a correcting LRCC one bit in this example and consequently, the total number of one bits in this block remains odd. The odd number of one bits toggle WD1 flip-flop three times, from an initial cleared state, thus ending in the set state. The resulting high output then enables the WD1 gate. This causes the enabled "nand" gate output to go low when the positive Display Period signal arrives. This low output signal lights the "1" (longitudinal) parity error light. At the same time, the clear-side output of the WD1 flip-flop activates the longitudinal parity error "or" gate U4 which provides a high signal to other read test board PCA error-detect circuits.

4-43. READ TEST ACCESSORY R/W OPERATION.

4-44. The read-after-write test operation is initiated, either automatically by triggering Stop/Start one-shot U21B (after a previous data block has been evaluated), or manually by cycling the ERROR STOP/NORM switch S5 from ERROR STOP to the NORM position, and back to ERROR STOP.(See figures 4-8 and 4-9.) Toggling S5 is necessary if the previous data block had a parity error and S5 was in the ERROR STOP position. This results in the Error Detect Latch FF being set by a low Parity Error signal. The low pin 6 output of the flip-flop then provides a low Error Inhibit signal, which disables "nand" gate U17B. This prevents U17B from passing a Stop/Start pulse. Toggling S5 to the NORM position causes a negative-going signal transition at pin 3 of the Error Detect Latch FF. This signal change on the Error Start/Reset line causes a negative-going trigger to be generated by the differentiating network. This trigger effectively by-passes inhibited gate U17B (inhibited by an error stop condition), to activate the Start Latch FF.

4-45. When S5 is in the NORM position, parity errors cannot halt the read-after-write operations. These operations also continue when S5 is in the ERROR STOP position and no parity errors were previously detected. The Stop/Start one-shot is triggered by the completion of a previous data block evaluation cycle. "Nand" gate U17B is now enabled by a high Error Inhibit signal. As a result, the positive-going pulse output of U21B pin 10 is inverted by U17B; providing a negative-going Start Latch FF trigger. This negative-going trigger also clears Vertical Parity Error Latch FF U74A/B at pin 13 (assuming S5 is in the NORM position and a vertical parity error was previously detected). At the same time, the negative-going pulse output of U21B pin 9 clears the longitudinal parity error circuits (S5 in NORM position) and the appropriate conditions are set to write and read the next block of data.

4-46. The negative-going trigger from U17B pin 3 sets the Start Latch FF, thereby driving output pin 10 low. This low signal sets the Drive Latch FF (U6A/B), causing its output, pin 3, to go high. "Nand" gate, U6C, is enabled by the CYCLE/CF switch S3 being in the CF position. As a result, the high input to U6C pin 10 drives its output (pin 8) low. This low CF signal is transferred to the tape unit via the control and status test PCA. When S1 is in the RD BL position the low CF signal initiates forward tape motion.

4-47. Writing data blocks is performed by the write test PCA. This data is read from the tape immediately after being written. The read-data block results in the generation of synchronous read clock pulses. The read data (RDP, RD0 through RD7) and the read clock is applied to the read test PCA when tape is in motion. The read clock pulses trigger Read Clock one-shot U12A, which responds by generating 2-microsecond read clock pulses. The first read clock pulse clears Start Latch FF U17 at pin 8, causing the Start Latch FF output to return to a high state. The first clock pulse also triggers the End-of-Data (EOD) Detect one-shot, U8A. Since U8A is a re-triggerable one-shot, its output will remain low as long as clock pulses are received within a fixed, 2-1/2 clock period time span. During this write/read data time in which the EOD Detect output is kept low by clock pulses, each data-block character is individually checked for correct parity by the vertical parity detect circuits (refer to paragraph 4-53). When incorrect parity is detected, a high error signal is generated which activates vertical parity gate U16B/U5A during a clock pulse interval. The resulting low Vert. Parity signal is applied to the tape unit and to Vertical Parity Error Latch FF U7A/B. The low input signal sets the flip-flop, causing a high output at pin 8. This output lights the LAT PAR error indicator, (light-emitting diode) CR5. The low clear-side output of the Vertical Parity Error Latch FF is applied to Error "or" gate U5C/D.

4-48. The EOD Detect one-shot interprets the absence of data clock pulses (in the 2-1/2 clock period time interval) as an end of data indication. The one-shot output then goes high 2-1/2 clock periods after the last data clock pulse was received. This low-to-high signal transition triggers 10-Clock Period Delay one-shot U8B. The 10 CL ADJ potentiometer, R10, is adjusted to obtain a negative-going pulse with a time duration equal to 10 clock periods. When this adjustment is made correctly the EOD Detect one-shot output time duration is equal to 2-1/2 clock periods (potentiometer R10 is common to the timing components of one-shots U8A and U8B). This adjustment is critical since false vertical parity and longitudinal parity error indications could result if it is improperly set. The output signals of the 10-Clock Period Delay one-shot perform two functions:

(1) The positive-going output signal (at U8B pin 10) delays the End-Of-Block (EOB) Generator U20B for

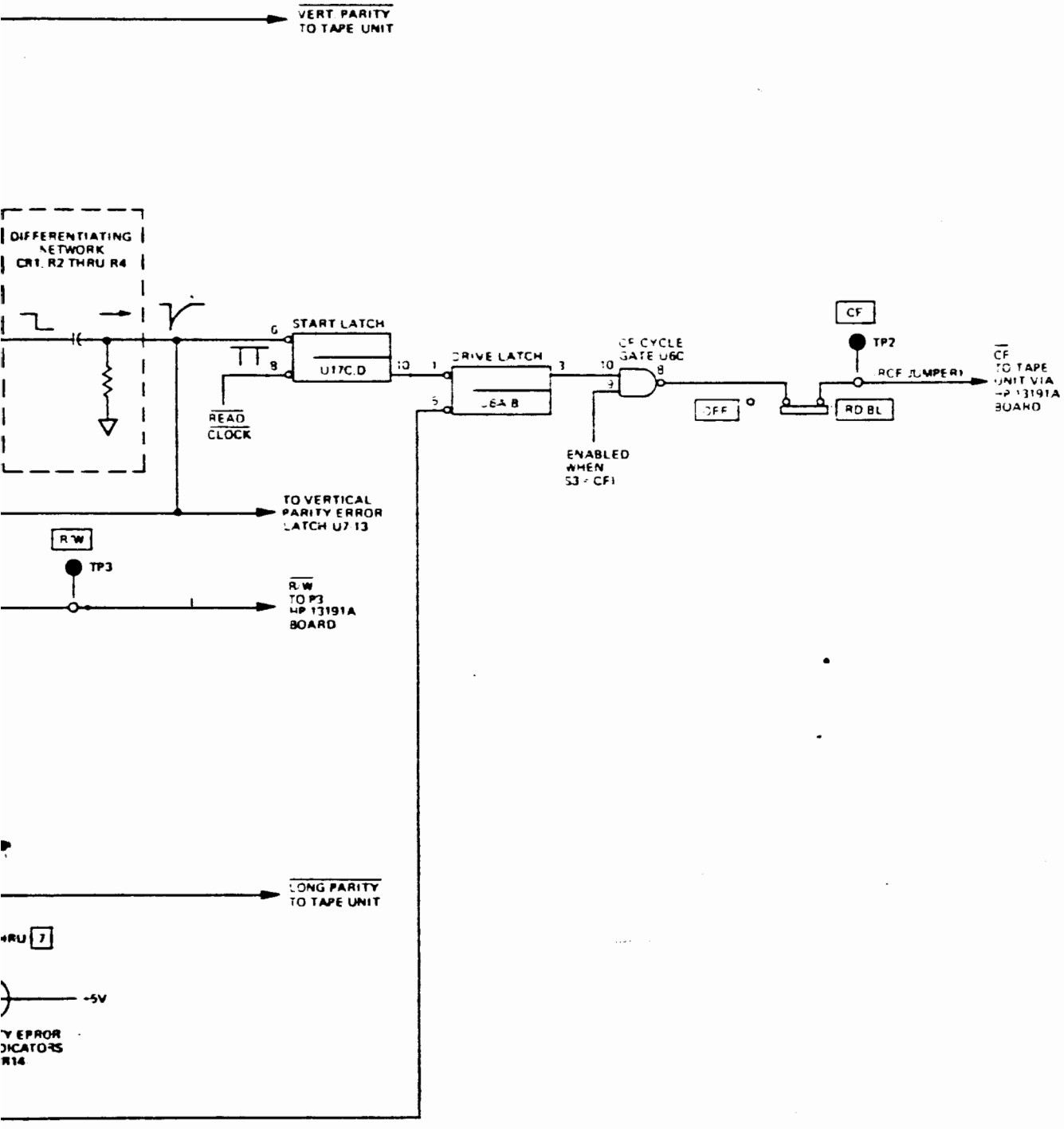
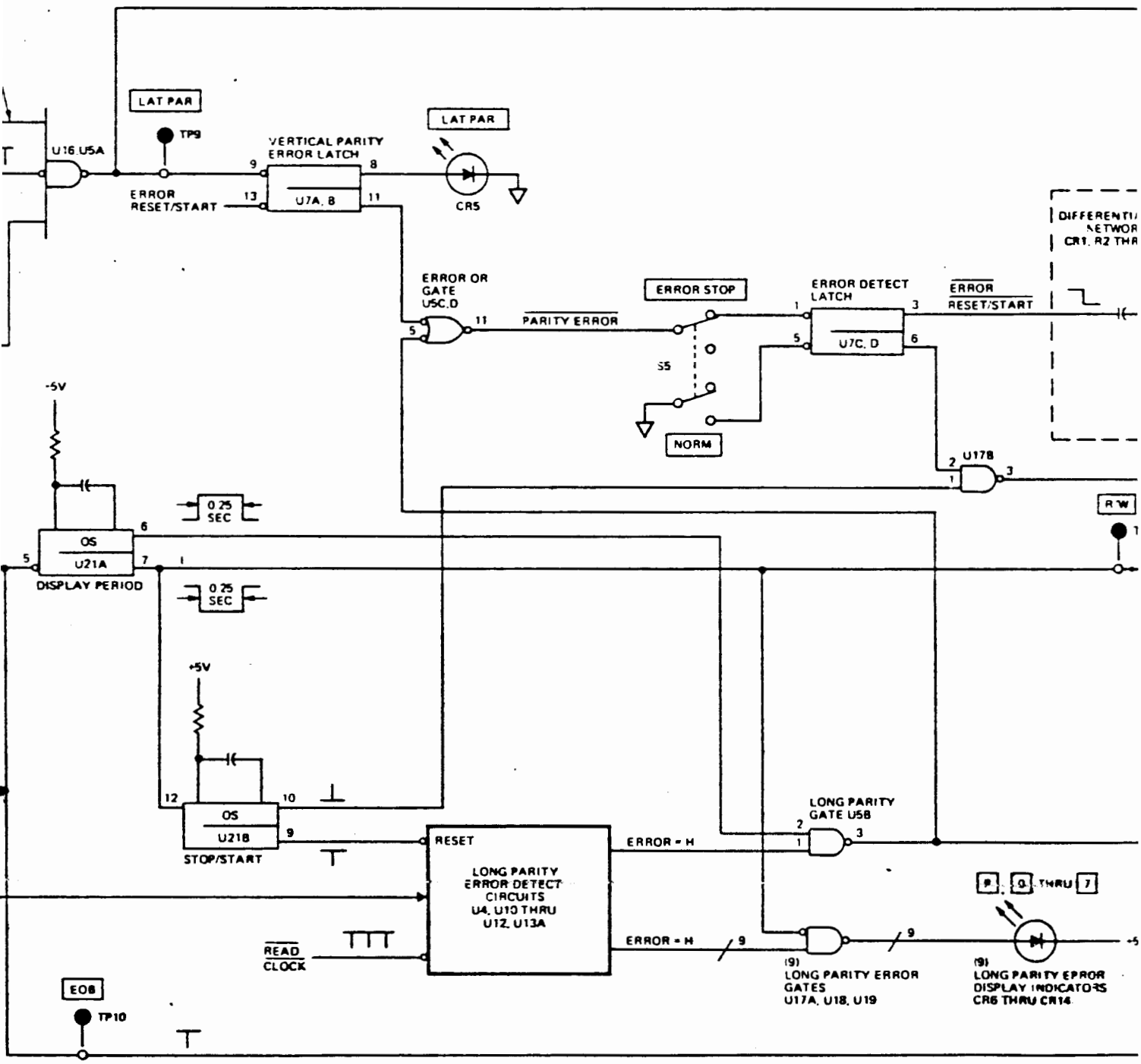
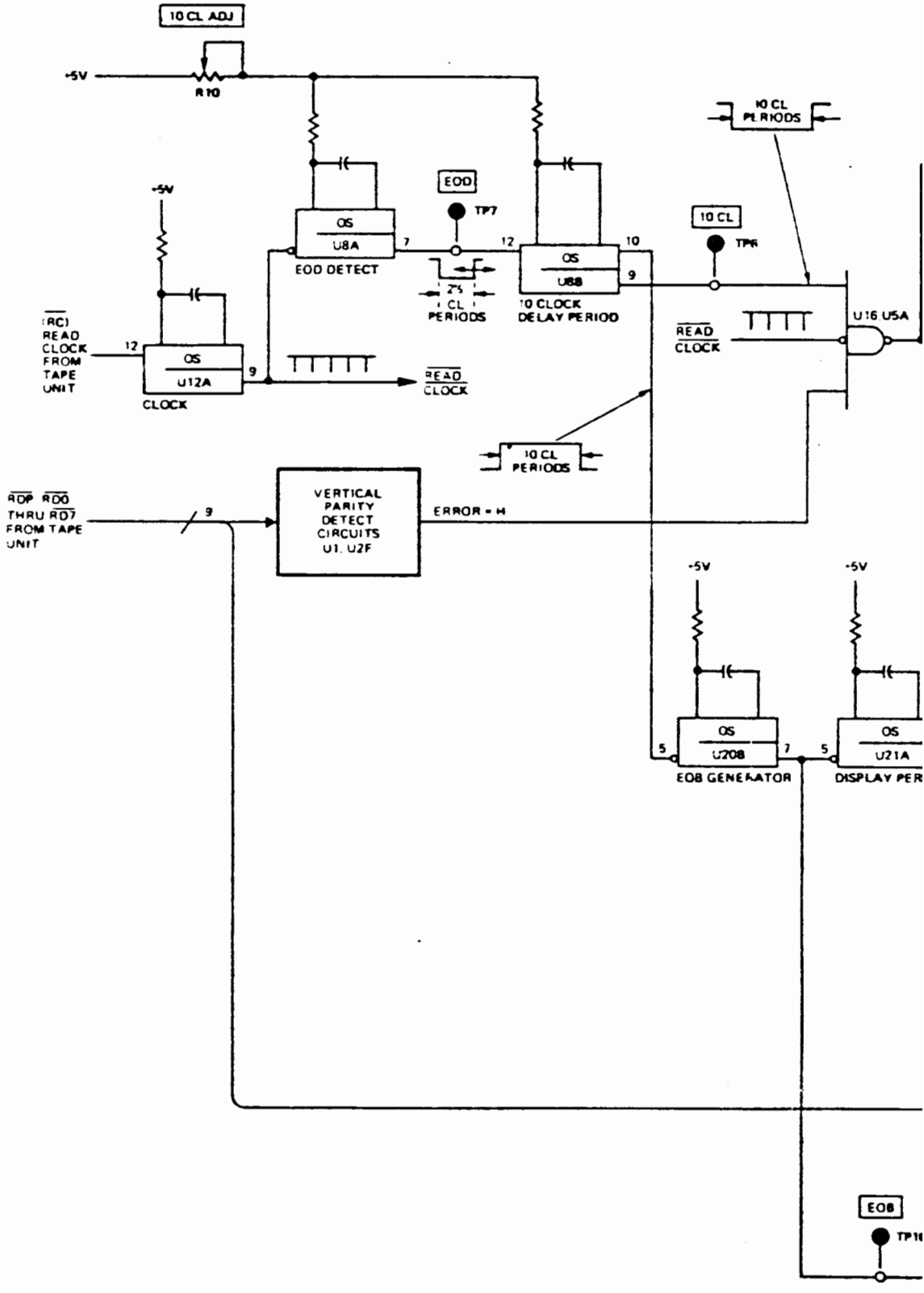


Figure 4-8. Read Test PCA Functional Diagram


LAT PAR
TP9
U16.U5A
VERTICAL PARITY ERROR LATCH
LAT PAR
ERROR RESET/START
U7A, B
CR5
ERROR OR GATE U5C,D
PARITY ERROR
ERROR STOP
ERROR DETECT LATCH
ERROR RESET/START
U7C, D
S5
NORM
U17B
+5V
0.25 SEC
OS
U21A
DISPLAY PERIOD
R/W
+5V
OS
U21B
STOP/START
RESET
LONG PARITY ERROR DETECT CIRCUITS U4, U10 THRU U12, U13A
ERROR = H
LONG PARITY GATE U58
READ CLOCK
ERROR = H
(9) LONG PARITY ERROR GATES U17A, U18, U19
(9) LONG PARITY ERROR DISPLAY INDICATORS CR6 THRU CR14
EOB
TP10


10 CL ADJ
+5V
R10
10 CL PERIODS
EOD
TP7
10 CL
TP8
OS
U8A
EOD DETECT
OS
U8B
10 CLOCK DELAY PERIOD
2½ CL PERIODS
+5V
(RC) READ CLOCK FROM TAPE UNIT
OS
U12A
CLOCK
READ CLOCK
U16 U5A
READ CLOCK
10 CL PERIODS
RDP RD0 THRU RD7 FROM TAPE UNIT
VERTICAL PARITY DETECT CIRCUITS U1, U2F
ERROR = H
-5V
-5V
OS
U20B
EOB GENERATOR
OS
U21A
DISPLAY PER
EOB
TP10

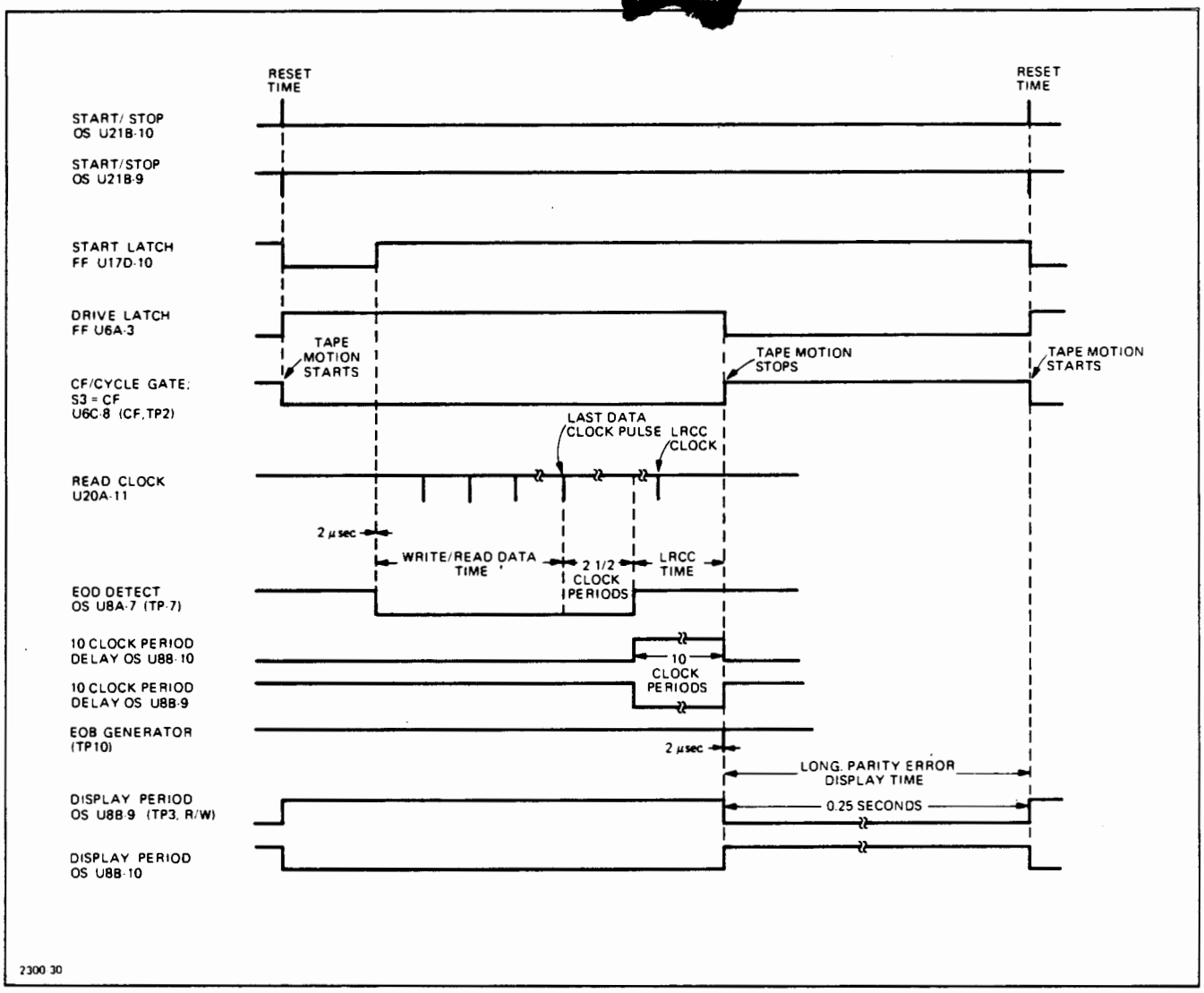


Figure 4-9. Read Test PCA R/W Waveforms

a 10 clock-period interval during which the tape unit generates the cyclic redundancy check character or CRCC (nine-track tape units only) and the longitudinal redundancy check character (LRCC).

(2) The negative-going output signal (at U8B pin 9) inhibits the vertical parity error display circuits (ie U5A) during LRCC-generation time. This is done because the LRCC does not necessarily have correct vertical parity.

4-49. If the 10-clock period signal were improperly adjusted, incorrect timing could preclude detection of the LRCC, or cause the vertical parity error display circuits to be active during LRCC time.

4-50. When the 10-clock period signal terminates, the LRCC has been detected, and the input data block is ended. The negative-going transition of the 10-clock period gate (trailing edge) from U8B pin 10 triggers EOB Generator U20B. The generator is a one-shot which responds by generating a negative-going, 2-microsecond EOB pulse. This pulse clears Drive Latch FF U6A/B (pin 5) and triggers Display Period one-shot U21A (at pin 5). Pin 3 of the cleared Drive Latch FF goes low. This low signal is inverted by U6C to provide a CF signal, which is applied to the tape unit (via the control and status test PCA). The tape unit responds to this signal by halting tape motion.

4-51. The Display Period one-shot responds to the negative-going EOB trigger by generating negative- and positive-going 250-millisecond period pulses. The negative-going signal is inverted and applied to the longitudinal parity display "nand" gates U17A, U18A/D, and U19A/D and to the control and status test PCA. All of these "nand" gates are enabled by the 250-millisecond signal. If the

longitudinal parity detect circuits sensed an error on any one of the data tracks (RDP, RD0 through RD7), an output line will be high. The corresponding display gate (now enabled by the Display Period signal) responds to this high by providing a low output that lights a longitudinal parity error indicator.

4-52. The negative-going 250-millisecond signal provides a low R/W signal to the control and status test PCA. This signal inhibits the main write test PCA so that data cannot be written during the parity error display interval.

4-53. The positive output of the Display Period one-shot enables longitudinal parity "nand" gate U5B at pin 2. As a result, the gate responds to a high error signal (originating from the longitudinal parity error detect circuits) by going low. This low Longitudinal Parity Error signal is applied to the tape unit and to error "or" gate U5C.

4-54. The error "or" gate responds to a low longitudinal or vertical parity error signal by going low at U5D pin 11. Had the NORM/ERROR STOP switch been in the ERROR STOP position, the read-after-write test operation would stop at this time. This error stop is caused by the low output of the error or gate setting the Error Detect Latch FF, U7C/D. The resulting low output of the flip-flop then disables U17B, thereby preventing a start trigger from reaching Start Latch FF U17C/D. In other words, when S5 is in the ERROR STOP position, and a parity error is detected, forward tape motion cannot resume and no further data blocks are read until S5 is manually toggled to the NORM position. Assuming S5 is left in the NORM position (inhibiting the error-stop function), the positive-going transition of the Display Period signal triggers Stop/Start one-shot U21B. The positive- and negative-going one-shot output pulses clears the parity error circuit, and triggers the Start Latch FF. Forward tape motion is resumed and the read test PCA is again configured to evaluate the next tape unit data-block input.

4-55. READ-ONLY TEST OPERATION.

4-56. In the read-only, block mode of operation, the read test PCA functions in the same manner as in the read-after-write test mode. The write test accessory is not used. Instead, a tape with pre-written block data is used. The same error-stop function used in the read-after-write mode can be selected in the read-only mode of operation. Since there is no requirement for writing control, the R/W line is not used for read-only operations.

4-57. Read-only, continuous operations treat all the read data (i.e. WDP, WD0 through WD7) as a massive block of data. In this respect the read-only, continuous mode is the same as the read only, block operation. A significant difference is that longitudinal parity error indications are ignored when reading continuous data.

4-58. READ-ONLY TEST CYCLE OPERATION. In the cycle mode of operation, the read test PCA reads the same data block while the tape is alternately driven in the forward and reverse direction. The forward reading cycle performs in the same way as the previously discussed R/W function (paragraphs 4-43 through 4-53) except data is only read, not written. In the cycle mode of operation, however, when end-of-data block is detected, instead of progressing to the next data block, tape motion reverses and the same data block is read backwards. As a result, the data sequence is reversed (i.e. the LRCC is read before the data). The read test PCA cycle control circuits perform this motion-reversing sequence. These circuits are activated when the CYCLE/CF switch S3 is set to the CYCLE position. The cycle control circuits then direct the reverse cycle, and toggle the read test PCA circuits back into the forward read cycle when the reverse read cycle is completed.

4-59. Assume, initially, that a forward read cycle has just ended (the CYCLE/CF switch is in the CYCLE position). S3 applies ground to the Error Detect Latch FF, U7C/D, forcing the non-error-stop condition. (See figures 4-10 and 5-13.) Cycle Control flip-flop U13B is enabled (i.e. the direct set input is now high). During clear time, the clear pulse (which clears parity error displays from the previous forward cycle), clocks the flip-flop. With the signal levels at both the J and K inputs high, the flip-flop responds to the clock input by toggling from the set condition to the cleared condition. As a result, the set-side output (U13B pin 15) goes low, driving U6C high at pin 8. This high, at U6C pin 8 RCF signal enables Two-Clock "nor" gate U15C at pin 9. The other input to the 2-clock "nand" gate is high because the 2-Clock Latch by the Reset Start Latch FF output was set during the previous clear time (see Start Latch FF Waveform, figure 4-9). These two high inputs drive the output of U15C low at pin 8, provinding a low 2-Clock Inhibit signal. This signal disables the EOD (End-Of-Data) Detect and the EOB (End-of-Block) one-shots. In addition, the 2-Clock Inhibit signal prevents the vertical parity error circuits from operating during LRCC time.

4-60. The high clear-side output of the cleared Cycle Control flip-flop U13B is applied to "nand" gate U6C. The other input to U6C is the high output of the Drive Latch FF (also set during clear time). As a result, U6C pin 11 goes low during clear time, providing a low RCR (Read Control Reverse) signal. This low signal is applied to the tape unit via the control and status test PCA, thereby initiating reverse tape motion.

4-61. Due to the reverse tape motion, the LRCC (longitudinal redundancy check character) is read first. Since there is a four- or eight-clock period time interval between the LRCC clock and the data clock pulses, the EOD Detect one-shot would normally interpret this pause as end-of-data and initiate the display time. This EOD function is presently inhibited, however, by the 2-Clock Inhibit signal input to the one-shot direct-clear input. The LRCC clock pulse does trigger Two-Clock Counter flip-flop U14A. U14A toggles immediately after the LRCC clock pulse is applied, from an initially cleared state to the set state. As a result, the flip-flop set-side output (U14A pin 15) goes high. The next input clock pulse (i.e. the first data clock pulse) triggers

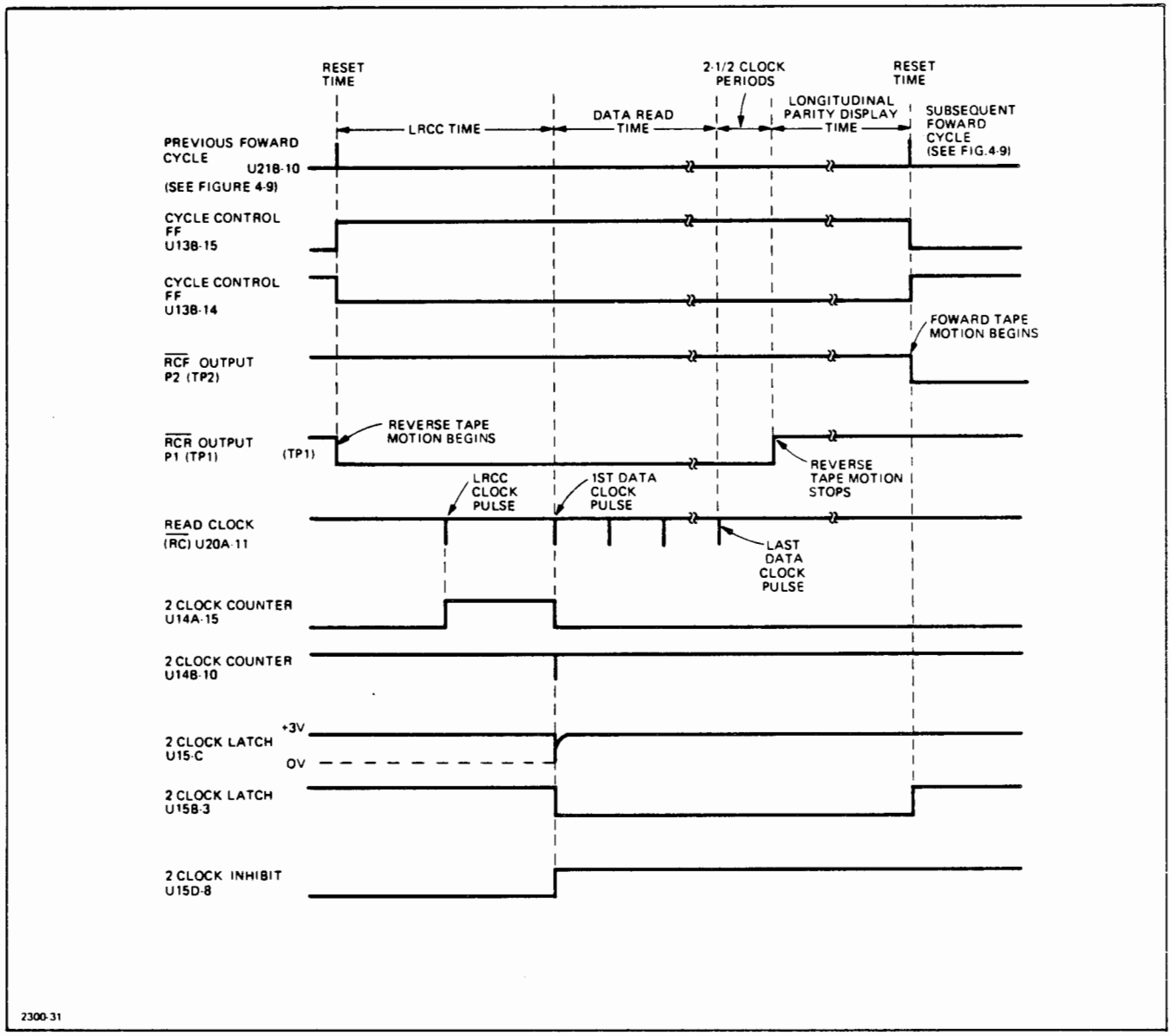


Figure 4-10. Read-Only Test, Cycle Function Waveform Diagram

2-Clock Counter flip-flop U14B. The initially cleared flip-flop responds to the trigger and the high J and K inputs by toggling to the set state. The resulting low clear-side output signal transition causes a negative-going pulse to be generated by the differentiating network C3, R5, R6, and R9. This negative-going pulse input to U15C pin 5 clears 2-Clock Latch FF U15B/C, resulting in a low output at U15A pin 3. This low signal forces the output of "nand" gate U15C pin 8 high, thereby terminating the 2-Clock Inhibit signal, and initiating a normal data read time sequence. This low 2-Clock Inhibit output signal is also returned to the 2-Clock Counter, directly clearing flip-flops U14A and U14B.

4-62. The reverse cycle now functions in the same manner as the read-after-write test operation. Twelve and one-half clock periods after the last data clock pulse is read, reverse tape motion is stopped, and the longitudinal parity error display time is initiated. The RCE signal is also terminated at this time by the low clear Drive Latch output. This low signal forces a high RCE and RCF (Read Control Forward) output. These high signals are returned to the J and K inputs of Cycle Control flip-flop U13B. As a result, when the next clear pulse is generated, the flip-flop toggles back to the set state. The high set-side output signal then enables U6D at pin 13. This results in a low RCF signal which initiates forward tape motion.

SECTION V MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains maintenance information for the HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory. Included are preventive maintenance and troubleshooting information. Parts location, waveform and schematic diagrams are provided to aid in troubleshooting.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in the HP computer documentation for the computer and tape unit. There are no separate preventive maintenance procedures for these test PCAs.

5-5. TROUBLESHOOTING.

5-6. Troubleshooting the test PCAs is accomplished by analyzing improper operation according to the theory of operation sections. Three basic test PCA failures and suggested troubleshooting techniques are described in this section. These failures are described during the read-after-write test mode of operation. This operating mode is used because it implements the HP 13191A control and status test accessory, as well as the write test and the read test accessories. References are made to supplemental information such as tables, diagrams and text located in sections 2, 3, and 4. Additional waveform diagrams and tables are provided in this section when necessary.

5-7. When using the troubleshooting diagrams (i.e., figures 5-1, 5-2, and 5-4) it is assumed that the tape unit and the control and status test PCA, are operating normally when the representative failures occur. It is emphasized that these faults are only representative, and in no way provide coverage for all possible failures that can occur in the write test or the read test accessories. Parts location and schematic diagrams with associated waveforms (figures 5-3 and 5-5 through 5-9) are used to support the troubleshooting diagrams.

5-8. TROUBLESHOOTING DIAGRAMS.

5-9. Table 5-1 lists the three representative HP 13192A/HP 13193A failures and the corresponding troubleshooting diagrams.

Table 5-1. Troubleshooting Diagrams Index

Fault	Troubleshooting Diagram
Incorrect Tape Motion	Figure 5-1
Incorrect Data Written	Figure 5-2
False Parity Error Indications	Figure 5-4

5-10. The troubleshooting information is presented in flow-diagram format. On the upper right-hand corner of each flowchart block is a letter that denotes the test PCA on which the operation is performed. These letters are defined in the following manner:

C = HP 13191A Control and Status Test Accessory.

W = HP 13192A Write Test Accessory.

R = HP 13193A Read Test Accessory.

5-11. PARTS LOCATION AND SCHEMATIC DIAGRAMS

5-12. Parts location, schematic, and waveform diagrams for the HP 13192A Write Test Accessory and HP 13193A Read Test Accessory are contained in figures 5-3 and 5-5 through 5-9.

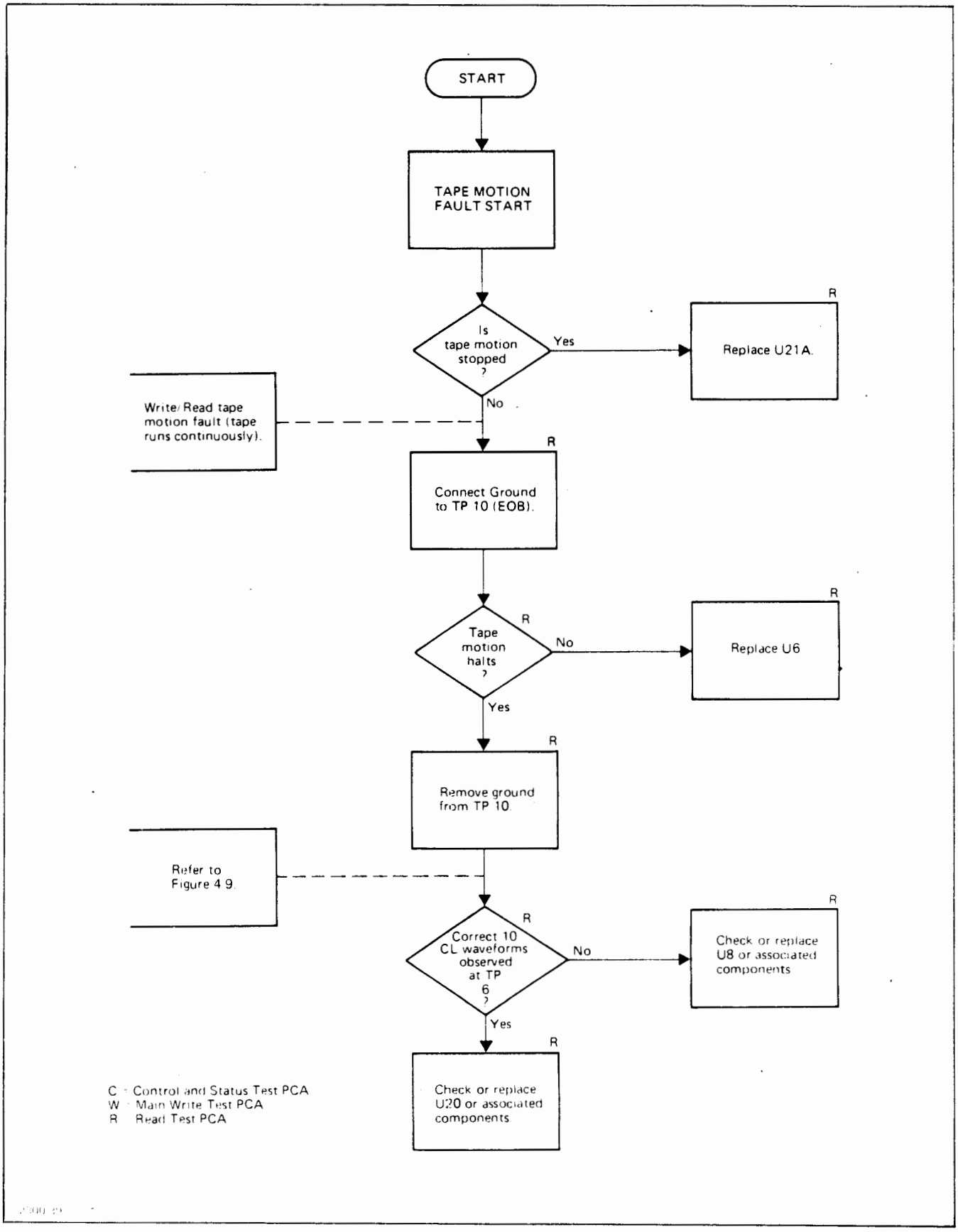


Figure 5-1. Tape Motion Fault Troubleshooting Diagram

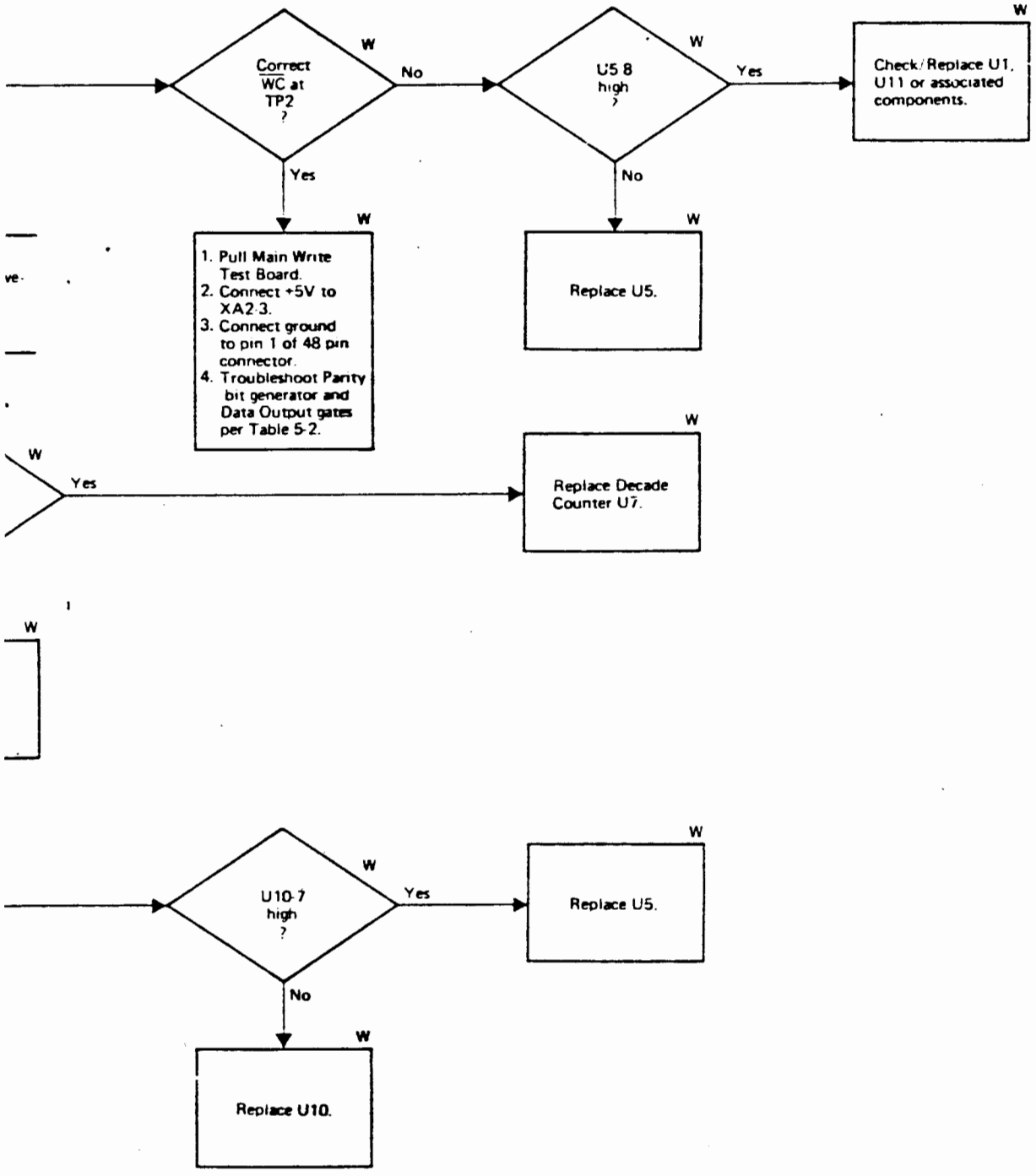
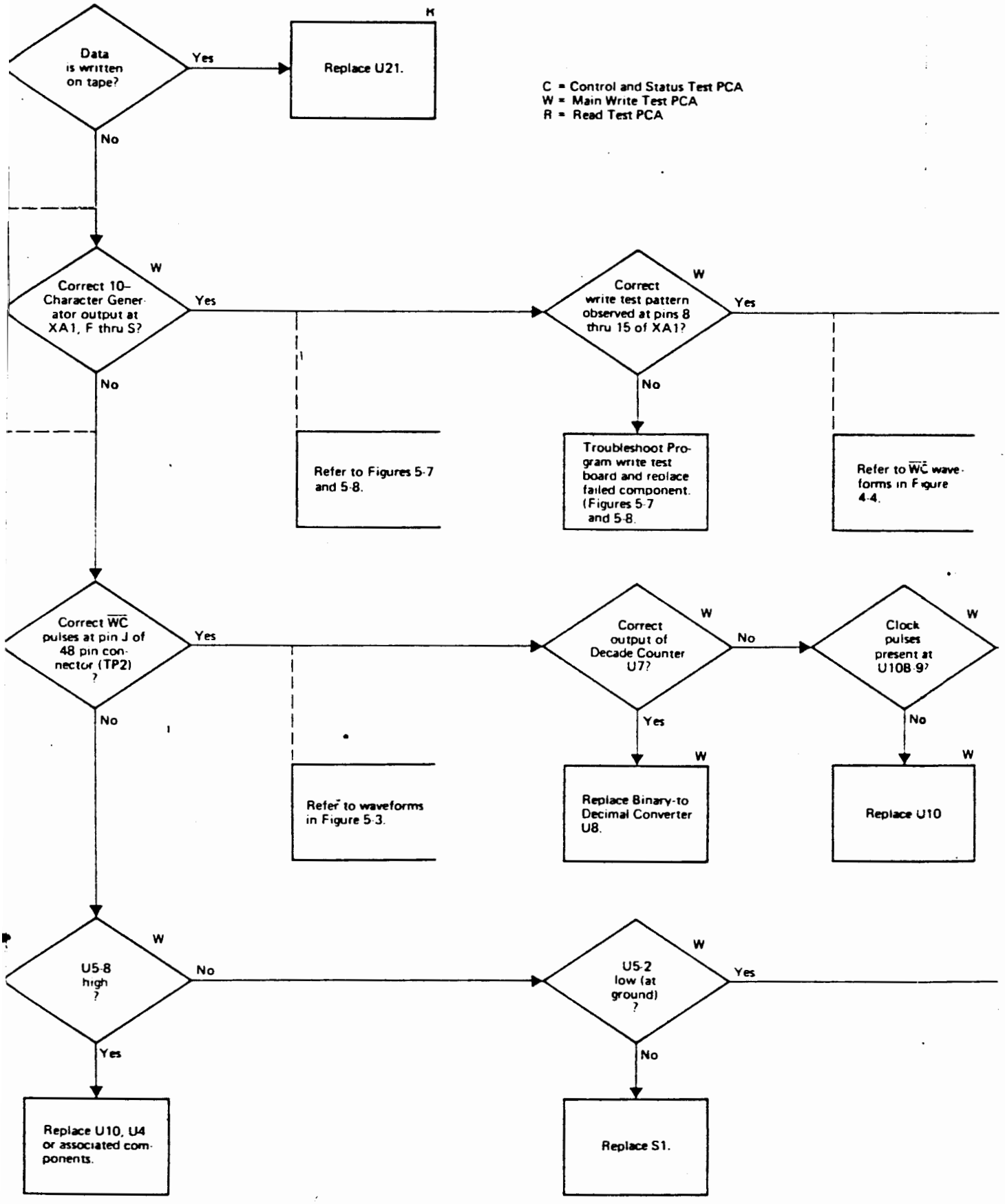
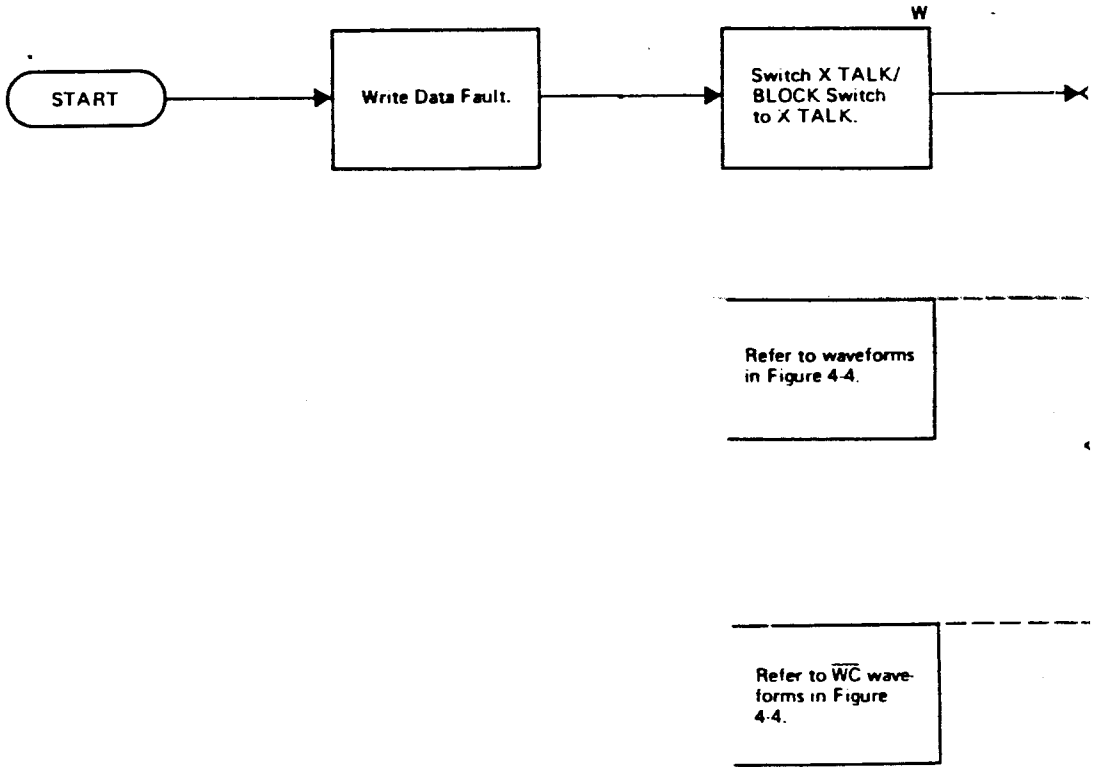


Figure 5-2. Write Data Fault Troubleshooting Diagram


R
Data is written on tape?
Yes
Replace U21.
No
C = Control and Status Test PCA
W = Main Write Test PCA
R = Read Test PCA
W
Correct 10-Character Generator output at XA1, F thru S?
Yes
No
Refer to Figures 5-7 and 5-8.
W
Correct write test pattern observed at pins 8 thru 15 of XA1?
Yes
No
Troubleshoot Program write test board and replace failed component. (Figures 5-7 and 5-8.
Refer to WC waveforms in Figure 4-4.
W
Correct WC pulses at pin J of 48 pin connector (TP2)?
Yes
No
Refer to waveforms in Figure 5-3.
W
Correct output of Decade Counter U7?
No
Yes
W
Replace Binary-to Decimal Converter U8.
W
Clock pulses present at U108-9?
No
W
Replace U10
W
U5-8 high?
No
Yes
Replace U10, U4 or associated components.
W
U5-2 low (at ground)?
Yes
No
Replace S1.


START
Write Data Fault.
W
Switch X TALK/ BLOCK Switch to X TALK.
Refer to waveforms in Figure 4-4.
Refer to $\overline{WC}$ waveforms in Figure 4-4.

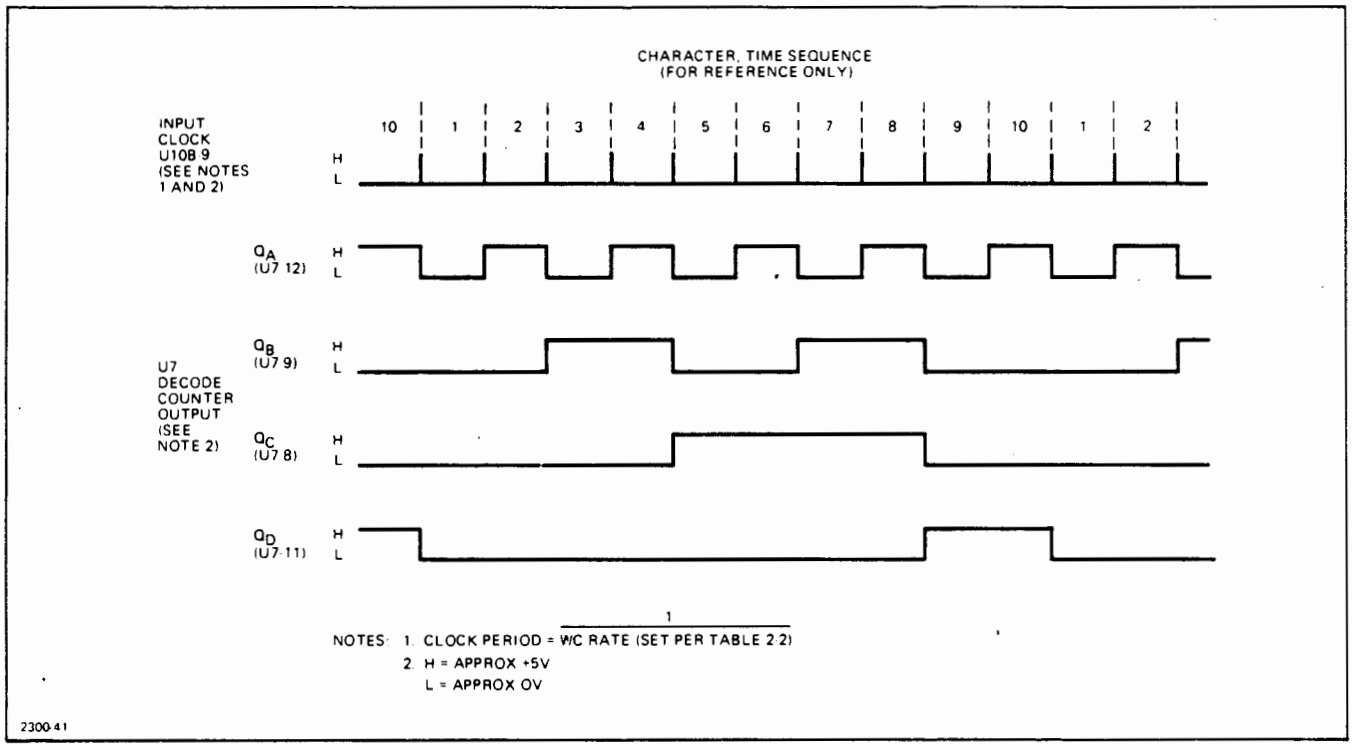


Figure 5-3. Decade Counter Waveform

Table 5-2. Parity Generator/Output Data Gate Check

FORCED TEST CONDITION (INPUT DATA)	PARITY GENERATOR OUTPUT Σ EVEN, U9-5		48 PIN OUTPUT CONNECTOR									
			$\overline{WDP}$ PIN K		$\overline{WD0}$ PIN L	$\overline{WD1}$ PIN M	$\overline{WD2}$ PIN N	$\overline{WD3}$ PIN P	$\overline{WD4}$ PIN R	$\overline{WD5}$ PIN S	$\overline{WD6}$ PIN T	$\overline{WD7}$ PIN U
	S2 = ODD	S2 = EVEN	S2 = ODD	S2 = EVEN								
XA1 8 thru 15 Open	H	L	L	H	L	L	L	L	L	L	L	L
Ground XA1 8, 10, 12, 14, 15	L	H	H	L	H	H	L	H	L	H	L	H
Ground XA1 9, 11, 13	L	H	H	L	L	L	H	L	H	L	H	L
FAILED COMPONENT	U9		U1		U2					U3		

NOTES:

1. If Parity Generator output, or output connector signal does not conform to signal levels listed, for any given forced condition, replace indicated failed component.
2. S3 = 9-TR
3. H = approx. +5V
   L = spprox. 0V

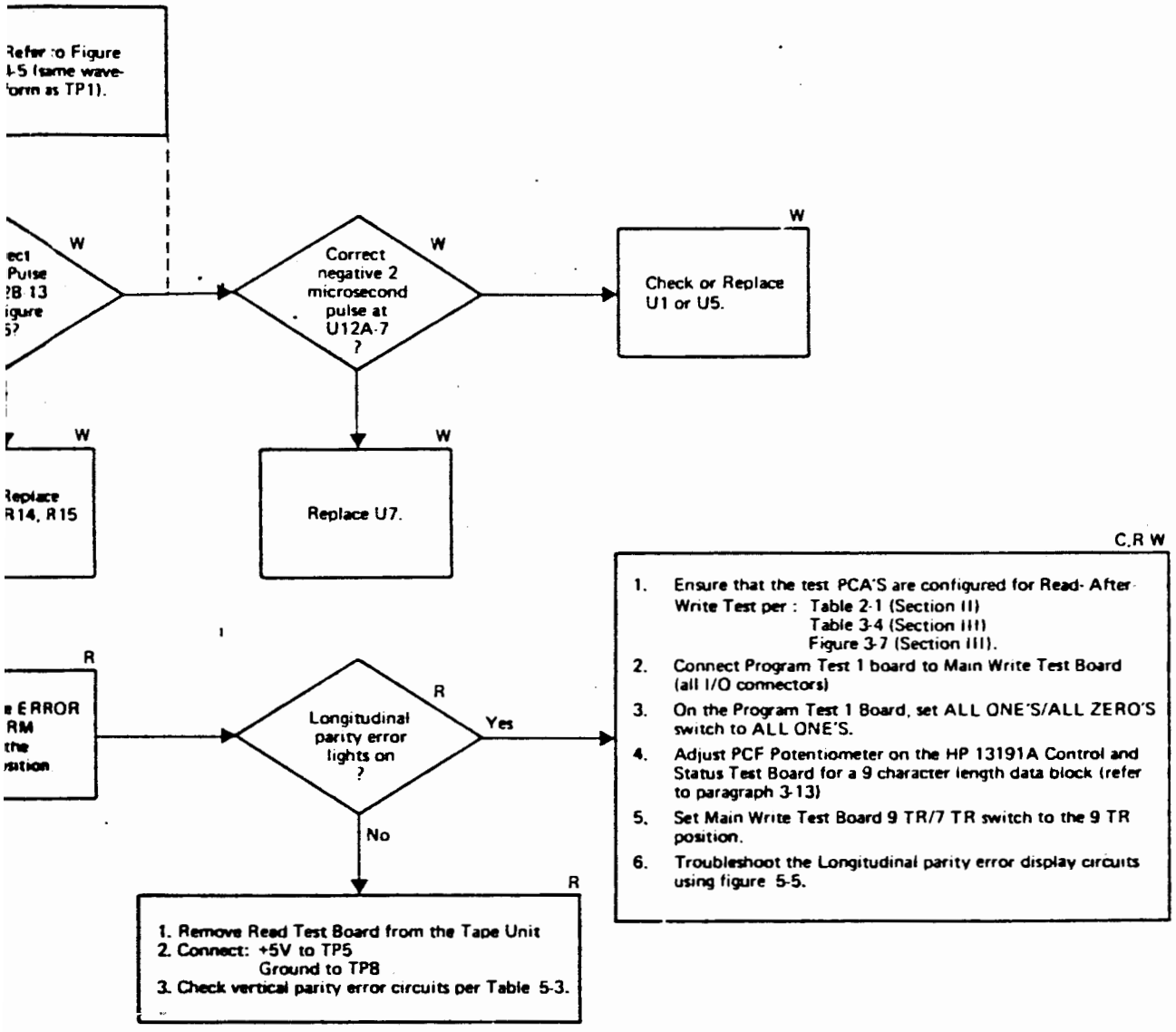
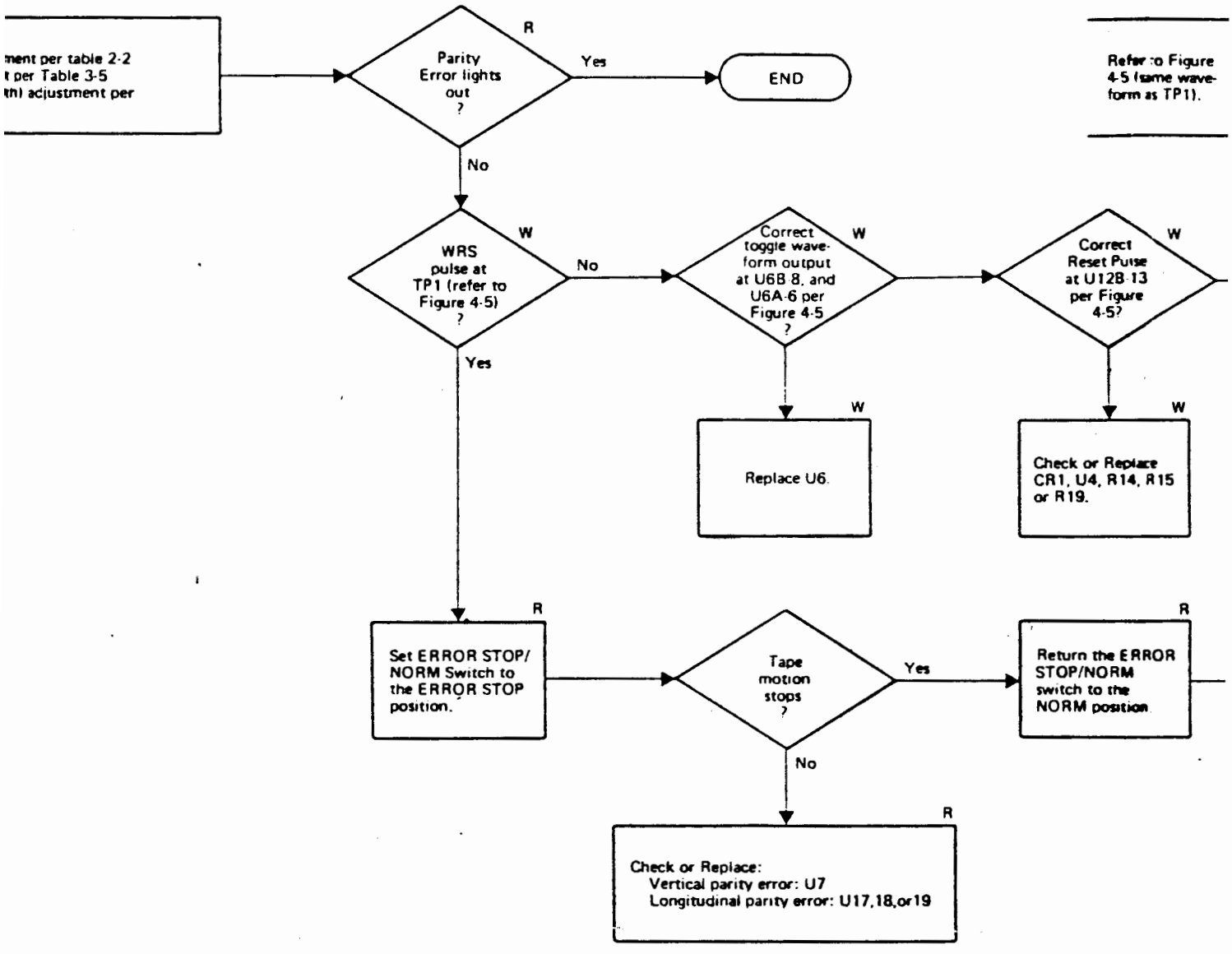
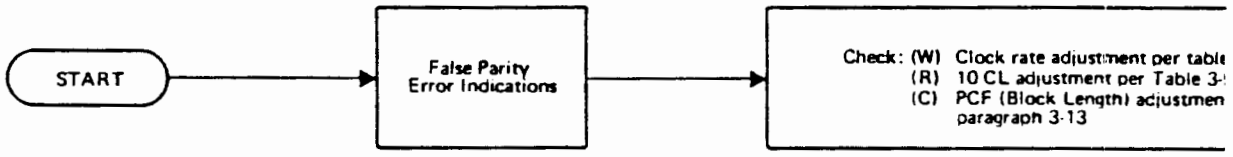
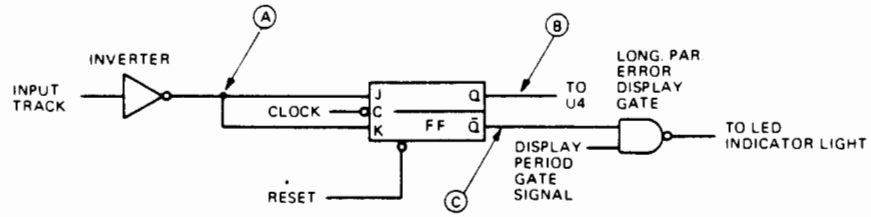


Figure 5-4. False Parity Error Indication Troubleshooting Diagram

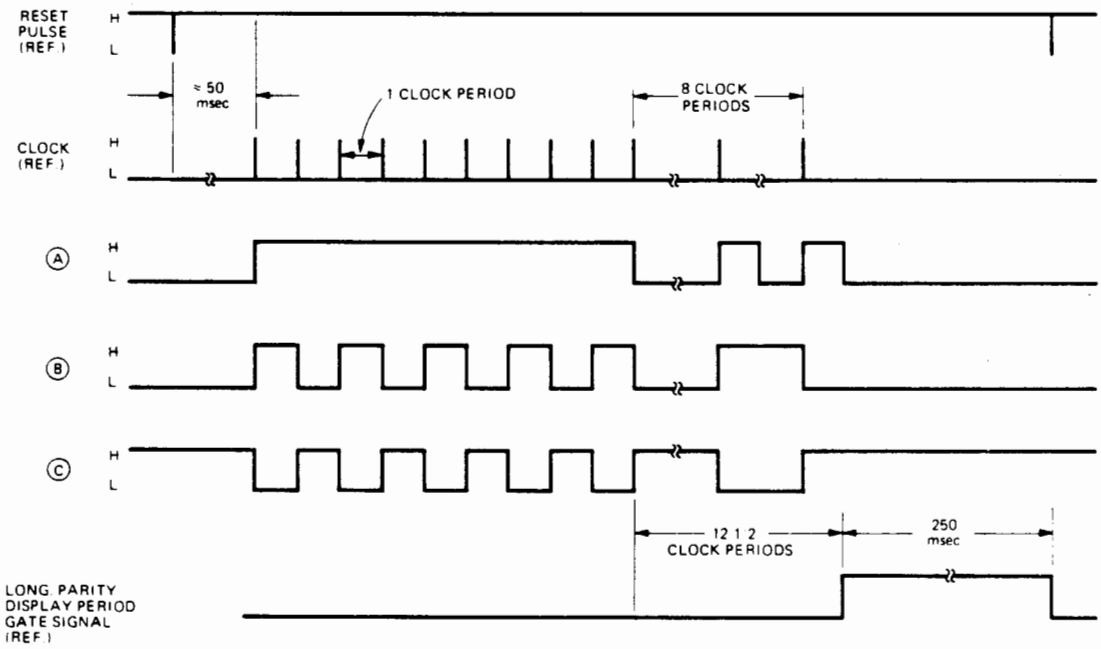

ment per table 2-2
t per Table 3-5
th) adjustment per
R
Parity Error lights out ?
Yes
END
Refer to Figure 4-5 (same waveform as TP1).
No
W
WRS pulse at TP1 (refer to Figure 4-5) ?
No
W
Correct toggle waveform output at U6B-8, and U6A-6 per Figure 4-5 ?
W
Correct Reset Pulse at U12B-13 per Figure 4-5?
Yes
W
Replace U6.
W
Check or Replace CR1, U4, R14, R15 or R19.
R
Set ERROR STOP/NORM Switch to the ERROR STOP position.
Tape motion stops ?
Yes
R
Return the ERROR STOP/NORM switch to the NORM position.
No
R
Check or Replace:
Vertical parity error: U7
Longitudinal parity error: U17,18,or19



C = Control and Status Test PCA
W = Main Write Test PCA
R = Read Test PCA



WAVEFORMS (SEE NOTES)



TABLE

INPUT TRACK	INVERTER INPUT (A)	FLIP-FLOP	F/F OUTPUT		LONG PAR ERROR DISPLAY GATE
			Q(B)	Q̄(C)	
$\overline{RDP}$ (PIN K)	U2 2	U11A	11	10	U17A
$\overline{RD0}$ (PIN L)	U2 4	U11B	15	14	U18A
$\overline{RD1}$ (PIN M)	U2 6	U10A	11	10	U18B
$\overline{RD2}$ (PIN N)	U3 12	U10B	15	14	U18C
$\overline{RD3}$ (PIN P)	U3 10	U9A	11	10	U18D
RD4 (PIN R)	U3 8	U9B	15	14	U19A
$\overline{RD5}$ (PIN S)	U3 2	U12A	11	10	U19B
$\overline{RD6}$ (PIN T)	U3 4	U12B	15	14	U19C
$\overline{RD7}$ (PIN U)	U3 6	U13A	11	10	U19D

NOTES
1. IF SIGNAL (A) IS INCORRECT, REPLACE INVERTER THAT CORRESPONDS TO THE TRACK PER TABLE
2. IF EITHER SIGNALS (B) OR (C) ARE INCORRECT REPLACE THE FLIP FLOP THAT CORRESPONDS TO THE TRACK PER TABLE
3. IF SIGNALS (A) (B) AND (C) ARE CORRECT AND THE TRACK PARITY ERROR INDICATOR LIGHT REMAINS ON, REPLACE THE LONG PARITY DISPLAY GATE THAT CORRESPONDS TO THE TRACK PER TABLE

2300-42

Figure 5-5. Longitudinal Parity Circuit Troubleshooting Diagram

Table 5-3. Vertical (LAT PAR) Parity Error Circuit Checks

DATA INPUT (FORCED CONDITIONS, GROUND = L, OPEN = H) (CONNECTOR PIN)									INVERTER	PARITY CHECKER (U1) INPUT U1, PINS										S2 OUTPUT	
																				S2-ODD	S2=EVEN
$\overline{RDP}$ (K)	$\overline{RD0}$ (L)	$\overline{RD1}$ (M)	$\overline{RD2}$ (N)	$\overline{RD3}$ (P)	$\overline{RD4}$ (R)	$\overline{RD5}$ (S)	$\overline{RD6}$ (T)	$\overline{RD7}$ (U)	U2F-13	4	2	3	11	12	10	8	1	9	13		
L	L	L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	L	H	L	L	H	L	L	H	L	H	L	H	L	H	H	L	H
L	H	L	H	L	H	L	H	H	L	H	H	L	H	L	H	L	H	L	L	H	L
H	H	H	H	H	H	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	L
FAILED COMPONENT									U2					U3						U1 or S2	

NOTE:

1. H = approx. +5V
   L = approx. 0V
2. Data input formatted by grounding appropriate pin for L and leaving pin open for H.
3. If inverter, Parity Checker, or S2 outputs are not as indicated in response to forced data input conditions, replace listed failed components.

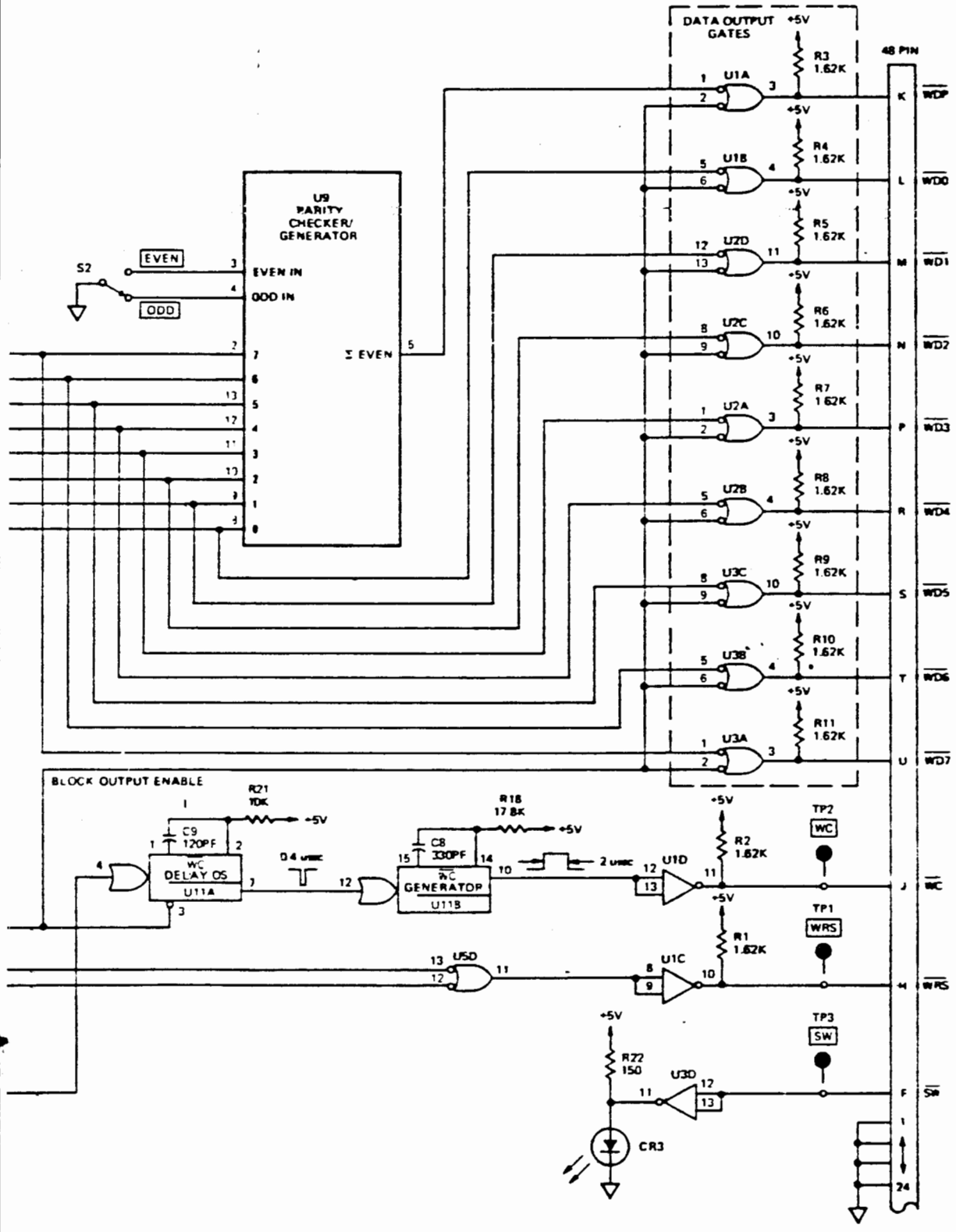
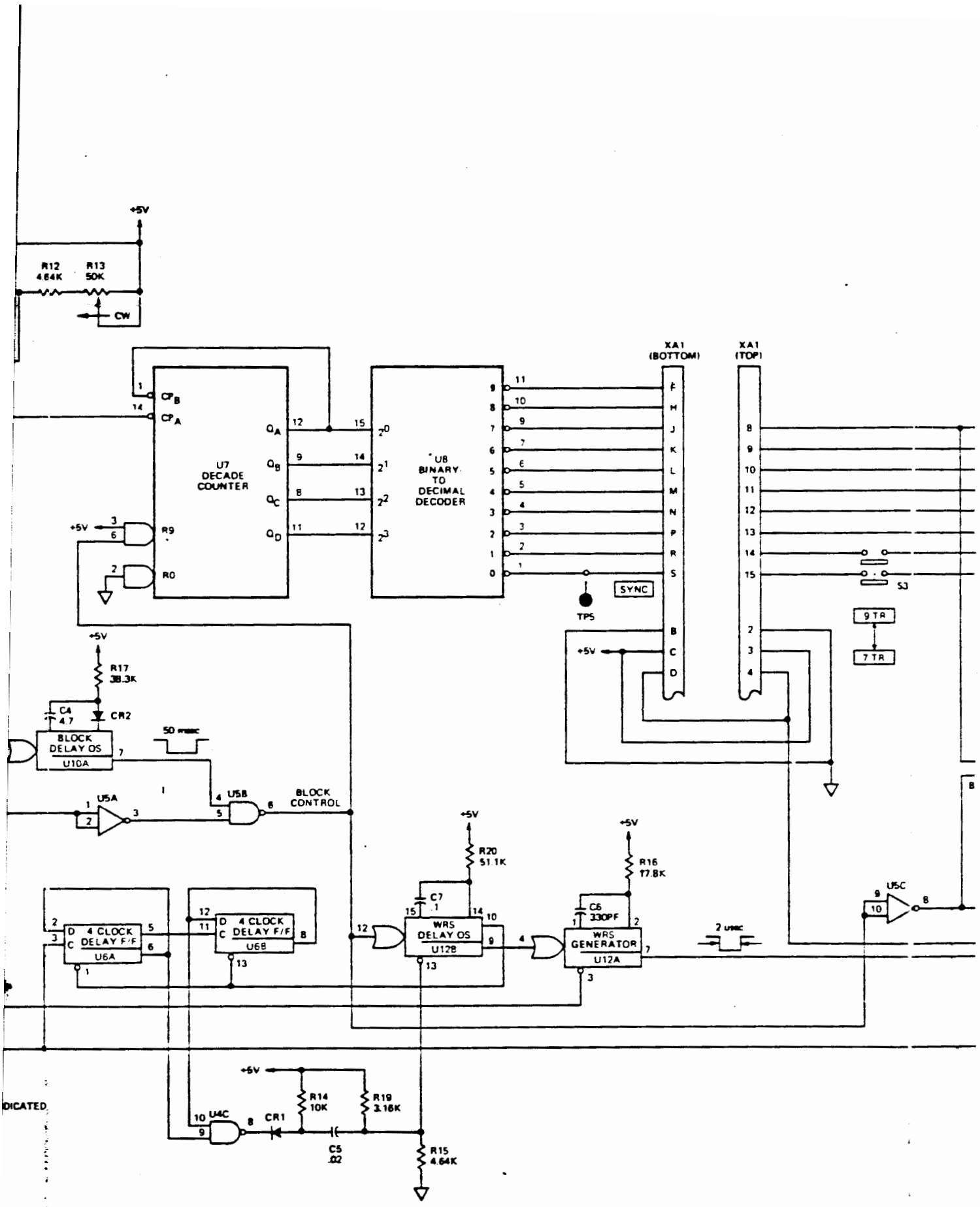
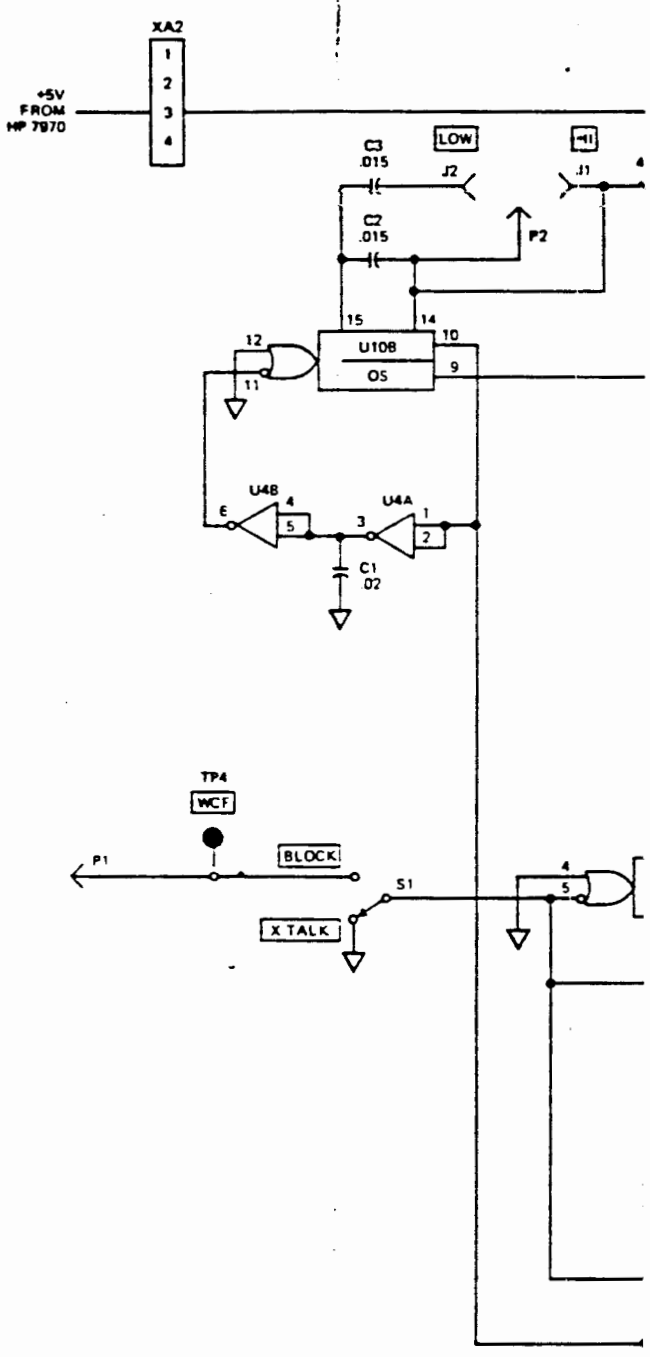


Figure 5-6. Main Write Test Board (A1) Component Location Diagram, Signal Summary Table, and Schematic Diagram


+5V
R12 4.64K
R13 50K
CW
U7 DECADE COUNTER
U8 BINARY TO DECIMAL DECODER
XA1 (BOTTOM)
XA1 (TOP)
SYNC
TP5
SJ
9 TR
7 TR
R9
R0
R17 38.3K
C4 4.7
CR2
BLOCK DELAY OS U10A
50 msec
U5A
U5B
BLOCK CONTROL
R20 51.1K
R16 77.8K
C7 .1
C6 330PF
WRS DELAY OS U12B
WRS GENERATOR U12A
2 usec
U5C
4 CLOCK DELAY F/F U6A
4 CLOCK DELAY F/F U6B
R14 10K
R19 3.16K
U4C
CR1
C5 .02
R15 4.64K



NOTE TOP AND BOTTOM PIN OF XA1 ARE NOT CONNECTED TO EACH OTHER

RESISTANCES IN OHMS

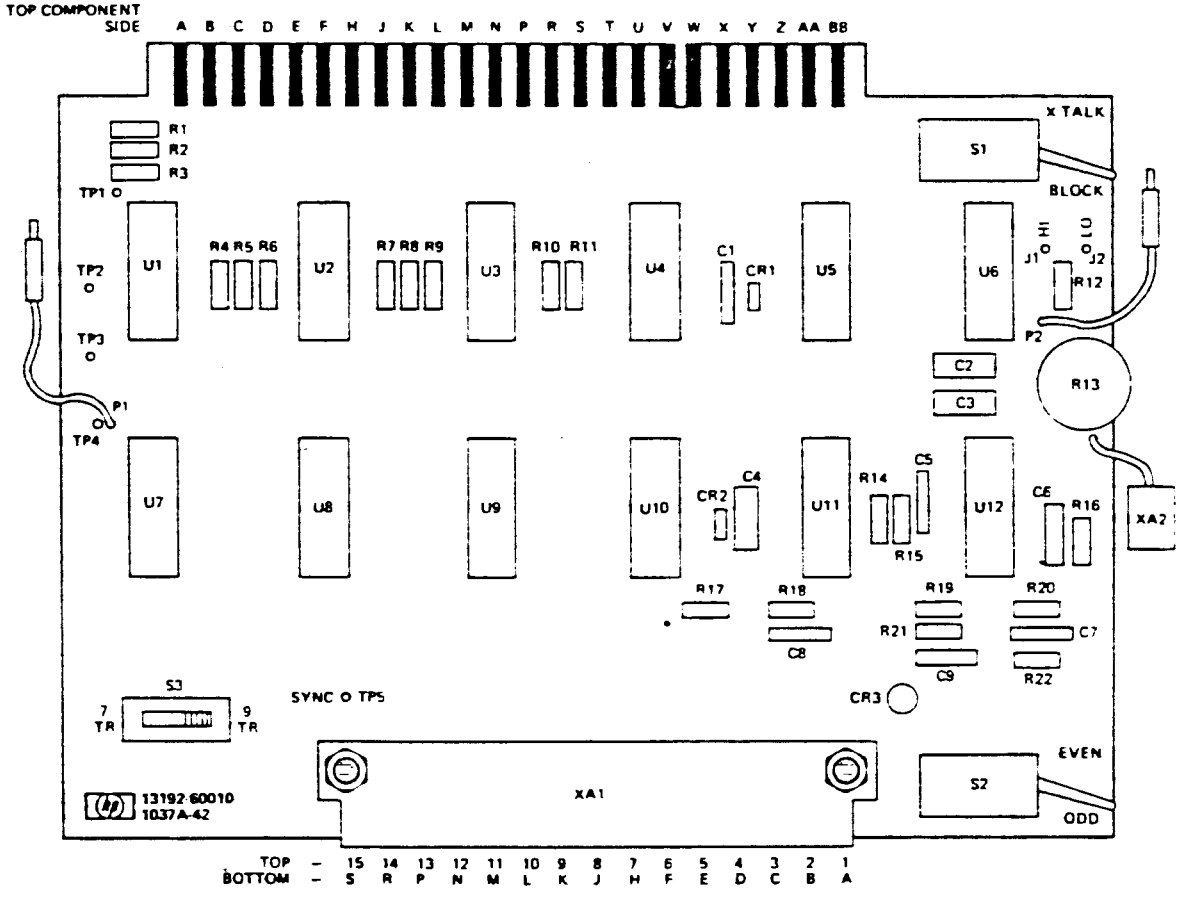
CAPACITANCE IN MICROFARADS UNLESS OTHERWISE INDICATED

U1 THRU U6, U9 = PIN 7 COM, PIN 14 = +5V
U8, U10, U11, U12 = PIN 8 COM, PIN 16 = +5V
U7 = PIN 10.2 COM, PIN 3,5,7 = +5V
U1, U2, U3 = MC8T58P – 1820 – 0256
U4, U5 = SN7400 – 1820 – 0054
U6 = SN7474 – 1820 – 0054
U7 = SN7490 – 1820 – 0055
U8 = SN7442 – 1820 – 0214
U9 = SN7418ON – 1820– 0435
U10, U11, U12 = 9602 – 1820 – 0515

2200-1A

SIGNAL SUMMARY

MNEMONIC	SIGNAL NAME	MNEMONIC	SIGNAL NAME
WDP	Write Data Parity Bit	WD5	Write Data Bit 5
WD0	Write Data Bit 0	WD6	Write Data Bit 6
WD1	Write Data Bit 1	WD7	Write Data Bit 7
WD2	Write Data Bit 2	WC	Write Clock
WD3	Write Data Bit 3	WRS	Write Reset
WD4	Write Data Bit 4	SW	Set Write
WCF	Write Foward Command		



2300 2

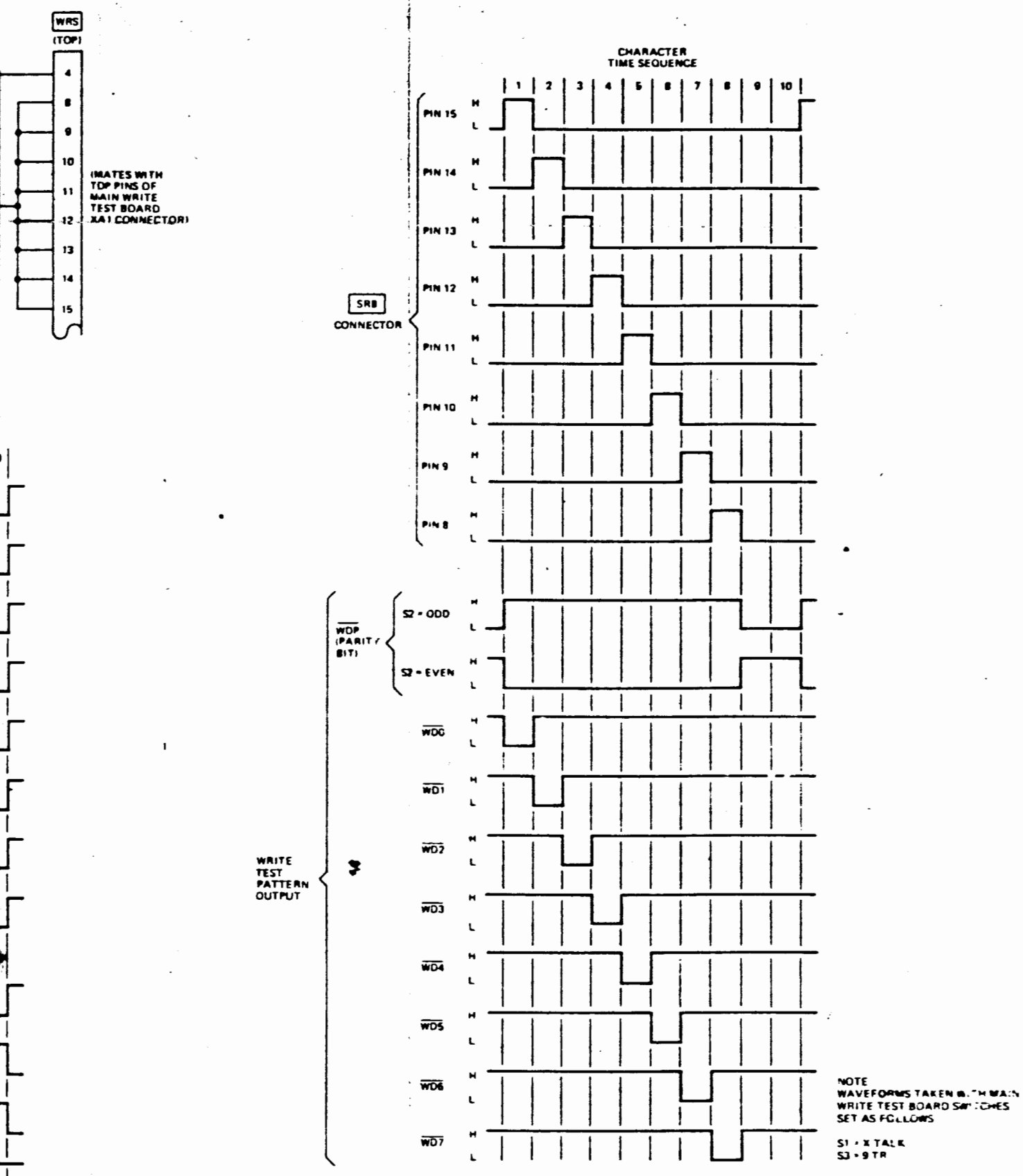
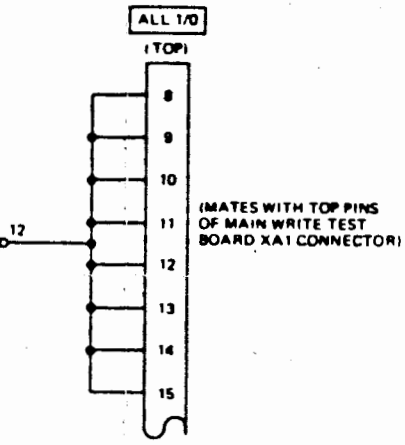
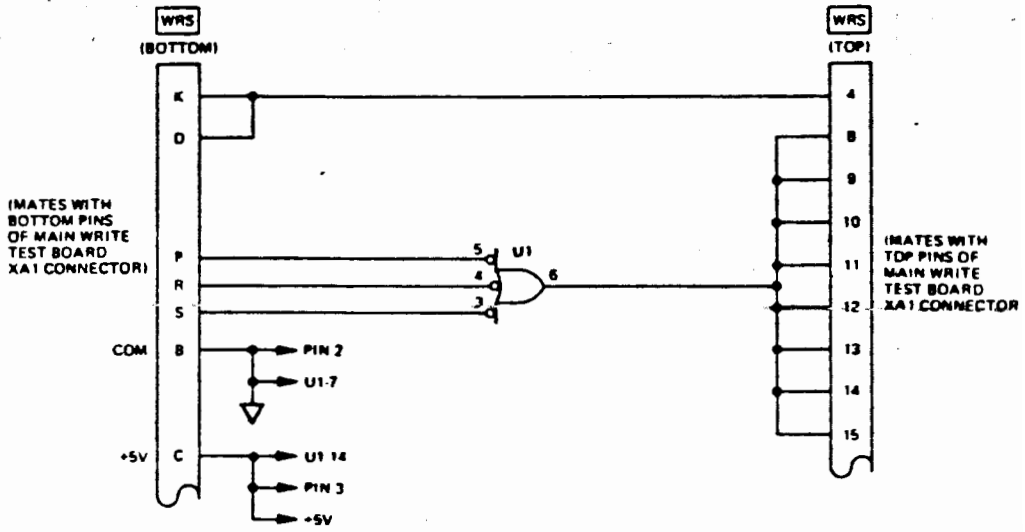
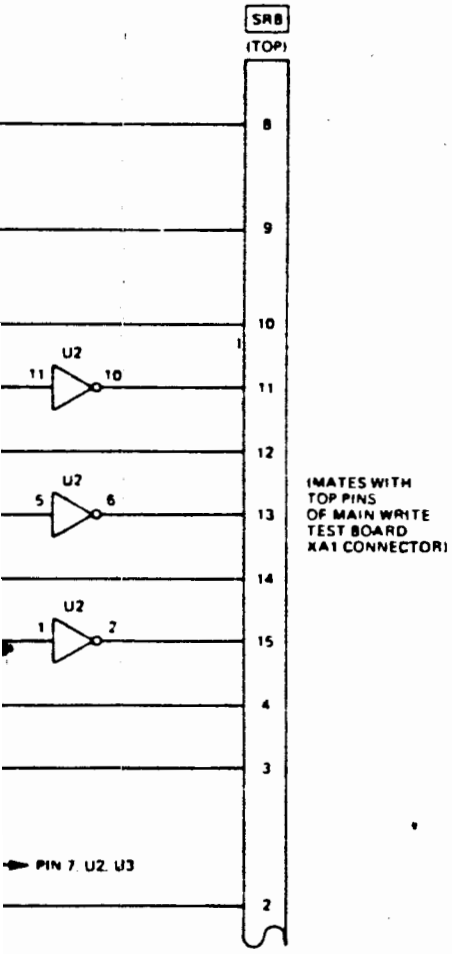
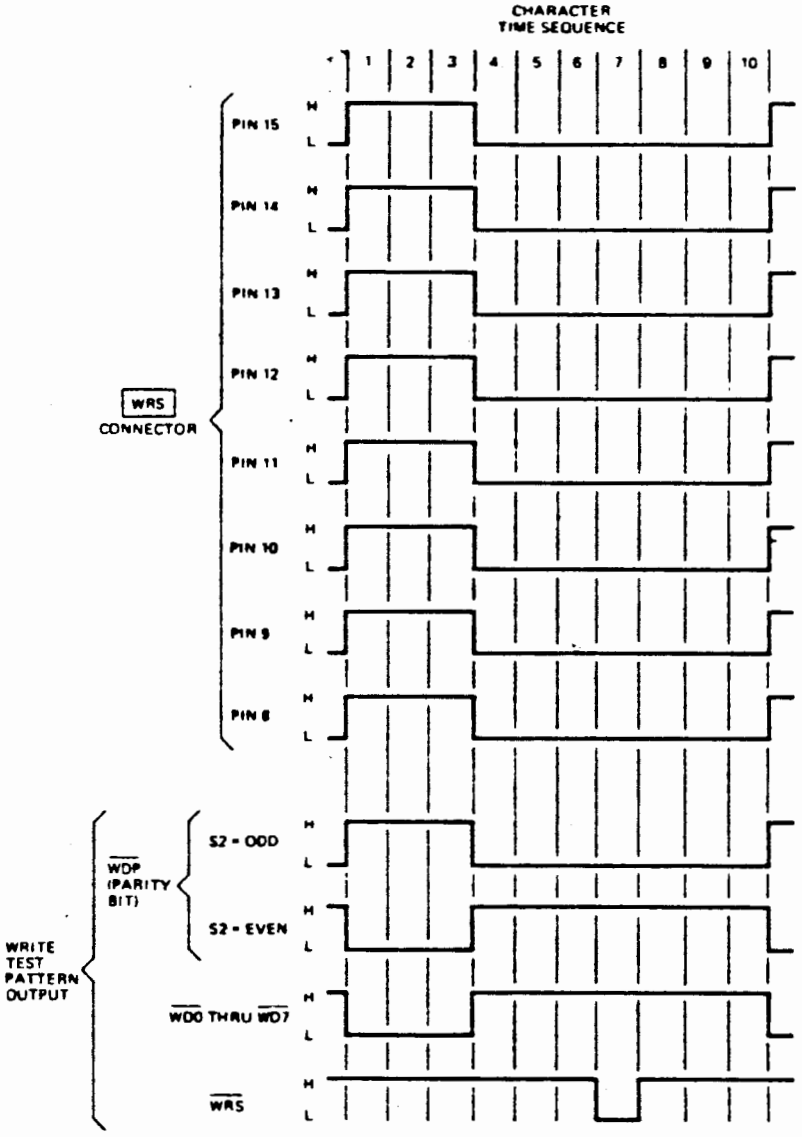


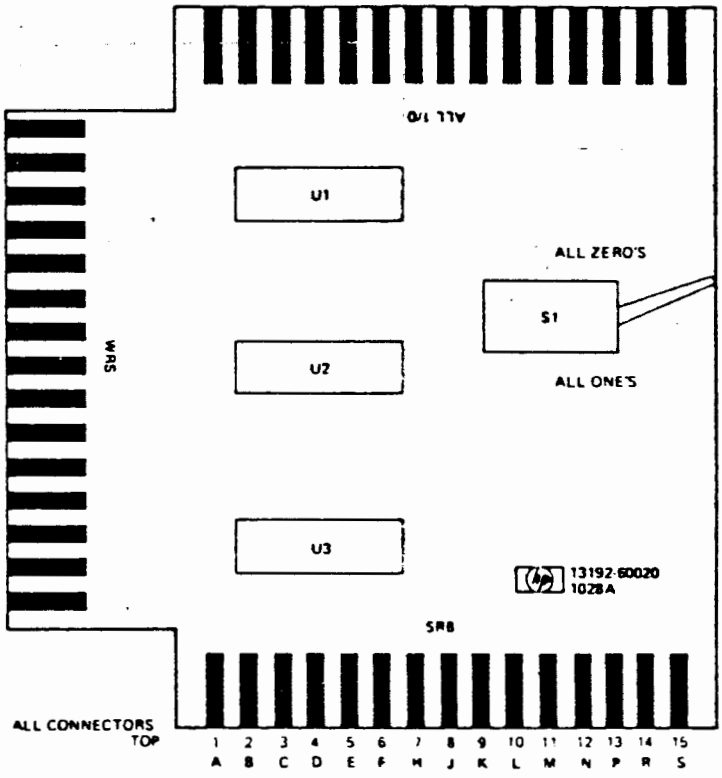
Figure 5-7. Write Program 1 Test Board (A2) Parts Location, Schematic and Waveform Diagrams


ALL 1/0
(TOP)
8
9
10
11
12
13
14
15
12
(MATES WITH TOP PINS OF MAIN WRITE TEST BOARD XA1 CONNECTOR)


WRS
(BOTTOM)
K
D
P
R
S
COM
B
+5V
C
(MATES WITH BOTTOM PINS OF MAIN WRITE TEST BOARD XA1 CONNECTOR)
5
4
3
U1
6
PIN 2
U1-7
U1 14
PIN 3
+5V
WRS
(TOP)
4
8
9
10
11
12
13
14
15
(MATES WITH TOP PINS OF MAIN WRITE TEST BOARD XA1 CONNECTOR)


SRB
(TOP)
8
9
10
11
12
13
14
15
4
3
2
U2
11
10
U2
5
6
U2
1
2
(MATES WITH TOP PINS OF MAIN WRITE TEST BOARD XA1 CONNECTOR)
PIN 7, U2, U3


CHARACTER TIME SEQUENCE
1
2
3
4
5
6
7
8
9
10
WRS CONNECTOR
PIN 15
PIN 14
PIN 13
PIN 12
PIN 11
PIN 10
PIN 9
PIN 8
H
L
WRITE TEST PATTERN OUTPUT
WDP (PARITY BIT)
S2 = ODD
S2 = EVEN
WD0 THRU WD7
WRS



FIXED OUTPUT LEVELS

A2S1 POSITION	ALL 1/0 CONNECTOR PINS 8 THRU 15	MAIN WRITE TEST BOARD OUTPUT PATTERN WD0 THRU WD7	MAIN WRITE TEST BOARD PARITY BIT WDP	
			A1S2 = ODD	A1S2 = EVEN
ALL ONE'S	H	L	L	H
ALL ZERO'S	L	H	L	H

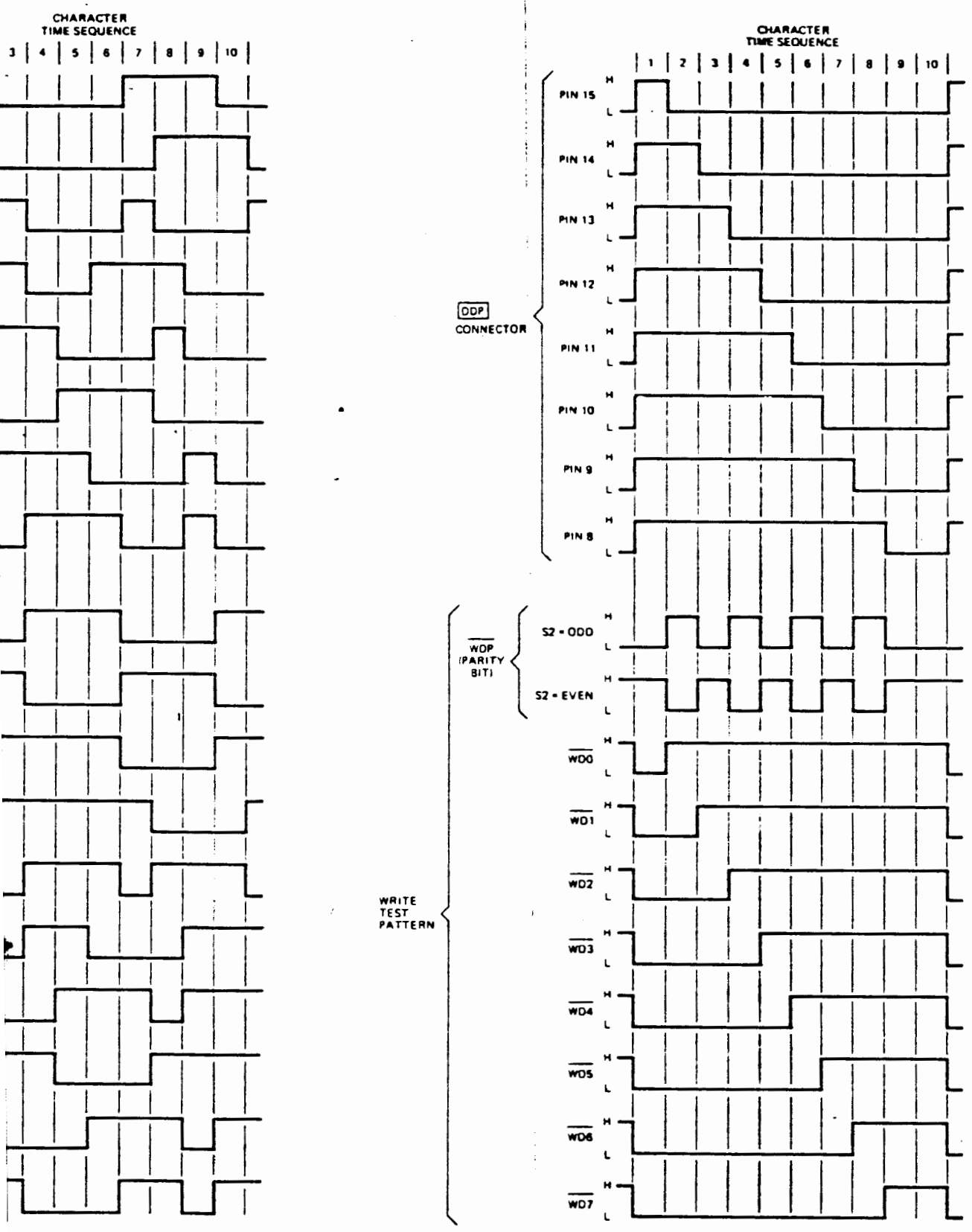
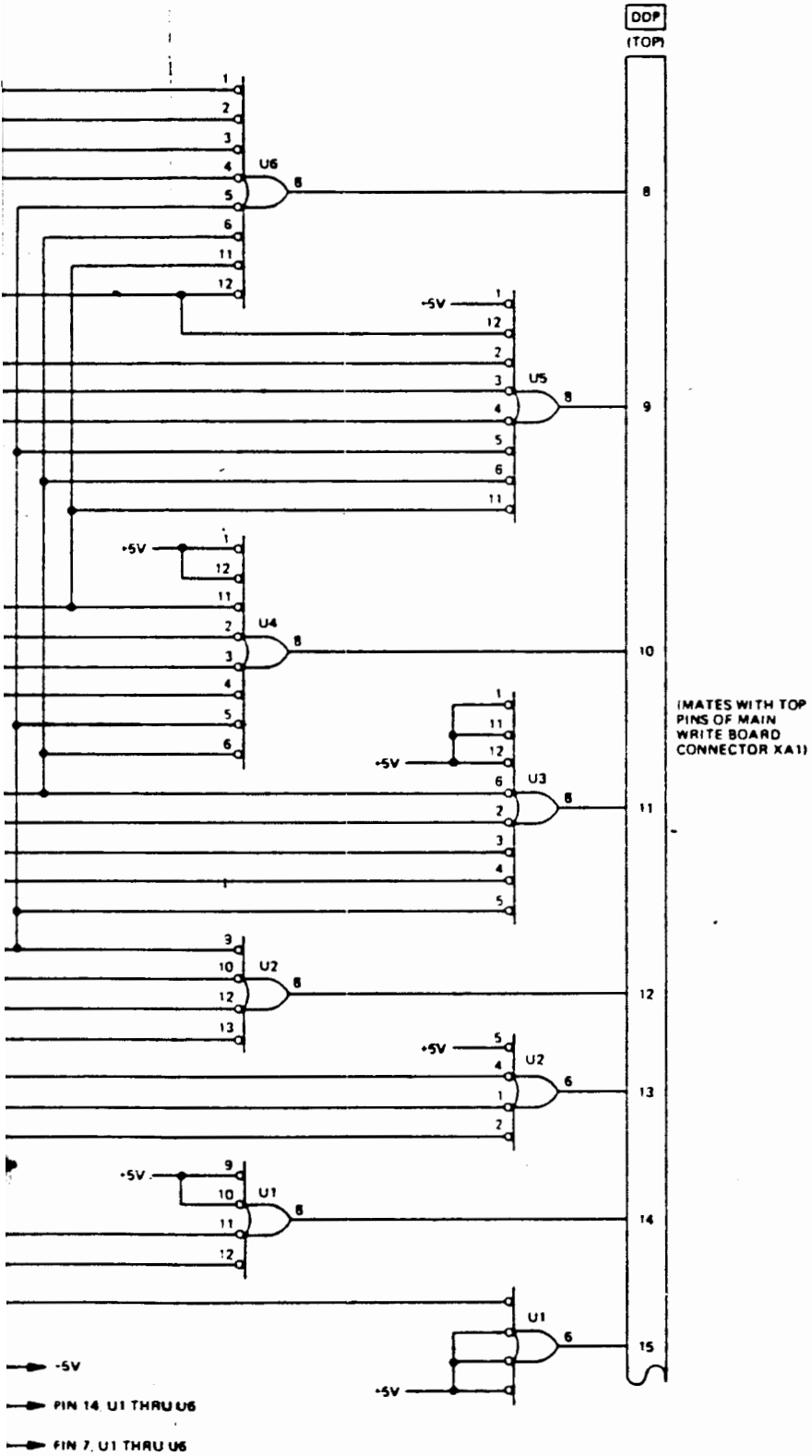
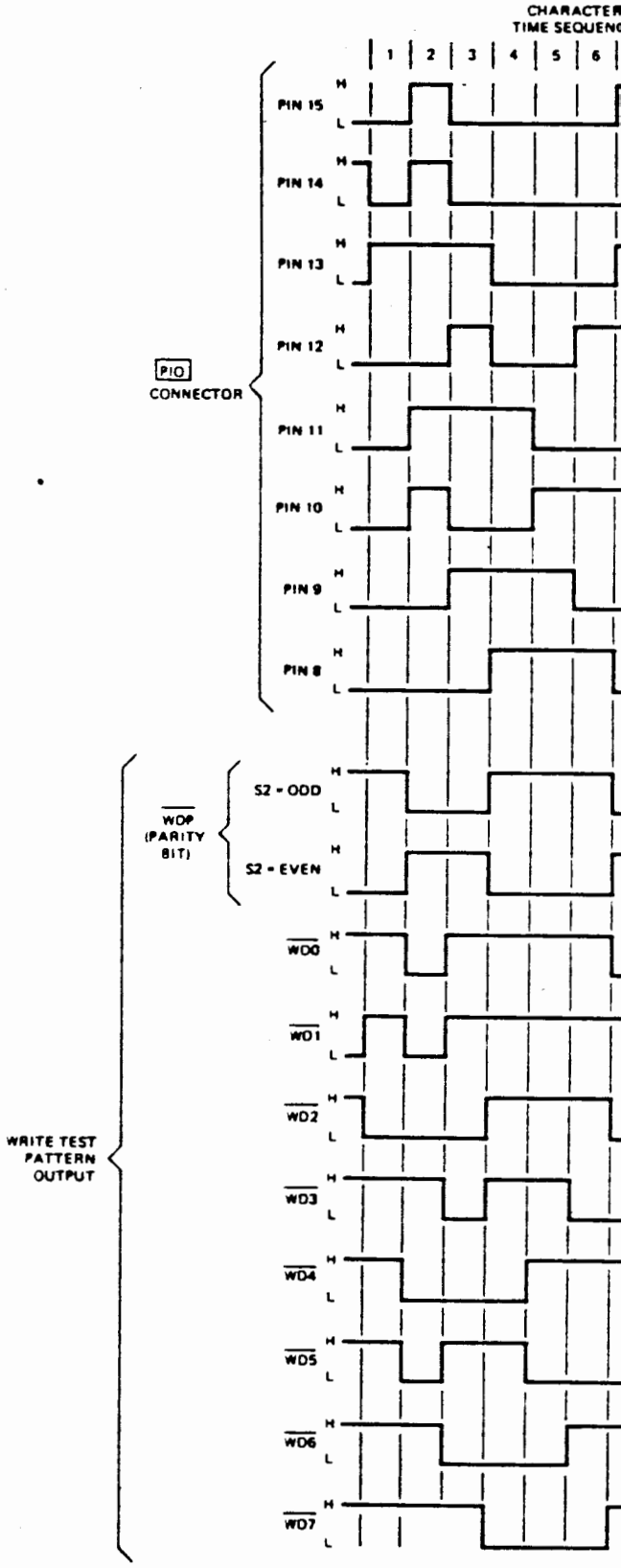
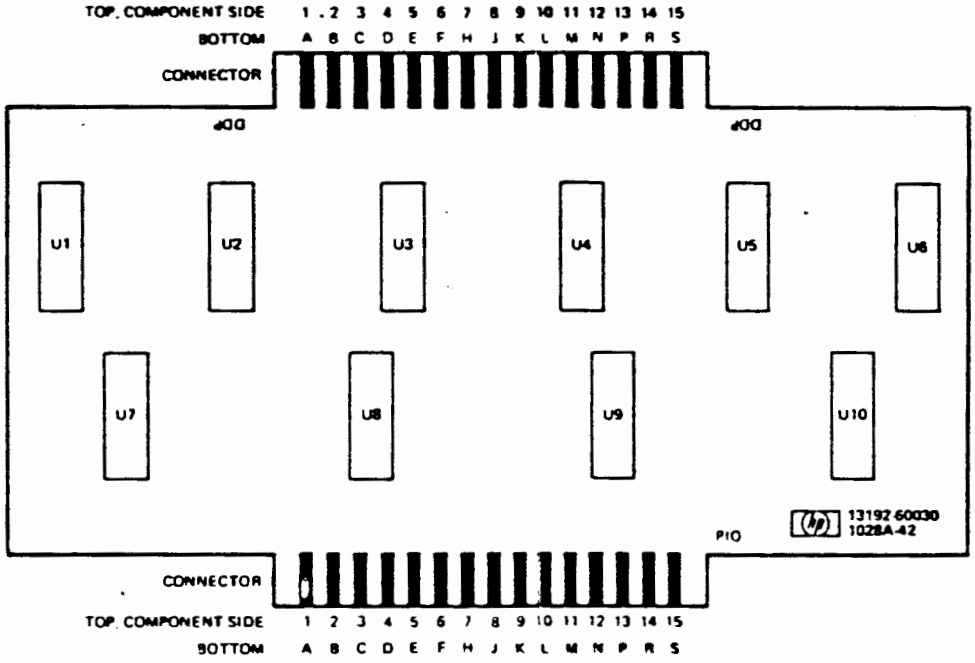
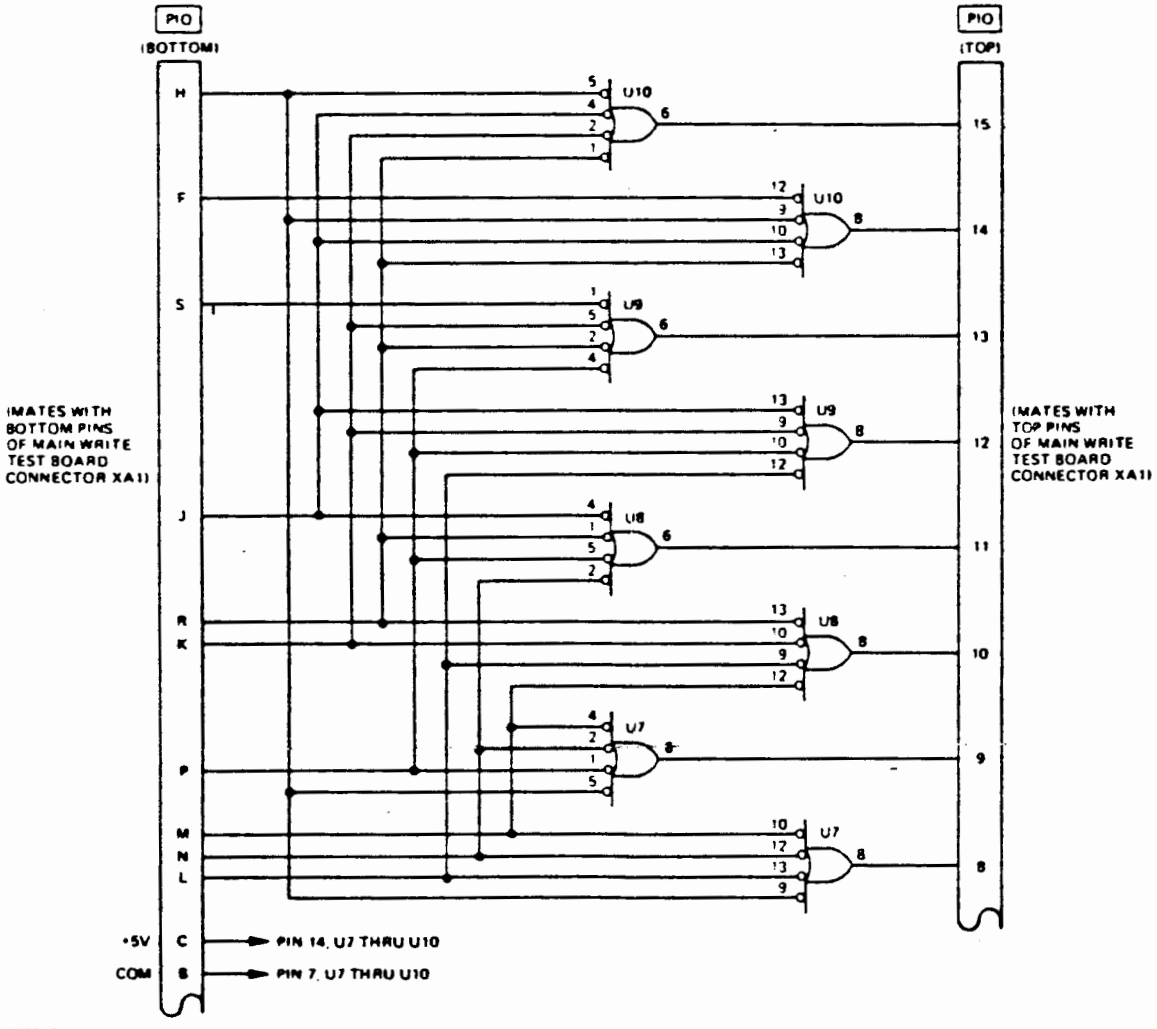


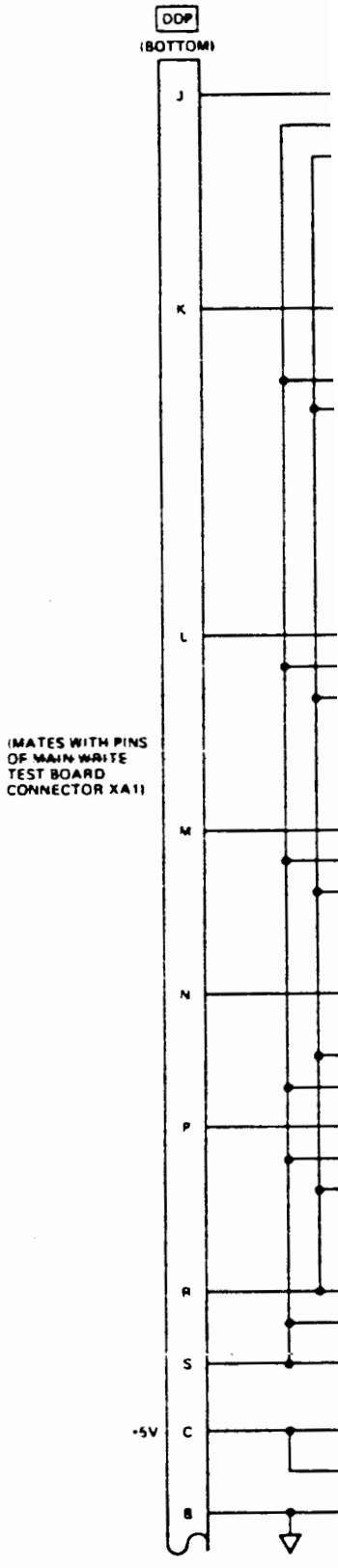
Figure 5-8. Write Program 2 Test Board (A3) Parts Location, Schematic, and Waveform Diagrams


DDP
(TOP)
U6
U5
U4
U3
U2
U2
U1
U1
+5V
-5V
8
9
10
11
12
13
14
15
(MATES WITH TOP PINS OF MAIN WRITE BOARD CONNECTOR XA1)
-5V
PIN 14, U1 THRU U6
PIN 7, U1 THRU U6


CHARACTER TIME SEQUENC
1
2
3
4
5
6
PIO CONNECTOR
PIN 15
PIN 14
PIN 13
PIN 12
PIN 11
PIN 10
PIN 9
PIN 8
H
L
WRITE TEST PATTERN OUTPUT
WDP (PARITY BIT)
S2 = ODD
S2 = EVEN
WD0
WD1
WD2
WD3
WD4
WD5
WD6
WD7


TOP, COMPONENT SIDE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
BOTTOM A B C D E F H J K L M N P R S
CONNECTOR
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
13192-60030
1028A-42
P10
CONNECTOR
TOP, COMPONENT SIDE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
BOTTOM A B C D E F H J K L M N P R S


P10
(BOTTOM)
P10
(TOP)
(MATES WITH BOTTOM PINS OF MAIN WRITE TEST BOARD CONNECTOR XA1)
(MATES WITH TOP PINS OF MAIN WRITE TEST BOARD CONNECTOR XA1)
H
F
S
J
R
K
P
M
N
L
+5V
COM
C
B
U10
U9
U8
U7
15
14
13
12
11
10
9
8
PIN 14, U7 THRU U10
PIN 7, U7 THRU U10


DDP
(BOTTOM)
(MATES WITH PINS OF MAIN WRITE TEST BOARD CONNECTOR XA1)
J
K
L
M
N
P
R
S
+5V
C
B

2300-45

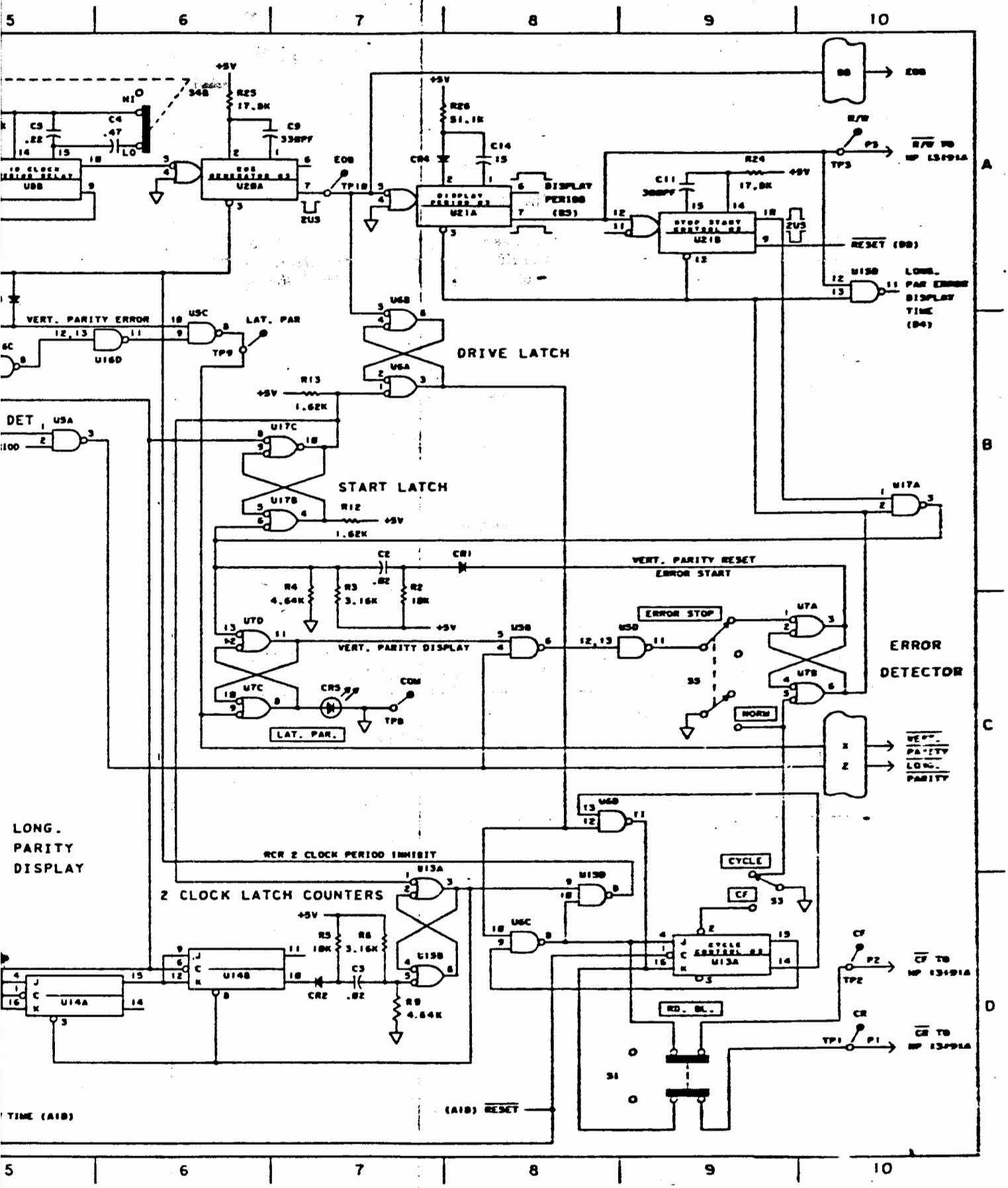
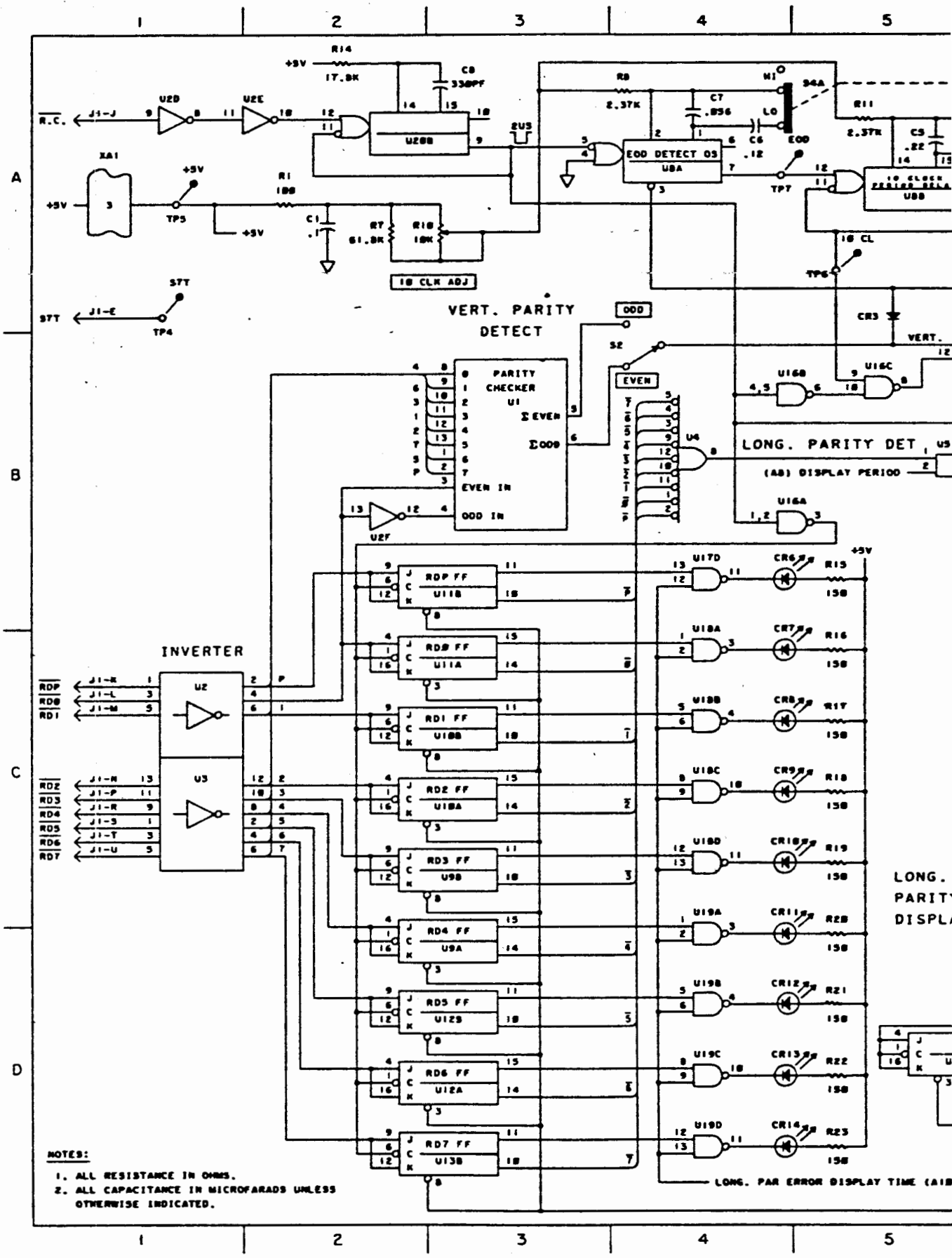
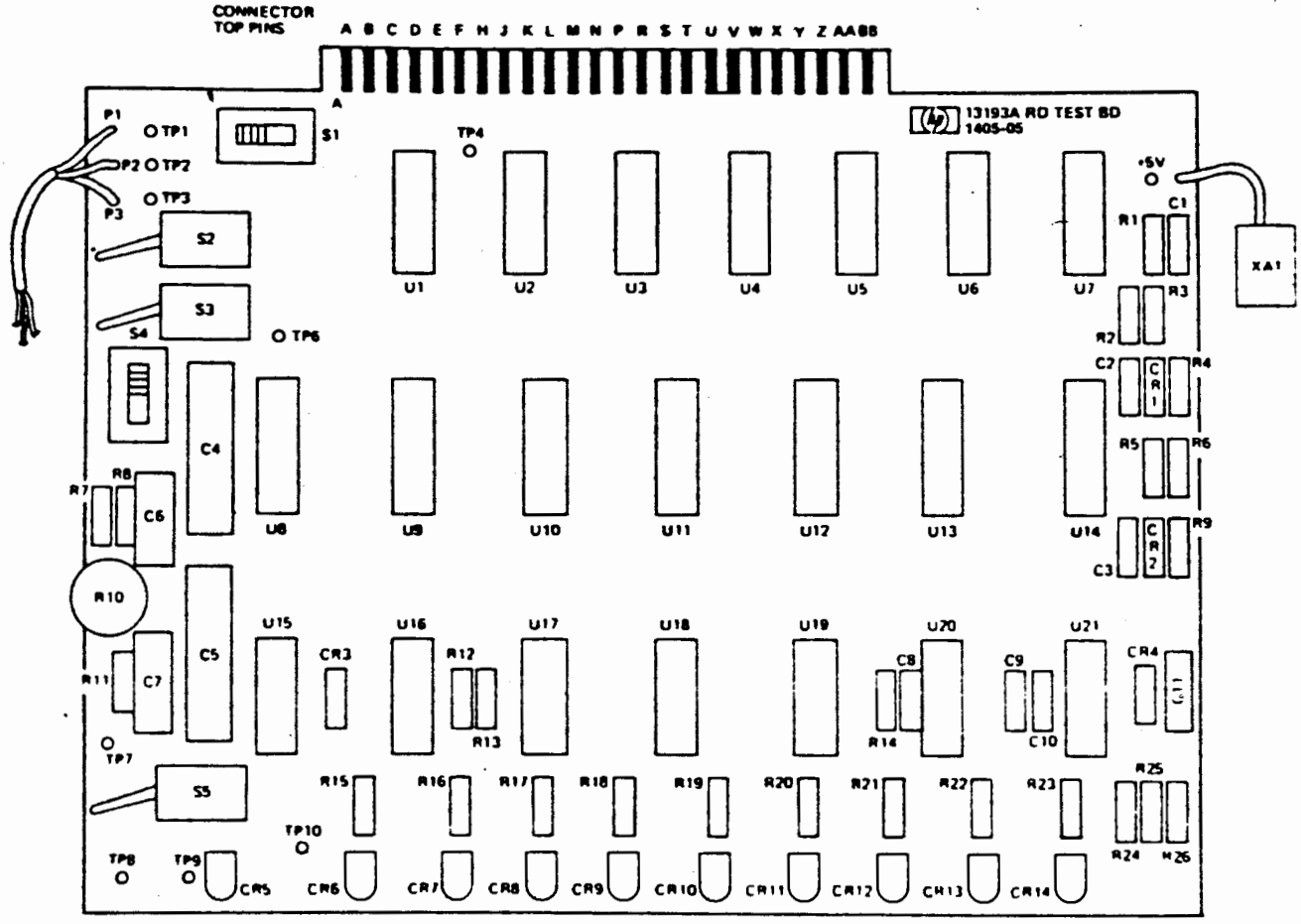


Figure 5-9. Read Test Board Component Location, Signal Summary Table, and Schematic Diagrams


VERT. PARITY DETECT
INVERTER
LONG. PARITY DET
EOD DETECT
PARITY CHECKER U1
RDP FF U11B
RD0 FF U11A
RD1 FF U10B
RD2 FF U10A
RD3 FF U9B
RD4 FF U9A
RD5 FF U12B
RD6 FF U12A
RD7 FF U13B
NOTES:
1. ALL RESISTANCE IN OHMS.
2. ALL CAPACITANCE IN MICROFARADS UNLESS OTHERWISE INDICATED.



2308-32

SIGNAL SUMMARY

MNEMONIC	SIGNAL NAME	MNEMONIC	SIGNAL NAME
EOB	End of Block	RD3	Read Data Bit 3
RC	Read Clock	RD4	Read Data Bit 4
S7T	7-Track Status	RD5	Read Data Bit 5
VERT. PARITY	Vertical Parity	RD6	Read Data Bit 6
LONG. PARITY	Longitudinal Parity	RD7	Read Data Bit 7
RDP	Read Data Parity Bit	RCF	Read Foward Command
RD0	Read Data Bit 0	RCR	Read Reverse Command
RD1	Read Data Bit 1	R/W	Read After Write Command
RD2	Read Data Bit 2		

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION.

6-2. This section contains information pertaining to replaceable parts for the HP 13192A Write Test Accessory and the HP 13193A Read Test Accessory. Included are parts lists and ordering information.

6-3. REPLACEABLE PARTS LIST.

6-4. Table 6-1 lists the major replaceable parts for the test accessory. Tables 6-2 through 6-5 list replaceable parts for the individual test PCAs. These components are listed in alphanumerical order, according to reference designations. The total quantity of each component is also specified in the parts list. Table 6-6 lists the manufacturers that correspond to the five digit MFR CODES shown in table 6-2 through 6-5.

6-5. ORDERING INFORMATION.

6-6. To order replacement parts, address the order or inquiry to the local HP sales and service office (refer to the list on the back of this manual). Specify the following information for each part ordered.

a. Model number of accessory.

b. HP part number for each part.

c. Description of each part.

d. Circuit reference designations (refer to figures 5-6 through 5-9 for reference designations).

Table 6-1. Test Accessory Parts List

TEST PCA	PART NUMBER	PARTS LIST TABLE
Main Write Test PCA	HP 13192-60010	Table 6-2
Write Program 1 Test PCA	HP 13192-60020	Table 6-3
Write Program 2 Test PCA	HP 13192-60030	Table 6-4
Read Test PCA	HP 13193-60010	Table 6-5

Table 6-2. Main Write Test PCA (A1) Parts List

REF DESIG	HP PART NUMBER	DESCRIPTION	QTY	MFR CODE	MFR PART NUMBER
C1, C5	0160-3459	Capacitor: Ceramic .02 μF ±10% VDC	2	56289	CO23F101H203MS22CDH
C2-C3	0160-0194	Capacitor: Encap Foil .015 μF ±10% 200 VDC	1	56289	192P15392-PTS
C4	0180-0100	Capacitor: Elec 4.7 μF ±20% 35 VDC	1	56289	150D475X9035B2-DYS
C6, C8	0160-2208	Capacitor: Ceramic 330 pF ±5% 300 VDC	2	28480	0160-2208
C7	0150-0121	Capacitor: Ceramic .1 μF ±10% 50 VDC	1	56289	5C50B15 CML
C9	0160-2205	Capacitor: Ceramic 120 pF ±5% 300 VDC	1	28480	0160-2205
CR1-CR2	1901-0040	Diode: Silicon 30MA 30WV	2	07263	FDG-1088
CR3	1990-0326	Diode: Visible Light Emitter	1	28480	1990-0326
J1-J2	0360-0124	Terminal: Solder Stud Pin	2	28480	0360-0124
P1-P2	1200-0063	Receptacle: Crimp	2	28480	1200-0063
R1-R11	0757-0428	Resistor: Met Film 1.62K Ohm ±1% 1/8W	11	28480	757-0428
R12	0698-3155	Resistor: Met Film 4.64K Ohm ±1% 1/8W	1	28480	0698-3155
R13	2100-1948	Resistor: Var 50K ohm 5%	1	28480	2100-1948
R14, R21	0757-0442	Resistor: Met Film 10K Ohm ±1% 1/8W	2	28480	757-0442
R15	0698-3155	Resistor: Met Film 4.64K Ohm ±1% 1/8W	1	28480	0698-3155
R16, R18	0698-3136	Resistor: Met Film 17.8K Ohm ±1% 1/8W	2	28480	0698-3136
R17	0698-3161	Resistor: Fxd Comp 38.3K Ohm ±1% 1/8W	1	28480	0698-3161
R19	0757-0279	Resistor: Met Film 3.16K Ohm ±1% 1/8W	1	28480	0757-0279
R20	0757-0458	Resistor: Met Film 51.1K Ohm ±1% 1/8W	1	28480	0757-0458
R22	0683-1515	Resistor: Fxd Comp 150 Ohm +5% 1/4W	1	01121	CB 1515
S1-S2	3101-1213	Switch: Toggle, DPST-DB-Sub Miniature	2	81640	T8001
S3	3101-0973	Switch: Slide DPDT, 0.5A 125V AC/DC	1	79727	G126-0018
TP1-TP5	0360-0124	Terminal: Solder Stud Pin	5	28480	0360-0124
U1-U3	1820-0256	Integrated Circuit: 4-2 in Gate O.C.	3	04713	MC858P
U4-U5	1820-0054	Integrated Circuit: 4X2 in Gate	2	01295	SN7400N
U6	1820-0077	Integrated Circuit: Dual D FF	1	01295	SN7474N
U7	1820-0055	Integrated Circuit: Decade Counter	1	01295	SN7490N
U8	1820-0214	Integrated Circuit: BCD – Decade Convert	1	01295	SN7442N
U9	1820-0435	Integrated Circuit: 8-Bit Odd/Even Gen./Checker	1	01295	SN74180N
U10-U12	1820-0515	Integrated Circuit: Dual Mono Multi	3	07263	U7B960259X
XA1	1251-2628	Connector: PC 30 Pin	1	05574	3VH50/1JN5
XA2	Ref Only	Connector: Plastic 4 Pin			
	1251-2097	–Contact: Pin Male	1	28480	1251-2097
	1251-2418	–Contact: Pin Female	3	27264	1381 TL
	1251-2512	–Body: Connector Plastic	1	27264	1490-R1
XA3*	1251-0149	Connector: Bi-Pin	1	02660	91-PC6F-1000

*Used only on series 1026 (and earlier) boards in lieu of Slide Switch S3.

Table 6-3. Write Program 1 Test PCA (A2) Parts List

REF DESIG	HP PART NUMBER	DESCRIPTION	QTY	MFR CODE	MFR PART NUMBER
S1	3101-1213	Switch: Toggle DPST-DB, Subminiature	1	81640	T8001
U1,U3	1820-0068	Integrated Circuit: 3X In Gate	2	12040	SN7410N
U2	1820-0174	Integrated Circuit: Hex Inverter	1	01295	SN7404N

Table 6-4. Write Program 2 Test PCA (A3) Parts List

REF DESIG	HP PART NUMBER	DESCRIPTION	QTY	MFR CODE	MFR PART NUMBER
U1,U2,U7-U10	1820-0069	Integrated Circuit: 2X4 In Gate	6	01295	SN7420N
U3-U6	1820-0070	Integrated Circuit: 8 In Gate	4	01295	SN7430N

Table 6-5. HP 13193A Read Test PCA Parts List

REF DESIG	HP PART NUMBER	DESCRIPTION	QTY	MFR CODE	MFR PART NUMBER
C1	0150-0121	Capacitor: Fxd Cer .1 μF 50 VDC	1	56289	5C50BIS-CML
C2-C3	0160-3459	Capacitor: Fxd Cer .02 μF 100 VDC	2	56289	C023F101H203MS22CDH
C4	0180-0376	Capacitor: Fxd Tant .47 μF 10% 200 VDC	1	56289	150D474X9035A2-DYS
C5	0160-0380	Capacitor: Fxd Mylar .22 μF 10% 200 VDC	1	28480	0160-0380
C6	0160-2117	Capacitor: Fxd Mylar .12 μF 10% 200 VDC	1	28480	0160-2117
C7	0160-0165	Capacitor: Fxd Mylar .056 μF 10% 200 VDC	1	56289	192P56392-PTS
C8-C10	0160-2208	Capacitor: Fxd Mica 330 pF 5% 300 VDC	3	28480	0160-2208
C11	0180-1746	Capacitor: Fxd Tant 15 μF 20% 20 VDC	1	28480	0180-1746
CR1-CR4	1901-0040	Diode: Silicon 30 mA 30 VDC	4	07263	FDG1088
CR5-CR14	1990-0326	Diode: Visible light emitter	10	28480	1901-0040
E1	0380-0381	Post: Binding Stand-off	2	28480	1990-0326
P1-P3	1200-0063	Receptacle: Crimp	3	28480	1200-0063
R1	0757-0401	Resistor: Fxd Comp 100 ohm 1% 1/8W	1	28480	0757-0401
R2, R5	0757-0442	Resistor: Fxd Comp 10 Kohm 1% 1/8W	2	28480	0757-0442
R3, R6	0757-0279	Resistor: Fxd Met Film 3.16Kohm 1% 1/8W	2	28480	0757-0279
R4, R9	0698-3155	Resistor: Fxd Met Film 4.64 Kohm 1% 1/8W	2	28480	0698-3155
R7	0757-0460	Resistor: Fxd Met Film 61.9 Kohm 1/ 1/8W	1	28480	0757-0460
R8, R11	0698-3150	Resistor: Fxd Comp 2.37 Kohm 1% 1/8W	2	28480	0698-3150
R10	2100-1776	Resistor: Var 10K ohm 5%	1	28480	2100-1776
R12-R13	0757-0428	Resistor: Fxd Comp 1.62 Kohm 1% 1/8W	2	28480	0757-0428
R14,R24,R25	0698-3136	Resistor: Fxd Comp 17.8 Kohm 1% 1/8W	3	28480	0698-3136
R15-R23	0683-1515	Resistor: Fxd Comp 150 ohm 5% 1/4W	9	01121	CB 1515
R26	0757-0458	Resistor: Fxd Comp 51.1 Kohm 1% 1/8W	1	28480	0757-0458
S1, S4	3101-0973	Switch: Slide DPDT 0.5A, 125V AC/DC	2	79727	G126-0018
S2,S3,S5	3101-1213	Switch: Toggle DPST-DB Subminiature	3	81640	T8001
TP1-TP10	0360-0124	Terminal: Solder Stud Pin	10	28480	0360-0124
U1	1820-0435	Integrated Circuit: 8 Bit Odd/Even Gen/Checker	1	01295	SN74180N
U2-U3	1820-0174	Integrated Circuit: Hex Inverter	2	01295	SN7404N
U4	1820-0454	Integrated Circuit: 10 Input NAND	1	04713	MC1805P
U5-U7,U15,U16	1820-0054	Integrated Circuit: 4-2 Input NAND	5	01295	SN7400N
U8,U20,U21	1820-0515	Integrated Circuit: Dual Re-Prog/Reset Mono Multi	2	07263	U7B960259X
U9-U14	1820-0076	Integrated Circuit: Dual JK FF W/PRESET CLOCK	6	01295	SN7476
U17-U19	1820-0256	Integrated Circuit: 4-2 Input Power Gate	3	04713	MC858P
XA1	13193-60020	Connector: 2 Pin	1	28480	13193-60020

Table 6-6. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen-Bradley Co.	Milwaukee, Wis.
01295	Texas Instruments Inc., Semiconductor Components Division	Dallas, Texas
02660	Bunkerramo Corp. Amphenol Connector Div.	Broadview, Ill.
04713	Motorola, Inc., Semiconductor Prod. Div.	Phoenix, Arizona
05574	Viking Industries, Inc.	Chatsworth, Calif.
07263	Fairchild Camera Inst. Corp., Semiconductor Div.	Mountain View, Calif.
12040	National Semiconductor Corp.	Danbury, Conn.
19701	Electra Mfg. Co.	Independance, Kansas
27264	Molex Products Co.	Grove, Ill.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
32997	Bourns Inc., Trimpot Prod. Div.	Riverside, Calif.
56289	Sprague Electric Company	N. Adams, Mass.
79727	Continental Wirt Electronics Corp.	Philadelphia, Pa.
81640	Controls Company of America, Control Switch Div.	Folcroft, Pa.

Table 6-7. List of Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or integrated circuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= jumper wire
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
Ag	= silver			phh	= phillips head
Al	= aluminum	H	= henries	pk	= peak
ar	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	prv	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
b	= base	hex	= hexagon, hexagonal	pwv	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rms	= root-mean-square
Be Cu	= beryllium copper	insul	= insulation, insulated	rwv	= reverse working voltage
		impgrg	= impregnated	rect	= rectifier
cpi	= characters per inch	incand	= incandescent	r/min	= revolutions per minute
coll	= collector	ips	= inches per second	RTL	= resistor-transistor logic
cw	= clockwise				
ccw	= counterclockwise	k	= kilo (10^3), kilohm	s	= second
cer	= ceramic			SB, TT	= slow blow
com	= common	lp	= low pass	Se	= selenium
crt	= cathode-ray tube			Si	= silicon
CTL	= complementary-transistor logic	m	= milli (10^{-3})	scr	= silicon controlled rectifier
		M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
Cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous		
		met. ox.	= metal oxide	Ta	= tantalum
dc	= direct current	mintr	= miniature	td	= time delay
dr	= drive			Ti	= titanium
DTL	= diode-transistor logic	n	= nano (10^{-9})	tgl	= toggle
depc	= deposited carbon	nc	= normally closed or no connection	thd	= thread
dpdt	= double-pole, double-throw			tol	= tolerance
dpst	= double-pole, single-throw	Ne	= neon	TTL	= transistor transistor logic
		no.	= number		
em	= emitter	n.o.	= normally open		
ECL	= emitter-coupled logic	np	= nickel plated	U(μ)	= micro (10^{-6})
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	V	= volt(s)
elctlt	= electrolytic			var	= variable
		NSR	= not separately replaceable	vio	= violet
F	= farads	NRFR	= not recommended for field replacement	Vdcw	= direct current working volts
FF	= flip-flop				
flh	= flat head			W	= watts
flm	= film	OD	= outside diameter	ww	= wirewound
fxd	= fixed	OBD	= order by description	wht	= white
filh	= fillister head	orn	= orange	WIV	= working inverse voltage
		ovh	= oval head		
G	= giga (10^9)	oxd	= oxide	yel	= yellow
Ge	= germanium				
gl	= glass	p	= pico (10^{-12})		
gnd	= ground(ed)	PC	= printed circuit		