OPERATING AND SERVICE MANUAL
13183B
DIGITAL MAGNETIC TAPE UNIT INTERFACE KIT

(FOR THE HP 21MX SERIES COMPUTERS)

HEWLETT-PACKARD
700 71st Avenue, Greeley, Colorado 80634

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Printed-Circuit Assemblies:

13183-60012, Series 2040
13183-60013, Series 2040

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

SECTION IV. THEORY OF OPERATION

SECTION V. MAINTENANCE

SECTION VI. REPLACEABLE PARTS

LIST OF ILLUSTRATIONS

Figure Page

LIST OF TABLES

Table Page

Figure 1.1 HP 13183B Digital Magnetic Tape Unit Interface Kit

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

This manual provides general information, installation, programming, theory of operation, maintenance, replaceable parts information and detailed schematic diagrams for the HP 13183B Digital Magnetic Tape Unit Interface Kit.

1-2. GENERAL DESCRIPTION

The interface kit contains the necessary control and interconnection circuits for connecting HP 7970E Digital Magnetic Tape Units to an HP 21MX-Series Computer. A single interface kit connects at least one master and any combination of master and slave tape units up to a total of four same-speed drives with read-after-write, 1600 cpi, and phase-encoded capability to a computer with direct memory access capability. The control circuits are on two plug-in printed-circuit assemblies (PCA's) that install in the I/O portion of the computer mainframe or in an I/O extender. The cable connects the PCA's to the master tape unit.

NOTE

If the interface kit is to be used in a system under DMA control, the interface PCA must be installed in the computer mainframe unless an I/O extender having DMA capability is available.

1-3. Options

The standard version of the interface kit is used with tape units operating at 45 ips. Option 001 is used with tape units operating at 37.5 ips. Option 002 is used with tape units operating at 25 ips. Option 003 is used with tape units operating at 12.5 ips.

1-4. Interface Kit

The interface kit consists of the following:

a. Mag tape 1 PCA (control), part no. 13183-60012.

b. Mag tape 2 PCA (data), part no. 13183-60013.

c. One 16-foot interconnecting cable, part no. 13183-60014

d. *Operating and Service Manual*, part no. 13183-90901.

1-5. IDENTIFICATION

Hewlett-Packard uses five digits and a letter (00000A) to identify standard interface kits. Options to the standard kit are identified by a three-digit suffix (001, 002, etc.). If the designation of the kit received does not agree with the designation of the title page of this manual, there are differences between the kit received and the kit described in this manual. These differences are explained in manual supplements available at HP Sales and Service Offices (Addresses of these offices are listed at the back of this manual.)

Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the PCA. The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical characteristics of the loaded PCA and the position of the components. The two-digit code identifies the division of Hewlett-Packard that manufactured the PCA. If the series code numbers do not correspond exactly with the code numbers on the title page of this manual, the PCA's differ from those described in this manual. These differences are explained in manual supplements available at the nearest HP Sales and Service Office.

The interconnecting cable is identified by a part number, marked on one of the connectors attached to the cable.

The manual and manual supplements are identified by title, part number, and publication date, marked on the title page of the document.

1-6. Related Documents

This manual must be used with the applicable documents for the computer used as well as the following:

a. *HP 7970B/E Digital Magnetic Tape Unit Service Manual*, part no. 07970-90887.

b. *HP 7970B/E Digital Magnetic Tape Unit Diagram and Parts Manual*, part no. 07970-90886.

c. *HP 13181/183 Diagnostic Manual*, part no. 13181-90095.

d. *HP 13196A Phase-Encode Test Accessory Operating and Service Manual*, part no. 13196-90000.

1-7. Specifications

Table 1-1 presents the specifications for the interface kit.

Table 1-1. Interface Kit Specifications

CHARACTERISTICS	SPECIFICATIONS	CHARACTERISTICS	SPECIFICATIONS
Data Transfer Rates (To/From HP 7970E)		**Power Requirements**†	
		Mag Tape 1	
12.5 ips	20k bytes/second	+4.85	1.1A
25 ips	40k bytes/second	-2.0V	.04A
37.5 ips	60k bytes/second	Mag Tape 2	
45 ips	72k bytes/second	+4.85	1.2A
		-2.0V	.02A
Tape Format	ANSI (1600 cpi PE)		
		Environment	
Input Levels		Operating Temperature	0° to 55°C (+32° to +131°F)
Logic 1	+2.4V minimum		
Logic 0	+0.4V maximum	Humidity	95% at +40°C
Output Levels		**Dimensions (PCA 1 and PCA 2)**	
Logic 1	+2.6V minimum	Height	8-11/16 inches (220.7 mm)
Logic 0	+0.4V maximum	Width	7-3/4 inches (196.8 mm)

†Power drawn from associated computer.

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section provides unpacking, initial inspection, and installation information for the HP 13183B Digital Magnetic Tape Unit Interface Kit. The computer and tape unit(s) should be installed and prepared for operation before installing the interface kit.

2-2. UNPACKING AND INITIAL INSPECTION

If the interface kit is received separately from the computer, inspect the carton containing the kit before opening. If there is external evidence of damage, or if the box rattles, request that the carrier's agent be present when the carton is opened.

Inspect each component of the kit as the parts are unpacked. If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-3. PREPARATION FOR INSTALLATION

2-4. Power Requirements

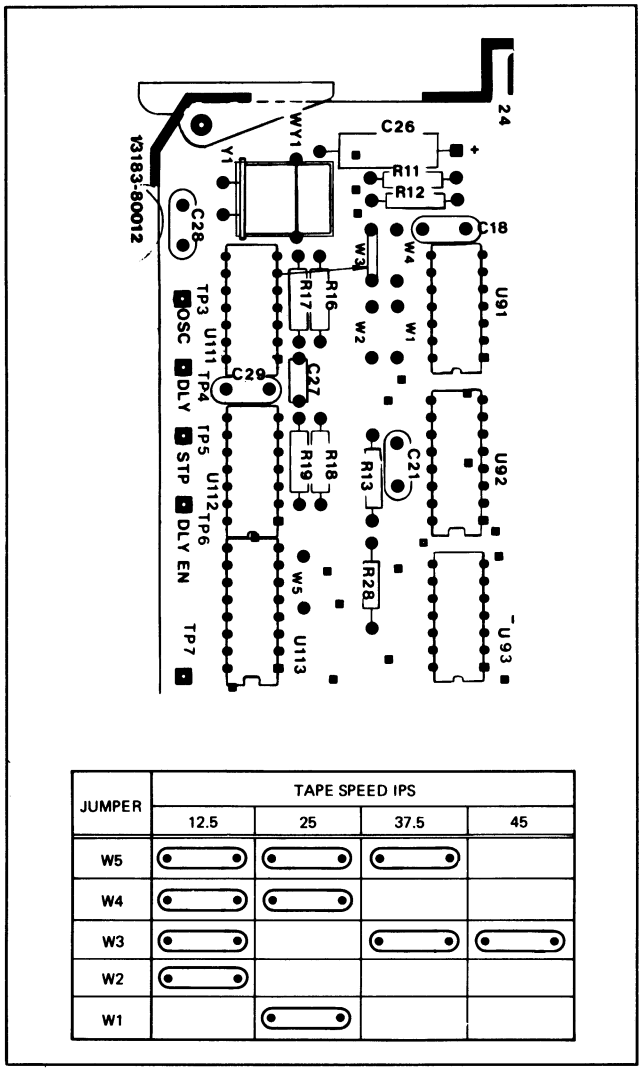
The two interface PCA's obtain power directly from the computer power supply. Before installing the interface PCA's into the computer card cage, determine if additional interface PCA's will overload the computer power supply. Refer to the applicable computer documentation. The two interface PCA's require a total of approximately 2.3 amperes from the +4.85-volt power supply and a total of approximately .06 amperes from the -2.0 volt power supply.

2-5. Tape-Speed Jumpers

The mag tape 1 PCA is equipped with jumpers that modify control circuit timing to permit interfacing of the various tape-speed options of the HP 7970E Digital Magnetic Tape Units. Before installing the interface PCA's, ensure that the jumpers are configured for the appropriate tape speed as shown in figure 2-1. The mag tape 2 PCA has wired jumpers that are all factory-installed and need be removed only for maintenance.

2-6. Cable Routing

Before installing the interface PCA's be sure that the tape unit to be interfaced with the computer is close enough to allow the interconnecting cable to be properly routed and connected.



JUMPER	TAPE SPEED IPS			
	12.5	25	37.5	45
W5	●	●	●	
W4	●	●		
W3	●		●	●
W2	●			
W1		●		

Figure 2-1. Tape Speed Jumper Configurations

2-7. INSTALLATION

Install the tape unit interface kit as follows:

a. Set computer and tape unit POWER switches to OFF.

b. Open the computer for access to I/O PCA slots and install mag tape 1 PCA into the PCA slot corresponding to the desired I/O select code for the interface data channel.

c. Install the mag tape 2 PCA into the next (lower priority, higher select code) slot.

d. Route the interconnecting cable in the computer as shown in figure 2-2.

e. Connect the MAG TAPE 1 cable connector to the mag tape 1 PCA and the MAG TAPE 2 connector to the mag tape 2 PCA.

f. Gain access to the tape unit interconnect facilities and route the interconnecting cable in the tape unit as shown in figure 2-2.

g. Connect read cable connector P3 to the read PCA in the tape unit.

h. Connect write cable connector P4 to the write PCA in the tape unit.

i. Connect control cable connector P5 to the control and status PCA in the tape unit.

2-8. INSTALLATION CHECKOUT

After installing the interface kit, restore power to the computer and tape unit and prepare the system for operation. Refer to the computer and tape unit operating instructions and perform the diagnostic test as described in *13181/183 Diagnostic Manual*, part no. 13183-90095.

2-9. RESHIPMENT

If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest HP Sales and Service Office.

If standard packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorne, N.J.) or equivalent and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

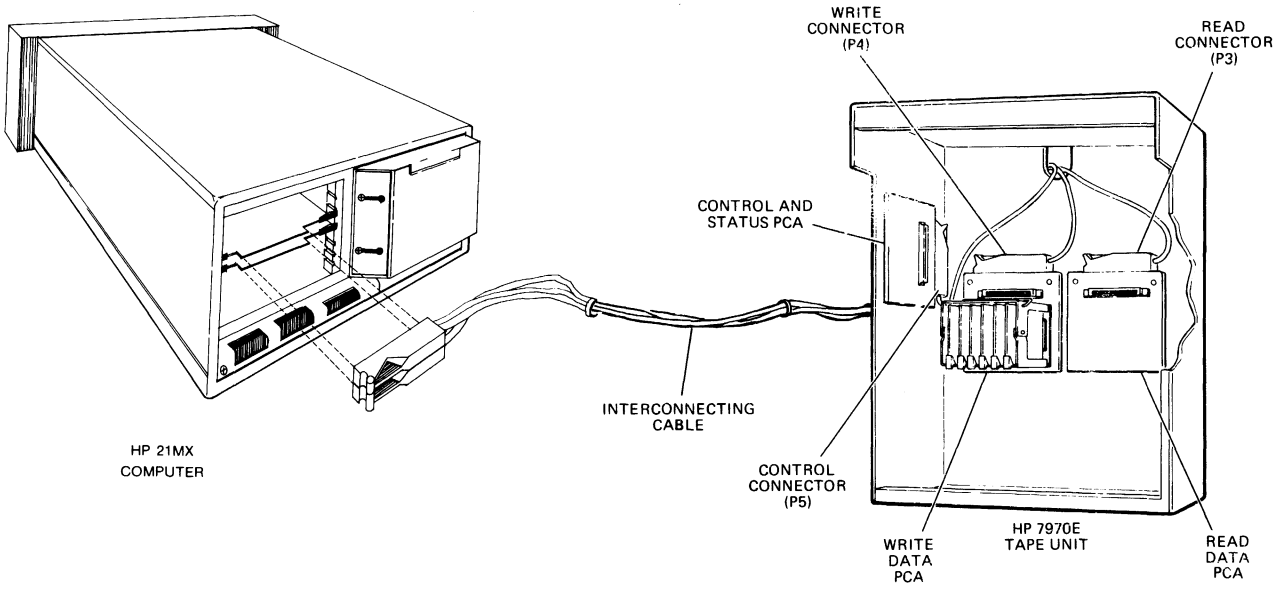


Figure 2-2. Interconnecting Cable Installation

SECTION III
PROGRAMMING

3-1. INTRODUCTION

This section contains programming considerations for systems employing the HP 13183B Digital Magnetic Tape Unit Interface Kit. Included are tape unit characteristics, command and status descriptions , and a typical assembly language program.

3-2. TAPE UNIT CHARACTERISTICS

The interface kit will interface an HP 21MX-Series Computer to as many as four HP 7970E Digital Magnetic Tape Units with the characteristics as shown in table 3-1.

Table 3-1. Tape Unit Characteristics

RECORDING MODE

Phase Encoding (PE) (Industry compatible) 1600 cpi nine track, read-after-write mode

HEAD GUIDE SPACING

Industry compatible

START/STOP TIMES

30 ms (at 12.5 ips)
15 ms (at 25 ips)
10 ms (at 37.5 ips)
8.33 ms (at 45 ips)

START/STOP TAPE TRAVEL

0.187 ± 0.020 inch (4.7625 ± 0.508 mm)

REWIND/FAST FORWARD

160 ips

LOAD POINT SEARCH

20 ips

BEGINNING-OF-TAPE AND END-OF-TAPE REFLECTIVE STRIP DETECTION

Photoelectric, Industry compatible

OPERATING ENVIRONMENT

Ambient Temperature:	+32° to +131°F (0° to 55°C)
Relative Humidity:	20 to 80% (non-condensing)
Altitude:	10,000 ft (3,048 m)

3-3. PHASE-ENCODED TAPE FORMAT

Figure 3-1 presents the physical format of a reel of phase-encoded tape. The format is the same as that for NRZI tape with the addition of an identification burst (IDB) written in track 4 (P channel) followed by a gap of three inches (76.2 mm) written near the beginning of tape (BOT) marker. All other tracks are dc-erased to the reset flux state. The computer program should verify that the tape unit has phase-encoded capability and that the tape is at the BOT. Note that when the tape is at load point and one of the four possible write commands is received, the controller automatically writes an IDB.

For non-DMA applications, the only restriction as to the maximum or minimum length of data that can be written on tape is the physical length of tape. For DMA applications, the minimum record length is two characters and 16,383 characters the maximum. A typical tape may have variable length records separated by a .78 inch nominal (19.8 mm) inter-record gap. Figure 3-2 presents the data block format for a phase-encoded tape.

In phase-encoded format the data block on tape consists of the data preceded by a preamble and followed by a postamble. The preamble consists of 40 logic 0's (in all tracks) followed by a logic 1's character. The postamble consists of a logic 1's character followed by 40 logic 0's. In reverse motion the postamble functions as the preamble and the preamble functions as the postamble. Note that the HP 13183B does not support reverse-read operations.

Figure 3-3 presents the format of the tape mark for phase-encoded tape. Tape marks may be written any number of times on a reel of tape. The tape mark consists of 80 flux reversals in tracks 1, 2, 4, 5, 7, and 8 with the other tracks dc-erased to the reset flux state.

3-4. COMMAND DESCRIPTIONS

All commands are transferred through the computer A- or B-register by an OTA/B instruction addressed to the command channel. Commands other than unit select commands described in the following paragraph are then stored by the interface. An STC,C instruction causes the interface to execute the command. When multiple OTA/B instructions are received before the STC,C instruction, the interface will execute the last OTA/B instruction issued (provided the command is not rejected, as described in paragraph 3-20). Table 3-2 lists the bits that make up the command word. Table 3-3 lists the commands to which the interface will respond. Commands other than those listed will cause improper operation.

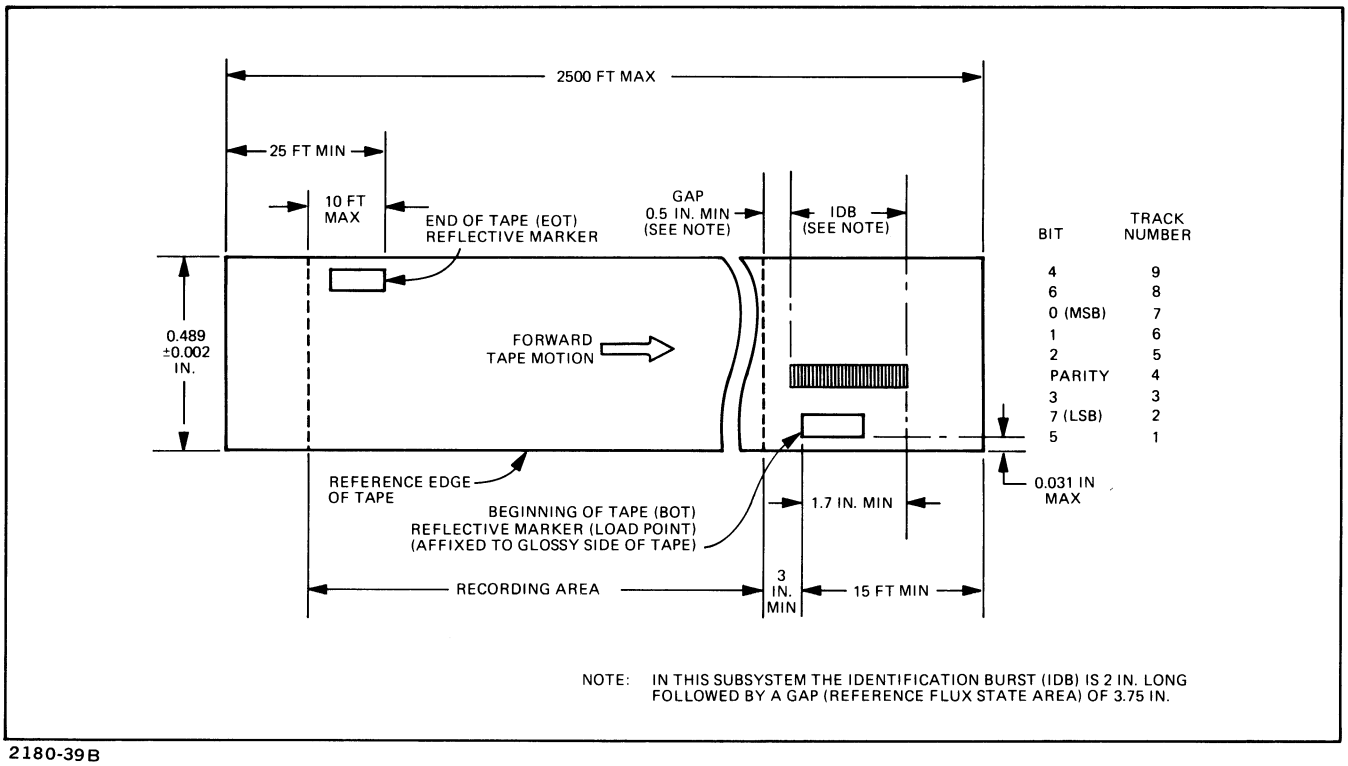


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Figure 3-1. Tape Format for Phase-Encoded Tape

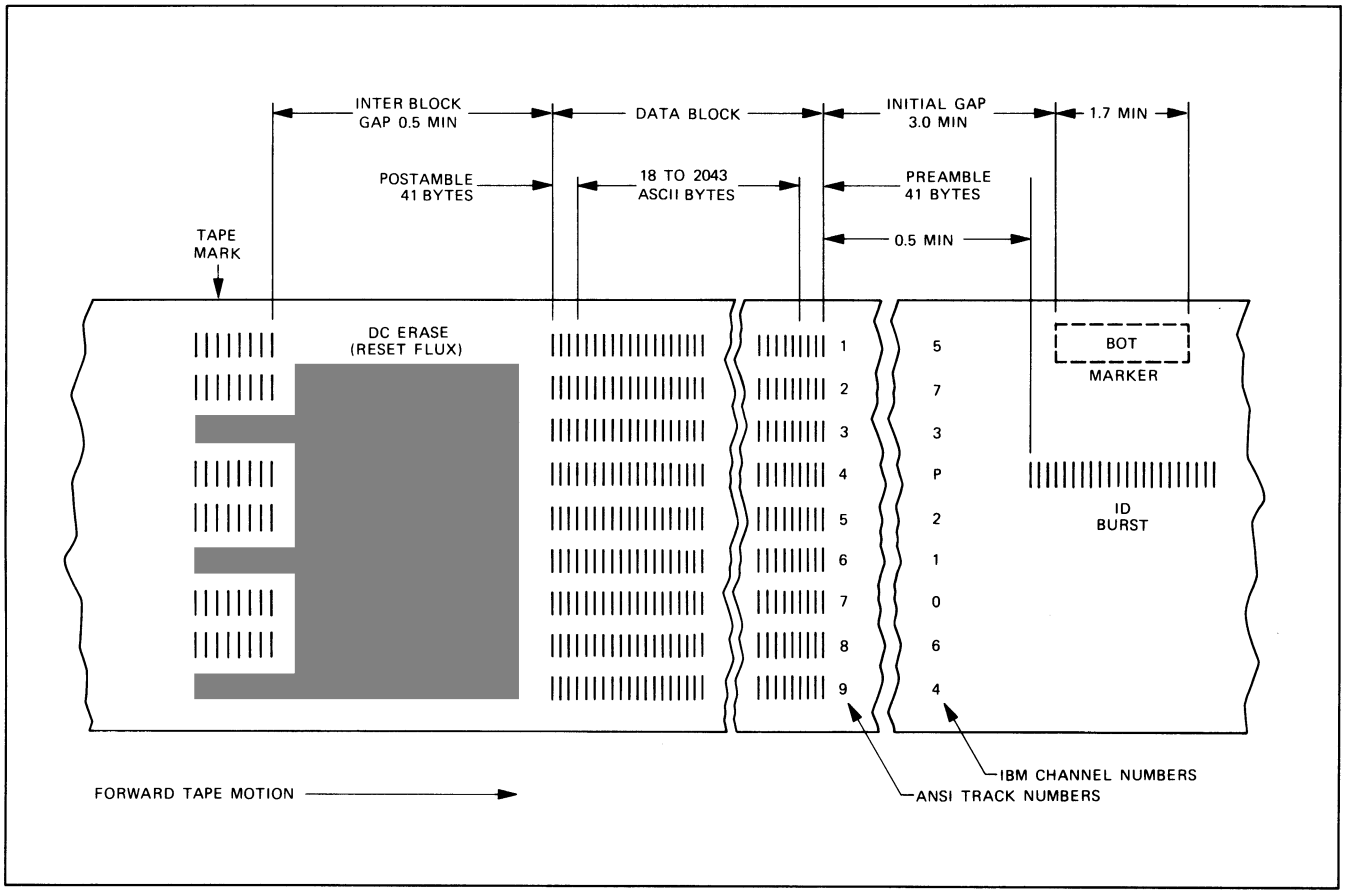

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Figure 3-2. Data Block Format for Phase-Encoded Tape

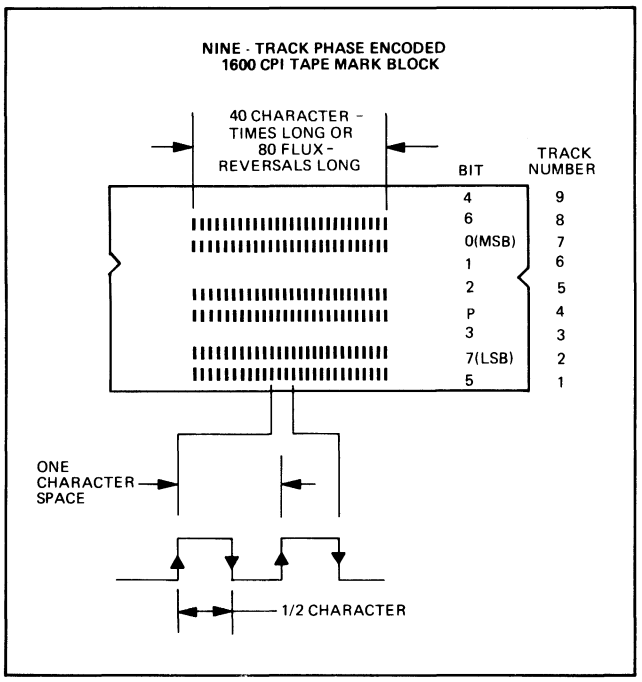

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Figure 3-3. Tape Mark Format for Phase-Encoded Tape

One of the four unit select commands, unless rejected, is executed by an OTA/B instruction in one computer cycle; no STC,C instruction should be issued. Since the unit select commands are executed immediately, they are not buffered nor do they cause an interrupt.

Data is transferred to and from the interface by an OTA/B or LIA/B instruction addressed to the data channel (or under DMA control). The Data Control FF must be set for data transfer to take place. Data transfer to and from the computer is in full 16-bit words; the interface performs all packing and unpacking. (For this reason, written records must be in even numbers of bytes.)

Clearing the Data Control FF during a write operation will initiate writing of a postamble. (The Command Flag FF will be set when the postamble is detected by the read head.) Clearing the Data Control FF during a read operation will inhibit further setting of the Data Flag FF and thus inhibit further data transfer. (Tape motion will continue to the next inter-record gap before the Command Flag FF is set.) The Command Control FF must be set to allow interrupts.

The Data Flag FF will be set to indicate that data transfer can take place. The Command Flag FF will be set by the interface to indicate that all operations (except rewind) requiring tape motion are complete, or that a clear operation is complete. For rewind operation, the Command Flag FF is set when rewind commences to release the tape unit while the tape is being rewound. In all cases, however, no time is allowed for actual tape motion to stop.

Because of this characteristic, successive Read or Write commands may be issued (before tape motion has stopped) to increase system efficiency when reading or writing a long series of records. Table 3-4 lists the maximum effective transfer rates for various record sizes and tape speeds when issuing successive read or write commands (assuming uniform tape speed and no slowdown because of software overhead).

To ensure proper tape formatting, a complete stop between records is required when writing under the following conditions:

a. If the present operation involves writing and the next operation does not.

Table 3-2. Command Word Bits

BIT	FUNCTION
0	Motion
1	Forward
2	Gap/Off-Line
3	Write/Clear
4	Not Used
5	Reverse
6	Rewind/Clear
7	File
8	Change Select
9	Select 0
10	Select 1
11	Select 2
12	Select 3

Note: Bits 13 thru 15 are not used in the command word.

Table 3-3. Computer-to-Interface Commands

COMMAND	MNEMONIC	OCTAL CODE
Clear	CLR	00110
Select 0	SL0	01400
Select 1	SL1	02400
Select 2	SL2	04400
Select 3	SL3	10400
Write One Record	WRT	00031
Write File Mark	WFM	00211
Gap and Write File Mark	GFM	00215
Gap	GAP	00015
Read One Record	READ	00023
Forward Space Record	FSR	00003
Backspace Record	BSR	00041
Forward Space File	FSF	00203
Backspace File	BSF	00241
Rewind	REW	00101
Rewind/Off-Line	RWO	00105

Table 3-4. Maximum Effective Transfer Rates (Kilobytes/Second)

RECORD LENGTH (CHARACTERS)	TAPE SPEED (IPS)			
	12.5	25	37.5	45
25	0.4	0.8	1.2	1.4
50	0.8	1.5	2.3	2.7
100	1.5	2.9	4.4	5.2
200	2.7	5.4	8.1	9.7
400	4.8	9.5	14.3	17.2
800	7.7	15.4	23.1	27.7
1600	11.1	22.2	33.3	40.0
3200	14.3	28.6	42.9	51.4
6400	16.7	33.3	50.0	60.0

b. If the present operation involves backspacing tape and the next operation does not.

c. If a successive OTA/B instruction issues a command under either of these conditions, the command will be stored by the interface. The subsequent STC,C instruction will also be stored until the tape stops, at which time the stored command will be executed. Interface busy status will be set when the STC,C instruction is issued. Any subsequent commands (except Clear) will set command rejected status; therefore, a subsequent command should not be issued until the Command Flag FF is set to indicate that previous operation has been completed.

3-5. Clear (CLR)

The CLR command sets the interface to its ready state. Any tape unit operation (except rewind) is terminated and interface status bits 1, 3, 4, 7, 8, 11, and 12 are cleared. A rewind operation in progress is completed. The CLR command is also initiated by a computer Preset or POPIO signal.

The Command Flag FF is normally set almost immediately after the STC,C which initiates the CLR command. This allows the next command to be output with minimum waiting. The time required to set the Command Flag FF does not exceed 36 ms at 12.5 ips, 18 ms at 25 ips, 12 ms at 37.5 ips, or 10 ms at 45 ips.

3-6. Select 0, 1, 2, and 3 (SL0 1, 2, 3)

The SL0, 1, 2, 3 commands select the designated tape unit for subsequent computer commands. The select command must precede any other commands to the tape unit.

3-7 Write One Record (WRT)

The WRT command initiates forward tape motion and sets the Data Flag FF when the tape has reached proper speed and the preamble has been written. The 16-bit computer words are unpacked by the interface and written as two 8-bit bytes each time the Data Flag FF is set, until the Data Control FF is cleared. The most significant eight bits are written first; the least significant eight bits are written second.

Once the Data Flag FF is set, the computer must output a word in one byte period. (One byte period = 50 μs at 12.5 ips, 25 μs at 25 ips, 16.66 μs at 37.5 ips, and 13.9 μs at 45 ips.) The timing error status bits (refer to table 3-5) will be set if a word is not presented in one byte period. The Data Control FF must be cleared within one byte period after the final data word is output. The interface will finish writing the final word and write a postamble to the record. If the Data Control FF is cleared after a Write command has been issued but before any data is written, 40 zeros will be written in all tape tracks and the data error status bit will be set. The Command Flag FF will be set when the read-after-write check has been completed.

If a Write One Record command is issued when the tape is at load point, an identification burst, consisting of alternate

Table 3-5. Status Word Bits

BIT	STATUS
0	Tape Unit Off-Line
1	Data Error (when set alone) Timing Error (when set with bit 4).
2	File Protected (no write enable ring)
3	Command Rejected
4	Timing Error (bit 1 also set)
5	End-of-Tape
6	Load Point (Beginning of Tape)
7	End-of-File
8	Interface Busy
9	Tape Unit Busy
10	Rewinding
11	Odd Number of Bytes
12	Single Track Error
13	Selected Tape Unit, Least Significant Bit
14	Selected Tape Unit, Most Significant Bit
15	1600-CPI Density

ones and zeros, will be written in track 4 (ANSI) while all other tracks are erased to the reset flux state. The interface will automatically execute the Write One Record command when the ID burst has been completed.

3-8. Write File Mark (WFM)

The WFM command writes 40 zeros in (ANSI) tracks 1, 2, 4, 5, 7, and 8, and dc-erases tracks 3, 6, and 9. The Command Flag FF is set when a file mark is read. The data error status bit is valid for this operation.

If a WFM command is issued when the tape is at load point, an ID burst will be written in track 4 (ANSI) while all other tracks are dc-erased. The interface will automatically execute the WFM command when the ID burst has been completed.

3-9. Gap And Write File Mark (GFM)

The GFM command initiates the same operation as for WFM (refer to paragraph 3-8) except that 3 inches of tape are erased before the file mark is written. The ID burst is automatically written when this command is issued at load point, and then the file mark is written.

3-10. Gap (GAP)

The GAP command erases 3 inches of tape. Any condition which causes detectable non-erasure of the tape will set the data error status bit. If a Gap command is issued when the tape is at load point, an ID burst will be written in track 4 (ANSI) while all other tracks are dc-erased. After the ID burst is written, 3 inches of tape are erased, the tape stops, and the Command Flag FF is set.

3-11. Read One Record (READ)

The READ command reads tape forward until an inter-record gap is detected. The first of each pair of data bytes is placed in the high-order eight bits of the computer word; the second byte is placed in the low-order eight bits. A byte with even parity will set the data error status bit. Single-track errors are corrected by the tape unit and are also flagged during read operations. Multi-track errors will cause the data error status bit to be set. If the record read is a tape mark, no data is transferred.

The Data Flag FF is set each time the second byte of a pair is read. Failure to respond to the flag within one byte period will cause the timing error status bits to be set. When reading less than a full record, the Data Control FF should be cleared to end the data transfer. This technique will prevent the Data Flag FF from being set for the remainder of the tape record and thus will prevent a timing error. Tape motion will continue to the inter-record gap before the Command Flag FF is set.

The Data Control FF should also be cleared each time the Command Flag FF is set. This technique will prevent setting the Data Flag FF during positioning operations that follow the reading of records that are shorter than the record requested. When reading records containing an odd number of bytes, the odd byte status bit is set, as is the Data Flag FF, when the final odd byte is read . The final odd byte is placed in the high-order eight bits, and the low-order eight bits contain the lower half of the preceding word. For this reason, the interface status word should be transferred to the computer and examined for odd byte status after each read operation.

3-12. Forward Space Record And Backspace Record (FSR,BSR)

The FSR and BSR commands cause the tape unit to space forward or backward over a record and stop at the next inter-record gap. Data is not transferred, but the data error status bit will be set if a multi-track error is detected. Odd byte status will be set if the record contains an odd number of bytes. A BSR command will be terminated if the load point is sensed during execution, but the command rejected, (CR) status bit is not set. (Refer to paragraph 3-20d.) Note that the CR bit is set only when the tape is already at load point when a BSR is given.

3-13. Forward Space File And Backspace File (FSF,BSF)

The FSF and BSF commands cause the tape unit to space forward or backward until a file mark is detected. Data is not transferred but the data status bit is set if a multi-track error is detected. The odd byte status will be set if an odd number byte count occurs (the file mark is not included in the byte count). A Forward Space File command will be interpreted as a Forward Space Record command if an end-of-tape mark is sensed during execution; i.e., the tape will stop at the next inter-record gap rather than after the file mark. A BSF command is terminated if the load point is sensed during execution.

3-14. Rewind (REW)

The REW command rewinds and positions the tape at load point. The interface busy status bit will be reset within 6.4 ms (at 12.5 ips, 1 ms at 25 ips, 0.67 ms at 37.5 ips, and 0.56 ms at 45 ips) after the STC,C instruction that initiated the REW command. As a result, the Command Flag FF will be set, interface busy status will be cleared, and the interface will be disconnected from the tape unit without waiting for completion of the REW operation. Although the Command Flag FF is set, the selected tape unit will not accept any motion commands while still rewinding. Any attempt to output a motion command (OTA/B) will set the command rejected status bit. Any attempt to execute a rejected command (STC,C) will be ignored.

However, any one of the four select commands or the Clear command may be output as soon as the Command Flag FF is set. If the selected tape unit is ready, normal operation may begin. If an REW command is issued and the tape is at load point, the command will be ignored. The interface will still require a maximum of 6.4 ms before clearing the interface busy status bit and setting the Command Flag FF.

3-15. Rewind/Off-Line (RWO)

The RWO command initiates the same operation as a Rewind command except that the tape unit is switched to off-line status. If the RWO command is issued when the tape is at load point; the rewind portion will be ignored and the tape unit will be set off-line. Operator intervention is required to restore on-line status before another command can be executed by the tape unit.

3-16. STATUS BIT DESCRIPTIONS

Status information is transferred to the computer A- or B-register by either an LIA/B or MIA/B instruction addressed to the command channel. The status word may be transferred any time the tape unit is selected. (Odd-byte, single-track-error, file-mark, and data-error status are only valid when a command has been completed.) The status word only applies to the currently-selected tape unit. Individual status bits are listed in table 3-5.

3-17. Tape Unit Off-Line

Tape unit off-line status (bit 0) is set when the selected tape unit has not been placed on-line or when the tape unit selected by the interface is not electrically connected to the interface.

3-18. Data/Timing Error

Data error status (bit 1) is set for controller hardware errors or if the tape unit detects a multi-track error during any motion command except Rewind or Rewind/Off-Line. Data error status is also set if the tape unit corrects a single-track error during a read-after-write check. Data error status is valid only after the Command Flag FF has been set, and thus does not indicate the data byte in error.

Timing error status (bit 1 and bit 4) is set if the setting of the Data Flag FF during a data transfer operation is not acknowledged within one byte period.

3-19. File Protected

File protected status (bit 2) is set if there is no write enable ring on the supply reel of the selected tape unit.

3-20. Command Rejected

Command rejected status (bit 3) is set if any of the following conditions exist:

a. Any command requiring tape motion is issued when the interface or selected tape unit is busy. (Interface busy or tape unit busy status will be set.)

b. Any Write Command is issued when the supply reel on the selected tape unit does not have a write enable ring. (File protected status will be set.)

c. Any Select command is issued when the interface is busy. (Interface busy status will be set.)

d. A Backspace Record or Backspace File command is issued when the tape is at load point. (Load point status will be set.) Command reject will be set under this condition if the tape is at load point when the OTA/B instruction is issued. If an otherwise executable Backspace Record or Backspace File command is in process when the load point is sensed, the Command Flag FF is set and the operation is terminated without setting the command rejected status bit.

Due to the fact the command rejected status bit is set when the the OTA/B instruction is issued, the status word should be transferred to the computer and tested for command rejected status before the subsequent STC,C instruction is issued. Select commands, which are normally initiated by an OTA/B instruction, will be ignored if they set the command rejected status bit. Any STC,C instructions will be ignored if issued when the command rejected status bit is set. The Command Flag FF will not be set. The command rejected status will be cleared when the next executable command is issued by an OTA/B instruction. A Clear command will never set command rejected status.

3-21. Timing Error

Timing error status (bit 1 and bit 4) is set if the Data FF is not acknowledged within one byte period.

3-22. End-Of-Tape

End-of-tape status (bit 5) is set when the end-of-tape reflective marker is sensed during a forward motion command and remains set until a Rewind, Rewind/Off-Line or Backspace command positions the end-of-tape reflective marker, behind the EOT sensor.

3-23. Load Point

Load point status (bit 6) is set whenever the beginning-of-tape reflective marker is sensed by the tape unit.

3-24. End-Of-File

End-of-file status (bit 7) is set when a file mark is detected during write, read, forward spacing, or backspacing operations.

3-25. Interface Busy

Interface busy status (bit 8) is set when the interface is executing a command. When interface busy status is cleared, the interface will accept another command (except after a Rewind or Rewind/Off-Line command as described in paragraph 3-15).

3-26. Tape Unit Busy

Tape unit busy status (bit 9) is set if any of the following conditions exist:

a. Selected tape unit is off-line.

b. Selected tape unit is rewinding.

c. Selected tape unit is executing initial load sequence, or positioning to load point following a rewind operation.

d. Selected tape unit is not connected to interface.

3-27. Rewinding

Rewinding status (bit 10) is set when the selected tape unit is rewinding or positioning to load point after rewinding. Rewinding status is only set if tape unit is on-line. Rewinding status is cleared following a Rewind/Off-Line command.

3-28. Odd Number Of Bytes

Odd number of bytes status (bit 11) is set if the previous record read or spaced over contains an odd number of bytes. Odd byte status is valid only for record operations and only after the Command Flag FF is set.

3-29. Selected Tape Unit

Selected tape unit status (least significant bit, bit 13; most significant bit, bit 14) identifies the currently selected tape unit as follows:

TAPE UNIT	BIT 14	BIT 13
0	0	0
1	0	1
2	1	0
3	1	1

Selected tape unit status is valid only after a Select command has been initiated by an OTA/B instruction, after power turn-on.

3-30. 1600 CPI Density

The 1600-cpi density status (bit 15) is continuously set to indicate character density of the currently selected tape unit.

3-31. Typical Program

Table 3-6 is a typical assembly language program that will transfer data to and from the tape unit under DMA control.

Note

To ensure reliable transfer of data, software must ensure that the maximum time between setting of the Data Flag FF and the corresponding OTA/B or LIA/B instruction does not exceed 10 microseconds.

Table 3-6. Typical Assembly Language Program Using DMA

```
READ1 NOP             ENTRY POINT.
      LDA BUFLN       GET WORD COUNT.
      CMA,CCE,INA     MAKE IT NEGATIVE, SET -E- FOR INPUT.
      STC 2           SET DMA TO ACCEPT WORD COUNT.
      OTA 2           SEND IT TO DMA WORD COUNT REGISTER.
      LDA BUFAD       GET BUFFER ADDRESS.
      RAL,ERA         SET DMA I/O BIT (BIT 15) FOR INPUT.
      CLC 2           SET DMA TO ACCEPT BUFFER ADDRESS.
      OTA 2           SEND IT TO DMA ADDRESS REGISTER.
      LDA DMACW       GET DMA CONTROL WORD -- CLEARS
*                     DATA CHANNEL CONTROL BIT AT END
*                     OF DATA TRANSFER.
      OTA 6           SEND IT TO DMA.
      LDA READ        GET READ ONE RECORD COMMAND.
REJCT OTA CMND        SEND IT TO CONTROLLER.
      LIB CMND        GET CONTROLLER STATUS.
      RBR,RBR         SHIFT COMMAND REJECT BIT TO Ø.
      RBR,SLB         IF COMMAND IS REJECTED,
      JMP REJCT         KEEP TRYING.
      STC CMND,C      COMMAND O.K., START TAPE.
      STC DATA,C      TURN ON DATA CHANNEL.
      STC 6,C         START DMA.
      SFS CMND        READ OPERATION COMPLETE?
      JMP *-1         NO, WAIT.
      CLC DATA,C      YES, CLEAR DATA CHANNEL CONTROL
*                     IN CASE PHYSICAL RECORD LENGTH
*                     ON TAPE WAS SHORTER THAN THAT
*                     REQUESTED BY DMA (I.E., DMA DID
*                     NOT COMPLETE DATA TRANSFER, AND
*                     THEREFORE DID NOT CLEAR DATA
*                     CHANNEL CONTROL BIT).
      LIA CMND        GET FINAL STATUS.
      JMP READ1, I    RETURN TO CALLING PROGRAM.
READ  OCT 23          READ ONE RECORD COMMAND CODE.

WRITE NOP             ENTRY POINT.
      LDA BUFLN       GET WORD COUNT.
      CMA,INA         MAKE IT NEGATIVE.
      STC 2           SET DMA TO ACCEPT WORD COUNT.
      OTA 2           SEND IT TO DMA WORD COUNT REGISTER.
      LDA BUFAD       GET BUFFER ADDRESS.
      CLC 2           SET DMA TO ACCEPT BUFFER ADDRESS.
      OTA 2           SEND IT TO DMA ADDRESS REGISTER.
      LDA DMACW       GET DMA CONTROL WORD -- CLEARS
*                     DATA CHANNEL CONTROL BIT AT END
*                     OF DATA TRANSFER.
      OTA 6           SEND IT TO DMA.
      LDA WRT         GET WRITE ONE RECORD COMMAND.
REJCT OTA CMND        SEND IT TO CONTROLLER.
      LIB CMND        GET CONTROLLER STATUS.
      RBR,RBR         SHIFT COMMAND REJECT BIT TO Ø.
      RBR,SLB         IF COMMAND IS REJECTED,
      JMP REJCT         KEEP TRYING.
      STC CMND,C      COMMAND O.K., START TAPE.
      STC DATA,C      TURN ON DATA CHANNEL.
      STC 6,C         START DMA.
      SFS CMND        WRITE OPERATION COMPLETE?
      JMP *-1         NO, WAIT.
      LIA CMND        YES, GET FINAL STATUS.
      JMP WRITE,I     RETURN TO CALLING PROGRAM.

*
BUFLN DEC 1Ø          BUFFER LENGTH (WORDS).
BUFAD DEF TABLE       BUFFER ADDRESS.
TABLE DEC 1,2,3,4,5,6,7,8,9,1Ø
DATA  EQU 1Ø8         DATA CHANNEL ADDRESS DEFINITION.
CMND  EQU DATA+1      COMMAND CHANNEL ADDRESS DEFINITION.
DMACW ABS 2ØØØØB+DATA   DMA CONTROL WORD, CONFIGURED
*                       FOR DATA CHANNEL.
WRT   OCT 31          WRITE ONE RECORD COMMAND CODE.
```

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION

This section provides the theory of operation for the HP 13183B Digital Magnetic Tape Unit Interface Kit. The interaction of the interface unit and the computer is described on the functional level by hardware-oriented flowcharts and block diagram discussions. For a detailed description of the computer I/O section refer to the applicable computer documentation.

Detailed schematic diagrams for the interface kit are located in section V of this manual. Figure 5-2 is the schematic of mag tape 1 PCA. Figure 5-3 is the schematic of mag tape 2 PCA.

4-2. INTERFACE DESCRIPTION

Figure 4-1 presents the interface block diagram for the HP 13183B Interface Kit. Figure 5-5 presents the detailed interface diagram for the interface kit. Mag tape 1 PCA provides most of the control and timing functions for the interface and the tape unit. This PCA also receives and decodes tape commands from the computer via the IOB lines. Status of the tape unit and controller and interrupt signals are sent to the computer via the IOB lines. Mag tape 1 also provides status and timing signals to mag tape 2. The HP 7970E Tape Unit is provided with commands and timing signals by mag tape 1 PCA. Status signals from the tape unit are transferred to mag tape 1 PCA at the end of each operation.

Mag tape 2 PCA provides the data transfer paths for the interface. During write operations mag tape 2 PCA unpacks 16-bit words from the computer and transfers them to the tape unit as two 8-bit bytes. During read operations mag tape 2 packs data bytes from the tape unit into 16-bit words. These words are transferred to the computer under control of mag tape 1. Each time two 8-bit bytes have been read from the tape unit, a Set Flag Buffer (SFB) signal is sent to mag tape 1 PCA. Mag tape 1 PCA then requests the computer to accept the data.

4-3. FUNCTIONAL DESCRIPTION

The following paragraphs present a discussion of mag tape 1 PCA and mag tape 2 PCA at the block diagram level. Associated with each block diagram is a flowchart describing the functional operation of the PCA.

4-4. Mag Tape 1 PCA

Figure 4-2 presents the block diagram of mag tape 1 PCA. Associated with the block diagram is the interface-to-computer flowchart, figure 4-3. The detailed schematic diagram for mag tape 1 PCA is presented in figure 5-2. Mag tape 1 PCA provides the timing and control functions for the interface kit. This PCA controls the transfer of commands to the tape unit, the transfer of data to and from the tape unit, and provides the timing signals for the interface.

When two bytes of data have been read, the data flag logic requests a transfer to the computer or DMA PCA by asserting the Service Request (SRQ) signal. The data flag logic is set by Set Flag Buffer (SFB) signal from mag tape 2 PCA. During write operations the data flag logic is set to request data from the computer. The DMA generates CLF (data) to acknowledge SRQ and clear the data flag logic.

The command flag logic indicates to the computer that an operation requiring tape motion or a clear operation has been completed. The command flag logic also indicates that a rewind operation has been started.

The data control logic is set by the Set Control (STC) command from the computer to the data channel to enable data transfers to and from the tape unit. The STC should be followed by a, C (clear flag). The data control logic is cleared by the Clear Control (CLC) or Control Reset (CRS) signal from the computer. Clearing the data control logic inhibits data transfers, the Interrupt Request Lower Select Code (IRQL) signal and Flag Signal Lower Select Code (FLGL) signal. When the data control logic is cleared during a write operation the postamble will be written on tape. The Data Control (DCL) signal informs the logic on the interface kit that a data transfer is occurring.

The command control logic is set by an STC command from the computer to the command channel to initiate operation of the interface . When the operation has been completed, the Priority Low (PRL) signal inhibits the interrupting by lower priority devices, the Command Flag FF is set, and an interrupt is sent to the computer. The computer returns the Interrupt Acknowledge (IAK) signal to reset the command control logic. The Interrupt Request Higher Select Code (IRQH) signal is sent to the computer to provide addressing and an interrupt request.

The skip flag test logic allows the computer to test the condition of the Data Flag flip-flop or Command Flag flip-flop in the interface. If the flag is in the condition tested for, an SKF signal is returned to the computer, and the computer skips the next instruction.

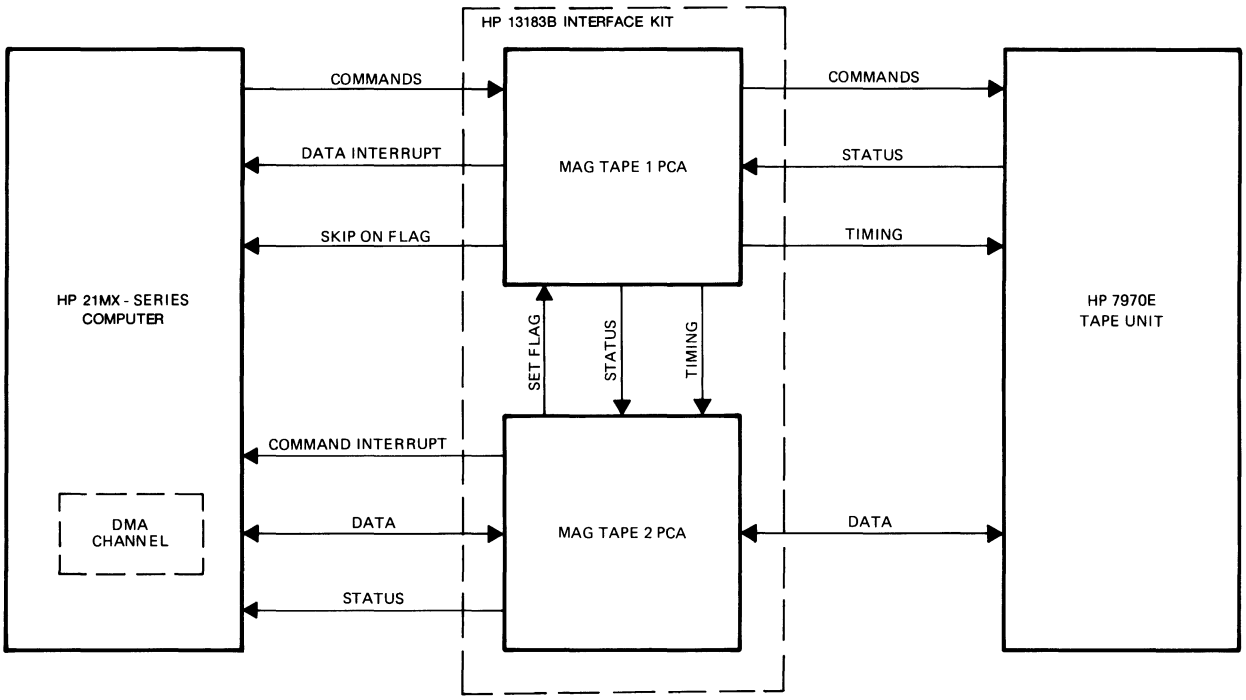


Figure 4-1. Interface Block Diagram

The control bits buffer stores the command information sent from the computer via the IOB lines. The outputs of the buffer select the tape unit or set the appropriate command and motion control flip-flops.

The timing and delay counters provide the interface with Master Clock Pulses (MCP's), Control Clock Pulses (CCP's), Spacing Clock Pulses (SCP's), Even-Odd Clock Pulses (EOC's), and specific time delays. (See figure 4-4.) The time delays are as follows:

a. 16 SCP delay at the end of an operation to allow tape motion to stop. (Command Flag Buffer FF is set at the beginning of this delay.)

b. 20 SCP delay at the beginning of write operations, except GAP and GFM and operations starting at load point, to allow tape to accelerate up to speed.

c. 96 SCP delay for End-of-Block (EOB) detection disable when an operation begins at load point.

d. 120 SCP delay for writing a three-inch gap on tape.

e. 288 SCP delay used for insertion of ID burst.

The operation Control flip-flops store the operation to be performed until the operation has been completed. When an operation is being performed, the Busy flip-flop is available to the computer and to the command reject logic to control the acceptance or rejection of the next command.

The Motion Control flip-flops store the forward, backward, or rewind command from the control bits buffer. At the end of an operation, the Motion Control flip-flops are cleared by the STOP signal.

The reject logic returns reject status to the computer when the computer sends a command to the interface that it cannot execute. Commands which will be rejected include: a write operation with no write enable ring installed, a backward motion command while the tape is at loadpoint, commands requiring tape motion when the interface or the tape unit is busy, or unit select commands when the interface is busy. The next executable command resets the reject status logic.

Normally, successive read, space or write commands can be executed without waiting for tape motion to stop. For the following two conditions, however, tape motion must be stopped before the next command is executed:

a. If a Write command is followed by a Backspace command, tape motion must be allowed to stop to ensure correct formatting of the IRG.

b. If a Backspace command is followed by a Write command, the backspace motion must be allowed to stop and the tape must be allowed to accelerate up to speed in the forward direction before the Write command is allowed to transfer data. The Set Control Inhibit (STC INH) delay is provided by the timing and delay counters to delay the execution of the next command when either of the two above conditions exist.

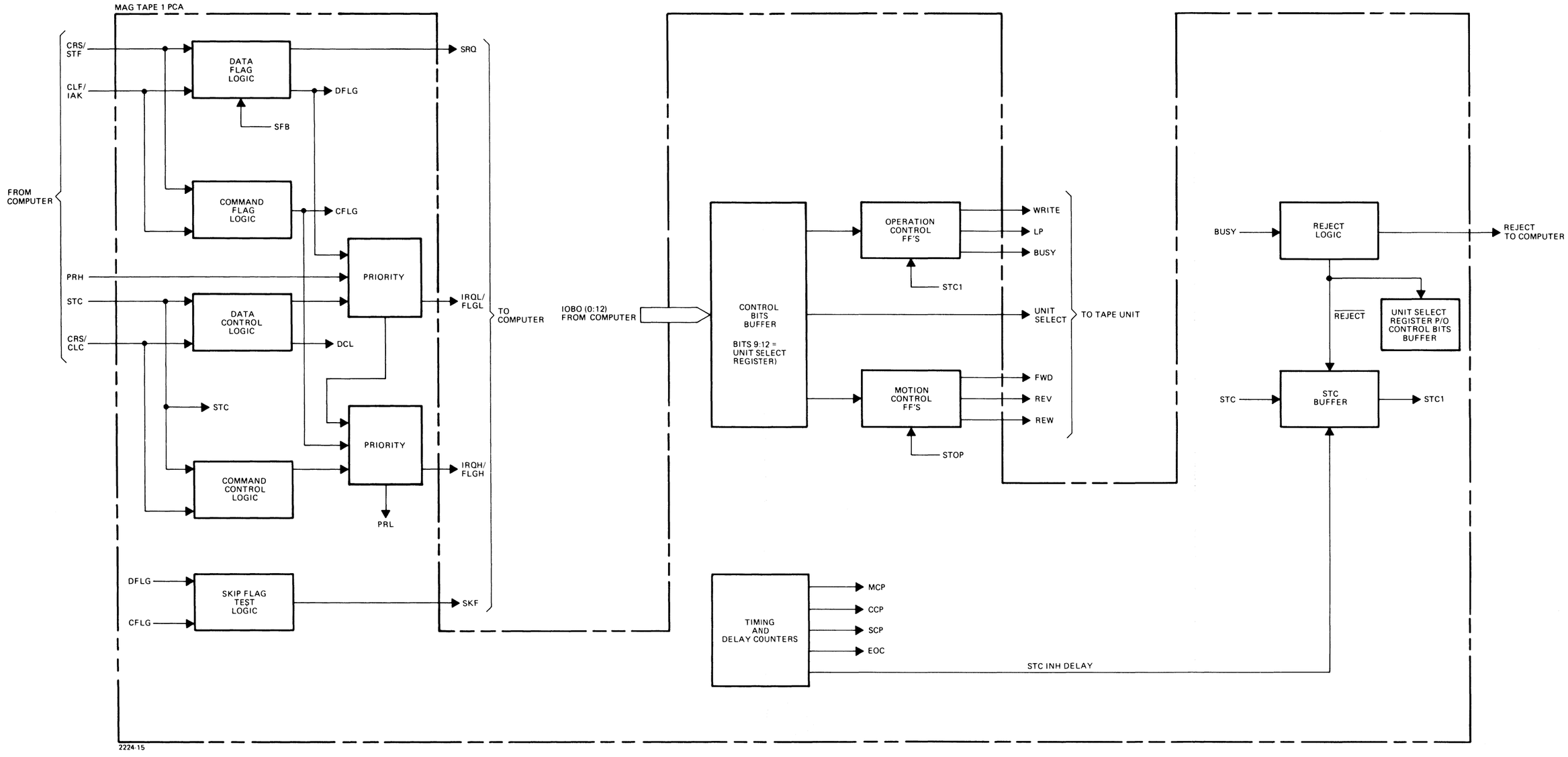
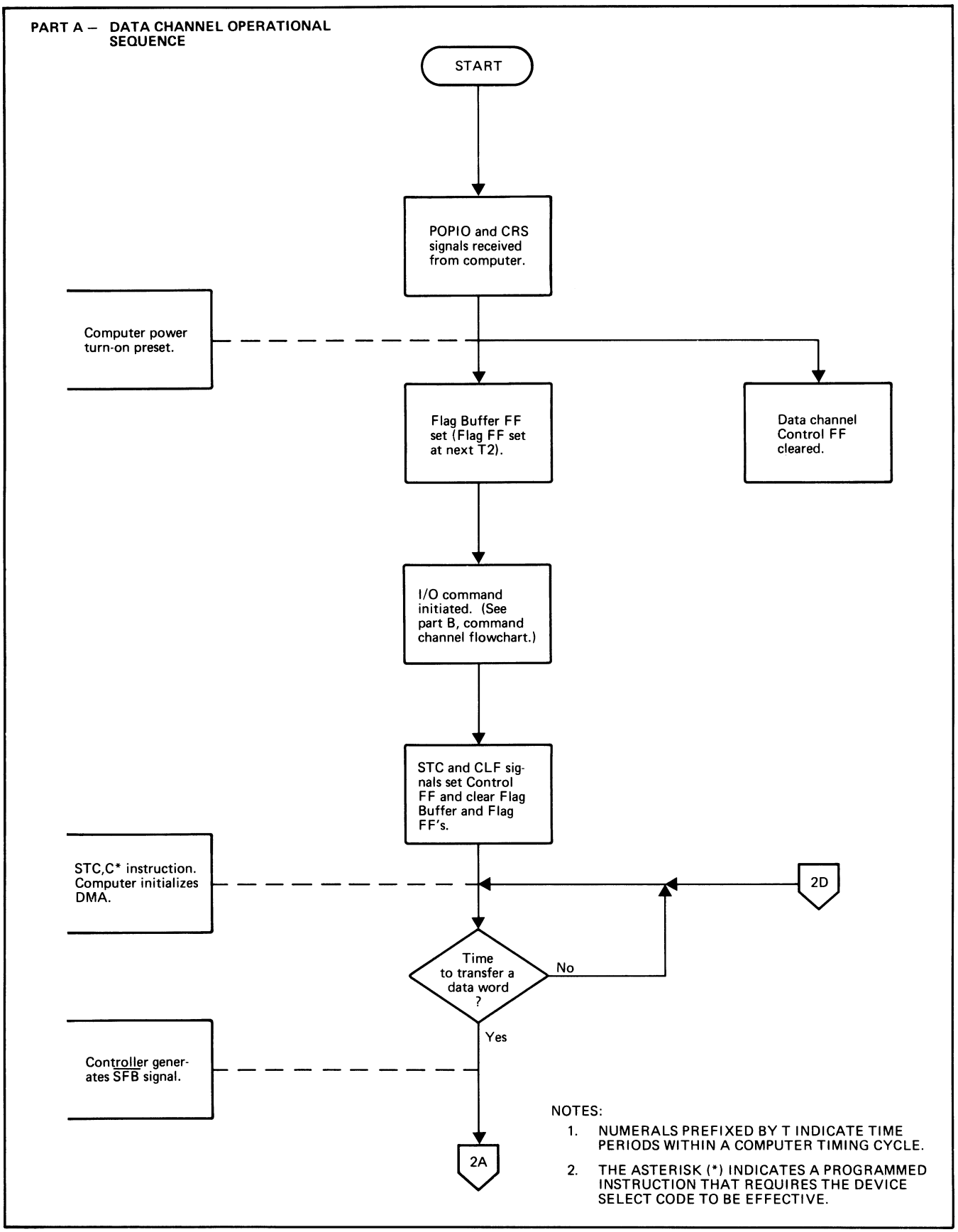
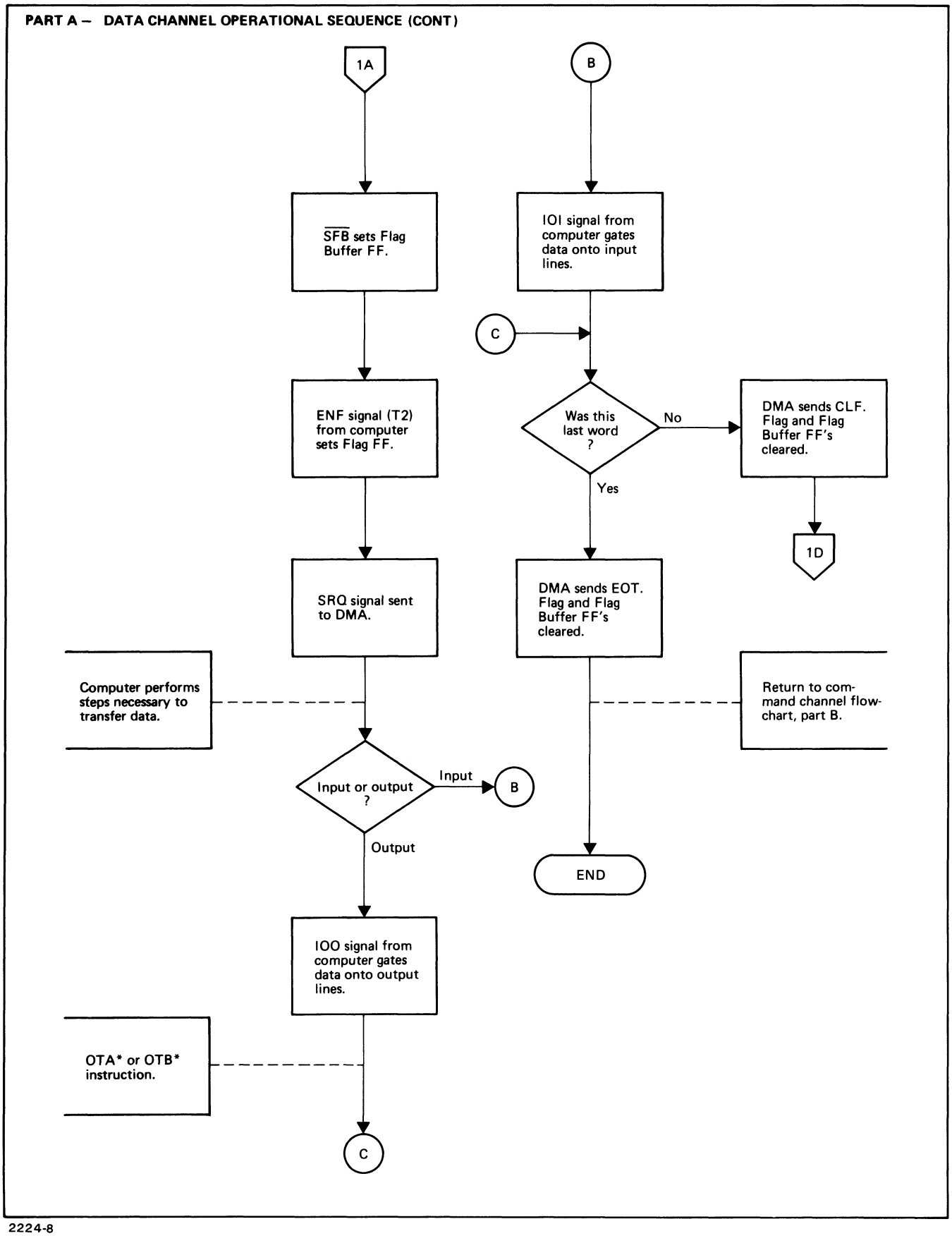


Figure 4-2. Mag Tape 1 PCA Block Diagram



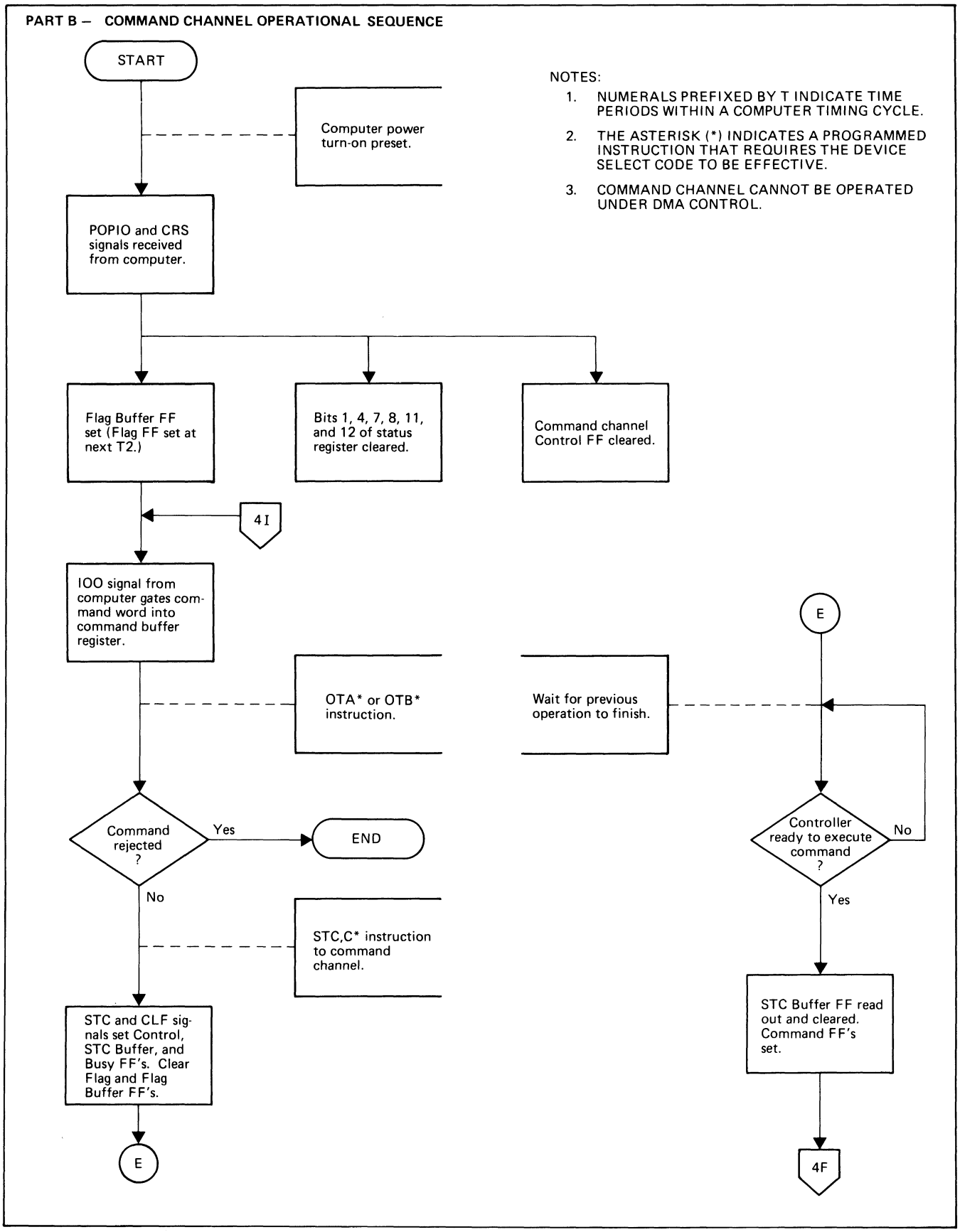
2224-5

Figure 4-3. Data and Command Channels Flowchart (Sheet 1 of 5)



2224-8

Figure 4-3. Data and Command Channels Flowchart (Sheet 2 of 5)



2224-36

Figure 4-3. Data and Command Channels Flowchart (Sheet 3 of 5)

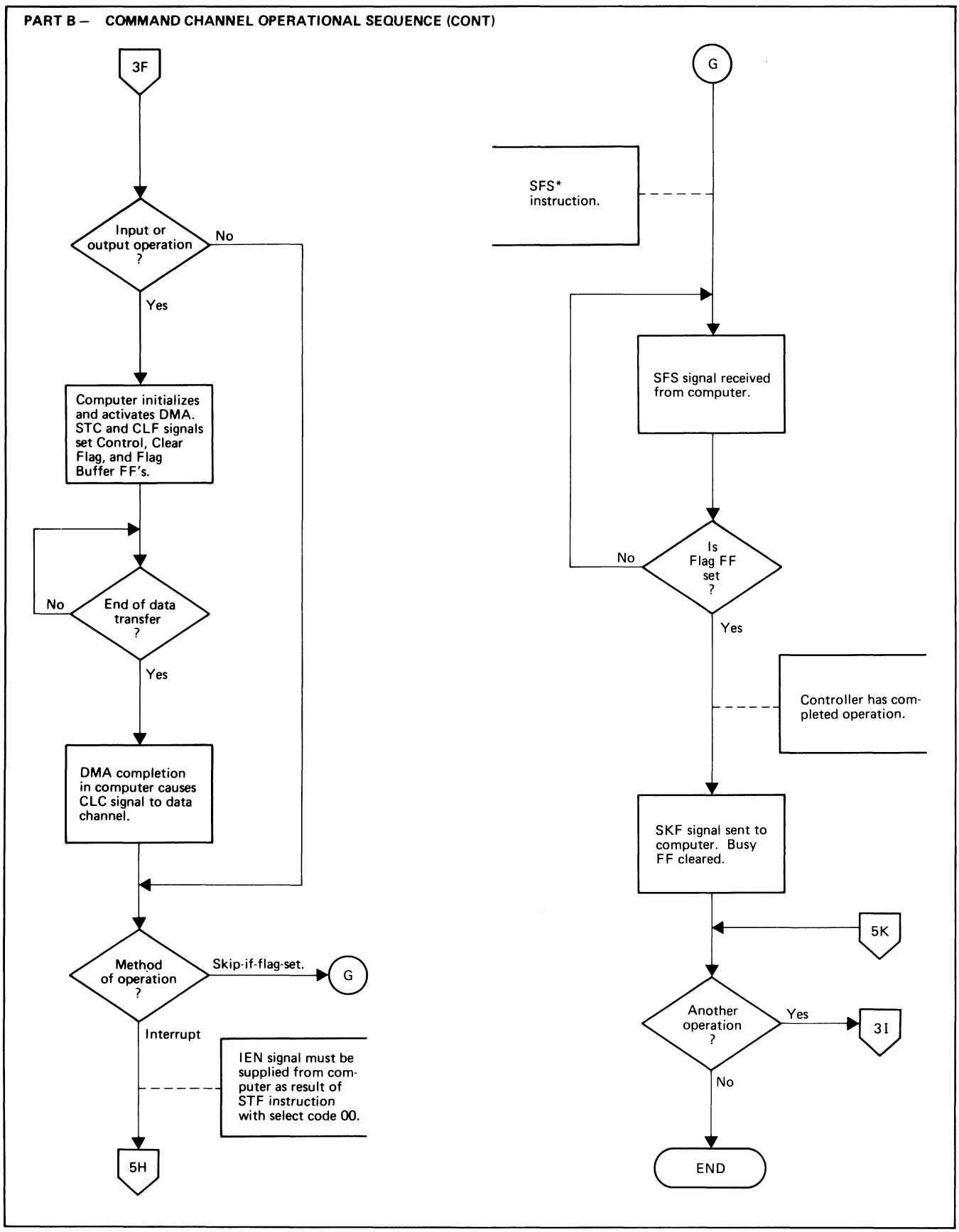


Figure 4-3. Data and Command Channels Flowchart (Sheet 4 of 5)

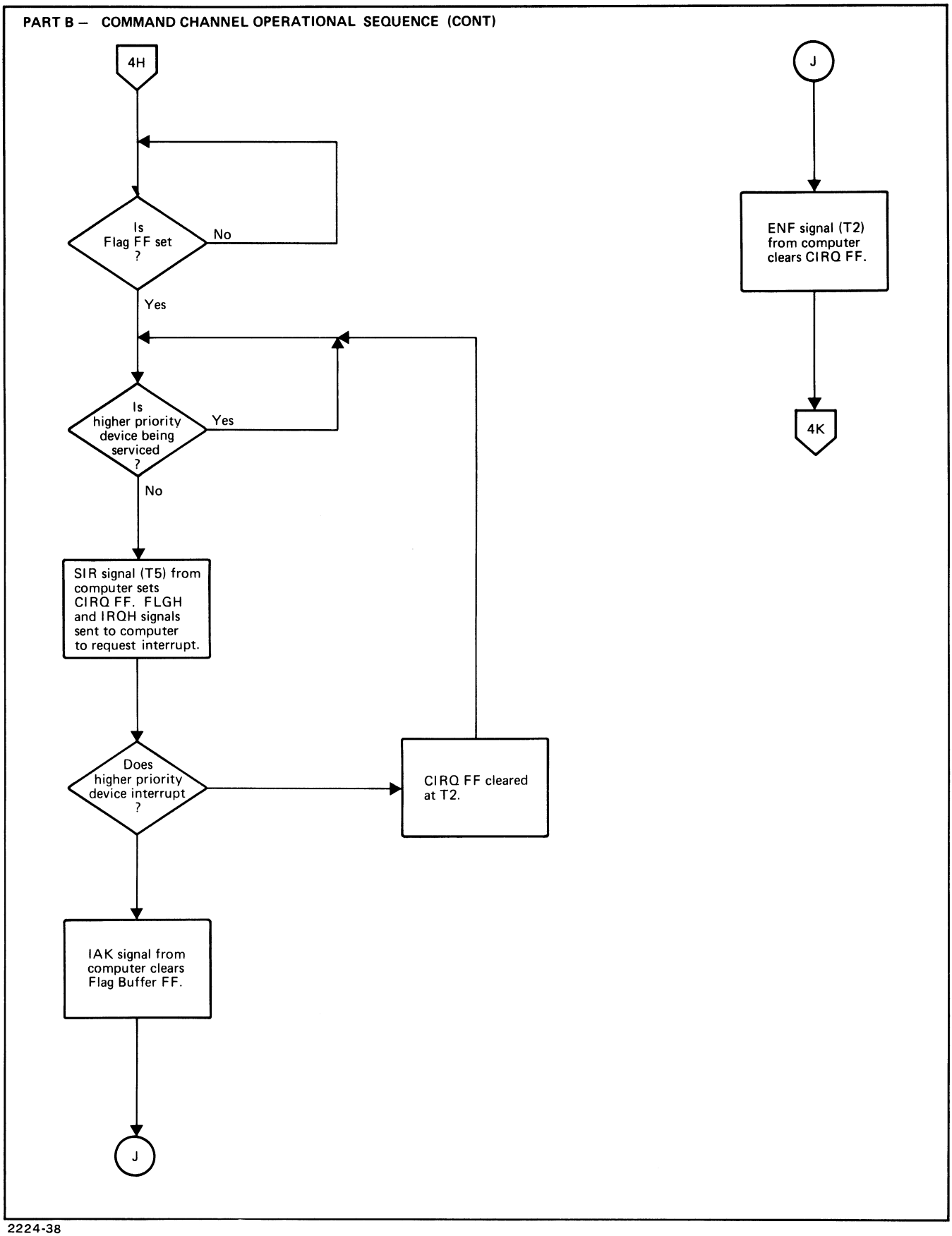
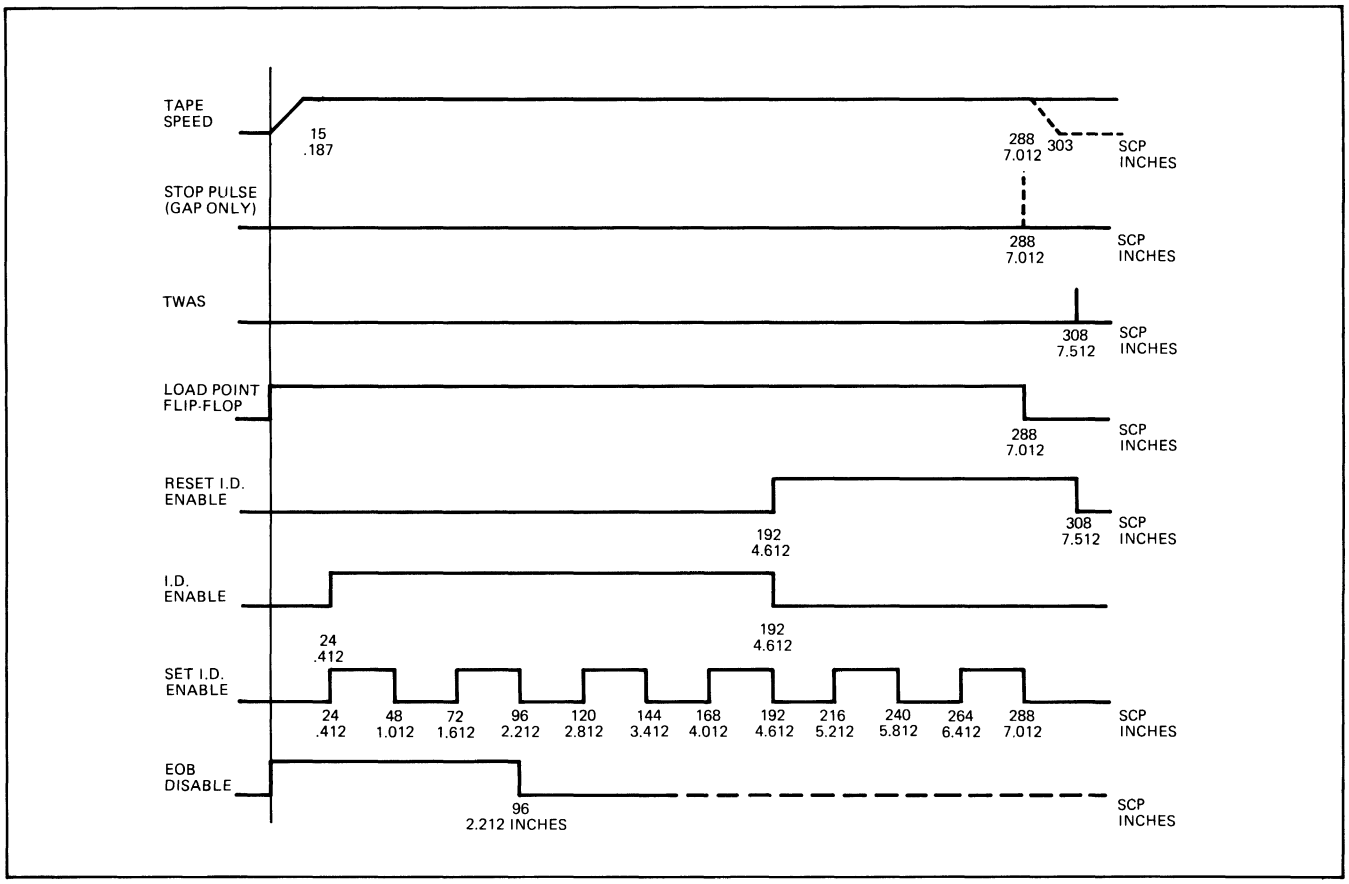


Figure 4-3. Data and Command Channels Flowchart (Sheet 5 of 5)



2224-35

Figure 4-4. ID Burst Timing Diagram

4-5. Mag Tape 2 PCA

Mag tape 2 PCA block diagram is presented in figure 4-5. The detailed schematic diagram for this PCA is presented in figure 5-4. Mag tape 2 PCA provides the data transfer paths between the computer and the tape unit.

Control of the write functions is primarily by the state control logic. The state control logic provides the sequencing signals necessary to activate various logic functions at the appropriate times. Six flip-flops and a variety of input gates control the operation of the state control logic. By sequencing the flip-flops and decoding, their outputs, appropriate groups of logic are enabled to perform specific write functions. The state control logic flowchart (see figure 4-6) presents the details of the operation of the state control logic.

The state control logic may be considered to exist in two functional groups. The first group, controlled by flip-flops C, D, E, and F, controls the various write functions such as writing an ID burst, a file mark, a preamble or postamble, or actual data. Most of these functions are performed by selectively activating the second functional group. This group, controlled by flip-flops A and B, control the writing of two bytes of data on tape.

This second group, designated the W1BYT subroutine on the flowchart, may operate at the same time that the first group of state control logic is sequencing. Each group of logic depends on control signals from the other to control some of its operations. Table 4-1 and table 4-2 summarize the decoded state logic outputs. Table 4-3 defines the mnemonics listed in tables 4-1 and 4-2. These mnemonics also appear on the detailed schematic diagram for mag tape 2 PCA.

The PREAM flip-flop is set by the output of the state decoder when writing the preamble appended to the data block. PREAM FF is set by the 40's counter after 40 zeros have been written. An all 1's character is written under control of the state decoder and write control logic.

The Set Flag Buffer (SFB) logic sends the SFB signal to mag tape 1 PCA to signal the computer that the next data word is required. The SFB signal is asserted when the lower byte is transferred to the write buffer from the input write buffer. (See figure 4-12.)

Table 4-1. State Decoder Outputs

STATE FLIP-FLOPS				STATE DECODER OUTPUT	FUNCTION
F	E	D	C		
0	0	0	0	$\overline{A}$	IDLE STATE
0	0	0	1	$\overline{B}$	WRTEN, CNTEN
0	0	1	0	$\overline{T}$	COMP, IDB
0	0	1	1	$\overline{J}$	IDB
0	1	0	0	$\overline{L}$	RETURN TO RESET FLUX
0	1	0	1	$\overline{K}$	RETURN TO RESET FLUX
0	1	1	0	–	ILLEGAL STATE
0	1	1	1	–	ILLEGAL STATE
1	0	0	0	$\overline{H}$	WRTEN, VPODD, BUFEN
1	0	0	1	$\overline{C}$	COMP, SUPPR, CLEAR
1	0	1	0	–	ILLEGAL STATE
1	0	1	1	$\overline{D}$	COMP
1	1	0	0	$\overline{G}$	WRTEN, VPODD, BUFEN, RPREM
1	1	0	1	$\overline{Q}$	WRTEN, VPODD, BUFEN
1	1	1	0	$\overline{F}$	BUFEN, BUFLD
1	1	1	1	$\overline{E}$	TRANSITION STATE

At the beginning of a write or read operation, the reset logic provides a RESET signal to the buffer registers and the status flip-flops.

The input write buffer accepts the 16-bits of data from the computer or DMA card via the IOB lines. The unpacking multiplexer selects the 16-bit word and, under control of the write control logic, transfers the appropriate eight-bit byte to the write buffer.

The output of the write buffer is monitored by the parity generator which adds the parity bit to the write data lines. The write clock logic provides the write clock to the tape unit under control of the state decoder and timing signals from mag tape 1 PCA. The complement (COMP) signal complements the outputs of the write buffer when alternate ones and zeros are being written for the ID burst or when the phase transition of a data cell is being written on tape.

The read buffer accepts eight-bit bytes from the tape unit and packs them into 16-bit words for transfer to the computer or DMA PCA. Parity is checked by the parity check logic at the input to the interface PCA and also in the tape unit.

The gap timing counter provides an appropriate delay to stop the forward or reverse drive. This delay ensures that the head will be positioned correctly within the IRG on tape. When the EOB signal is sent from the tape unit, the gap timing counter delays its output signal (EOR) to the Forward or Reverse flip-flops on mag tape 1 PCA.

Status is latched into the status flip-flops by EOB at the end of each operation. The outputs of the status flip-flops are available to the computer via the IOB lines at the end of each command. The Illegal State, Parity Error (PAR ERR) and Multiple Track Error (MTE) signals set the Data Error status flip-flop. The Timing Error (TIMNG ERR), Tape Mark (TM) and Single Track Error (STE) signals set the appropriate status flip-flops. In addition, the Data Error Status FF is set if STE is detected during a read-after-write operation.

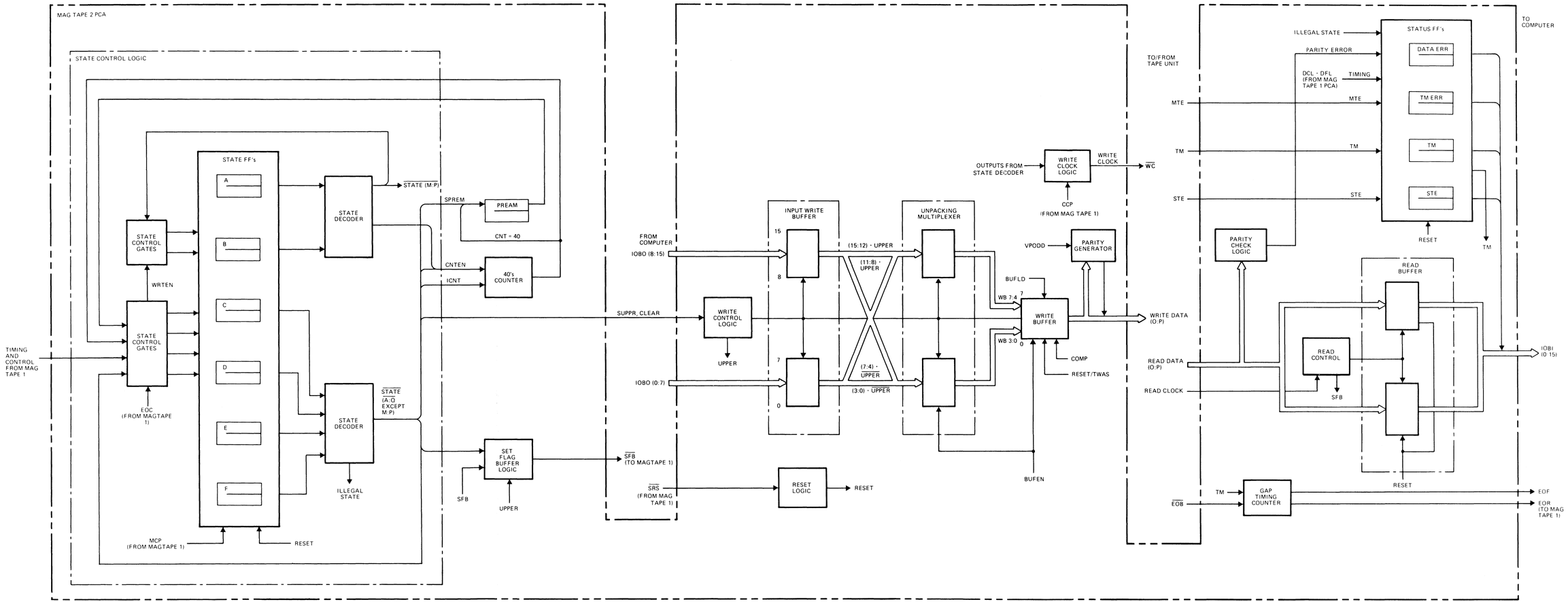


Figure 4-5. Mag Tape 2 PCA Block Diagram

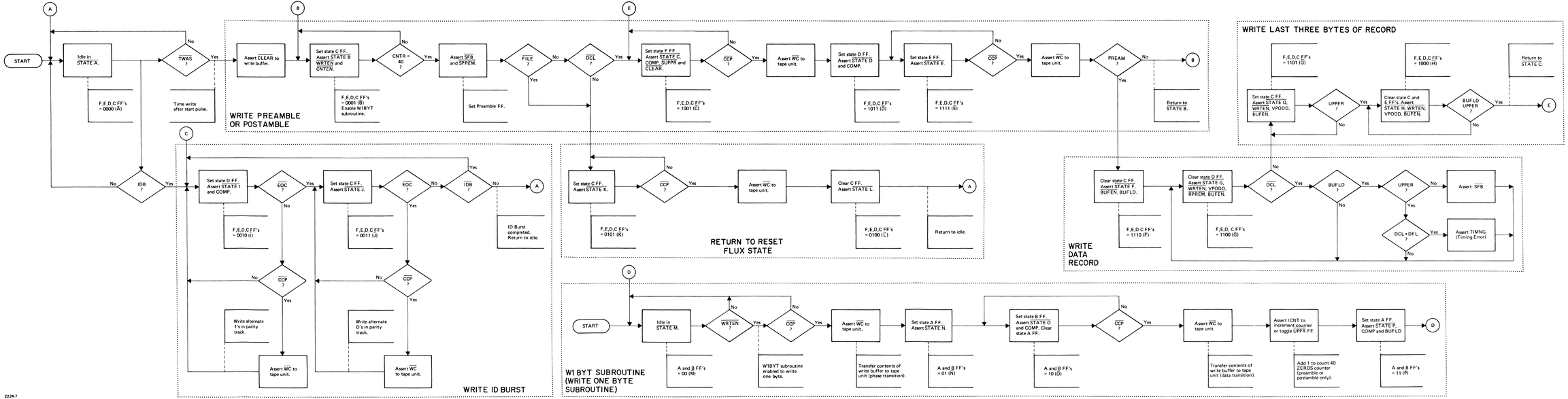


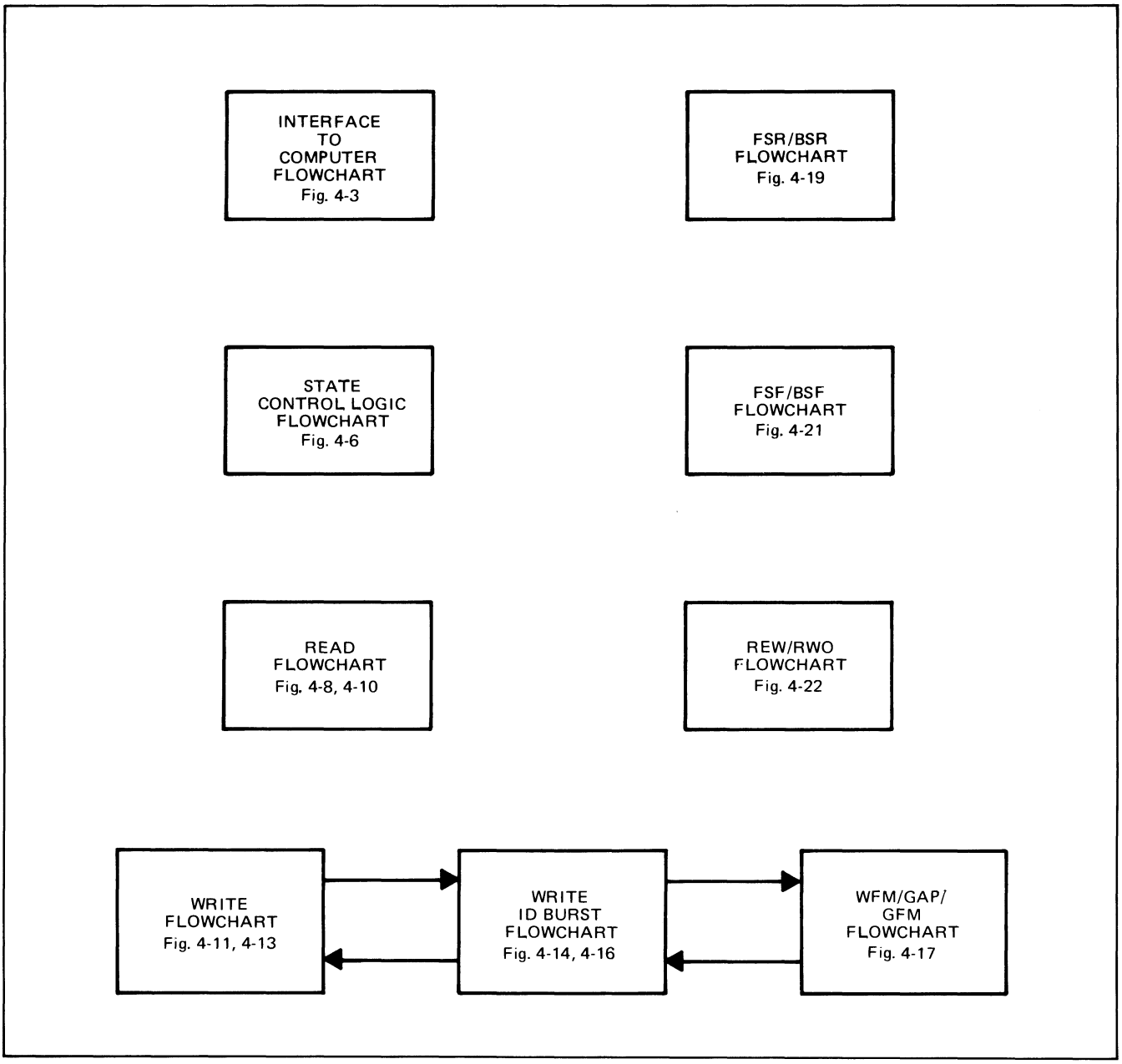
Figure 4-6. State Control Logic Flowchart

Table 4-2. W1BYT Subroutine State Decoder Outputs

STATE FF'S		STATE OUTPUT	FUNCTION
B	A		
0	0	$\overline{M}$	IDLE STATE
0	1	$\overline{N}$	TRANSITION STATE
1	0	$\overline{O}$	COMP
1	1	$\overline{P}$	COMP, BUFLD

4-6. FLOWCHARTS

The functional operation of the interface is illustrated in the following hardware flowcharts and block diagrams. (See figures 4-8 through 4-23.) Figure 4-7 presents an overview of the flowcharts. Each function is described by flowcharts and a block diagram. For the first three functions, the first flowchart relates to mag tape 2 PCA, and the block diagram presents the hardware associated with that function. The second three functions are presented on single flowcharts. All the flowcharts are annotated with explanatory comments.

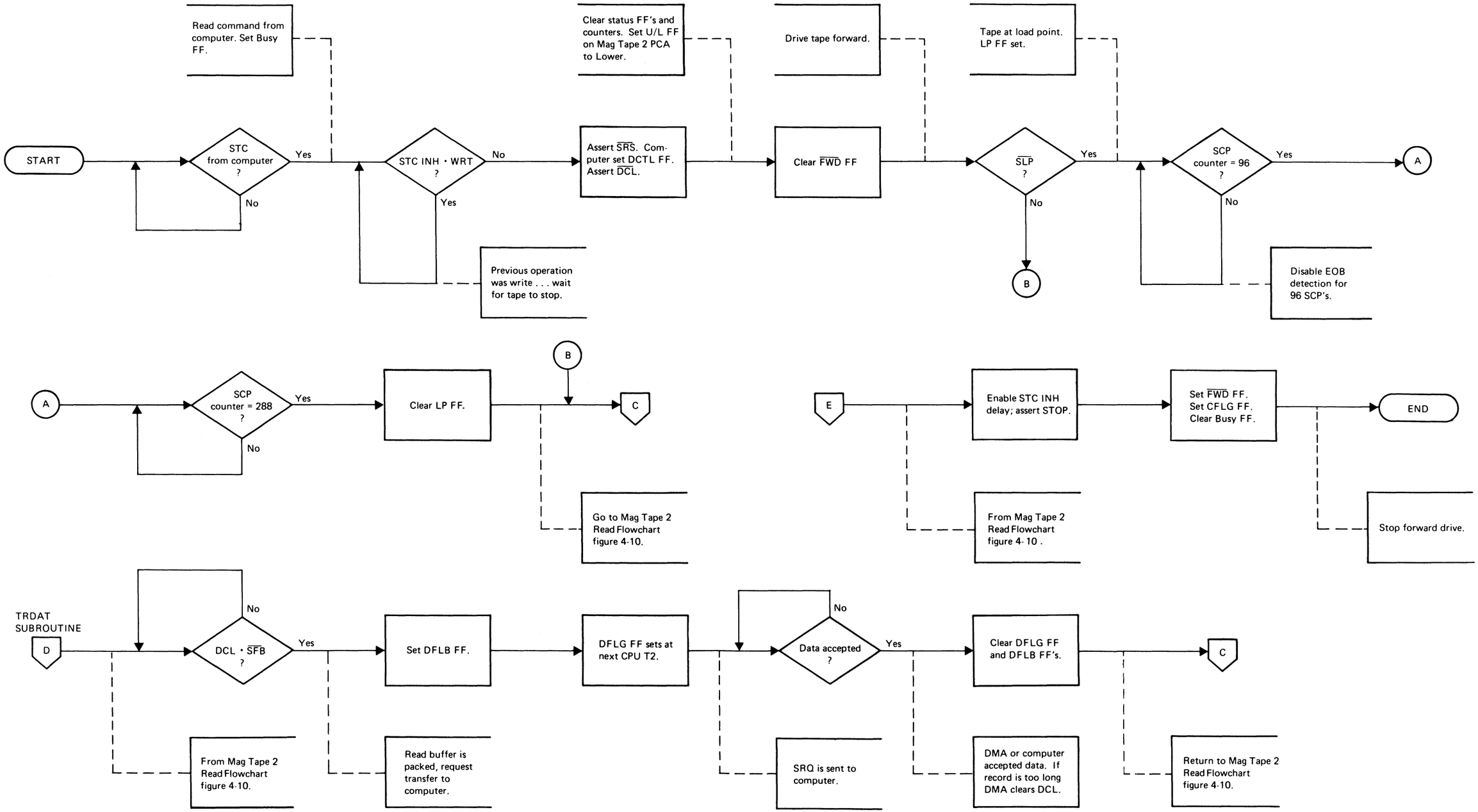


2224-6

Figure 4-7. Flowcharts Overview

Table 4-3. State Control Logic Mnemonics

MNEMONIC	DEFINITIONS
BUFEN	The Buffer Enable signal enables the unpacking multiplexer and the write buffer.
BUFLD	The Buffer load signal transfers the selected byte of the input computer word to the write buffer.
CCP	Control Clock Pulses occur at twice the byte transfer rate. They are used to clock flux transitions to the tape, and for control purposes.
CLEAR	The Clear signal clears the write buffer to zero.
CNT	The Count signal is high when the 40 zeroes counter reaches 40.
CNTEN	The Count Enable signal enables the 40 zeroes counter to respond to ICNT and count 40 zeroes.
COMP	The Complement signal complements all data outputs to write the second (data) transition of the bits.
DCL	The Data Control signal is high during data transfers.
DFL	The Data Flag signal is high when the Data Flag flip-flop is set.
EOC	The Even-Odd Clock runs at 1/2 the byte transfer rate.
FILE	The File signal is high when writing a file mark or spacing a file.
ICNT	The Increment Counter signal counts the 40 zeroes of the preamble, postamble, or file mark. In the data portion of a record, ICNT toggles the UPPR (byte) flip-flop.
IDB	The ID Burst enable signal is high when the ID burst is being written.
PREAM	The Preamble flip-flop determines whether a preamble or a postamble operation is being performed.
RPREM	The Reset Preamble signal clears the Preamble flip-flop.
SFB	The Set Flag Buffer signal sets the data channel flag buffer (on mag tape 1 PCA) to request the next data word from the computer or to request the computer to accept the word in the read buffer.
SPREM	The Set Preamble signal sets the Preamble flip-flop.
SUPPR	The Set Upper signal sets the UPPR flip-flop at the start of a record. This is so the first byte will be taken from the upper half of the first data word.
TIMNG	The Timing Error signal sets the TMG ERR status flip-flop which may be read by the program. The data channel flag was not serviced before new data was required by the tape unit.
TWAS	The Time Write After Start signal from mag tape 1 PCA initiates writing of data or a file mark.
UPPR	This signal is high if the UPPR (byte) flip-flop is set to process the upper byte of a data word.
VPODD	The Vertical Parity Odd signal sets the parity generator to odd vertical parity.
WC	The Write Clock signal is sent to the tape drive to write the flux transition.
WRTEN	The Write Enable signal enables the W1BYT subroutine to write data on tape.



2224-17

Figure 4-8. Mag Tape 1 Read Flowchart

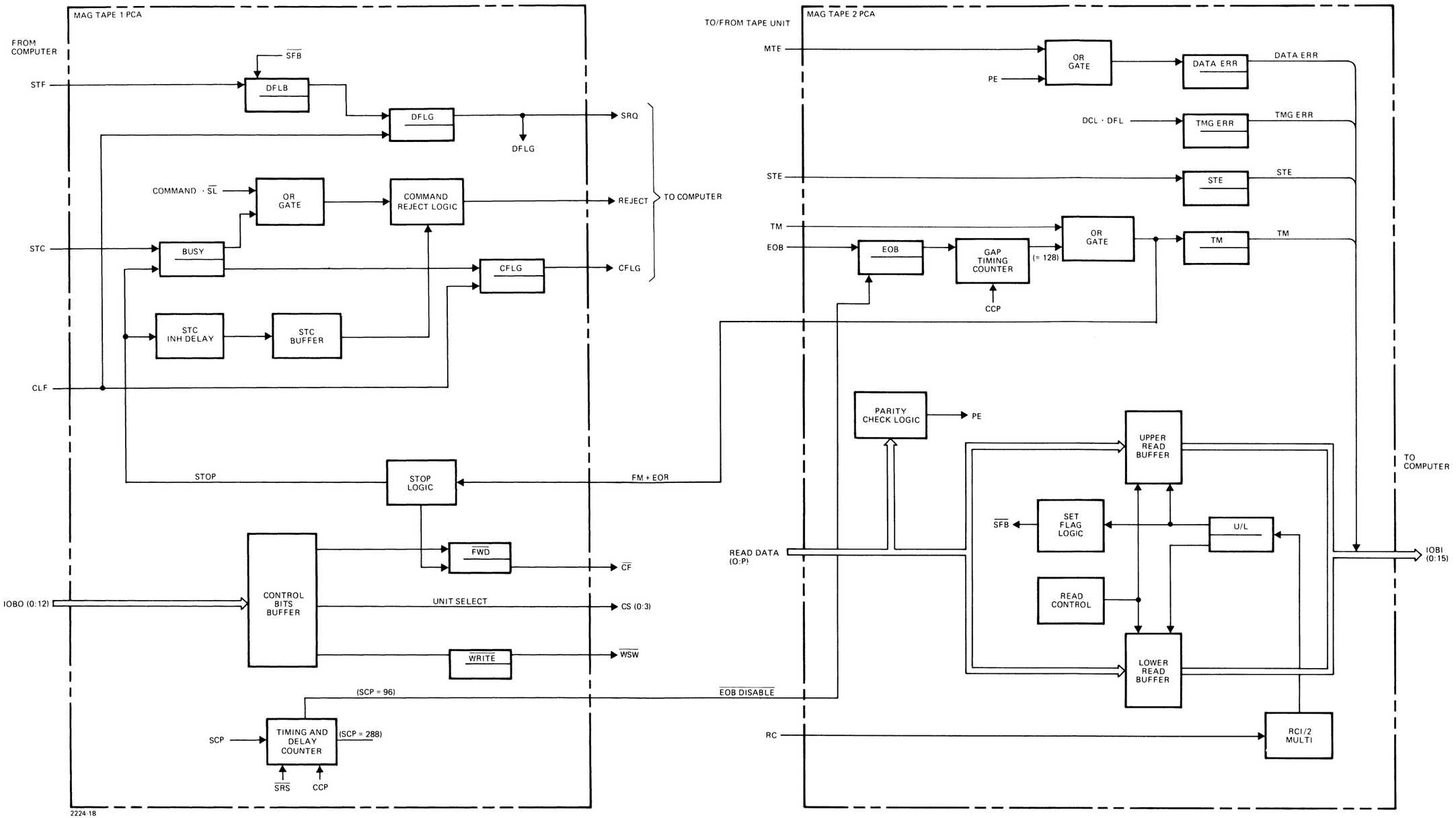


Figure 4-9. Read Block Diagram

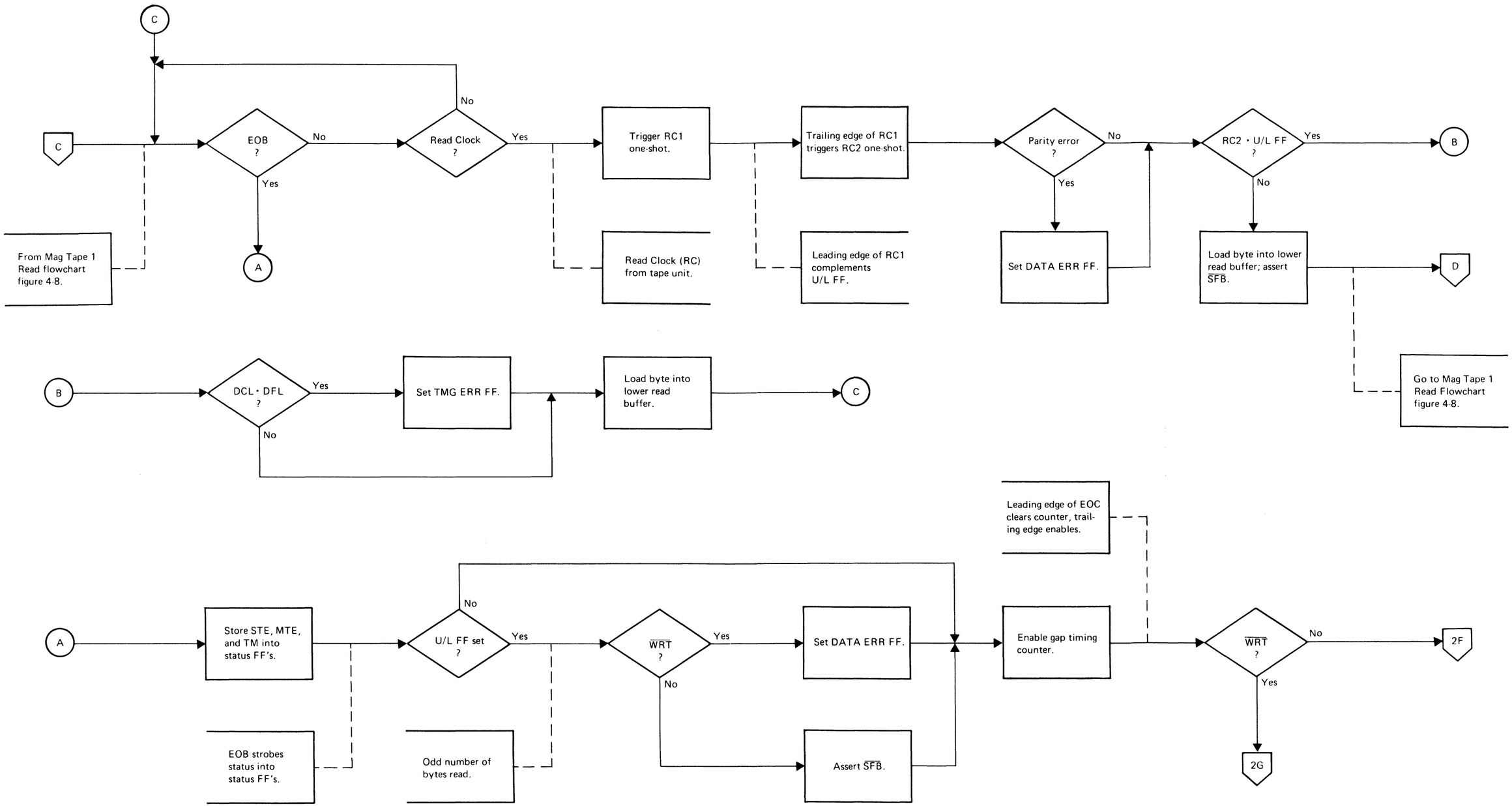
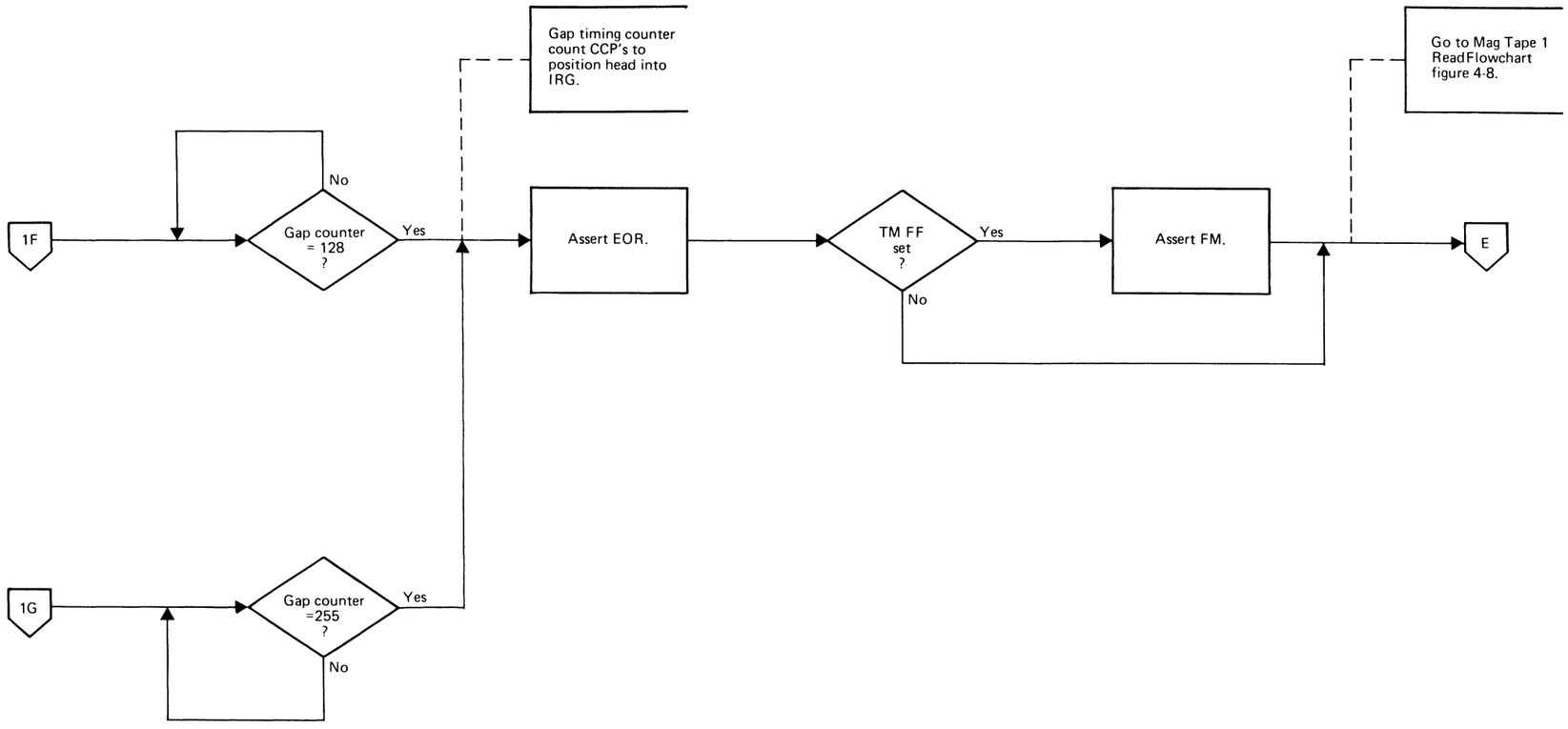
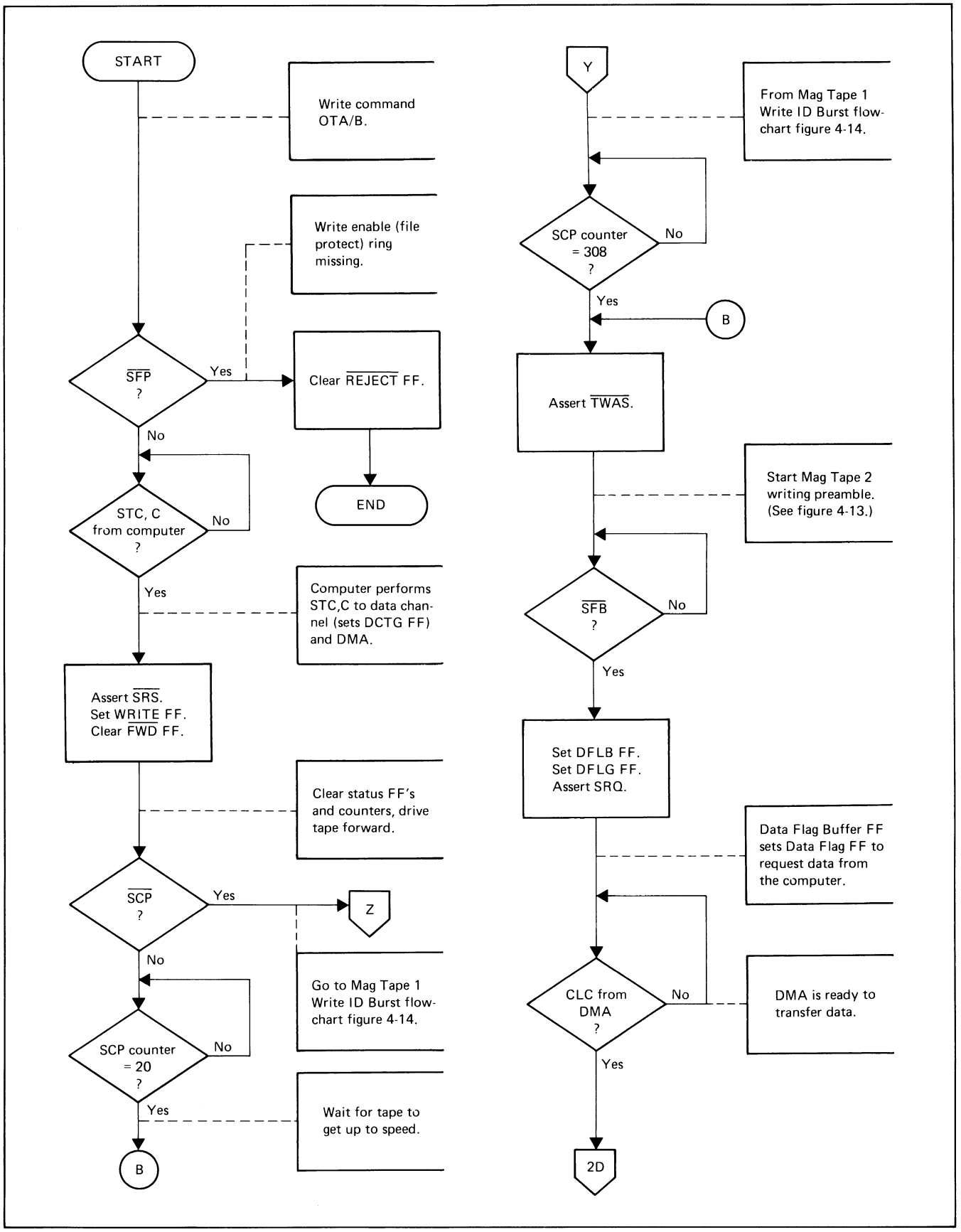


Figure 4-10. Mag Tape 2 Read Flowchart (Sheet 1 of 2)



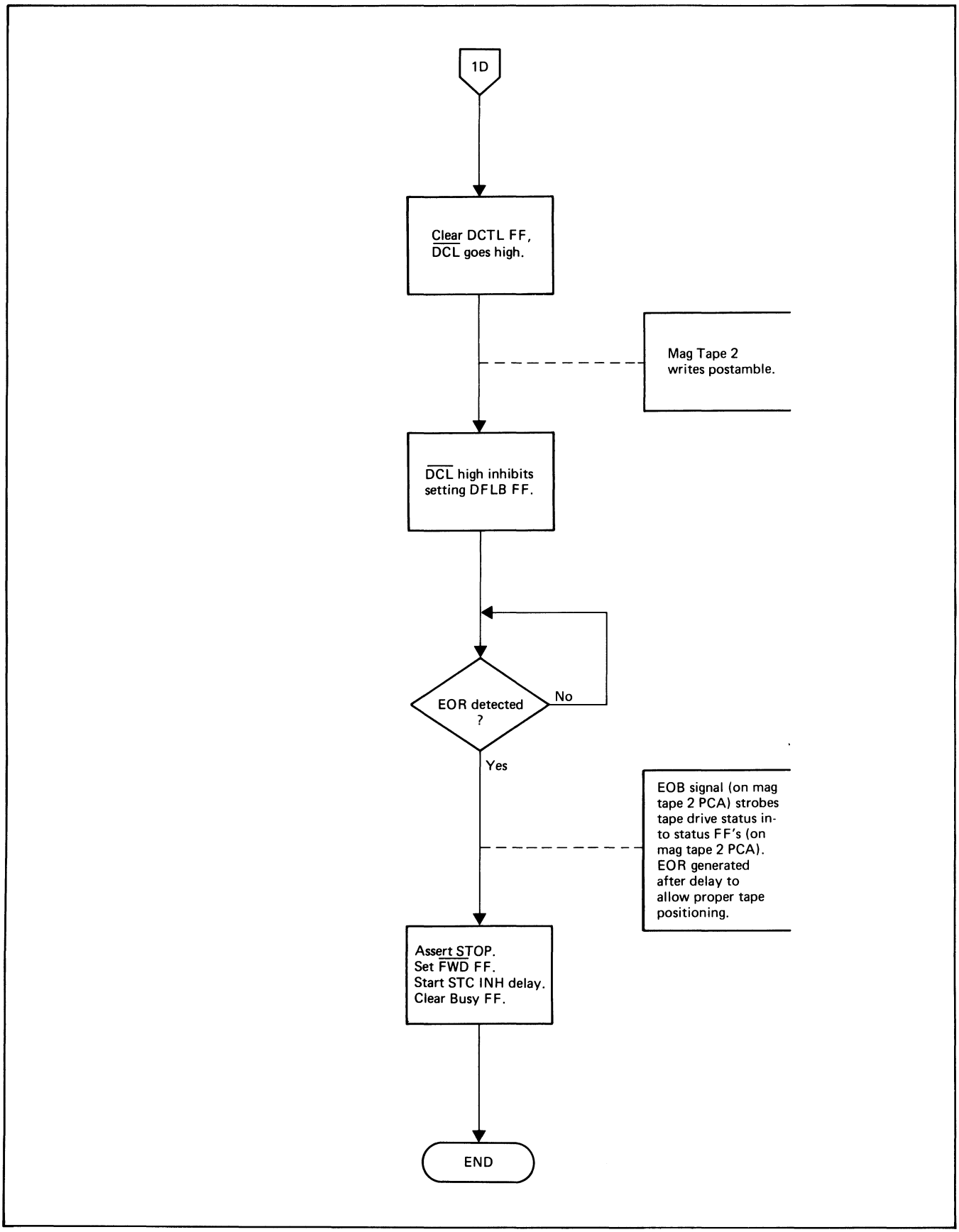
2224-20

Figure 4-10. Mag Tape 2 Read Flowchart (Sheet 2 of 2)



2224-21

Figure 4-11. Mag Tape 1 Write Flowchart (Sheet 1 of 2)



2224-22

Figure 4-11. Mag Tape 1 Write Flowchart (Sheet 2 of 2)

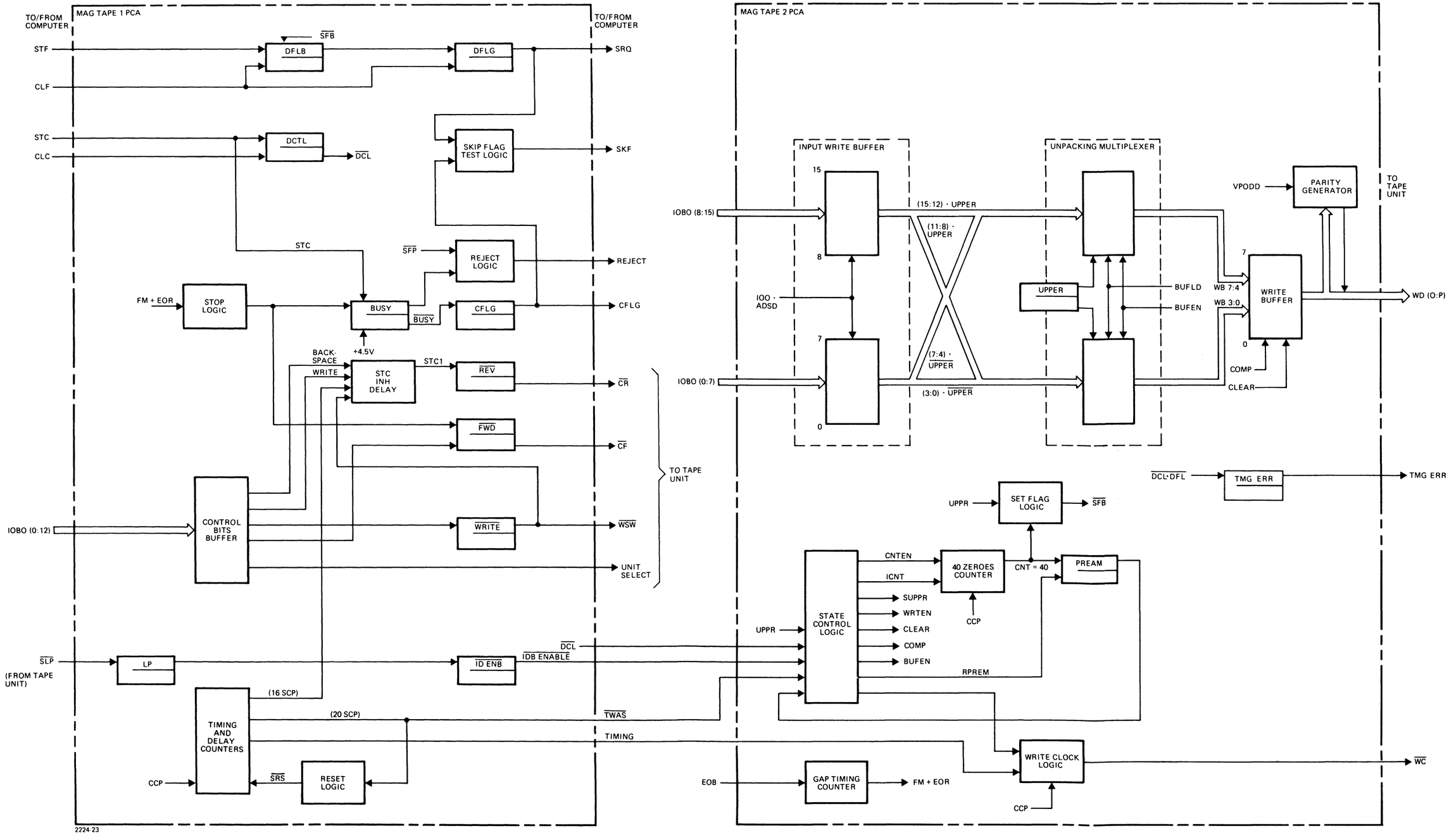


Figure 4-12. Write Block Diagram

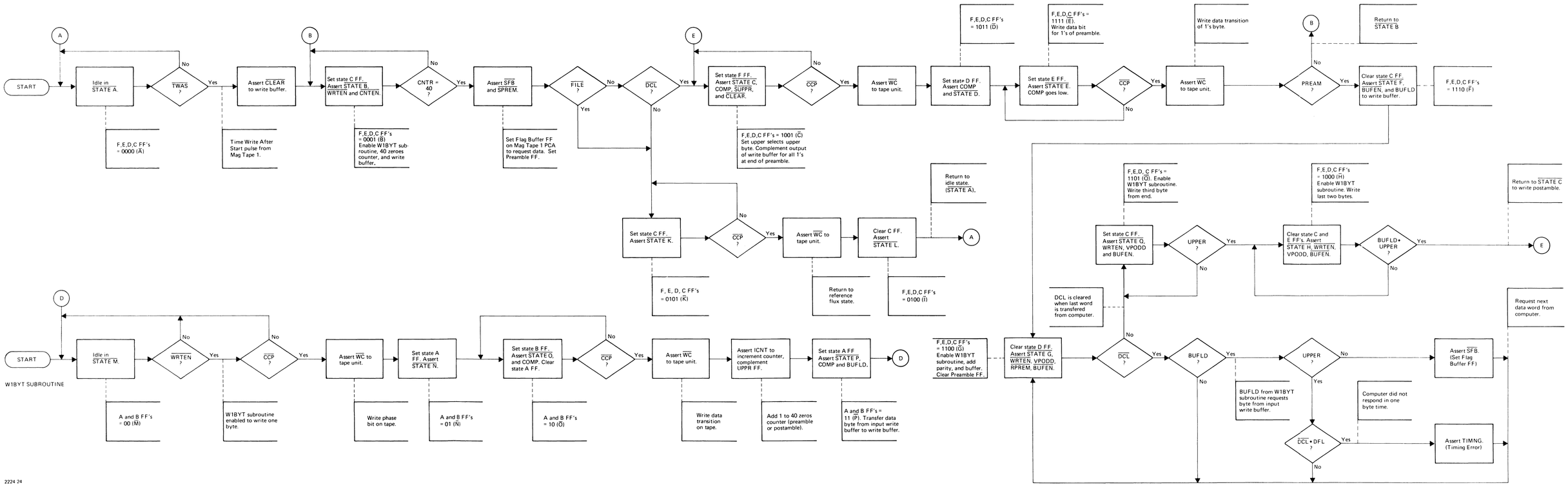
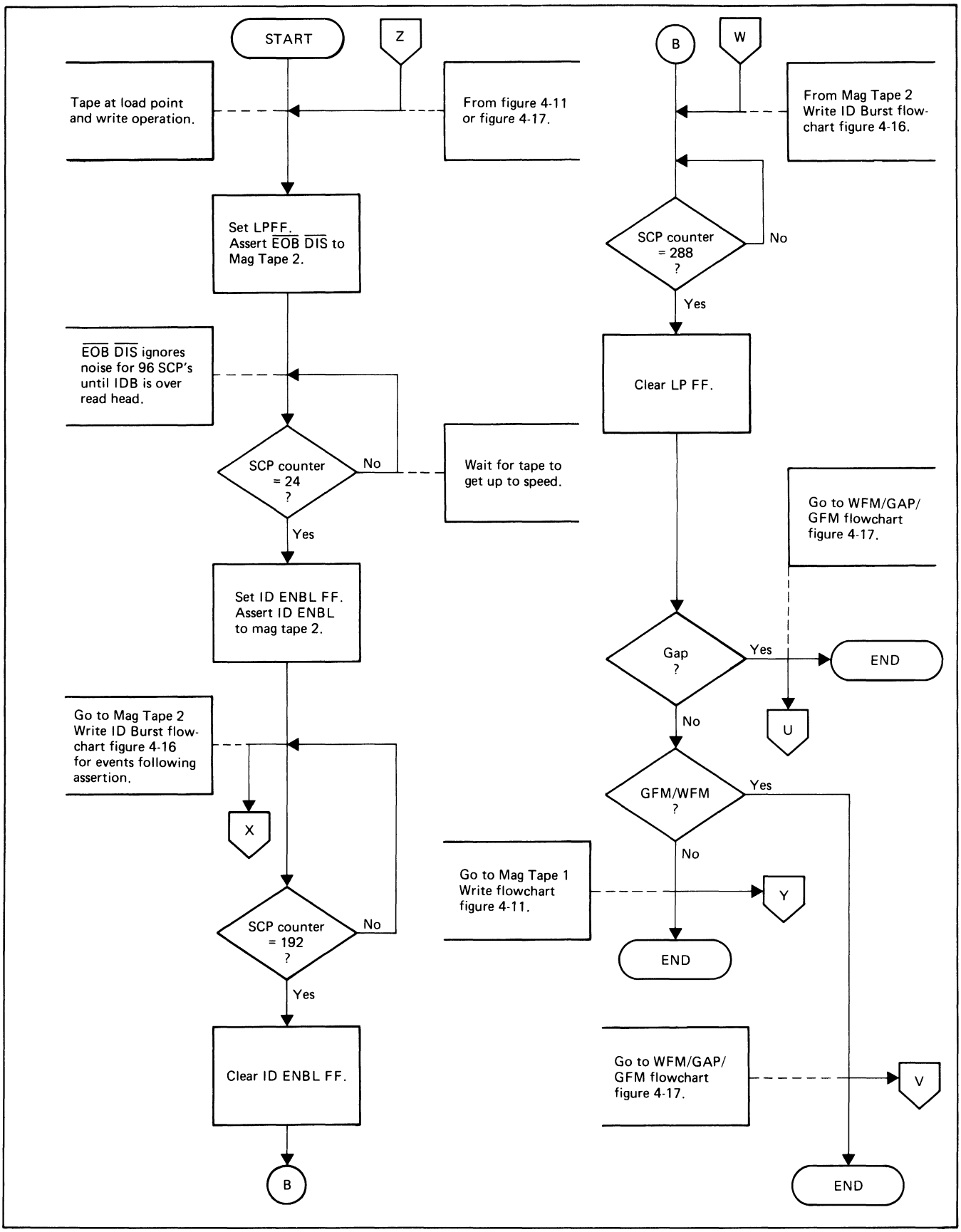


Figure 4-13. Mag Tape 2 Write Flowchart



2224-25

Figure 4-14. Mag Tape 1 Write ID Burst Flowchart

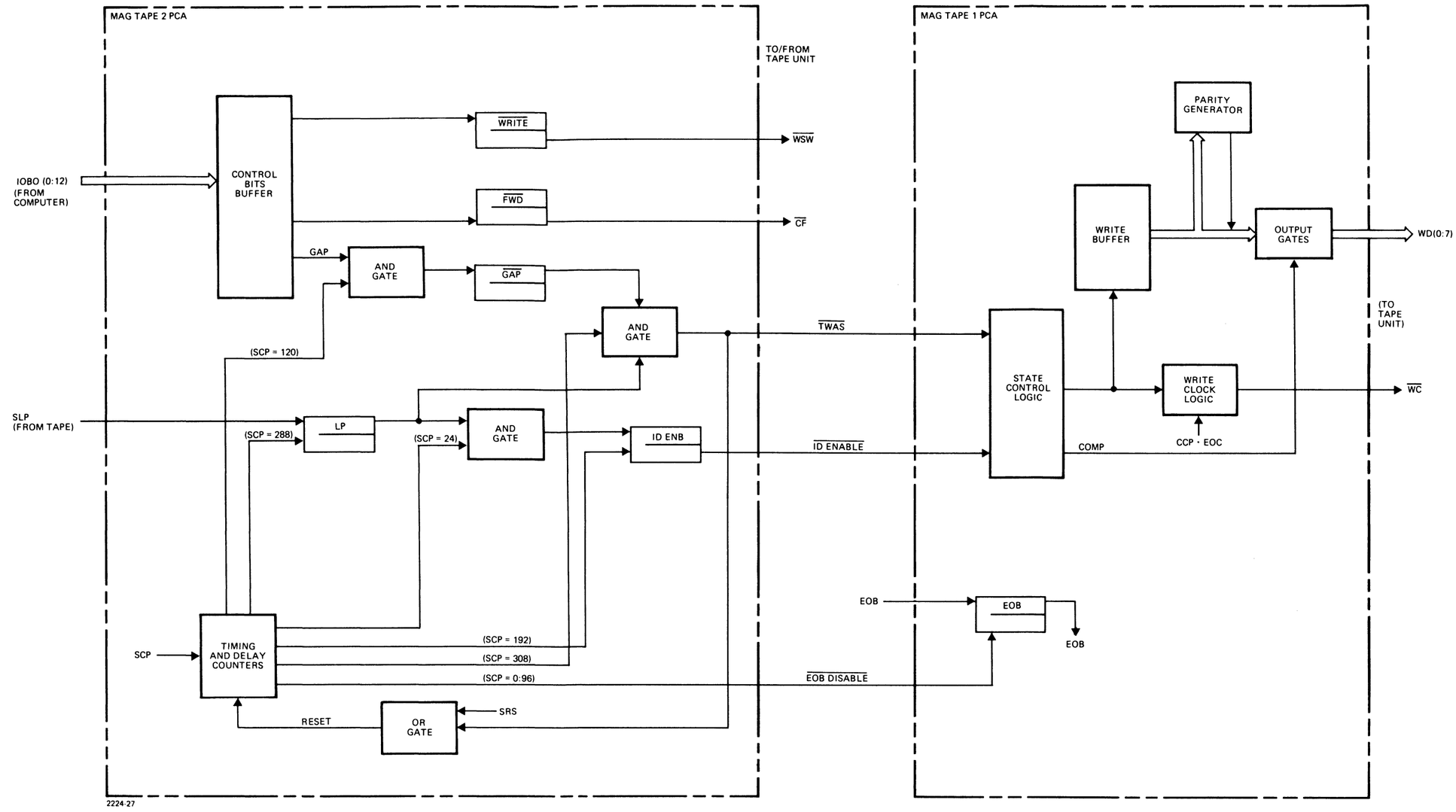


Figure 4-15. Write ID Burst Block Diagram

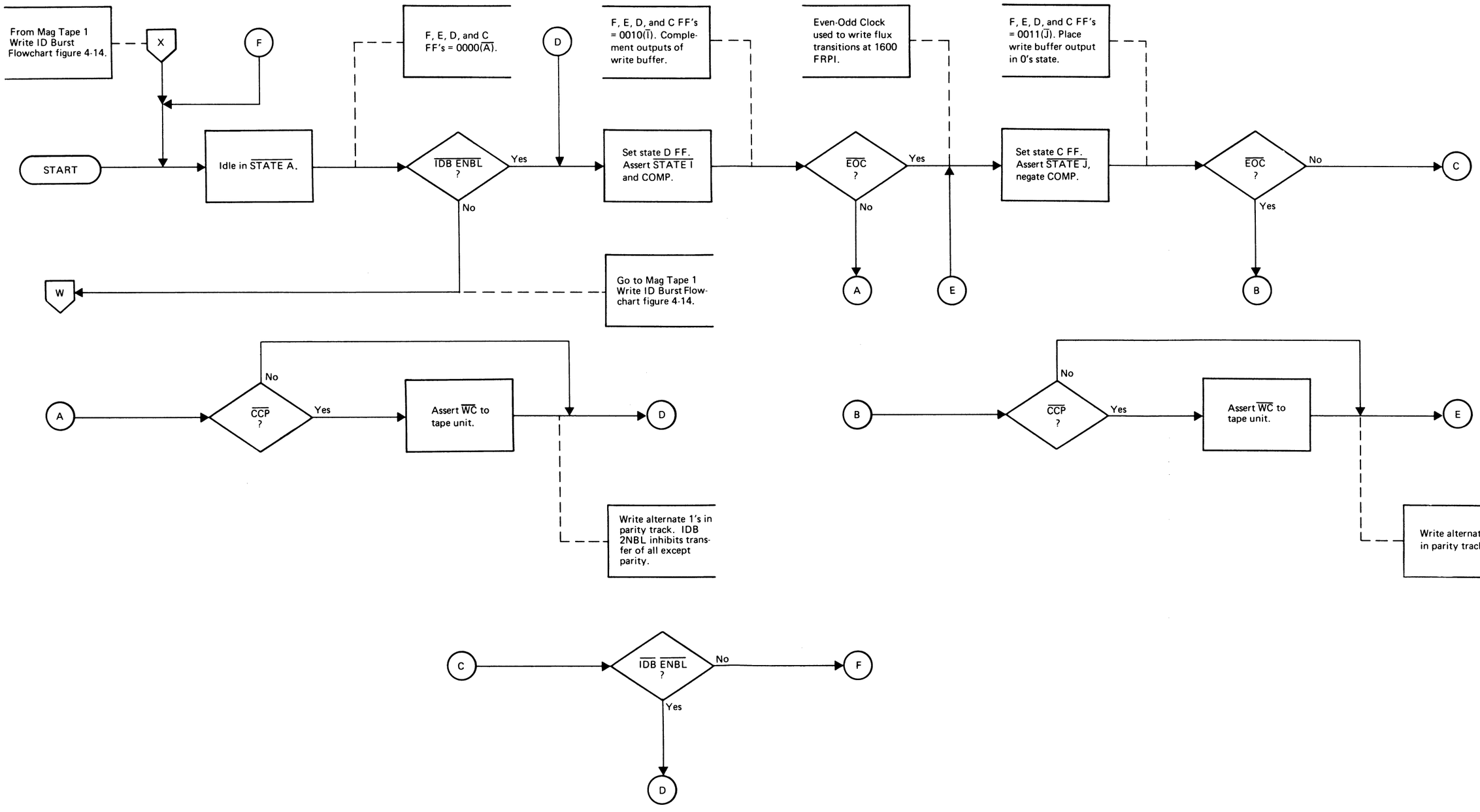
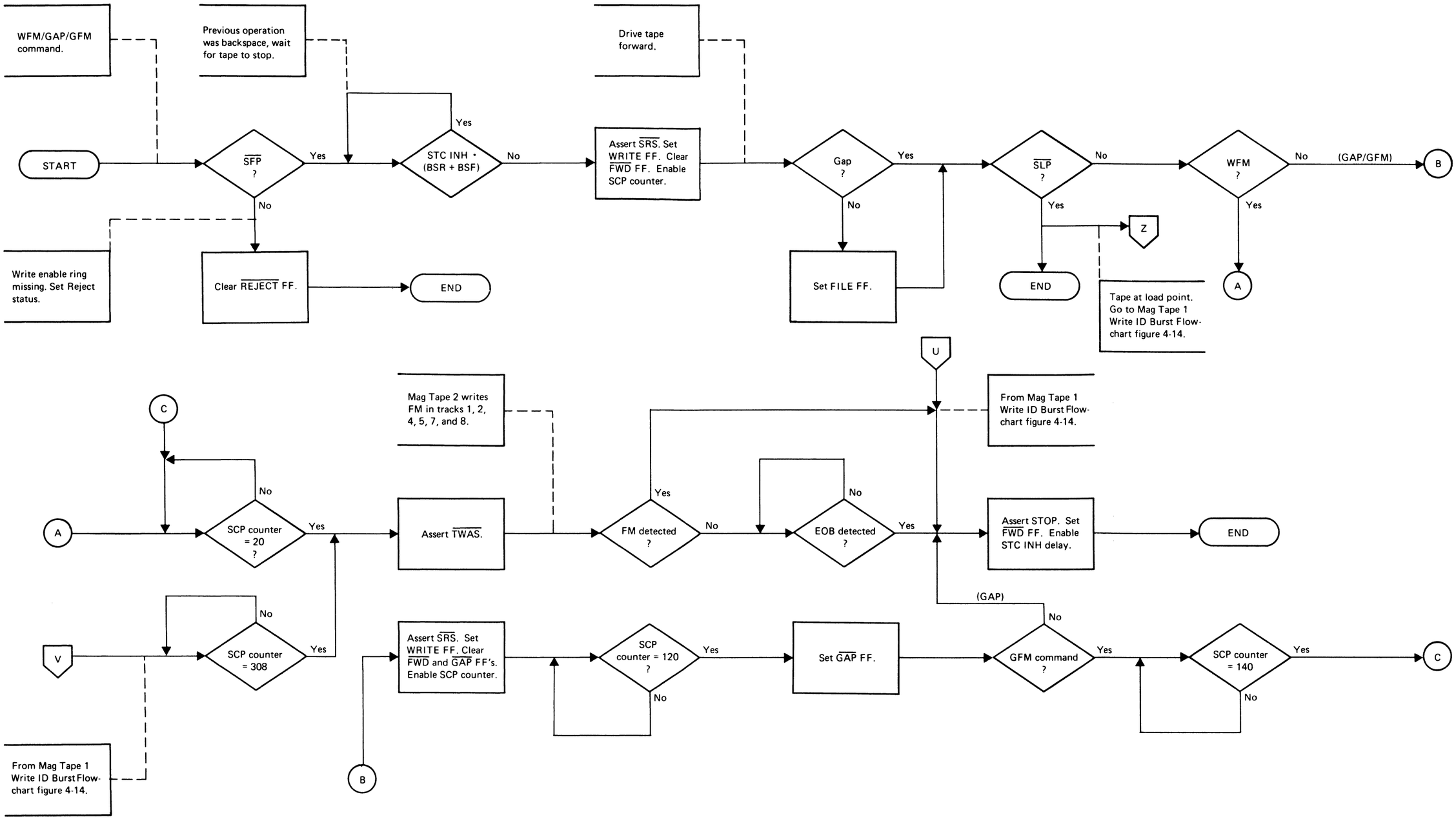


Figure 4-16. Mag Tape 2 Write ID Burst Flowchart



2224-28

Figure 4-17. WFM/GAP/GFM Flowchart

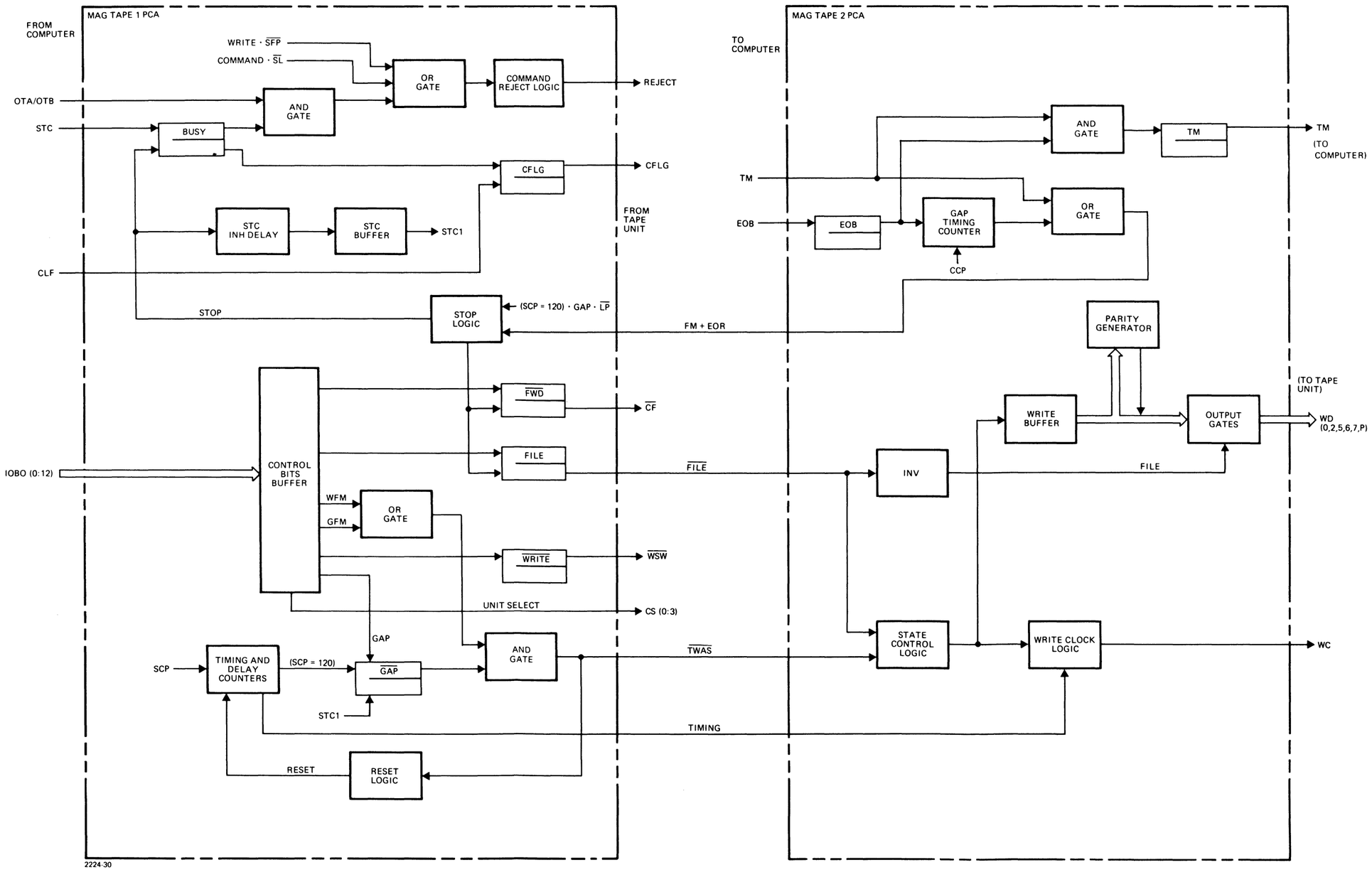
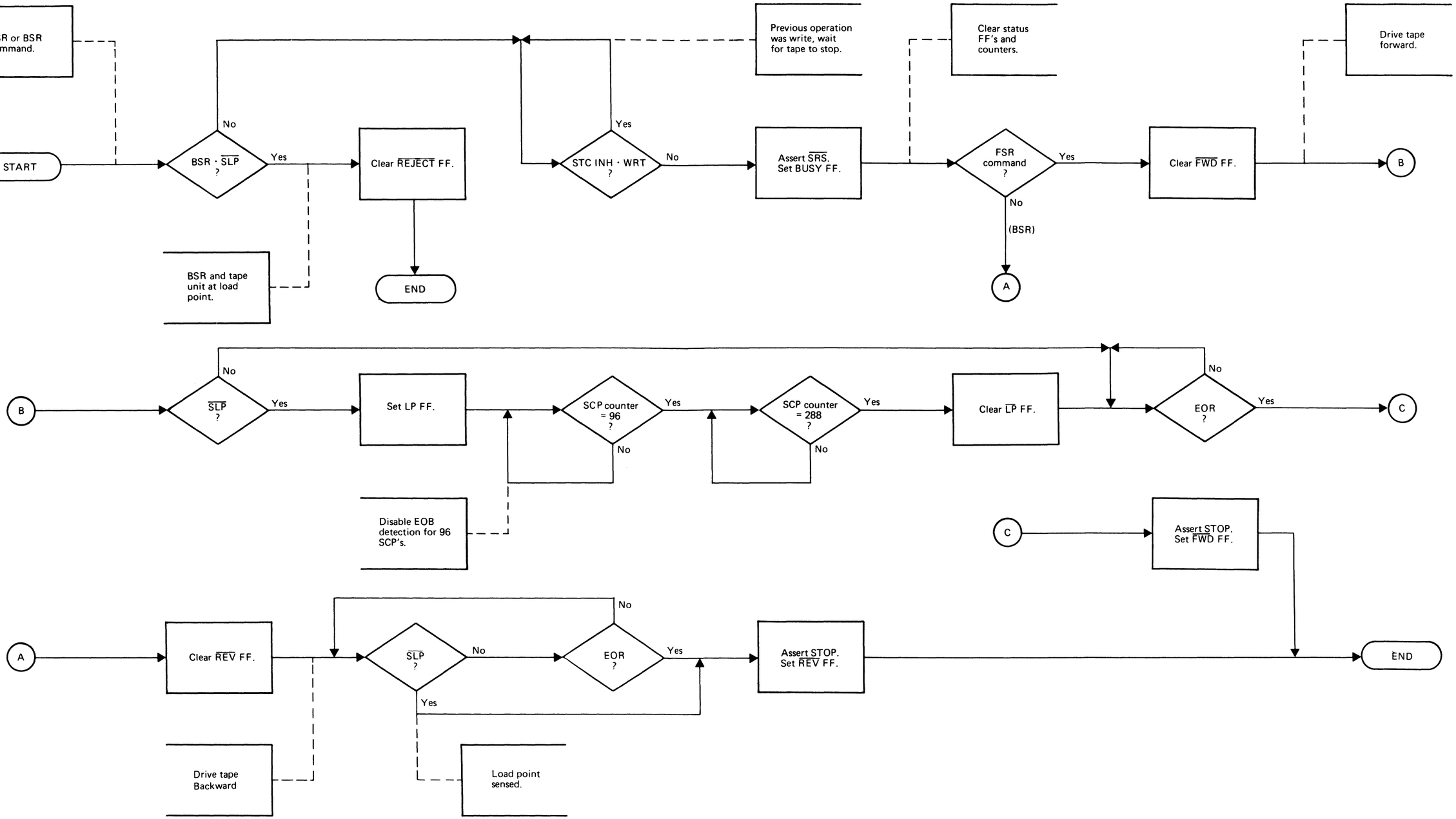


Figure 4-18. WFM/GAP/GFM Block Diagram



2224-29

Figure 4-19. FSR/BSR Flowchart

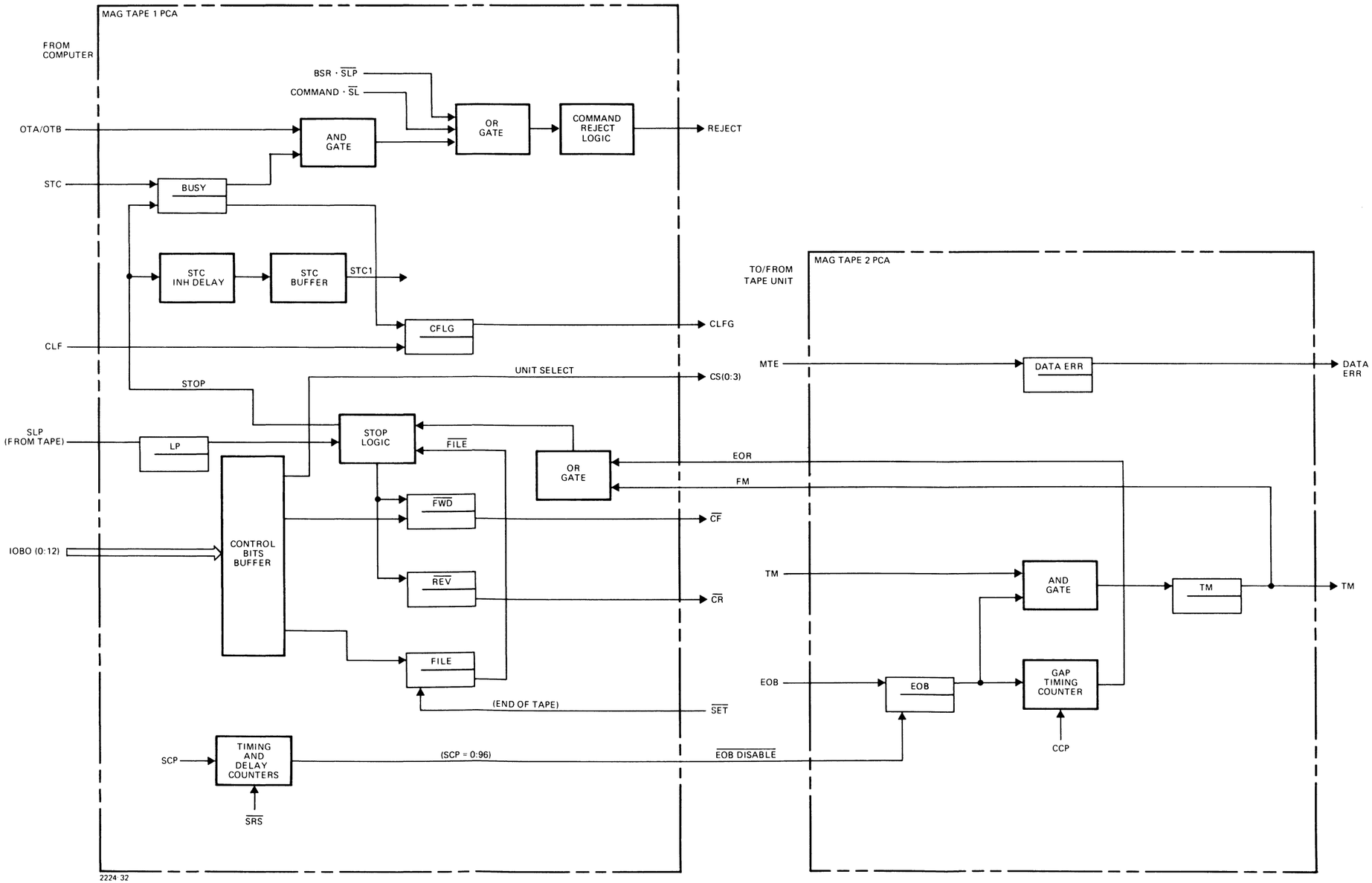
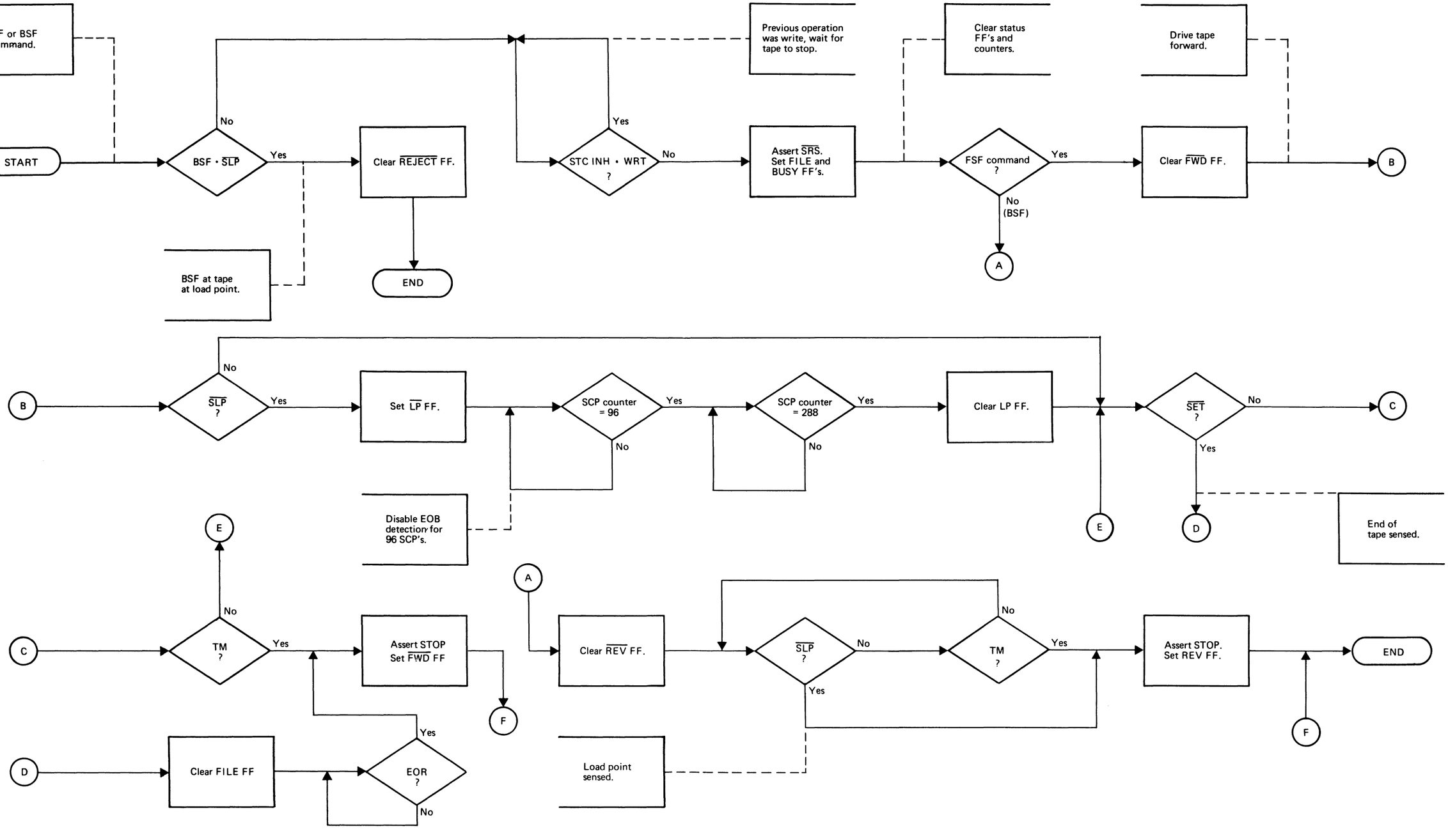
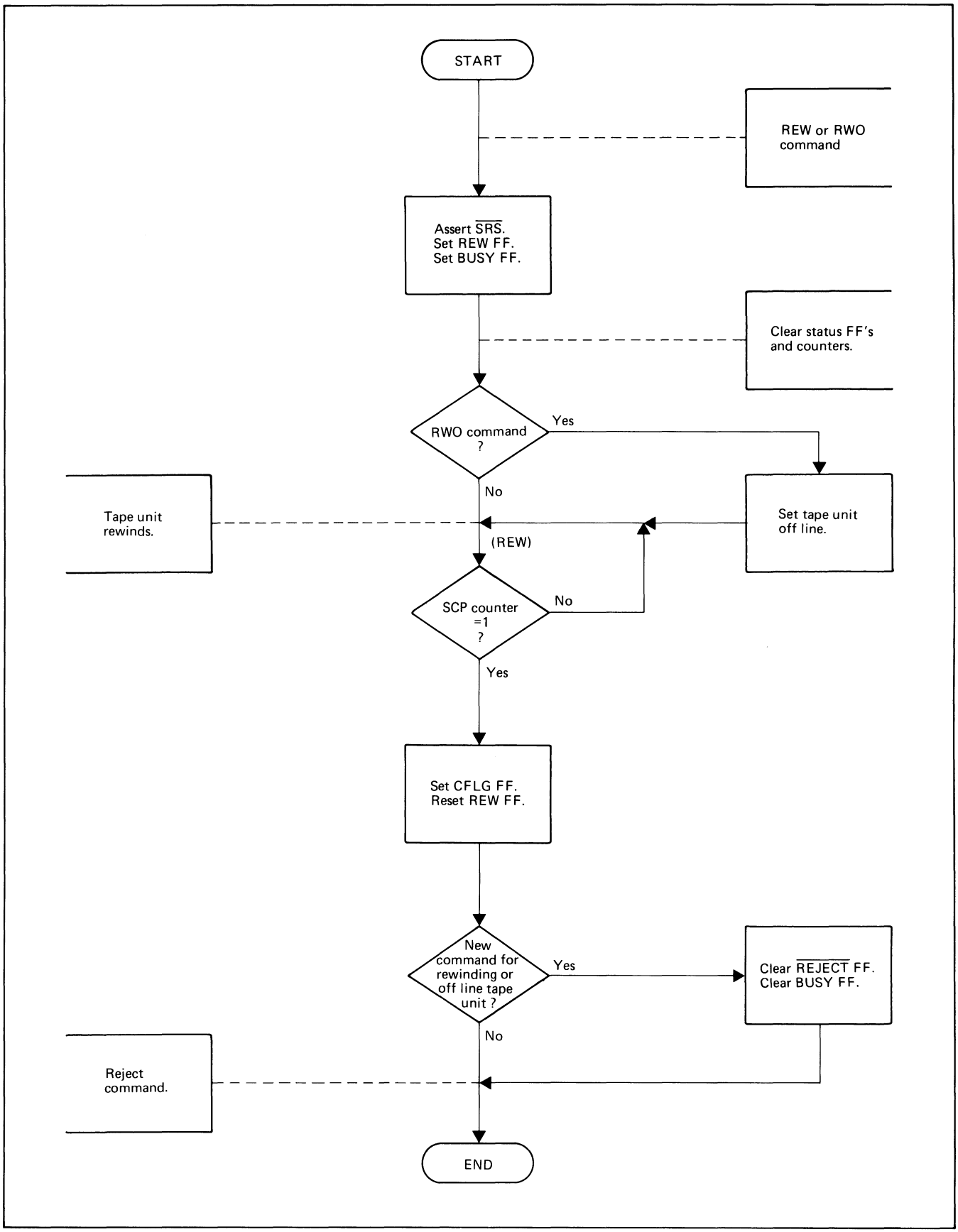


Figure 4-20. FSR/BSR/FSF/BSF Block Diagram



2224-33

Figure 4-21. FSF/BSF Flowchart



2224-31

Figure 4-22. REW/RWO Flowchart

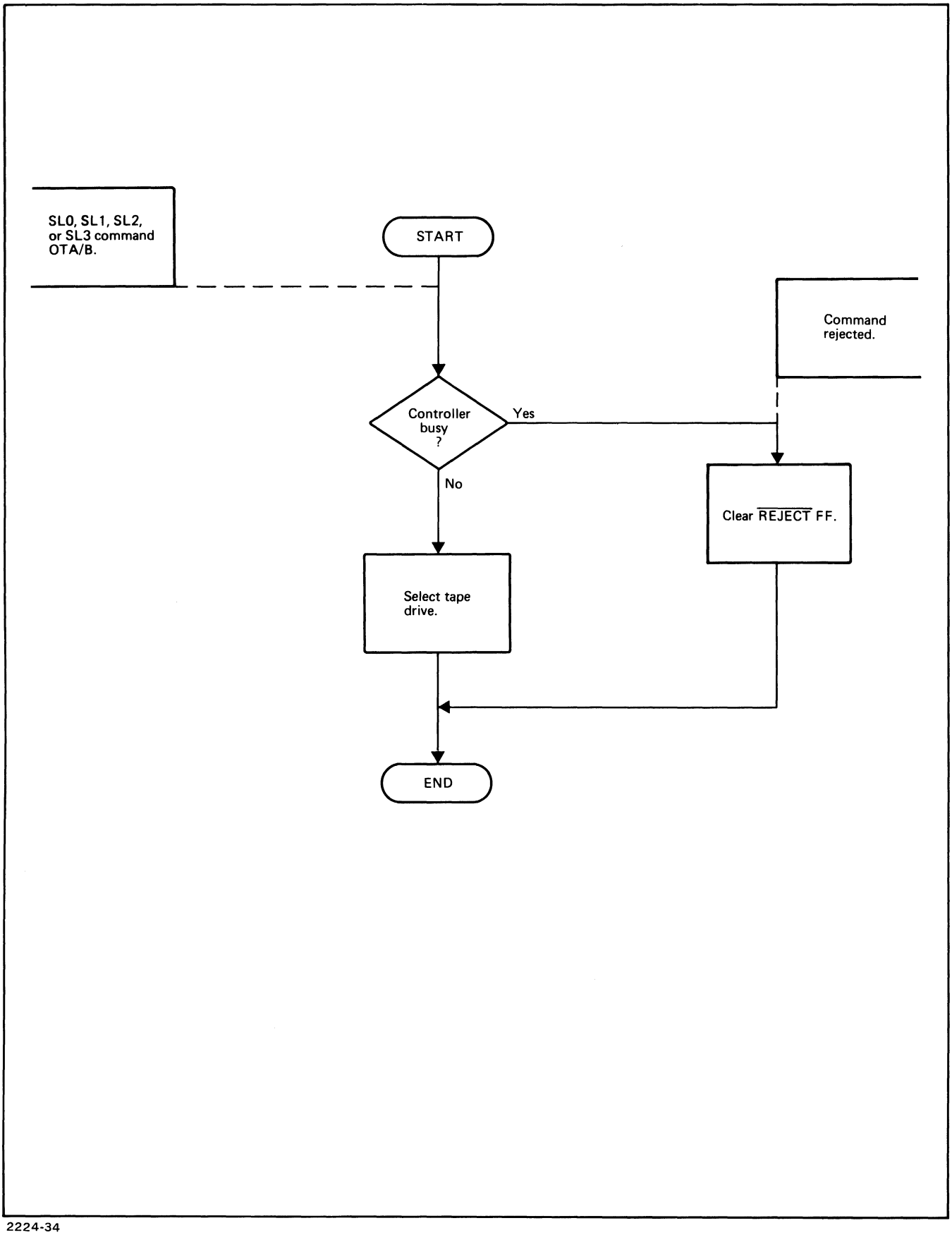


Figure 4-23. Unit Select Flowchart

SECTION V
MAINTENANCE

5-1. INTRODUCTION

This section provides maintenance information for the HP 13183B Digital Magnetic Tape Unit Interface Kit. Also included in this section are references to pertinent information in other manuals.

5-2. GENERAL SERVICING INFORMATION

Ensure that the PCA's are firmly seated in their slots with their extractor handles locked. All cable connectors should be firmly seated.

When performing maintenance on the interface kit observe the following warning and caution.

WARNING

Ensure that the ground for any test equipment used is connected to the same ground as that used in the computer. Failure to heed this warning may result in injury or death.

CAUTION

Turn computer power off before removing PCA's from the computer.

5-3. SERVICING EQUIPMENT

Tools, test equipment and supplies useful in servicing the interface kit are listed in table 5-1. Items normally carried by the field service man are not included in table 5-1.

5-4. PRINCIPAL SERVICING POINTS

The principal servicing points for the interface kit are presented in figure 5-5 (Interface Diagram) and listed in tables 5-6 through 5-9.

5-5. PREVENTIVE MAINTENANCE

Detailed preventive maintenance procedures and schedules are provided in the applicable computer documentation. There are no separate preventive maintenance procedures to be performed on the interface PCA's.

5-6. TROUBLESHOOTING

Troubleshooting the interface is accomplished by performing the diagnostic program procedure and analyzing the error halts that occur as the test is being run. To further isolate a malfunction, refer to the schematic diagrams and parts location diagrams in figures 5-1 through 5-4. Tables 5-10 and 5-11 list the replaceable parts for the mag tape 1 and mag tape 2 PCA's, respectively.

Paragraph 1-4 contains a list of related documents pertinent to the interface kit. In addition, table 5-2 presents a list of flip-flops and one-shots and their major functions. Tables 5-3 through 5-5 define the mnemonics associated with the tape unit, interface kit, and HP 21MX-Series Computers.

5-7. DIAGNOSTICS

Procedures for running the magnetic tape diagnostic are contained in the *HP 13181/183 Diagnostic Manual*, part number 13183-90095.

Table 5-1. Recommended Test Equipment and Servicing Devices

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Dual-trace oscilloscope	Rise time: ≤10 ns. Vertical deflection: 1 volt/division and 10 volts/division (including attenuator probe, if used). Horizontal sweep speed: 0.1 microsecond/division to 1 second/division.	HP 180A Oscilloscope with 10004A Probe and the following plug-in units. HP 1801A Dual Channel Vertical Amplifier HP 1820A Time Base or HP 1821A Time Base and Delay Generator.
Digital voltmeter	At least 4-digit readout. Minimum input resistance: 10 megohms. Full-scale ranges: 9.999 and 99.99 V dc.	HP 3465A/B Digital Voltmeter
Logic probe	Indication: logic true > + 1.4 volts.	HP 10525A
IC test clip	None	None

Table 5-2. Flip-Flop and One-Shot Functions

FLIP-FLOP	FUNCTIONS
BIT (0:12)	These flip-flops store the control bits and commands from the computer.
BUSY	The Busy flip-flop is set when the interface is executing a command.
CCTL	The Command Control flip-flop is set when the interface is to execute the command that has been transferred.
CFLB	The Command Flag Buffer flip-flop is set when the command has been executed or the interface requires service from the computer.
CFLG	The Command Flag flip-flop is set at CPU T2 time (ENF) when the CLFB flip-flop is set.
CIRQ	The Command Interrupt Request flip-flop is set to request service from the computer.
DATA ERR	The Data Error status latch is set during read if a MTE or parity error occurs during an illegal state, or during write if an STE or odd number of bytes occurs.
DCTL	The Data Control flip-flop is set to enable data transfers between the interface and the tape unit.
DFLB	The Data Flag Buffer flip-flop is set to request a data transfer to or from the computer.
DFLG	The Data Flag flip-flop is set when the DFLB flip-flop is set and the ENF signal from the computer is true.
DLY ENB	The Delay Enable flip-flop is set to enable the stop delay counter.
EOR	The End Of Record is set when the tape unit detects an end of record (end of block).

Table 5-2. Flip-Flop and One-Shot Functions (Continued)

FLIP-FLOP	FUNCTIONS
FILE	The File flip-flop is set when a file mark (tape mark) is to be written on tape or when a file is to be spaced over.
FWD	The Forward flip-flop is cleared whenever tape is moved forward.
GAP	The Gap flip-flop is cleared when a gap is to be written on tape.
ID ENBL	The Identification Burst Enable flip-flop is set to enable the logic associated with writing the ID burst.
LPFF	The Load Point flip-flop is set when the tape is positioned at load point.
PREAM	The Preamble flip-flop is set when the interface is writing a preamble.
RC1	The Read Clock 1 one-shot delays the tape drive read clock.
RC2	The Read Clock 2 one-shot delays RC1 and with the U/L flip-flop reads data into the upper or lower read buffer.
REJECT	The Reject flip-flop is cleared when a command is issued from the computer which the interface cannot execute.
REV	The Reverse flip-flop is cleared when the tape is moved backward (except rewind).
REW	The Rewind flip-flop is set when the command from the computer is a rewind or rewind off line.
STE	The Single Track Error flip-flop is set if the tape unit detects a single track error on tape.
TM	The Tape Mark flip-flop is set if the tape unit detects a tape mark (file mark).
TMG ERR	The Timing Error flip-flop is set when the data flag flip-flop is not acknowledged within one byte period.
TWAS	The Time Write After Start flip-flop (and pulse) enables the write data or write file mark logic.
UPPR	The Upper flip-flop determines whether the upper or the lower half of the 16-bit byte from the computer is to be loaded into the 8-bit buffer to the tape unit.
WRITE	The Write flip-flop is set whenever tape is to be written on (includes GAP).

Table 5-3. Tape Unit Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
CF	Forward Command	SFP	File Protect Status
CL	Off Line Command	SL	On Line Status
CR	Reverse Command	SLP	Load Point Status
CRW	Rewind Command	SR	Ready Status
CS0-CS3	Select Unit 0 thru 3	SRW	Rewind Status
EOB	End of Block	STE	Single Track Error
IDB	ID Burst	TM	Tape Mark
MTE	Multiple Track Error	WC	Write Clock
RC	Read Clock	WDP	Write Data, Channel P
RDP	Read Data, Channel P	WD0	Write Data, Channel 0
RD0	Read Data, Channel 0	WD1	Write Data, Channel 1
RD1	Read Data, Channel 1	WD2	Write Data, Channel 2
RD2	Read Data, Channel 2	WD3	Write Data, Channel 3
RD3	Read Data, Channel 3	WD4	Write Data, Channel 4
RD4	Read Data, Channel 4	WD5	Write Data, Channel 5
RD5	Read Data, Channel 5	WD6	Write Data, Channel 6
RD6	Read Data, Channel 6	WD7	Write Data, Channel 7
RD7	Read Data, Channel 7	WSW	Set Write Command
SET	End of Tape Status		

Table 5-4. Controller Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
ACI	Address Command Input	EOR	End of Record
ADSC	Address Command Channel	FILE	FILE Operation
ADSD	Address Data Channel	FM	File Mark
BOT	Beginning of Tape (Load Point)	FWD	Forward
CCP	Control Clock Pulse	IDB	Identification Burst
CIRQ	Command Interrupt Request	IDB ENBL	Identification Burst Enable
CFLB	Clear Flag Buffer	MCP	Master Clock Pulse
CFLG	Command Flag	RC	Read Clock
CLR	Clear (Controller)	REV	Reverse
CRS	Control Reset	SCP	Spacing Clock Pulse
DCL	Data Control	SFB	Set Flag Buffer
DFL	Data Flag	SFC	Skip if Flag is Clear
DFLB	Data Flag Buffer	SFS	Skip if Flag is Set
DFLG	Data Flag	SRS	Start Reset
DIRQ	Data Interrupt Request	TWAS	Time Write After Start
DTF	Data Transfer Flag	WFM	Write File Mark
EOC	Even-Odd Clock	WRT	Write

Table 5-5. HP 21MX Series Computer Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
CLC	Clear Control FF	POPIO	Power On Preset I/O
CLF	Clear Flag FF	PRL	Priority Low
CRS	Control Reset	PRH	Priority High
EDT	End Data Transfer	SCL	Select Code Least Significant Digit (lower address)
ENF	Enable Flag	SCM	Select Code Most Significant Digit (lower address)
FLGH	Flag Signal, Higher Select Code	SFC	Skip Flag Clear (Skip next instruction if Flag FF is reset.)
FLGL	Flag Signal, Lower Select Code	SFS	Skip Flag Set (Skip next instruction if Flag FF is set.)
IAK	Interrupt Acknowledge	SIR	Set Interrupt Request
IEN	Interrupt Enable	SKF	Skip Flag (Skip next instruction if SFS or SFC test is true.)
IOBI (0:15)	I/O Bus Input, Bits 0 thru 15	SRQ	Service Request
IOBO (0:15)	I/O Bus Output, Bits 0 thru 15	STC	Set Control FF
IOG	I/O Group Instruction	STF	Set Flag FF
IOI	I/O Input Instruction		
IOO	I/O Output Instruction		
IRQH	Interrupt Request, Higher Select Code		
IRQL	Interrupt Request, Lower Select Code		
PON	Power On Normal		

Table 5-6. Mag Tape 1 Connector J1 Pin/Signal List

J1-PIN	SIGNAL DEFINITION	MNEMONIC	J1-PIN	SIGNAL DEFINITION	MNEMONIC
A	Select Unit 0	CS0	1	Ready Status	SR
B	Select Unit 1	CS1	2	Rewind Status	SRW
C	Select Unit 2	CS2	3	Not used	
D	Select Unit 3	CS3	4	On Line Status	SL
E	Command Forward	CF	5	File Protect Status	SFP
F	Command Reverse	CR	6	Not used	
H	End Of Block Disable	EOB DIS	7	Not used	
J	Not used		8	End of Record	EOR
K	File Mark	FM	9	Data Control	DCL
L	Address Command Input	ACI	10	File Operation	FILE
M	Start Reset	SRS	11	Not used	
N	Not used		12	Not used	
P	Identification Burst Enable	IDB ENBL	13	Not used	
R	Time Write After Start	TWAS	14	Not used	
S	Off Line Command	CL	15	End of Tape Status	SET
T	Command Rewind	CRW	16	Load Point Status	SLP
U	Address Data Channel	ADSD	17	Not used	
V	Set Flag Buffer	SFB	18	Not used	
W	Write Command	WRT	19	Not used	
X	Set Write Command	WSW	20	Not used	
Y	Control Clock Pulse	CCP	21	Not used	
Z	Data Control and Data Flag	DCL•DFL	22	Not used	
AA	Master Clock Pulse	MCP	23	Not used	
BB	Even Odd Clock	EOC	24	Not used	

Note: Pins 11 thru 14 and 17 thru 24 are connect to ground.

Table 5-7. Mag Tape 1 Connector P1 Pin/Signal List

P1-PIN	SIGNAL DEFINITION	MNEMONIC	P1-PIN	SIGNAL DEFINITION	MNEMONIC
1,2	Common		31	I/O Bus Input, Bit 10	IOBI 10
3	Priority Low	PRL	32	Set Interrupt Request	SIR
4	Flag, Lower Select Code	FLGL	33	Interrupt Request, Higher Select Code	IRQH
5	Skip next instruction if Flag is Clear	SFC	34	Select Code Least significant digit	HSCL
6	Interrupt Request, Lower Select Code	IRQL	35	I/O Bus Output, Bit 0	IOBO 0
			37	Select Code Most significant digit	HSCM
7	Clear Flag FF	CLF	38	I/O Bus Output, Bit 1	IOBO 1
8	Interrupt Enable	IEN	39,40	+4.85 Volts	+4.85V
9	Set Flag FF	STF	41	I/O Bus Output, Bit 2	IOBO 2
10	Interrupt Acknowledge	IAK	45	I/O Bus Output, Bit 3	IOBO 3
12	Skip next instruction if SFS or SFC condition met	SKF	46	Enable Flag	ENF
			47,48	-2 Volts	-2V
13	Control Reset	CRS	49	Flag signal, Higher Select Code	FLGH
14	Select Code Most significant digit	LSCM	51	I/O Bus Output, Bit 5	IOBO 5
15	I/O Group instruction	IOG	52	I/O Bus Output, Bit 7	IOBO 7
16	Select Code Least significant digit	LSCL	53	I/O Bus Output, Bit 6	IOBO 6
			54	I/O Bus Output, Bit 8	IOBO 8
17	Power On Preset to I/O	POPIO	55	I/O Bus Output, Bit 11	IOBO 11
19	Service Request	SRQ	56	I/O Bus Output, Bit 9	IOBO 9
20	I/O Output instruction	IOO	57	I/O Bus Output, Bit 12	IOBO 12
21	Clear Control FF	CLC	58	I/O Bus Output, Bit 10	IOBO 10
22	Set Control FF	STC	59	Not used	
23	Priority High	PRH	62	End Data Transfer	EDT
24	I/O Input instruction	IOI	64	I/O Bus Input, Bit 3	IOBI 3
25	Skip next instruction if Flag FF is Set	SFS	66	Power On Normal	PON
			79	I/O Bus Input, Bit 13	IOBI 13
26	I/O Bus Input, Bit 0	IOBI 0	80	I/O Bus Input, Bit 5	IOBI 5
27	I/O Bus Input, Bit 8	IOBI 8	81	I/O Bus Input, Bit 6	IOBI 6
28	I/O Bus Input, Bit 9	IOBI 9	82	I/O Bus Input, Bit 14	IOBI 14
30	I/O Bus Input, Bit 2	IOBI 2	85,86	Common	

Notes:
1. Pins listed as pairs are connected together on the slot connector and on the interface PCA.
2. Corresponding IOBO and IOBI bit lines are connected together on the slot connector.

Table 5-8. Mag Tape 2 Connector J1 Pin/Signal List

J1-PIN	SIGNAL DEFINITION	MNEMONIC	J1-PIN	SIGNAL DEFINITION	MNEMONIC
A	Address Command Input	ACI	1	Write Data 3	WD3
B	Write Data 6	WD6	2	Write Data 4	WD4
C	Write Data 5	WD5	3	Write Data 2	WD2
D	Write Data P	WDP	4	Write Data 7	WD7
E	Write Data 0	WD0	5	Write Data 1	WD1
F	Time Write After Start	TWAS	6	Multiple Track Error	MTE
H	Single Track Error	STE	7	Not used	
J	Write Clock	WC	8	Not used	
K	Data Control	DCL	9	Not used	
L	Control Clock Pulse	CCP	10	Start Reset	SRS
M	Write	WRT	11	Read Data Parity	RDP
N	File	FILE	12	Not used	
P	Set Flag Buffer	SFB	13	Not used	
R	File Mark	FM	14	Not used	
S	Address Data Channel	ADSD	15	Not used	
T	Master Clock Pulse	MCP	16	Data Control and Data Flag	DCL•DFL
U	Tape Mark	TM	17	Even Odd Clock	EOC
V	End of Block	EOB	18	Identification Burst	IDB
W	Not used		19	End Of Record	EOR
X	Read Data 2	RD2	20	Read Data 1	RD1
Y	Read Data 0	RD0	21	Read Data 3	RD3
Z	Read Clock	RC	22	Identification Burst Enable	IDB ENB
AA	Read Data 5	RD5	23	Read Data 7	RD7
BB	Read Data 4	RD4	24	Read Data 6	RD6

Note: Pins 7, 8, 9 and 12 thru 15 are connected to ground.

Table 5-9. Mag Tape 2 Connector P1 Pin/Signal List

P1-PIN	SIGNAL DEFINITION	MNEMONIC	P1-PIN	SIGNAL DEFINITION	MNEMONIC
1,2	Common		54	I/O Bus Output, Bit 8	IOBO 8
20	I/O Output instruction	IOO	55	I/O Bus Output, Bit 11	IOBO 11
24	I/O Input instruction	IOI	56	I/O Bus Output, Bit 9	IOBO 9
26	I/O Bus Input, Bit 0	IOBI 0	57	I/O Bus Output, Bit 12	IOBO 12
27	I/O Bus Input, Bit 8	IOBI 8	58	I/O Bus Output, Bit 10	IOBO 10
28	I/O Bus Input, Bit 9	IOBI 9	60	I/O Bus Input, Bit 11	IOBI 11
29	I/O Bus Input, Bit 1	IOBI 1	61	I/O Bus Output, Bit 13	IOBO 13
30	I/O Bus Input, Bit 2	IOBI 2	64	I/O Bus Input, Bit 3	IOBI 3
31	I/O Bus Input, Bit 10	IOBI 10	65	I/O Bus Output, Bit 14	IOBO 14
35	I/O Bus Output, Bit 0	IOBO 0	74	I/O Bus Output, Bit 15	IOBO 15
38	I/O Bus Output, Bit 1	IOBO 1	77	I/O Bus Input, Bit 4	IOBI 4
39,40	+4.85 Volts	+4.85V	78	I/O Bus Input, Bit 12	IOBI 12
41	I/O Bus Output, Bit 2	IOBO 2	79	I/O Bus Input, Bit 13	IOBI 13
42	I/O Bus Output, Bit 4	IOBO 4	80	I/O Bus Input, Bit 5	IOBI 5
45	I/O Bus Output, Bit 3	IOBO 3	81	I/O Bus Input, Bit 6	IOBI 6
47,48	-2V	-2V	82	I/O Bus Input, Bit 14	IOBI 14
51	I/O Bus Output, Bit 5	IOBO 5	83	I/O Bus Input, Bit 15	IOBI 15
52	I/O Bus Output, Bit 7	IOBO 7	84	I/O Bus Input, Bit 7	IOBI 7
53	I/O Bus Output, Bit 6	IOBO 6	85,86	Common	

Notes:
1. Pins listed as pairs are connected together on the slot connector and on the interface PCA.
2. Corresponding IOBO and IOBI bit lines are connected together on the slot connector.

Table 5-10. Mag Tape 1 PCA Replaceable Parts

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
C1, C3 thru C11 C13, C14, C16 thru C20, C22 thru C25, C29 thru C33	CAPACITOR: Fixed .01uF 100V	0160-2055
C2, C12, C15 C26	CAPACITOR: Fixed 4.7uF, 35 Vdc	0180-0100
C21	CAPACITOR: Fixed 330 pF	0160-3572
C27	CAPACITOR: Fixed 27 pF, 300V	0160-2306
C28	CAPACITOR: Fixed 220 pF	0160-0134
R1, R3, R6, R7, R9, R15	RESISTOR: Network 1.5K	1810-0276
R2, R5, R14	RESISTOR: 1K	0683-1025
R4	RESISTOR: Network 240-560	1810-0127
R8, R10, R20 thru R29	RESISTOR: Fixed 1.5K	0683-1525
R11, R12	RESISTOR: Fixed 4.7K	0683-4725
R13	RESISTOR: Fixed 10K	0683-1035
R16, R17	RESISTOR: Fixed 330	0683-3315
U12	IC: SN74LS51N	1820-1210
U13, U15, U46, U76	IC: SN7400N	1820-0054
U14, U86	IC: SN74LS08N	1820-1201
U16, U36	IC: SN7410N	1820-0068
U17, U22, U23, U32, U37, U44, U53, U63, U72, U84, U111	IC: SN74LS00N	1820-1197
U24, U32, U45, U52, U82, U105	IC: SN74LS74N	1820-1112
U25	IC: SN7451N	1820-0063
U26, U34, U85	IC: SN74LS20N	1820-1204
U27, U57, U67,	IC: DIGITAL DRIVER	1820-0758
U33, U66	IC: SN7432N	1820-0661
U35, U56, U93	IC: SN7404N	1820-0174
U43	IC: SN74LS02N	1820-1144

Table 5-10. Mag Tape 2 PCA Replaceable Parts (Continued)

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
U47, U65	IC: 7411PC	1820-1066
U54, U95, U114	IC: SN74107N	1820-0281
U55	IC: SN74LS54N	1820-1258
U61, U62, U71	IC: SN7438N	1820-0621
U64, U96, U104	IC: SN74LS10N	1820-1202
U73, U94, U106	IC: SN74LS11N	1820-1203
U75	IC: SN7408N	1820-0511
U77	IC: SN74273N	1820-1461
U81	IC: 8T13	1820-1080
U83	IC: SN7402N	1820-0328
U87	IC: SN74175N	1820-0839
U91, U116	IC: 74LS92N	1820-1420
U92	IC: SN74LS221N	1820-1437
U97	IC: SN74LS21N	1820-1205
U107, U112	IC: SN74LS51N	1820-1210
U113	IC: SN74160N	1820-0899
U115	IC: SN74LS393N	1820-2096
U117	IC: SN74LS293N	1820-1443
W3	JUMPER	1258-0124
Y1	CRYSTAL, 7.2 Mhz	0410-044
	PC EXTRACTOR: UPR	13181-40006
	PC EXTRACTOR: LWR	13183-40005

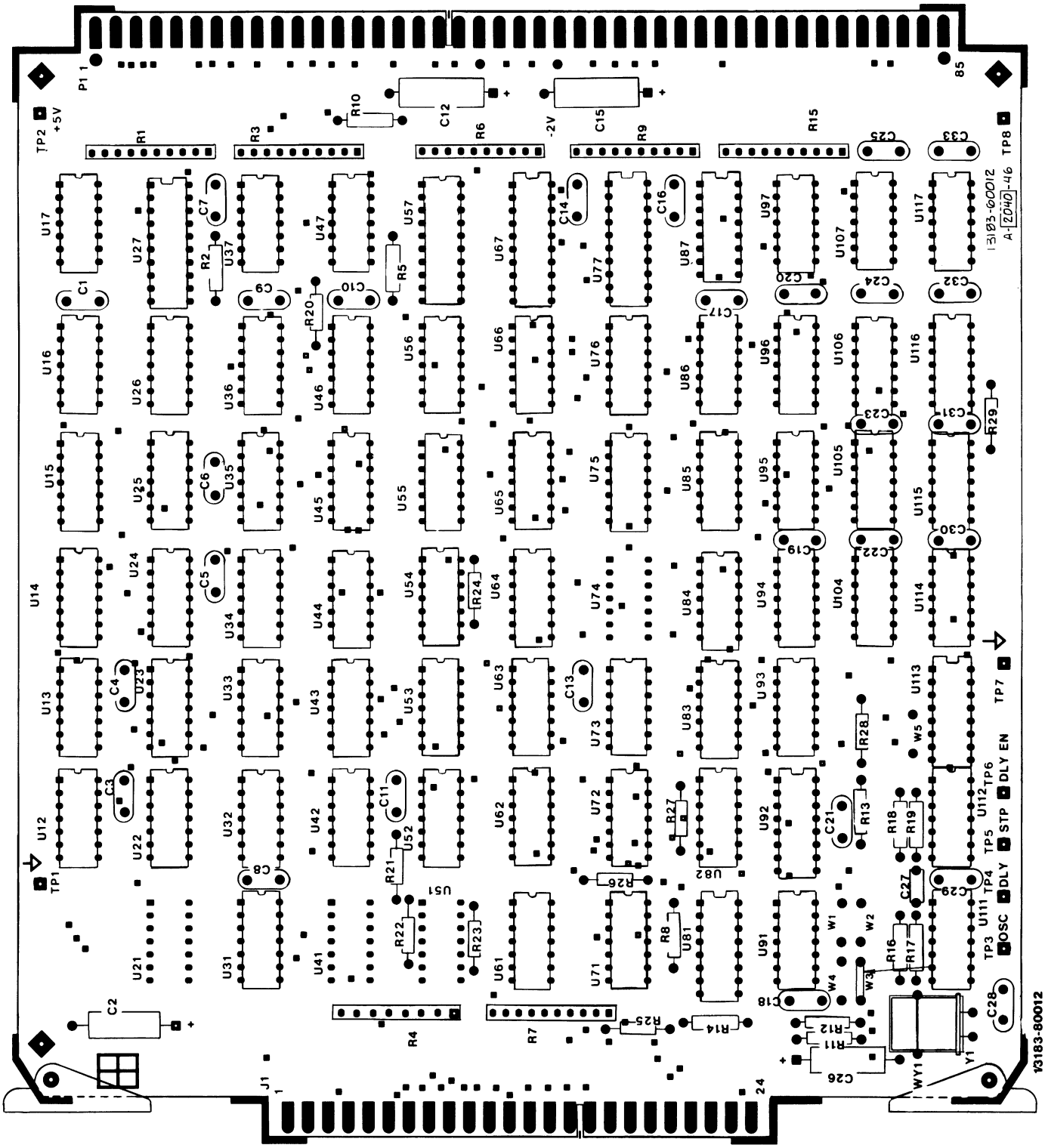


Figure 5-1. Mag Tape 1 PCA Parts Location Diagram

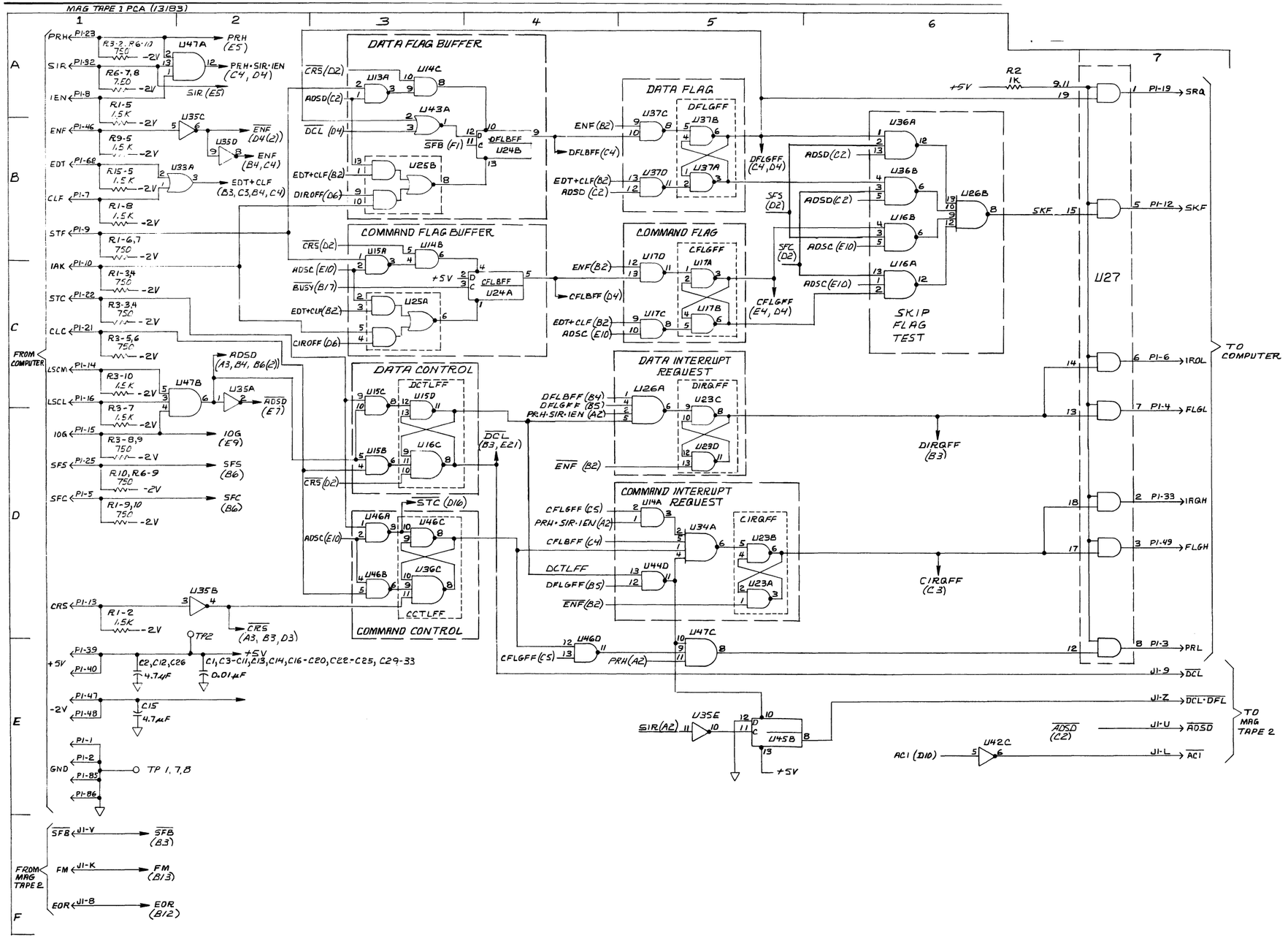
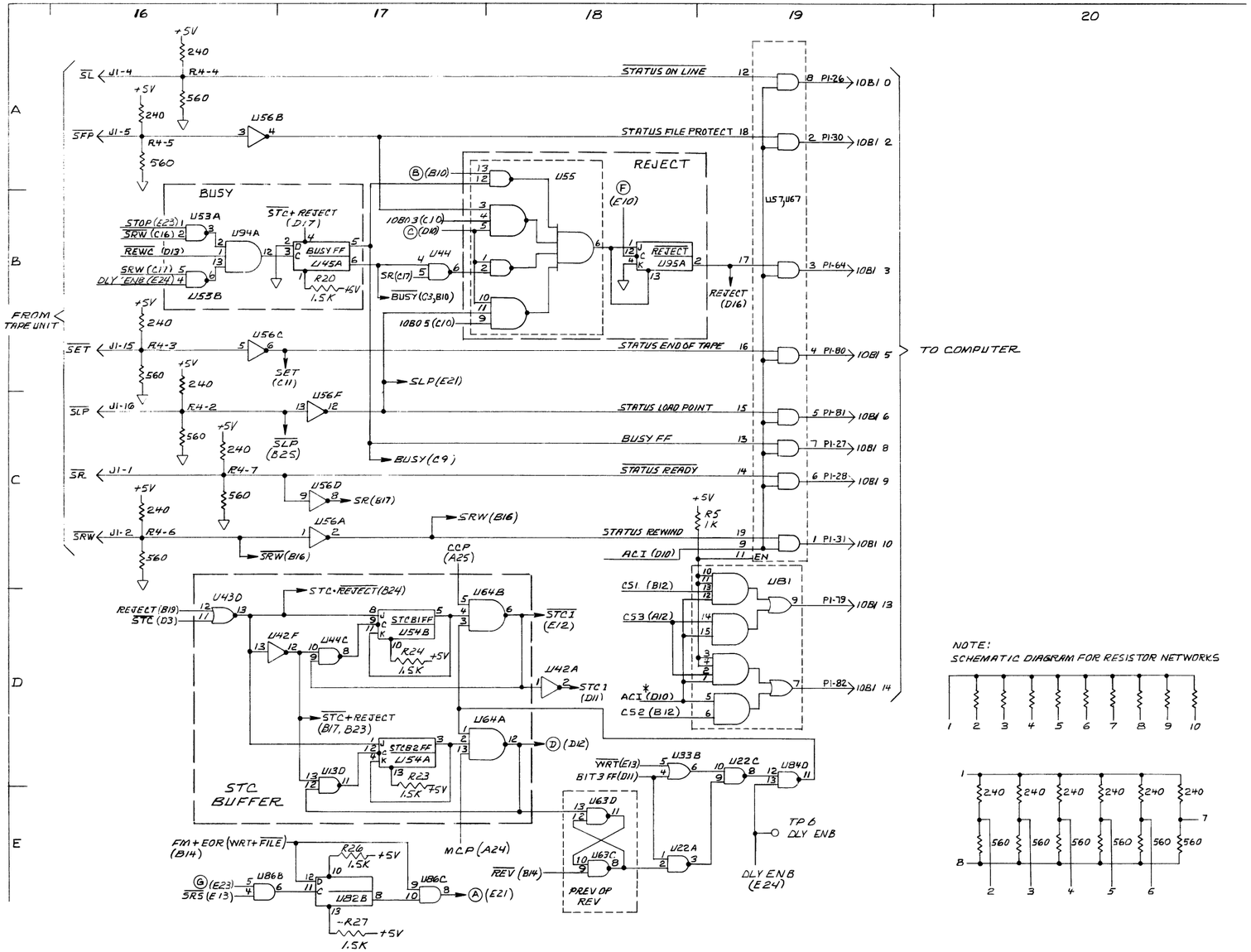


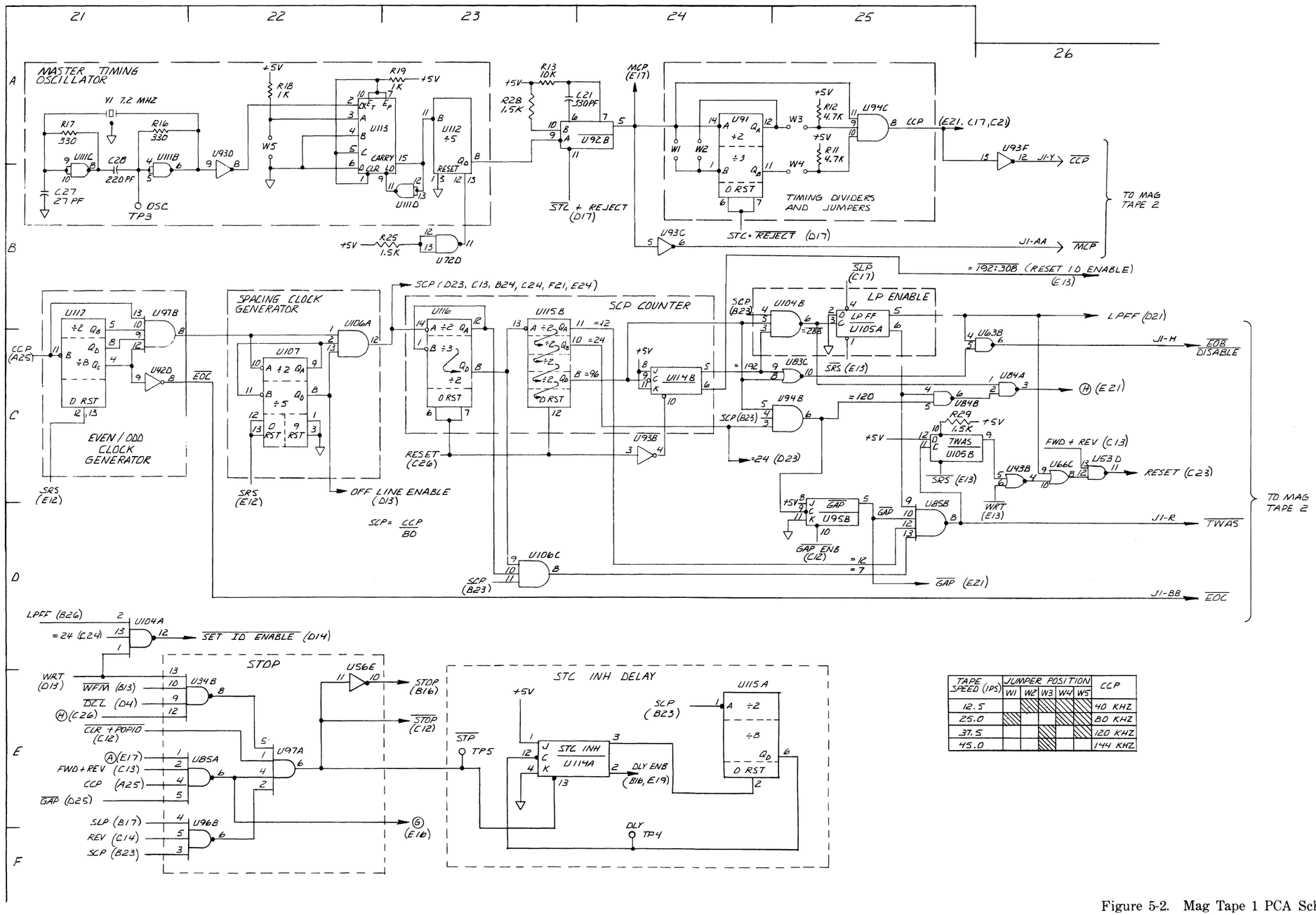
Figure 5-2. Mag Tape 1 PCA Schematic Diagram (page 1 of 4)

Figure 5-2. Mag Tape 1 PCA Schematic Diagram (page 2 of 4)



NOTE:
SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS

Figure 5-2. Mag Tape 1 PCA Schematic Diagram (page 3 of 4)



TAPE SPEED (IPS)	JUMPER POSITION W1	W2	W3	W4	W5	CCP
12.5						40 KHZ
25.0						80 KHZ
37.5						120 KHZ
45.0						144 KHZ

Figure 5-2. Mag Tape 1 PCA Schematic Diagram (page 4 of 4)

Table 5-11. Mag Tape 2 PCA Replacement Parts

REFERENCE DESIGNATION	DESCRIPTION HP	PART NO.
C1 thru C6, C9 thru C22 C24, thru C27 C29 thru C32 C35 thru C41	CAPACITOR: Fixed .01 uF	0160-2055
C7, C8, C23	CAPACITOR: Fixed 4.7 uF	0180-0100
C28	CAPACITOR: Fixed 27 pF	0160-2306
C33	CAPACITOR: Fixed 150 pF	0140-0196
C34	CAPACITOR: Fixed 560 pF	0160-3535
R1, R12, R13	RESISTOR: Fixed 1.5K	0683-1525
R2, R4, R6	RESISTOR: Network, 1.5K	1810-0276
R3, R5, R8	RESISTOR: Network, 240-560	1810-0127
R7, R9	RESISTOR: Fixed 10K	0683-1035
R10	RESISTOR: Fixed 10K	0683-1035
R11	RESISTOR: Fixed 4.7K	0683-4725
U12, U15, U36, U55, U75, U85, U104	IC: SN74LS32N	1820-1208
U13, U74, U101	IC: SN74LS04N	1820-1199
U14, U24, U35, U83	IC: SN74107N	1820-0281
U16, U45, U93	IC: SN74LS08N	1820-1201
U17	IC: SN74LS390N	1820-1991
U21	IC: SN74LS30N	1820-1207
U22	IC: SN74154N	1820-0495
U23	IC: SN74LS11N	1820-1203
U25, U84	IC: SN74LS10N	1820-1202
U26, U106	IC: SN74LS02N	1820-1144
U27	IC: SN74LS27N	1820-1206
U32, U42, U52	IC: SN7438N	1820-0621
U33, U43, U53	IC: SN74LS86N	1820-1211
U34	IC: SN74LS20N	1820-1204
U44, U66, U76	IC: SN74LS273N	1820-1730
U46, U56	IC: SN74LS157N	1820-1470

Table 5-11. Mag Tape 2 PCA Replacement Parts (Continued)

REFERENCE DESIGNATION	DESCRIPTION	HP PART NO.
U47, U57	IC: SN74273N	1820-1461
U54, U65	IC: SN74LS280N	1820-1859
U62	IC: SN7432N	1820-0661
U67, U77, U86 U87, U96, U97	IC: DIGITAL DRIVER	1820-0758
U72	IC: SN74LS21N	1820-1205
U73	IC: SN7408N	1820-0511
U81	IC: SN7414N	1820-1053
U82, U92	IC: SN74LS221N	1820-1437
U95	IC: SN74LS279N	1820-1440
U102, U103	IC: SN74LS161N	1820-1437
W1 thru W4	JUMPER	1258-0124

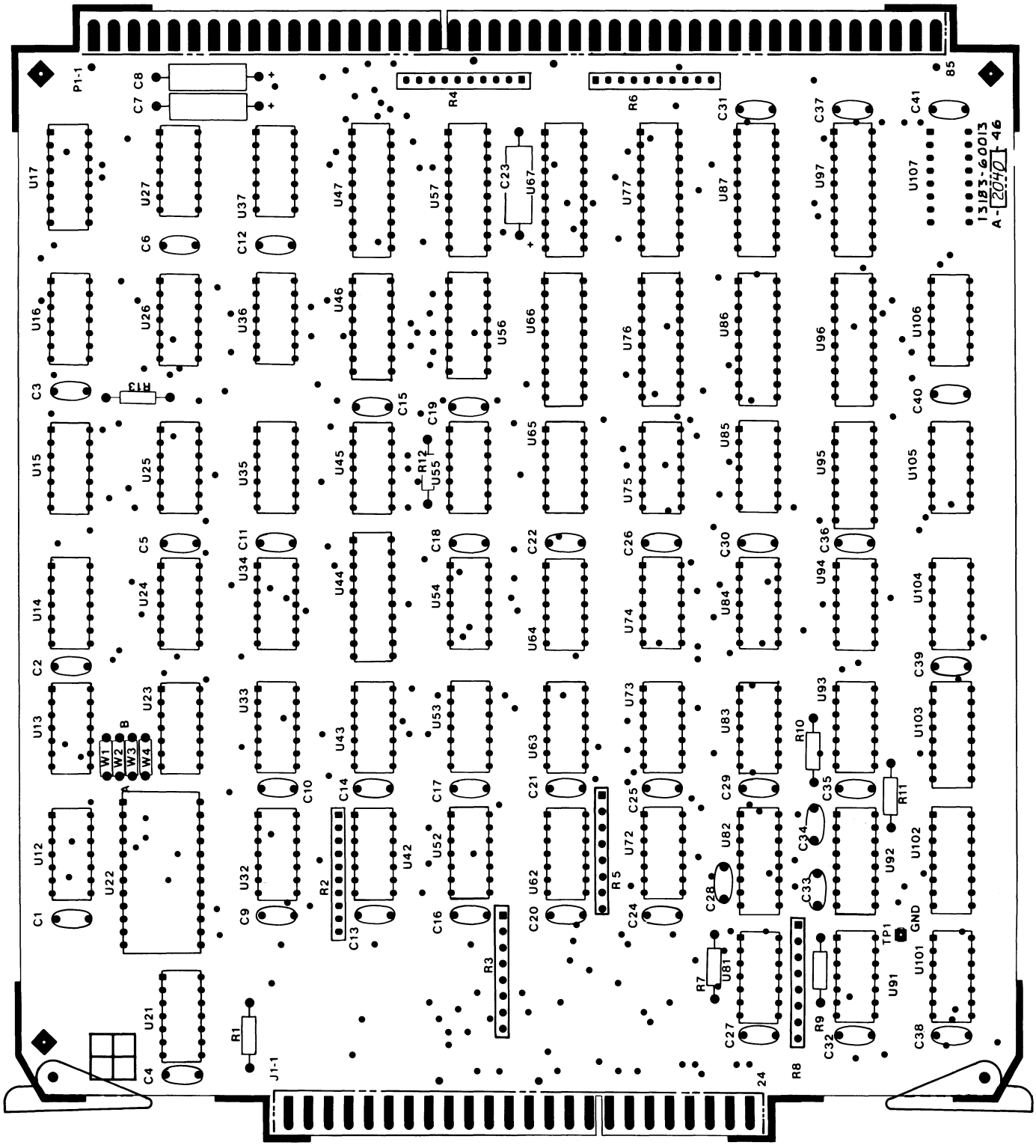


Figure 5-3. Mag Tape 2 PCA Parts Location Diagram

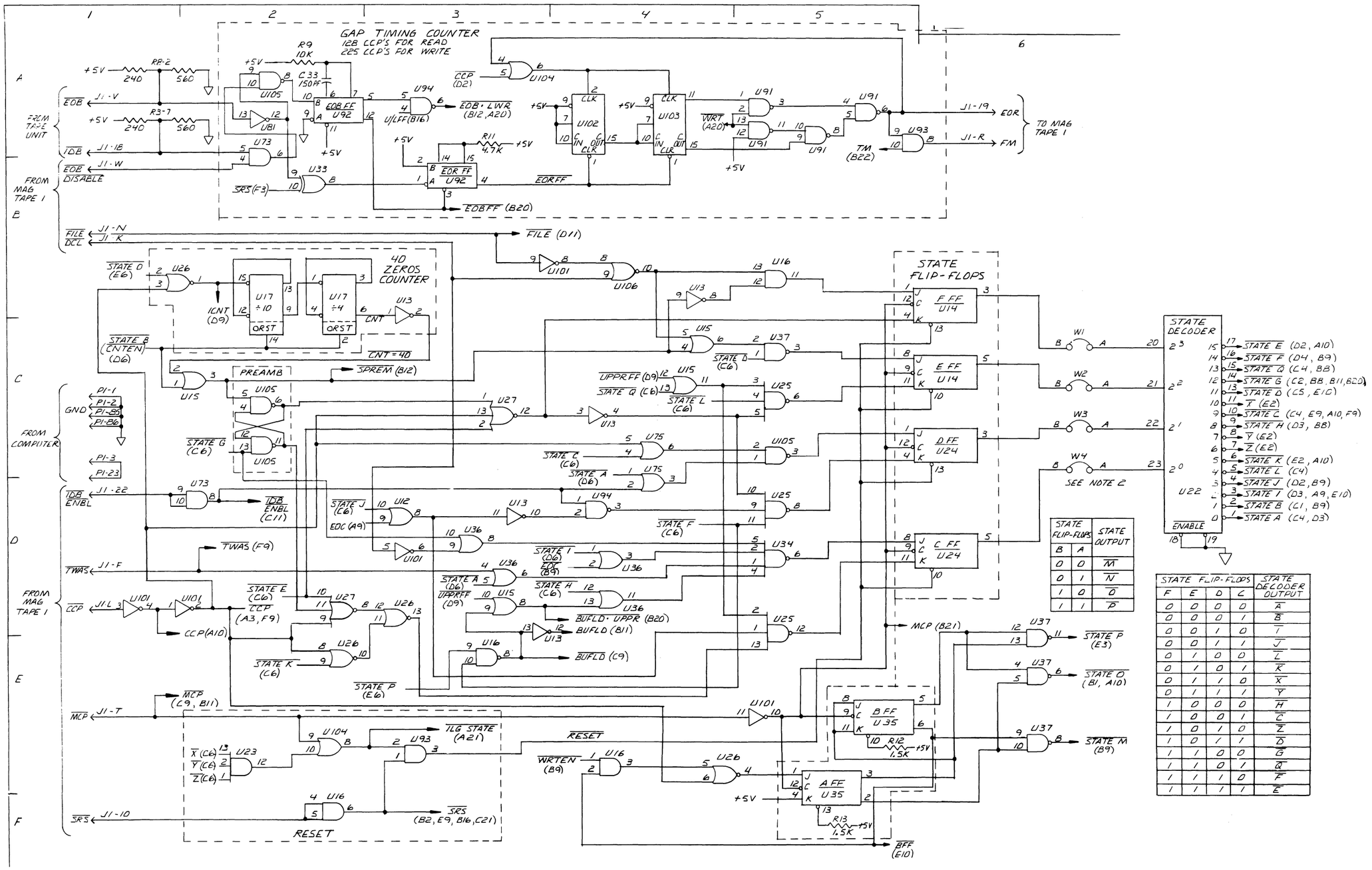


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (page 1 of 4)

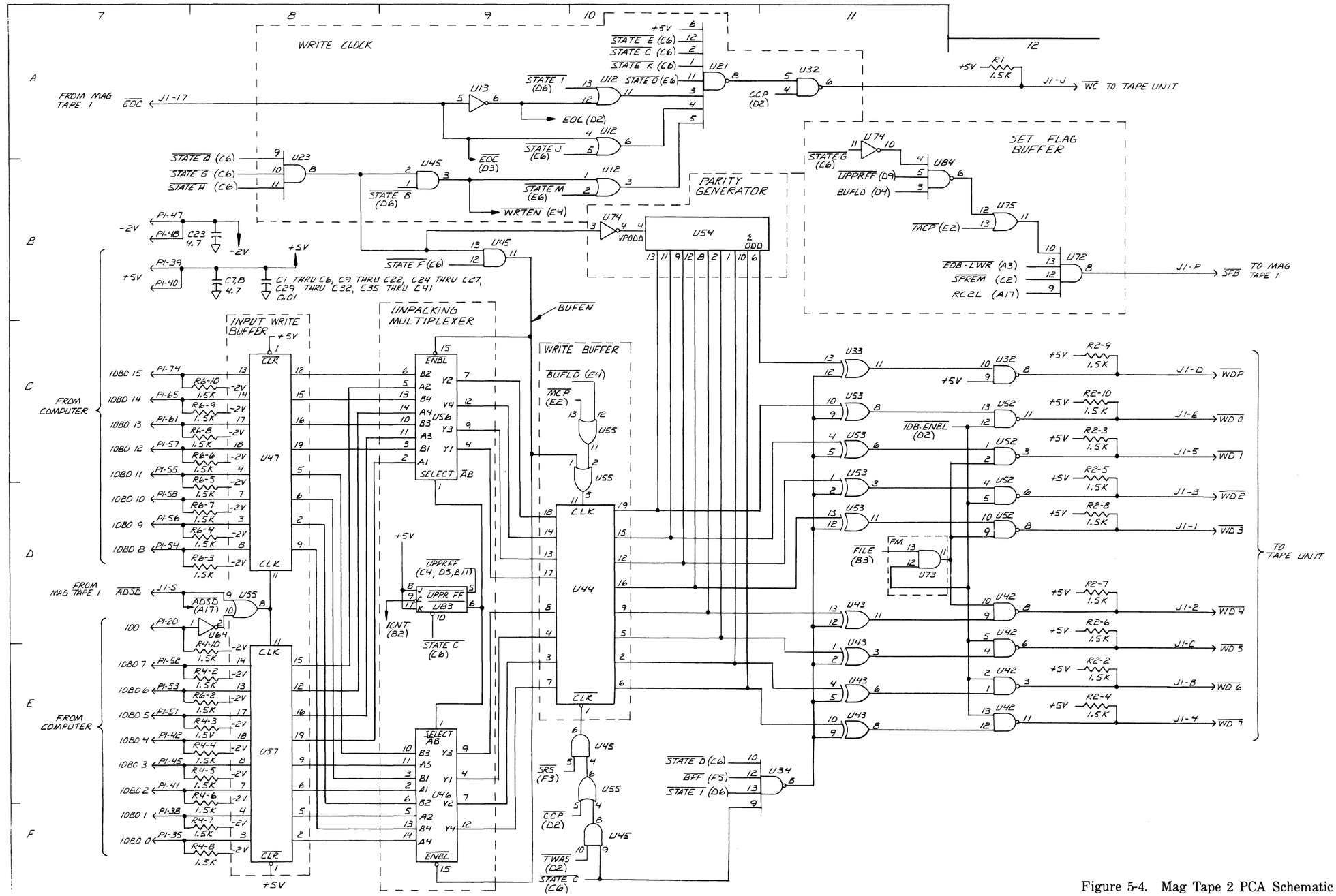


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (page 2 of 4)

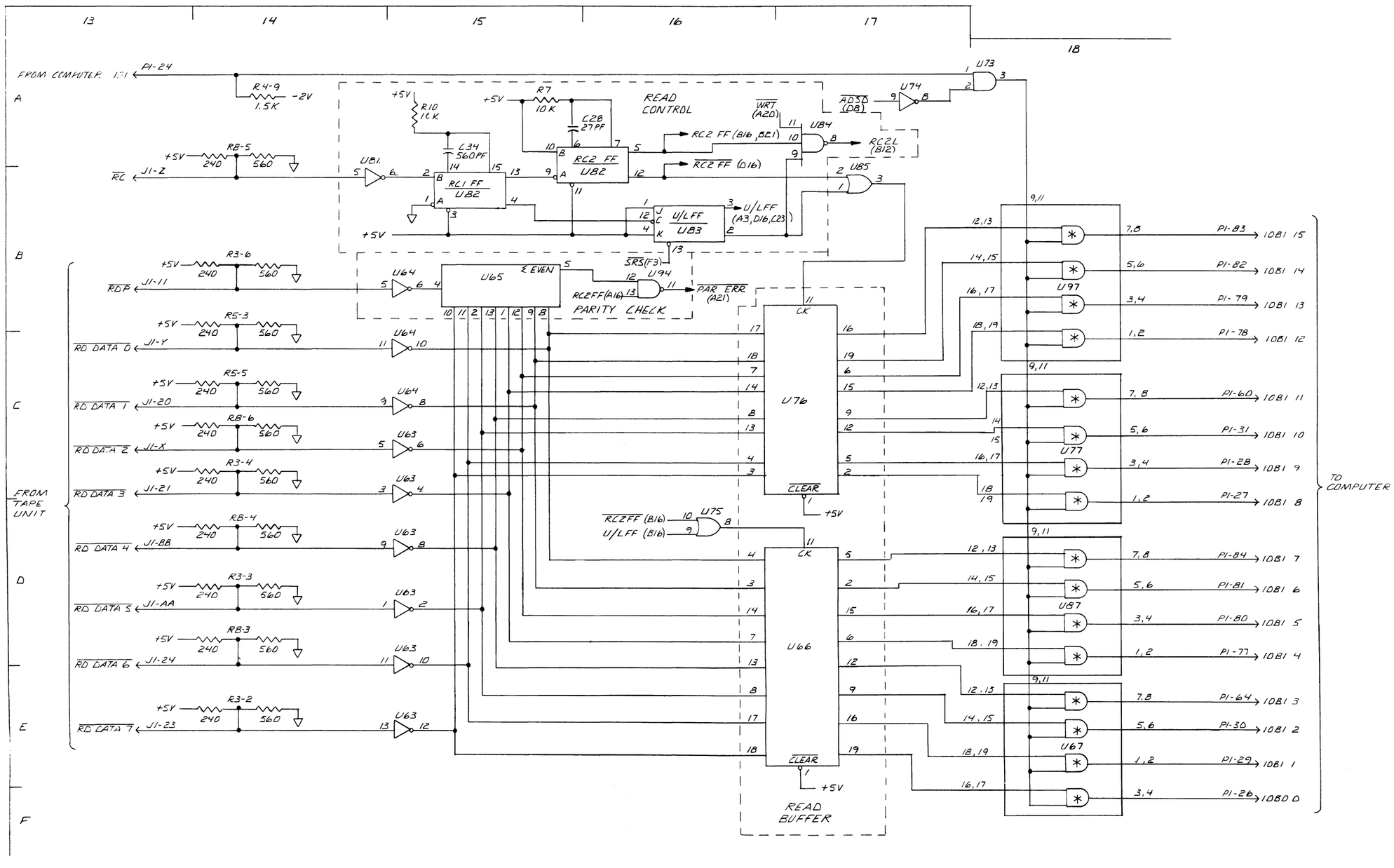


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (page 3 of 4)

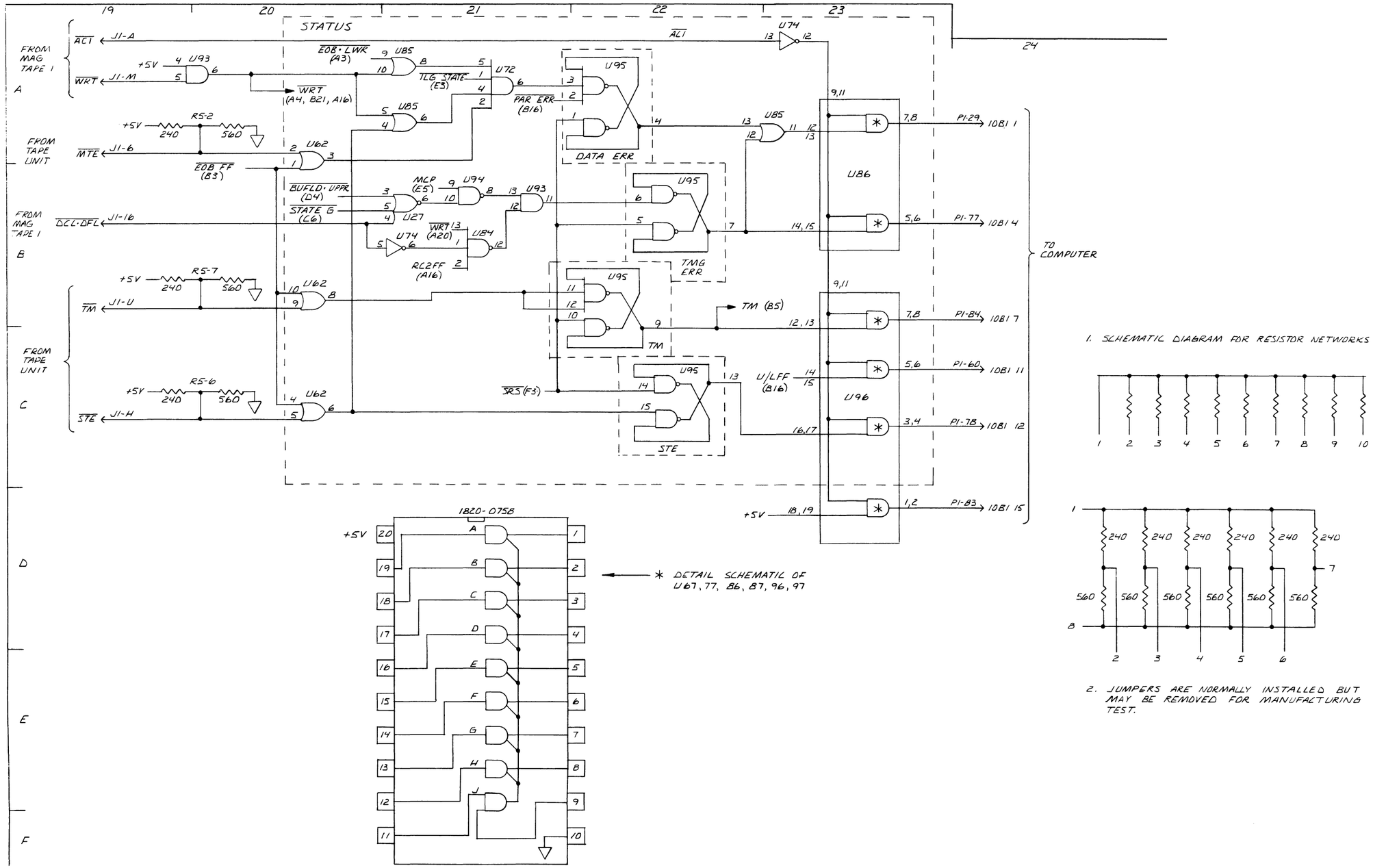


Figure 5-4. Mag Tape 2 PCA Schematic Diagram (page 4 of 4)

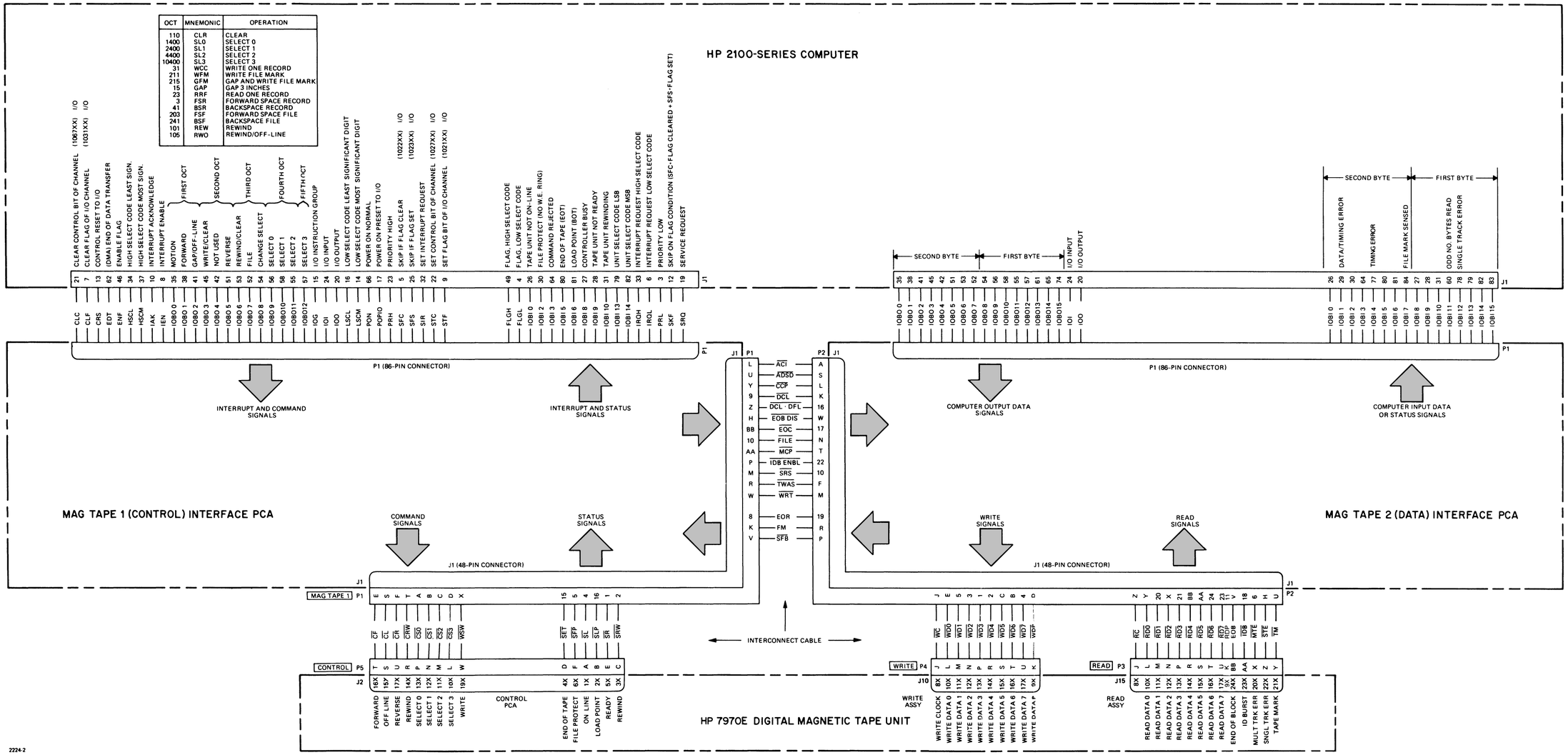


Figure 5-5. Interface Diagram

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section provides information for ordering replacement parts for the HP 13183B Digital Magnetic Tape Unit Interface Kit. Separate parts lists and parts location diagrams are provided for each printed-circuit assembly in section V of this manual. Parts are listed in these tables in alphanumeric order by reference designation. Table 6-1 is a complete parts list for the interface kit.

Table 6-1 lists the following information for each part:

a. Hewlett-Packard part number.

b. Description of the part.

Table 6-1. HP 13183B Digital Magnetic Tape Unit Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION
13183-60012	MAG TAPE 1 PCA (Refer to table 5-10).
13183-60013	MAG TAPE 2 PCA (Refer to table 5-11).
13183-60014	INTERCONNECTING CABLE
13183-90901	OPERATING AND SERVICE MANUAL

6-2. ORDER INFORMATION

To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Kit model number.

b. HP stock number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

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Arranged alphabetically by country

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C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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Martinez 1640 **BUENOS AIRES**
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Telex: 17595 BIONAR
Cable: HEWPACKARG
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1399 BUENOS AIRES
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Telex: 17595 BIONAR
M

Fate S.A. I.C.I.Electronica
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1095 BUENOS AIRES
Tel: 37-9020, 37-9026/9
Telex: 9234 FATEN AR
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Brisbane, Queensland Office

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Canberra, Australia Capital Territory Office

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BAHRAIN
Tel: 25503-250950
Telex: 84419
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Wael Pharmacy
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Tel: 256123
Telex: 8550 WAEL GJ
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B-1200 **BRUSSELS**
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Arturo Burhle 065
Casilla 16475
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Casilla 256-V
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P.O. Box 418
1A Lane 2, Luchang St.
Beiwei Rd., Xuanwu District
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Carrera 7 No. 48-75
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6

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