HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

13181A

DIGITAL MAGNETIC TAPE UNIT INTERFACE KIT

(FOR 2100 SERIES COMPUTERS)

Printed-Circuit Assemblies:

13181-60010, Series 1237
13181-60040, Series 1237
13181-60070, Series 1237

Note

This manual may be backdated to cover earlier versions of the interface kit by incorporating appropriate backdating information from appendix A.

13181-90000

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HEWLETT PACKARD

13181A

DIGITAL MAGNETIC TAPE UNIT INTERFACE KIT
OPERATING AND SERVICE MANUAL

UPDATING SUPPLEMENT

19 APR 1974

MANUAL IDENTIFICATION

Manual Serial No. Prefix: N/A

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Microfiche Part No.: 13181-90091

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to adapt the manual to equipment containing production improvements made subsequent to the printing of the manual and to correct manual errors. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left. For any given instrument serial number prefix, all change steps noted for prior serial number prefixes must be incorporated in addition to those for the given prefix.

INSTRUMENT CHANGES

Serial No. Prefix	Change
All (Errata)	1

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Series	Changes

Change 1 dated 19 April 1974.

11000 Wolfe Road, Cupertino, California 95014, Tel. (408) 257-7000, TWX 910-338-0221

Europe: 1217 Meyrin-Geneva, Switzerland • Cable "HEWPACKSA" Tel. (022) 41.54.00

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CHANGE	DESCRIPTION
1	Appendix A, change 32 of the backdating supplement should have the following information added: "Delete a daggar symbol (†) preceding C4 through 14, 16 (part no. 0160-2055) in table 5-3 and a note at the bottom of the page reading: "† Series 1213 and above only." This information plus the existing information in change 32 enables PCA's 13181-60040 and 13181-60070 to be changed from a 1213 series code to 1141.

LIST OF ILLUSTRATIONS

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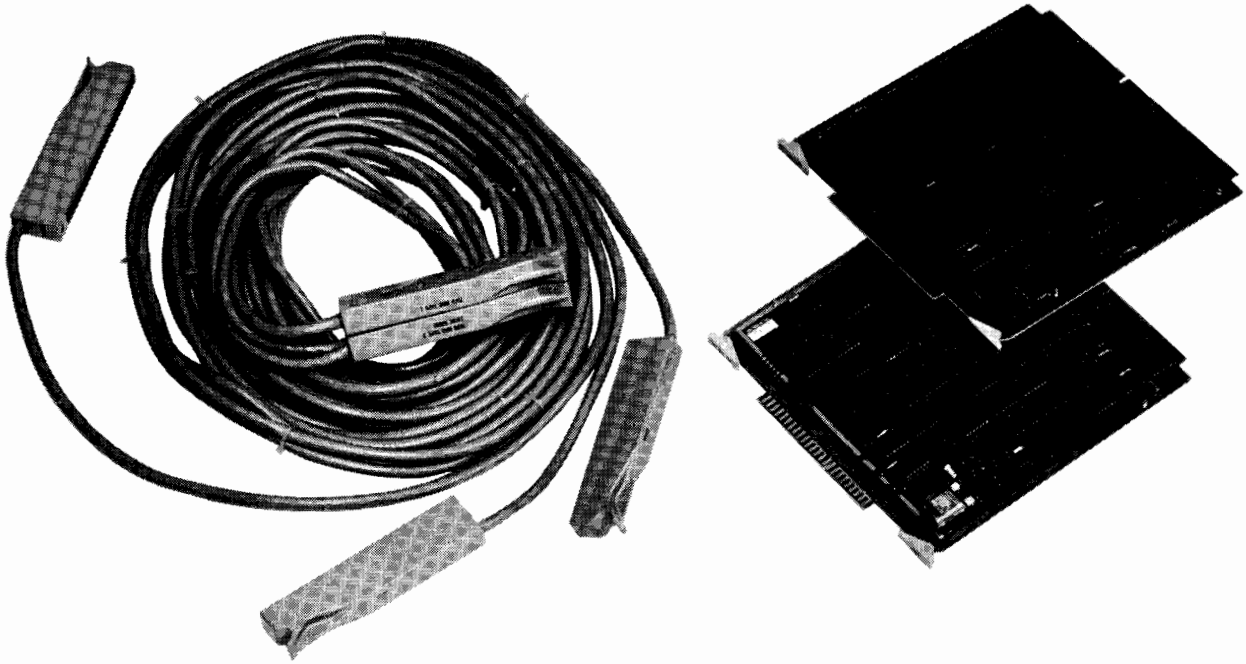


13181-42

Figure 1-1. Hewlett-Packard 13181A Tape Unit Interface Kit

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 13181A Tape Unit Interface Kit. Options 001, 002, and 003 for the interface kit are also covered in this manual.

1-3. GENERAL DESCRIPTION.

1-4. The HP 13181A Tape Unit Interface Kit interfaces up to four nine-track HP 7970 Series Digital Magnetic Tape Units with a single HP 2100 Series Computer. The interface kit includes two plug-in printed-circuit assemblies, which contain complete tape motion and data transfer control circuitry. An interconnect cable is provided to connect the printed-circuit assemblies to the tape unit. DMA is always required for 45 ips configurations. DMA is recommended for 37.5 ips tape units interfaced with an HP 2114 Computer. For all other configurations DMA may be used but is not required.

1-5. INTERFACE KIT CONTENTS.

1-6. The HP 13181A Tape Unit Interface Kit contains:

a. Mag Tape 1 (Control) Card.

Part No. 13181-60040 (37.5 ips; 25 ips, option 001; 12.5 ips, option 002)

Part No. 13181-60070 (45 ips, option 003).

b. Mag Tape 2 (Data) Card, Part No. 13181-60010.

c. Interconnect cable, Part No. 13181-60030.

d. Operating and Service Manual, Part No. 13181-90000.

1-7. IDENTIFICATION.

1-8. Hewlett-Packard utilizes five digits and a letter (00000A) to identify standard HP interface kits. Options to the standard kit are identified by a three-digit numerical suffix (001, 002, etc). If the HP designation on the interface kit does not correspond to the designation on the title page of this manual (13181A), the kit received is different from the kit described in this manual.

1-9. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the card. The letter identifies the etched trace pattern on the unloaded board. The four-digit series code identifies a particular configuration of the loaded printed-circuit board. The two-digit division code identifies division of Hewlett-Packard that manufactured the assembly. If the series code numbers do not correspond exactly with the code numbers on the title page of this manual, the assemblies differ from those described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office.

1-10. The interconnect cable is identified by a part number marked on one of the attached connectors.

1-11. OPTIONS.

1-12. The standard version of the interface kit is for use with tape units that operate at 37.5 ips. Option 001 provides the interface assemblies used for operation at 25 ips, option 002 for 12.5 ips, and option 003 for 45 ips. The only physical difference between the assemblies is in the jumper arrangement on the printed-circuit board and a different oscillator crystal in the case of 45 ips. All information in this manual applies to options 001, 002, and 003, as well as the standard interface kit, except where differences are noted.

1-13. SPECIFICATIONS.

1-14. Specifications for the interface kit are listed in tables 1-1 and 1-2.

Table 1-1. Interface Kit Specifications

POWER REQUIRED FROM COMPUTER

+4.5 Volt Supply: 2.9 amperes
-2.0 Volt Supply: 0.08 amperes

MINIMUM DATA RECORD

One computer word (two EBCDIC or ASCII data characters) plus CRCC and LRCC.

TAPE DENSITY

800 characters (bytes) per inch (Refer to table 1-2.)

TAPE SPEEDS

12.5, 25, 37.5, and 45 inches per second (Refer to table 1-2.)

OPERATING TEMPERATURE

0° C to 55° C

STORAGE TEMPERATURE

-40° C to 75° C

Table 1-2. Multispeed Characteristics

TAPE SPEED (IPS)	DATA CHANNEL BYTE RATE (IN CPS)	MAXIMUM DATA CHANNEL FLAG READ SERVICE TIME (IN μs)	DATA CHANNEL FLAG OCCURRENCE INTERVAL (IN μs)
12.5	10,000	82	200
25	20,000	41	100
37.5	30,000	27	67
45	36,000	22	56

SECTION II
INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides instructions for unpacking, initial receiving inspection, and installation of the HP 13181A Tape Unit Interface Kit. The computer and tape unit should be installed and in operating condition prior to interface kit installation.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

2-5. POWER REQUIREMENTS.

2-6. The two interface assemblies obtain operating power directly from the power supply of the associated computer. The assemblies require 2.9 amperes from the +4.5 volt source and 0.08 amperes from the -2.0 volt source. Prior to interface assembly installation, check that the assemblies will not overload the computer power supply. If the addition of the two assemblies will result in an overload, a power supply extender should be ordered for the computer. Prior to installation, ensure that the tape unit to be interfaced with the computer is close enough to allow the cable to be properly routed and connected.

2-7. INSTALLATION PROCEDURES.

2-8. Interface kit installation consists of inserting the Mag Tape 1 (control) printed-circuit assembly and Mag Tape 2 (cata) printed-circuit assembly into appropriate computer I/O slots and then routing the interconnect cable to the tape unit.

2-9. INTERFACE ASSEMBLY INSTALLATION.

2-10. Install the mag tape 1 and mag tape 2 printed-circuit assemblies as follows (see figure 2-1):

a. Turn off all power to the tape unit.

b. Set the computer power switch off.

c. Access the computer card cage and select the two adjacent slots corresponding to the desired I/O select codes. Make certain that all higher priority slots have either another I/O card or a priority jumper card installed.

CAUTION

The printed-circuit assemblies are keyed to prevent improper insertion. Do not use force when inserting the assemblies and make certain the slots in the printed-circuit boards correspond to the proper keys in the connectors.

Note

Interface PCA's equipped with one white and one red extractor should be installed with the red extractor down.

d. Insert the mag tape 1 assembly into the higher priority (lower numbered) slot.

e. Insert the mag tape 2 assembly into the lower priority slot.

2-11. INTERCONNECT CABLE INSTALLATION.

2-12. The interconnect cable consists of three twisted-pair cables with keyed connectors and is installed as described below (see figure 2-2):

a. Route the 13181-60030 Interconnect Cable in the computer as illustrated in figure 2-1. Allow sufficient cable slack to prevent strain at the connectors.

b. Connect MAG TAPE 1 and MAG TAPE 2 hooded connectors P1 and P2 to the mag tape 1 and mag tape 2 assemblies, respectively.

c. Gain access to the tape unit interconnect facilities and route the cable within the tape unit as illustrated in figure 2-2.

d. Connect READ hooded connector P3 to the read data assembly.

e. Connect WRITE hooded connector P4 to the write data assembly.

f. Connect CONTROL hooded connector P5 to the control and status printed-circuit assembly.

2-13. INSTALLATION CHECKOUT.

2-14. After installing the interface kit, restore power to the tape unit and computer and prepare the system for operation. Refer to the computer and tape unit operating instructions, and perform the diagnostic test as described in the Diagnostic Program Procedure, part no. 13181-90040, contained in the Manual of Diagnostics.

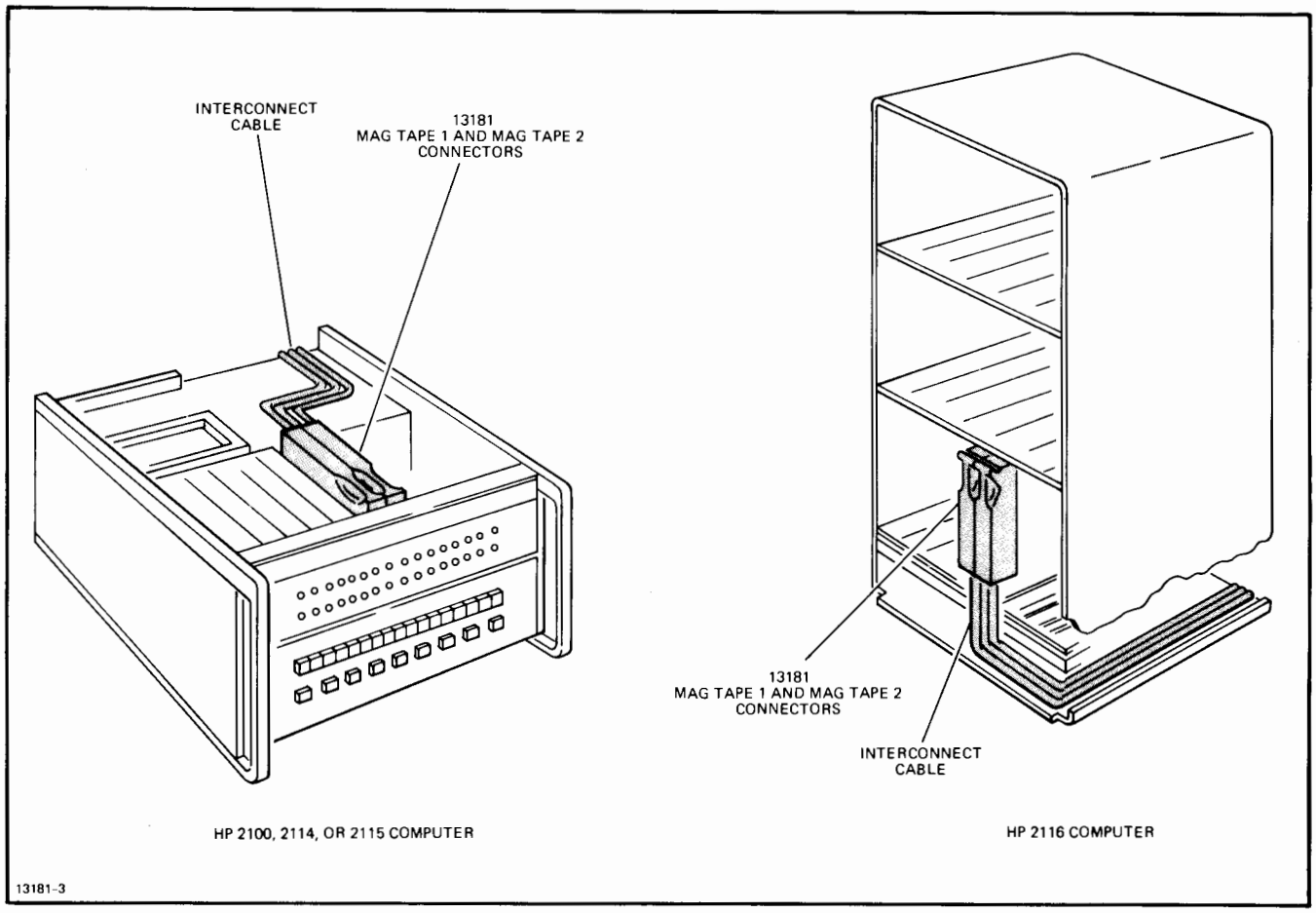


Figure 2-1. Typical Interconnect Cable Installation at the Computer

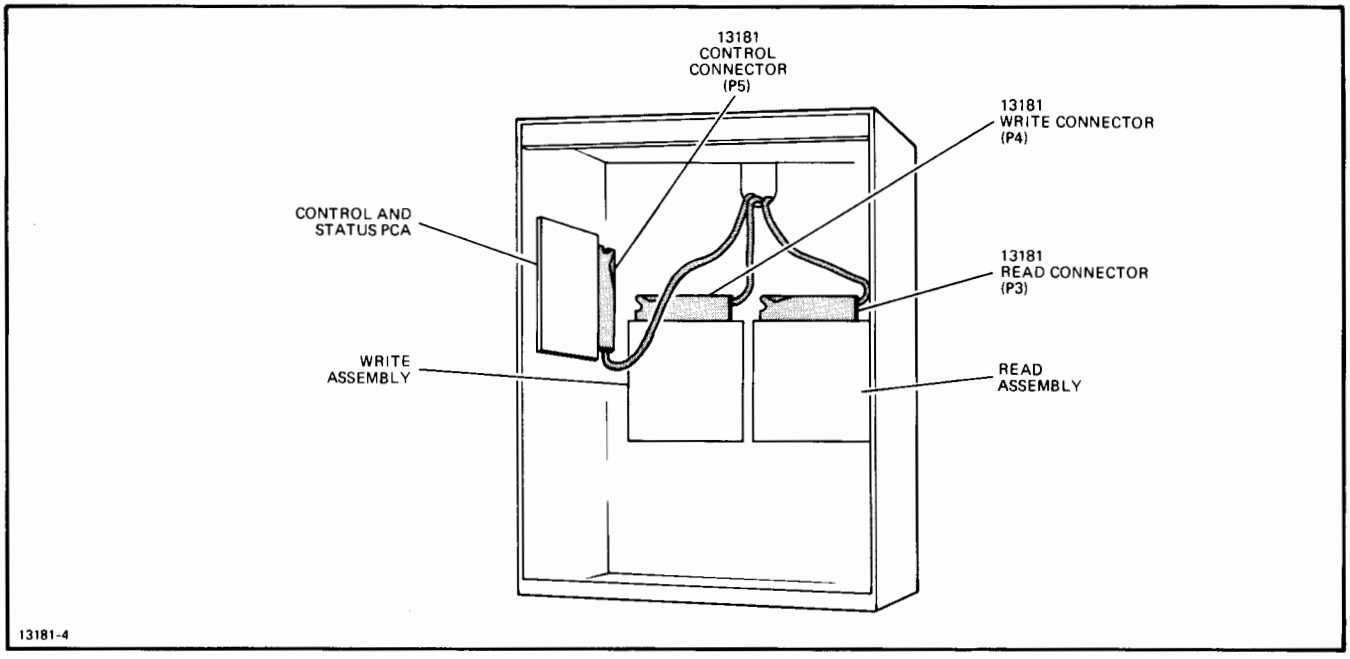


Figure 2-2. Interconnect Cable Installation at the Tape Unit

SECTION III
PROGRAMMING

3-1. INTRODUCTION.

3-2. This section contains programming information for the interface kit, including tape unit characteristics, controller commands and status, parity, packing densities, and data transfer rates.

3-3. TAPE UNIT CHARACTERISTICS.

3-4. The HP 13181A Tape Unit Interface Kit provides a complete nine-track interface between up to four paralleled HP 7970 Series Digital Magnetic Tape Units and a single HP 2100 Series Computer. The interface provides all tape motion and data transfer control signals required for generating IBM-compatible nine-track formats. The multi-speed capability of the interface kit permits interfacing with tape units operating at 12.5, 37.5, or 45 inches per second with a packing density of 800 characters per inch. (Commonly controlled paralleled tape units must be at the same tape speeds.)

3-5. The interface kit requires two computer I/O addresses: a command channel address and a data channel address. The data channel is assigned the higher priority I/O address. DMA is always required for 45 ips tape units. DMA is recommended for 37.5 ips tape units interfaced with an HP 2114 Computer. For all other configurations DMA may be used but is not required.

3-6. CONTROLLER COMMANDS.

3-7. All commands are transferred through the A- or B-register of the computer to the command channel by an OTA/B instruction. The commands are stored in the controller and executed when a Set Control (STC) instruction is transmitted to the control circuits, except for tape unit select commands. The STC instruction causes the controller to execute the command. In the event of multiple OTA/B instructions before an STC instruction, the controller will execute the last instruction.

3-8. All valid commands switch the interface from the ready to the busy state and clear controller oriented status bits.

3-9. The four unit select commands, unless rejected are output by the OTA/B instruction in one computer cycle. The unit select commands are executed immediately; they do not require buffering and do not cause an interrupt.

Note

The Reject FF will be set if either a command requiring write current is given while the write enable ring is not installed on the tape unit, a reverse motion command is given at the beginning of tape (BOT), a command requiring motion is given when the tape unit or controller is not ready, or a unit select command is given when the controller is not ready.

3-10. A command channel flag is generated by the interface to indicate that all on-line operations requiring tape motion have been completed, that a clear operation is complete, or that a Rewind or Rewind/Off-Line command has been initiated. The command channel flag is set when the interface is not busy. The control bits in each channel of the interface operate as in a normal I/O assembly, except that clearing a control bit in the data channel during a write operation initiates the writing of an end-of-record sequence and stops tape motion. Clearing the control bit in the data channel during a read operation inhibits transfer of data to the computer, although the read operation continues in the tape unit and controller until the interrecord gap is reached. At this time the controller is ready and the command channel flag is set.

3-11. The bits that make up command words are detailed in table 3-1.

Table 3-1. Command Word Bits

BIT	FUNCTION	BIT	FUNCTION
0	Motion	7	File
1	Forward	8	Change Select
2	Gap/Off-Line	9	Select 0
3	Write/Clear	10	Select 1
4	Data Transfer	11	Select 2
5	Reverse		
6	Rewind/Clear	12	Select 3

3-12. The interface responds to the commands listed in table 3-2. Commands other than those listed will cause improper operation. The following paragraphs describe each of the computer commands for the command channel.

Table 3-2. Computer to Controller Commands

CODE (OCTAL)	MNEMONIC	FUNCTION
31	WCC	Write One Record
15	GAP	Write 4 Inches Blank Tape
23	RRF	Read One Record
3	FSR	Forward Space One Record
41	BSR	Backspace Record
105	RWO	Rewind and Off-Line
101	REW	Rewind
110	CLR	Clear Controller
211	WFM	Write File Mark
1400	SEL0	Select Unit 0 (1)
2400	SEL1	Select Unit 1 (1)
4400	SEL2	Select Unit 2 (1)
10400	SEL3	Select Unit 3 (1)
203	FSF	Forward Space File
241	BSF	Backspace File
215	GFM	Gap and Write File Mark

Note:

1. Tape unit select commands are to be applied only with an OTA/B instruction; do not apply a subsequent STC,C instruction.

3-13. WRITE ONE RECORD (WCC).

3-14. The Write One Record command switches the tape unit to the write mode, which turns on the write head current, initiates forward motion, and causes the interface to set the data flag for each computer word to be written on the tape. The computer word is unpacked and written on tape. (The high eight bits of the computer word are written first, the low eight bits second.) At 37.5 ips the computer has 33 microseconds to output the requested word after the data channel flag bit is set. The interface generates odd parity for each character resulting from the output word as the character is written. The Longitudinal and Cyclic Redundancy Check Character (LRCC and CRCC) signals are automatically generated after the end-of-record sequence is started by a Clear Control instruction (CLC). The CLC instruction is addressed to the data channel to clear the data channel control bit immediately following the last word to be written. If the tape is at BOT when the WCC command is given, the interface will automatically erase 4-inches of tape before requesting the first computer word. All written records are automatically read by the tape unit and vertical parity, LRCC, and CRCC are checked. (The CRCC is not checked except for its contribution to the LRCC.) Thus each record can be verified by checking the parity/timing error bit of the status word after writing. When the read-after-write check is complete, the tape drive stops and the command channel flag bit is set to signal that the interface is ready to accept the next command.

3-15. GAP 4-INCHES (GAP).

3-16. The Gap 4-Inches command turns on the write current and causes the tape unit to erase 4-inches of tape. When the operation is completed, motion is terminated, the command channel flag bit is set, and the interface is ready for the next command.

3-17. READ ONE RECORD (RRF).

3-18. The Read One Record command causes the interface to input characters read from tape via bits 0 through 15 of the input data channel. The first of each pair of bytes is placed in the high eight bits of the computer word, the second byte in the low eight bits. Tape characters are read, vertical parity is checked, the parity bit is discarded, and the characters packed into one 16-bit computer word. The data channel flag is set when the second byte is read. Failure to respond to the flag within the data channel flag occurrence interval (refer to table 1-2) will set the parity/timing error bit and the timing error status bit. If the available core area in the computer is smaller than the tape record, the program should clear the data channel control bit when the available core area is full. This prevents the data channel flag from being set and thus prevents a timing error. Tape motion continues until the nex IRG is detected. The parity of the entire record (including the CRC and LRC character) is checked

and the tape is halted in the IRG. The CRCC and LRCC signals are not input to the computer. If a parity error occurred, the parity/timing error bit (bit 1) in the status word is set. The flag on the command channel is set to signal that the interface is ready to accept the next command. A file mark is treated as a record. The 023 octal file mark character is input and the EOF bit (bit 7) and the Odd Number of Bytes Read bit (bit 11) within the status word are set. The program can terminate reading anywhere within a record by addressing a Clear Control (CLC) instruction to the data channel. The tape will continue until the IRG is found, but additional data channel flags will not occur. However, both vertical and longitudinal parity will be checked.

Note

Records written with the controller will always contain an even number of bytes; however, records written on other systems may contain an odd number of bytes. During a read one record forward operation, the controller will read the final (odd) byte but will not immediately set the data channel flag bit since the byte only fills the high eight bits of the data word. The read operation will be interrupted for the equivalent of three byte times. At this time, an internal counter will signal end of data. The combination of the odd byte and the end of data is sensed, and command channel status bit 11 is set. The same combination now sets the data flag bit to load the final byte. The final byte occupies the upper eight bits of the final word. The lower eight bits are indeterminate. When reading a record written on a system that records an odd number of bytes, always load the command channel status bit 11 following an RRF operation. This will allow bit 11 to be tested in order to determine the actual number of tape bytes (2n or 2n-1 bytes, where n = number of words transmitted). Bit 11 should be ignored if bit 7 (EOF) is set.

3-19. FORWARD SPACE ONE RECORD (FSR).

3-20. The Forward Space One Record command moves the tape forward until the next IRG is detected, and tape motion ceases. The command channel flag is then set to signal that the interface is ready. Data is not transferred, but a parity error can be detected.

3-21. BACKSPACE ONE RECORD (BSR).

3-22. The Backspace One Record command moves the tape backwards until either the IRG or the BOT (beginning-of-tape) is detected. Motion is then terminated, the command channel flag is set, and bit 6 of the status word is set If BOT was detected. Data is not transferred, but a parity error can be detected.

Note

A record containing an odd number of data bytes will set the parity error bit during a BSR because the CRCC for such records has even vertical parity.

3-23. REWIND (REW).

3-24. The Rewind command causes the tape to rewind until the BOT reflective marker is found. If the tape is already at BOT, no action is taken. The command reject bit is not set.

3-25. After the Rewind command is output to the tape unit, the controller is set ready for use with any other tape drive while the rewind is in process. (A different tape unit may be selected.) While the selected tape unit is rewinding, the rewind bit (bit 10) and the transport busy bit (bit 9) will be set in the status word.

3-26. Any command that requires tape motion is rejected if given while the selected unit is rewinding, and the Reject FF and the reject status bit (bit 3) will be set.

3-27. REWIND OFF-LINE (RWO).

3-28. The Rewind Off-Line command positions the tape at BOT and switches the transport from on-line to off-line status. It operates in the same manner as the Rewind command, except the selected tape unit is switched to off-line status as well. When the command is issued at load-point, rewind is not affected but the tape unit does go off-line.

Note

Use of this command will require operator intervention to restore on-line status before another command may be given to the tape unit addressed by the RWO signal.

3-29. WRITE FILE MARK (WFM).

3-30. The Write File Mark command writes the file mark code (023 octal) on tape, and then the accompanying LRCC (023 octal) eight character-spaces following. When tape motion has ceased, the interface sets the command channel flag bit.

3-31. CLEAR CONTROLLER (CLR).

3-32. The Clear Controller command may be given at any time. The command clears the command and data channel control Flag FF's to the initial states (normal, ready state), terminating any tape unit operation except rewind. The parity/timing error bit, reject bit, data timing error bit, end of file bit, and odd number of bytes read bit are cleared. The command channel flag and not busy status is set at the end of a tape unit operation.

3-33. FORWARD SPACE FILE (FSF).

3-34. The Forward Space File command moves the tape forward until the next file mark or the end of tape is detected. The command channel flag is set, and bit 7 of the status word (EOF) is set when the tape stops if the file mark was detected. If the end of tape was detected, the EOT status bit (bit 5) is set, the FSF signal is changed to an FSR signal, and the tape will stop in the next IRG rather than after the file mark. If the previous record contained an odd number of bytes status bit is set.

3-35. BACKSPACE FILE (BSF).

3-36. The Backspace File command moves the tape in the reverse direction until a file mark or the beginning of tape is detected. The command channel flag is set, and bit 7 of the status word is set when tape motion ceases if the file mark was detected. If the load-point was detected, the load-point status bit (bit 6) is set.

3-37. GAP AND WRITE FILE MARK (GFM).

3-38. The Gap and Write File Mark command combines GAP and WFM to erase 4 inches of tape and writes the file mark code (023 octal) and the accompanying LRCC character in the eighth character space following.

3-39. SELECT UNIT 0, 1, 2, OR 3 (SEL).

3-40. The Select Unit 0, 1, 2, or 3 command causes the designated tape unit to be selected for subsequent computer commands, and status from that tape unit to be sent to the controller. Tape unit selection must be made after power turn-on, as the selected register contents are random at that time.

3-41. CONTROLLER STATUS.

3-42. Status information is transferred via the computer A- or B-register through the command channel with the standard I/O instructions: Load into A- or B-register (LIA/B), or Merge into A- or B-register (MIA/B). The status word bits are listed in table 3-3, and the bits are described in the following paragraphs. The tape unit status bits are available only when that tape unit is selected.

3-43. The 12-bit status word may be input through the command channel at any time using an LIA or LIB instruction. Normally, status is only checked when the interface signals "ready" after an operation has been completed.

3-44. LOCAL (BIT 0).

3-45. The local bit is high when the selected tape unit is in the local mode (under manual control only). When this is low, the unit is under computer control.

3-46. PARITY/TIMING ERROR (BIT 1).

3-47. The parity/timing error bit is high if a vertical or longitudinal parity error is detected during a read, read-after-write, BSR, FSR, BSF, or FSF operation. This bit is also set if the data channel flag bit has not been cleared or the interrupt request not acknowledged within one data channel flag occurrence interval (refer to table 1-2) while reading or writing (timing error).

Note

During a read operation, if the record on the tape is larger than the available computer input buffer area, the data channel control bit should be cleared after the required number of words are transferred. This prevents setting bit 1 unless a parity error has occurred.

3-48. NO WRITE RING (BIT 2).

3-49. The no write ring (file protected) bit is high when the tape unit supply reel is not equipped with a write enable ring. The tape unit is write-enabled when this bit is low.

Table 3-3. Controller Status Word Bits

BIT	STATUS	BIT	STATUS
0	Local	6	Load Point
1	Parity/Timing Error	7	End of File
2	No Write Ring	8	Controller Busy
3	Reject	9	Transport Busy
4	Data Timing Error	10	Rewind
5	End of Tape	11	Odd Number of Bytes Read

3-50. REJECT (BIT 3).

3-51. The reject bit is set when one of the following conditions occur at OTA/B time:

a. Tape motion is required but the tape unit or controller is busy.

b. Backspace command (BSR or BSF) received, but tape is at beginning of tape (BOT).

c. Command requiring write current received and no write ring present

d. A Select Tape Unit command is given and the controller is busy.

Note

Under no circumstances should the STC,C be given if bit 3 is set since improper operation may result.

3-52. Because the reject bit is set at OTA/B time, it is necessary to load the status word and test this bit between OTA/B time and STC,C time. The reject bit is cleared by the next executable (non-rejectable) OTA/B command.

3-53. DATA TIMING ERROR (BIT 4).

3-54. The data timing error bit is high if in the read mode (RRF) the computer has not accepted a word by the time the next one is ready, or in the write mode (WCC) the computer has not output a word by the time the next one is required.

3-55. END OF TAPE (BIT 5).

3-56. The end-of-tape (EOT) bit is high when the EOT reflective marker passes under the tape unit photosense head while the tape is moving forward. The bit remains high until a REW or RWO command is given, a BSR or BSF command positions the EOT marker ahead of the photosense head, or another tape unit is selected which has not sensed the EOT marker. (The former tape unit will re-establish the EOT but when it is selected again.)

3-57. LOAD POINT (BIT 6).

3-58. The beginning-of-tape (BOT) bit is high when the tape is at the load point, which is indicated when the tape load point marker (of the selected unit) is under the tape unit photo-sensor.

3-59. END OF FILE (BIT 7).

3-60. The end-of-file (EOF) bit is set when end-of-file mark (023 octal) is detected through the read circuits, while moving a record or file (FSR, BSR, FSF, BSF), while reading (RRF), or after writing the file mark (WFM, GFM).

3-61. CONTROLLER BUSY (BIT 8).

3-62. The controller busy bit is set when the interface is executing a command. When the bit is low, the interface is ready to accept a new command.

3-63. TRANSPORT BUSY (BIT 9).

3-64. The transport busy bit is high when the tape transport is busy, and low when the transport is ready to be used.

3-65. REWIND (BIT 10).

3-66. The rewind bit is high when the transport is rewinding and low when the transport is not rewinding. Rewind is still considered to be in operation while the tape moves forward to the load point following the actual rewind.

3-67. ODD NUMBER OF BYTES READ (BIT 11).

3-68. The odd number of bytes read bit is set if the previous record read or spaced over contains an odd number of data bytes.

Note

Since the controller always writes at least one computer word at a time (two tape bytes), this condition only occurs following a file mark for tapes written with this controller.

3-69. TYPICAL PROGRAMS.

3-70. Tables 3-4 and 3-5 contain typical assembly language programs. The program in table 3-4 will transfer data from the tape unit to the computer (read) using the computer interrupt method. The program in table 3-5 transfers data from the computer to the tape unit (write) using the DMA method.

Table 3-4. Assembly Language Program (Read) Using Computer Interrupt System

```
0001  00000                NAM SHOWN
0002                       ENT SHOWN
0003  00000          A     EQU 0
0004  00001          B     EQU 1
0005  00010          DATA  EQU 10B
0006  00011          CMND  EQU 11B
0007*
0008*     13181 CONTROLLER INTERRUPT BINARY READ OPERATION
0009*     CONTROLLER ASSUMED TO BE IN SLOTS 10,11
0010*
0011  00000                ORB           .BASE PAGE LINKAGE
0012  00000 000023R I.1    DEF I1        .DATA LINK (L1)
0013  00001 000035R C.1    DEF C1        .COMMAND LINK (L2)
0014  00000                ORR           .RELOCATIBLE PROGRAM
0015  00000 000000  SHOWN NOP
0016  00001 102100         STF 0         .TURN ON INTERRUPTS
0017  00002 062040R        LDA JSBL1
0018  00003 070010         STA DATA      .INTERRUPT LINK FOR DATA CHANNEL
0019  00004 062041R        LDA JSBL2
0020  00005 070011         STA CMND      .INTERRUPT LINK FOR CMND CHANNEL
0021  00006 062042R        LDA BUFAD
0022  00007 072043R        STA POINT     .SET BUFFER POINTER
0023  00010 062044R        LDA LBUF
0024  00011 072045R        STA COUNT     .SET BUFFER COUNTER
0025  00012 062046R        LDA READ      .READ COMMAND
0026  00013 102611  REJCT OTA CMND       .OUTPUT READ COMMAND TO CONTROLL
0027  00014 106511         LIB CMND      .TEST FOR REJECT
0028  00015 005323         RBR,RBR
0029  00016 005310         RBR,SLB       .REJECT?
0030  00017 026013R        JMP REJCT     .YES, KEEP TRYING
0031  00020 103711         STC CMND,C    .SET CMND CHANNEL
0032*     CONTROLLER STARTS TAPE MOTION
0033  00021 103710         STC DATA,C    .SET DATA CHANNEL
0034*
0035*     DATA TRANSFER WILL NOW TAKE PLACE
0036*     A JUMP SELF LOOP FOLLOWS
0037  00022 026022R        JMP *         .JUMP SELF UNTIL INTERRRUPT OCCURS
0038  00023 000000  I1     NOP           ..DATA TRANSFER ROUTINE
0039  00024 072047R        STA SAVA      .SAVE A REGISTER
0040  00025 103510         LIA DATA,C    .INPUT DATA FROM CONTROLLER
0041  00026 172043R        STA POINT,I   .STORE POINTER
0042  00027 036043R        ISZ POINT     .NEXT
0043  00030 062047R        LDA SAVA
0044  00031 036045R        ISZ COUNT     .DONE ?
0045  00032 126023R        JMP I1,I      .NO
0046  00033 106710         CLC DATA      .YES
0047  00034 126023R        JMP I1,I
0048  00035 000000  C1     NOP           .OPERATION COMPLETE ROUTINE
0049  00036 106711         CLC CMND      .TRANSFER DONE
0050  00037 102077         HLT 77B
0051*
0052*     PROGRAM SHOULD COME TO A HLT 77B
0053*
0054*     PROGRAM CONSTANTS
0055*
0056  00040 114000B JSBL1 JSB I.1,I
0057  00041 114001B JSBL2 JSB C.1,I
0058  00042 000050R BUFAD DEF BUFF
0059  00043 000000  POINT NOP
0060  00044 177634  LBUF  DEC -100
0061  00045 000000  COUNT NOP
0062  00046 000023  READ  OCT 23
0063  00047 000000  SAVA  NOP
0064  00050 000000  BUFF  BSS 124
0065                      END SHOWN
**  NO ERRORS*
```

Table 3-5. Assembly Language Program (Write) Using DMA

```
0001  00000                NAM EXAMP
0002                       ENT EXAMP
0003  00010          DATA  EQU 10B
0004  00011          CMND  EQU 11B
0005*
0006*     13181 CONTROLLER DMA BINARY WRITE OPERATION
0007*     CONTROLLER ASSUMED TO BE IN SLOTS 10,11
0008*     DMA CHANNEL 6 IS USED
0009*
0010  00000                ORB            .BASE PAGE RELOCATIBLE
0011  00000 000030R LINK1  DEF COMPL      .CMND COMPLETE LINK
0012  00000                ORR            .RELOCATIBLE PROGRAM
0013  00000 000000  EXAMP  NOP
0014  00001 102100         STF 0          .TURN ON INTERRUPTS
0015  00002 062033R        LDA JSBL1
0016  00003 070011         STA 11B        .SET CMND TRAP CELL
0017  00004 062035R        LDA CLDMA       .TURN DMA OFF
0018  00005 070006         STA 6           .WHEN IT INTERRUPTS
0019  00006 062034R        LDA PWC
0020  00007 102606         OTA 6B         .SET DMA PROGRAM CONTROL WORD
0021  00010 106702         CLC 2B
0022  00011 062036R        LDA BUFF
0023  00012 102602         OTA 2B         .SET DMA BUFFER ADDRESS
0024  00013 102702         STC 2B
0025  00014 062233R        LDA LBUFF
0026  00015 102602         OTA 2B         .SET DMA BUFFER LENGTH
0027*
0028*     DMA IS NOW READY TO MAKE A WRITE TRANSFER
0029*
0030  00016 066234R        LDB WCC         .WRITE COMMAND
0031  00017 106611  REJCT  OTB CMND       .OUTPUT WRITE COMMAND TO CONTROLL
0032  00020 102511         LIA CMND        .TEST FOR REJECT
0033  00021 012235R        AND MASK2
0034  00022 002002         SZA             .REJECT?
0035  00023 026017R        JMP REJCT       .YES, KEEP TRYING
0036  00024 103711         STC CMND,C      .NO,SET CMND CHANNEL
0037*     CONTROLLER STARTS TAPE MOTION
0038  00025 103710         STC DATA,C     .SET DATA CHANNEL
0039  00026 103706         STC 6B,C       .START DMA
0040*
0041*     DATA TRANSFER WILL NOW TAKE PLACE
0042*      A JUMP SELF FOLLOWS
0043*
0044  00027 026027R        JMP *          .JUMP SELF UNTIL INTERRUPT OCCURS
0045  00030 000000  COMPL  NOP            .OPERATION COMPLETE
0046  00031 106711         CLC CMND
0047  00032 102077         HLT 77B
0048*
0049*     PROGRAM SHOULD COME TO A HALT 77B
0050*
0051*     PROGRAM CONSTANTS
0052*
0053  00033 114000B JSBL1  JSB LINK1,I
0054  00034 020010  PWC    OCT 20010
0055  00035 107706  CLDMA  CLC 6,C
0056  00036 000037R BUFF   DEF BUFF1
0057  00037 000000  BUFF1  BSS 124
0058  00233 177634  LBUFF  DEC -100
0059  00234 000031  WCC    OCT 31
0060  00235 000010  MASK2  OCT 10
0061                       END EXAMP
**  NO ERRORS*
```

SECTION IV
THEORY OF OPERATION

This section contains block diagrams and timing information for interface kit operations.

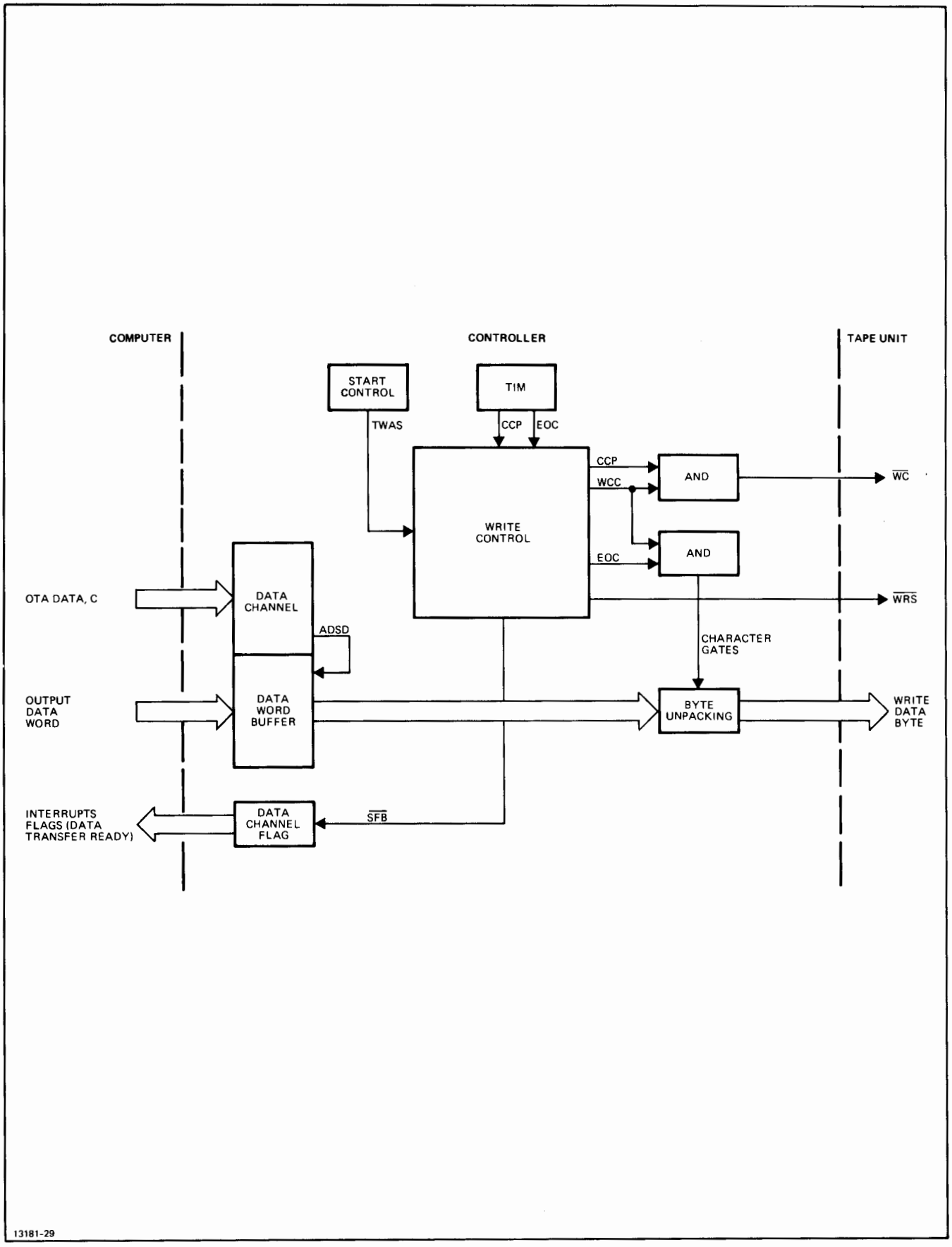


Figure 4-1. Write Data Control Block Diagram

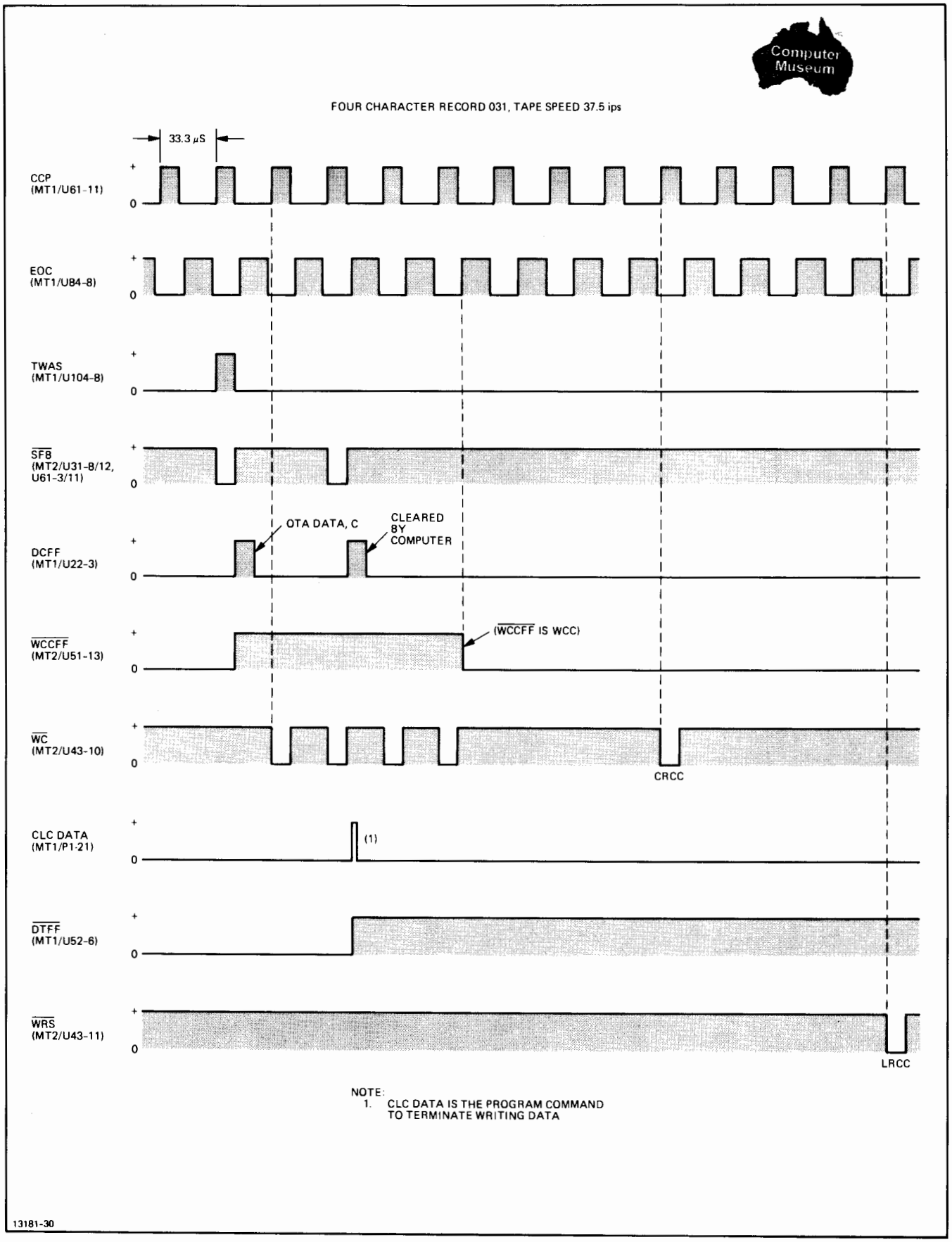


Figure 4-2. Write Data Control Timing Diagram

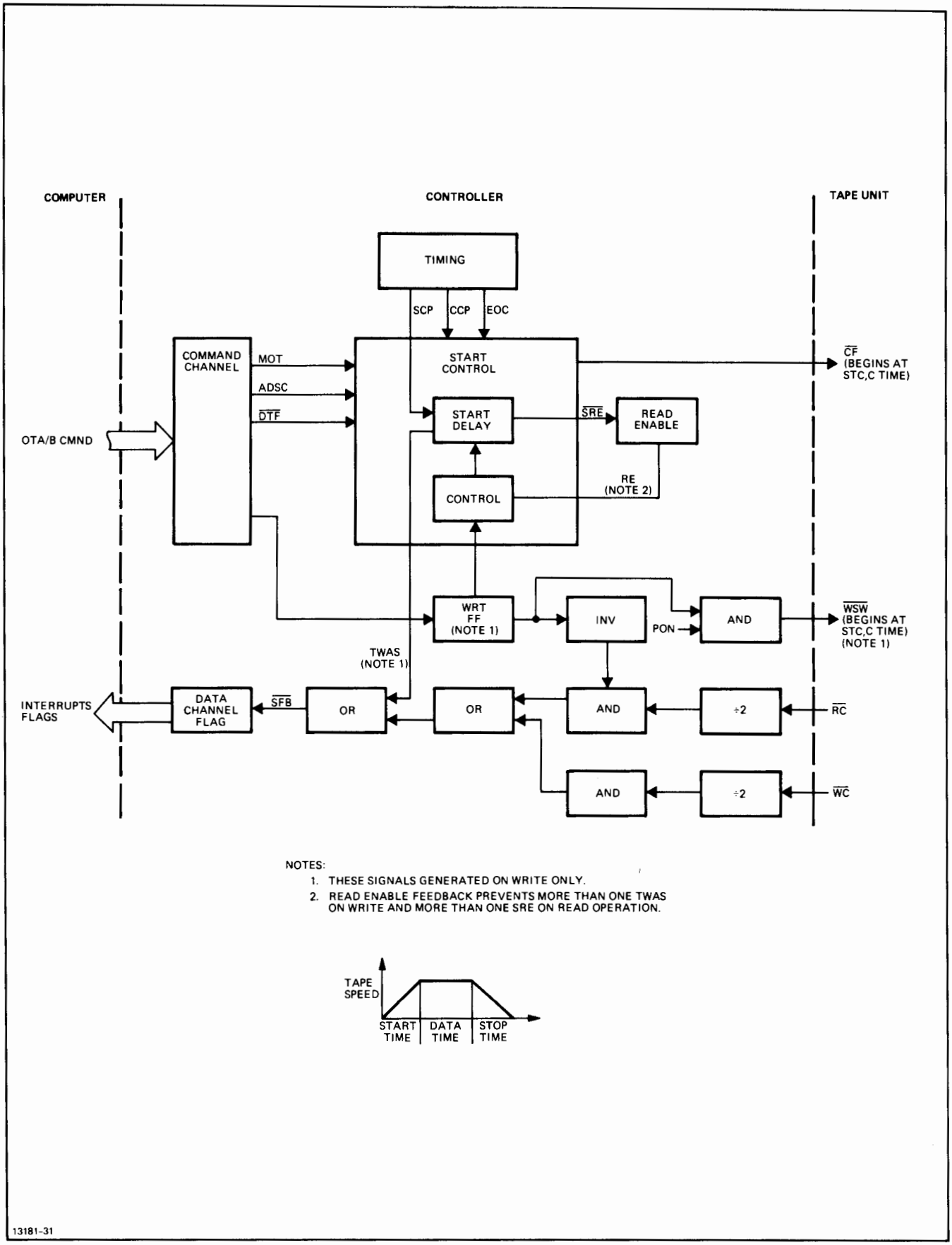


Figure 4-3. Start Data Operation Block Diagram

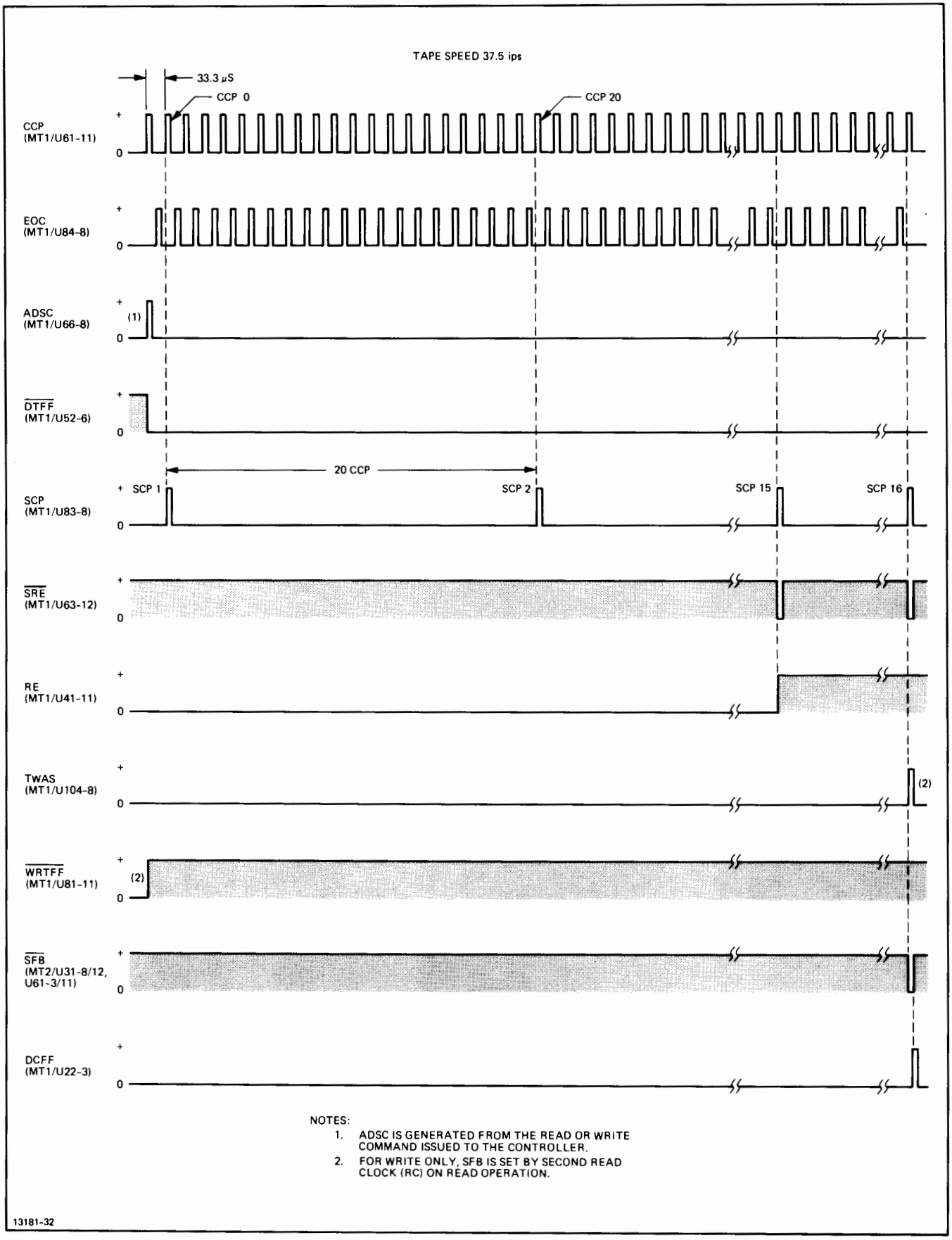


Figure 4-4. Start Data Operation Timing Diagram

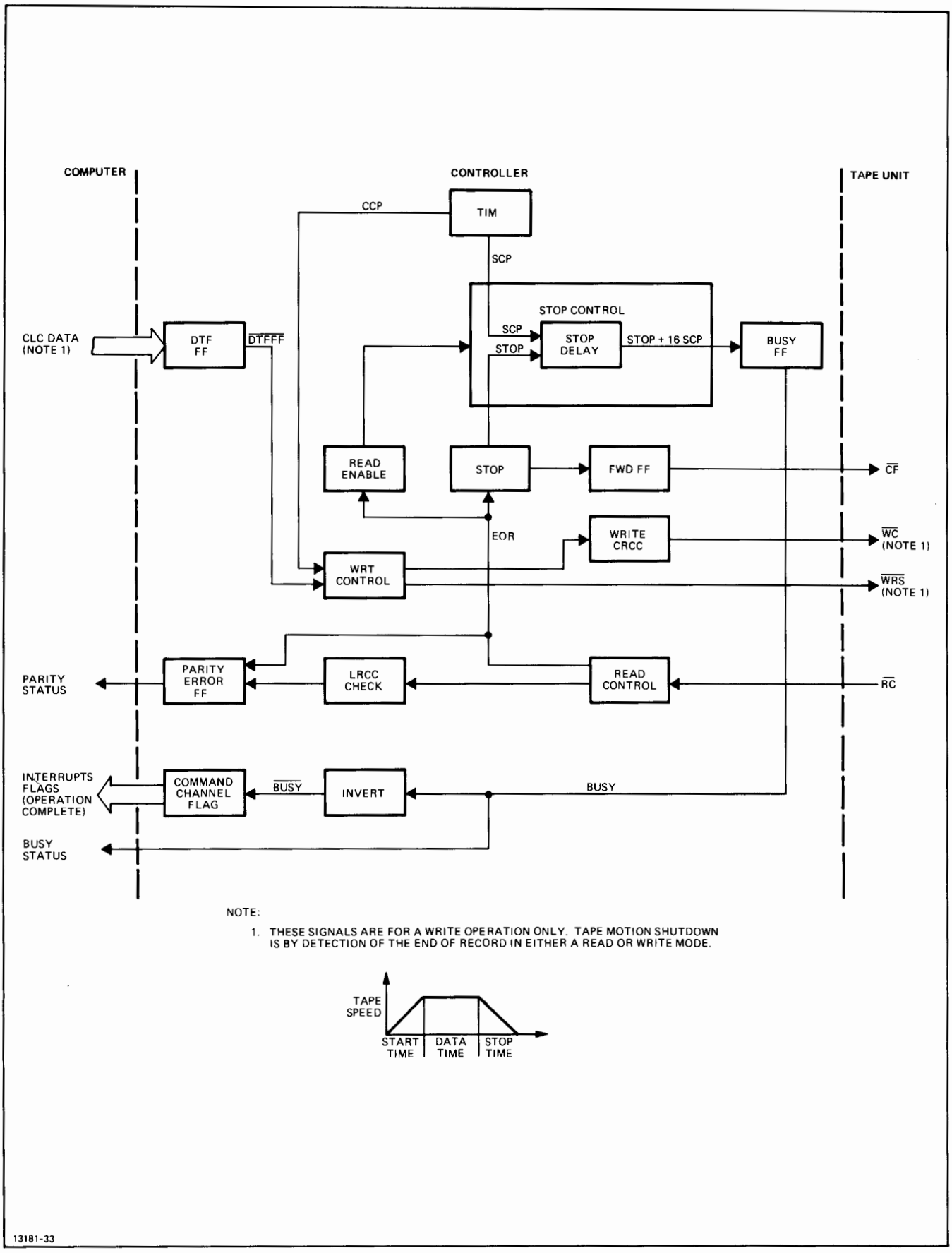


Figure 4-5. Stop Data Operation Block Diagram

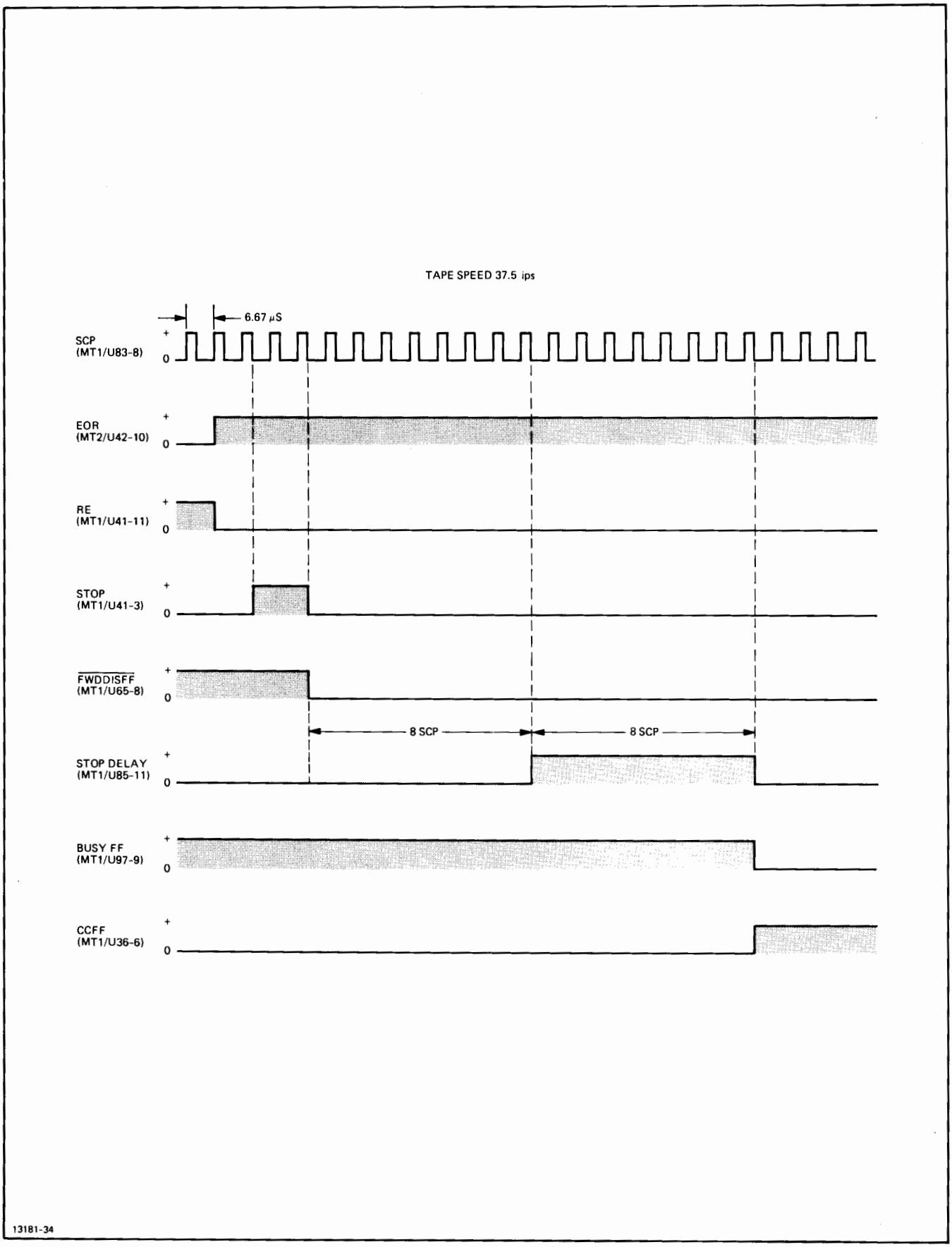
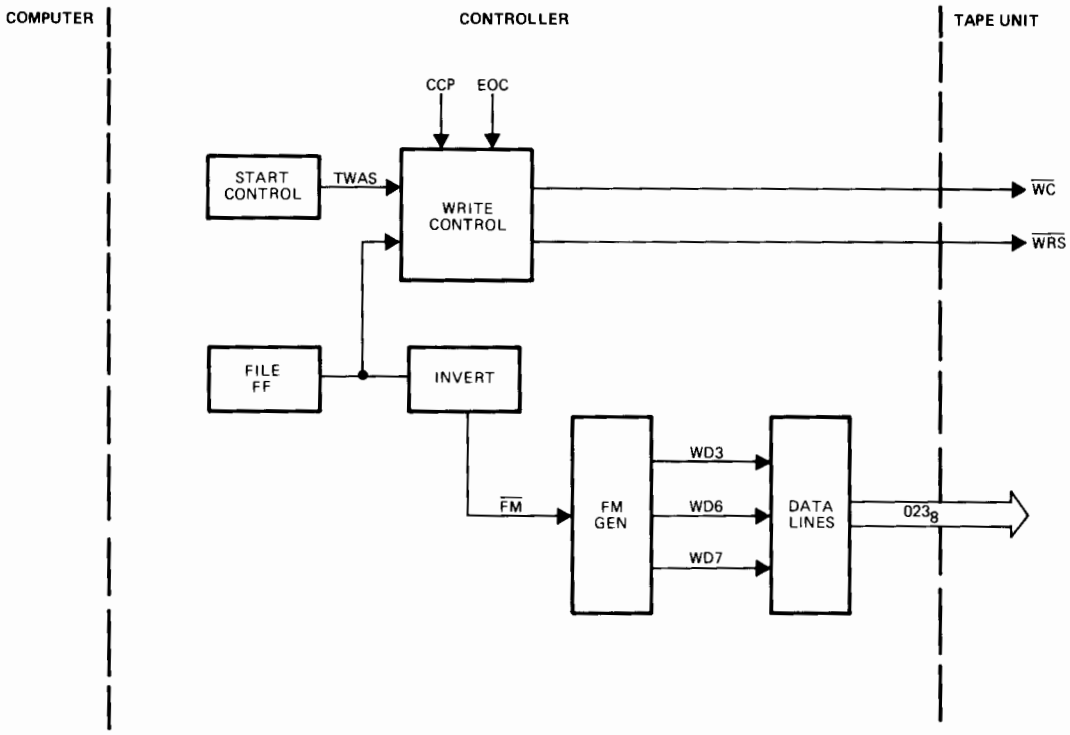
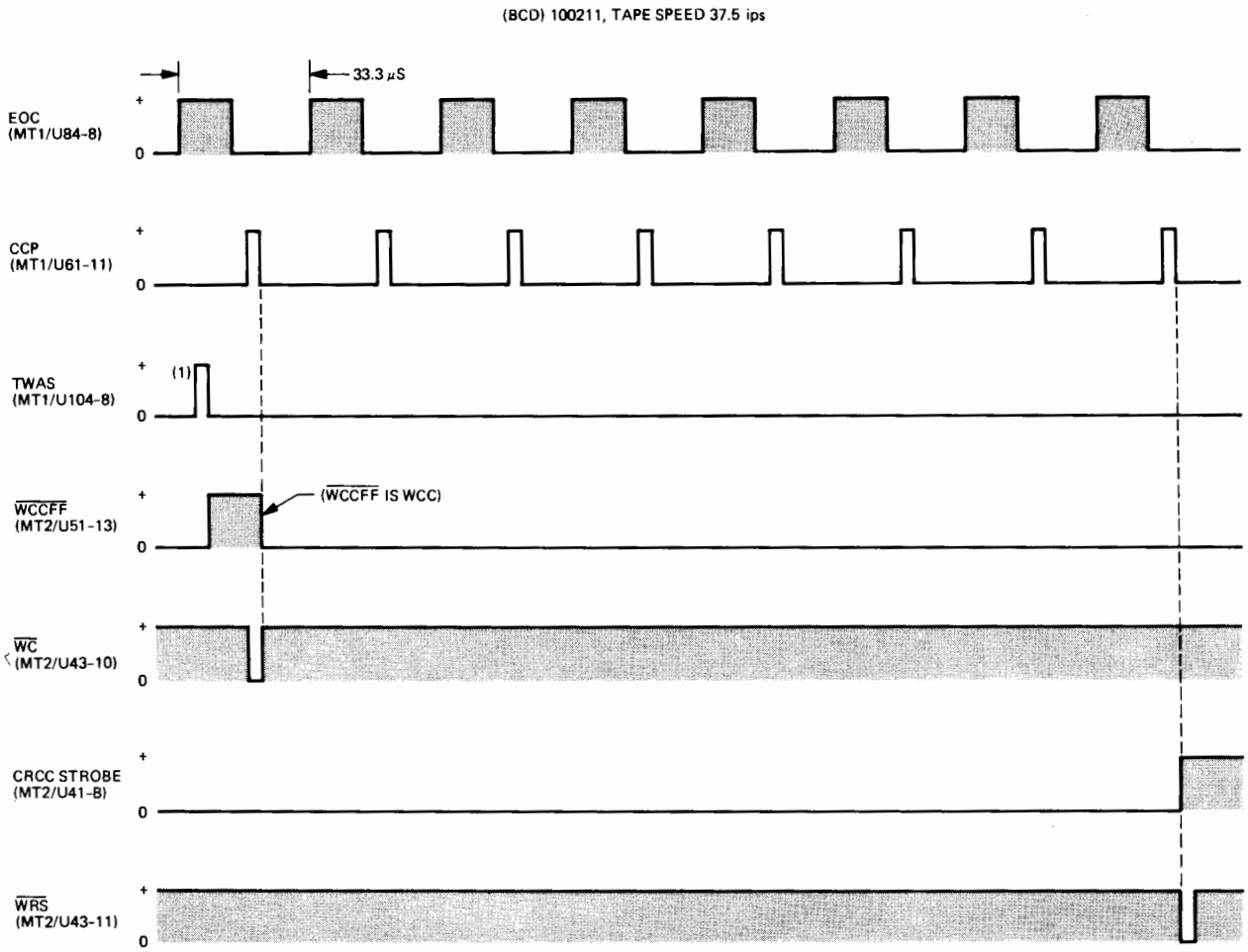


Figure 4-6. Stop Data Operation Timing Diagram



13181-35

Figure 4-7. Write File Mark Block Diagram



NOTE:

1. SF8 IS NOT GENERATED BECAUSE THE FILE FF IS SET AT OTA/B CMND TIME (ADSC). THE FM IS GENERATED IN THE CONTROLLER.

13181-36

Figure 4-8. Write File Mark Timing Diagram

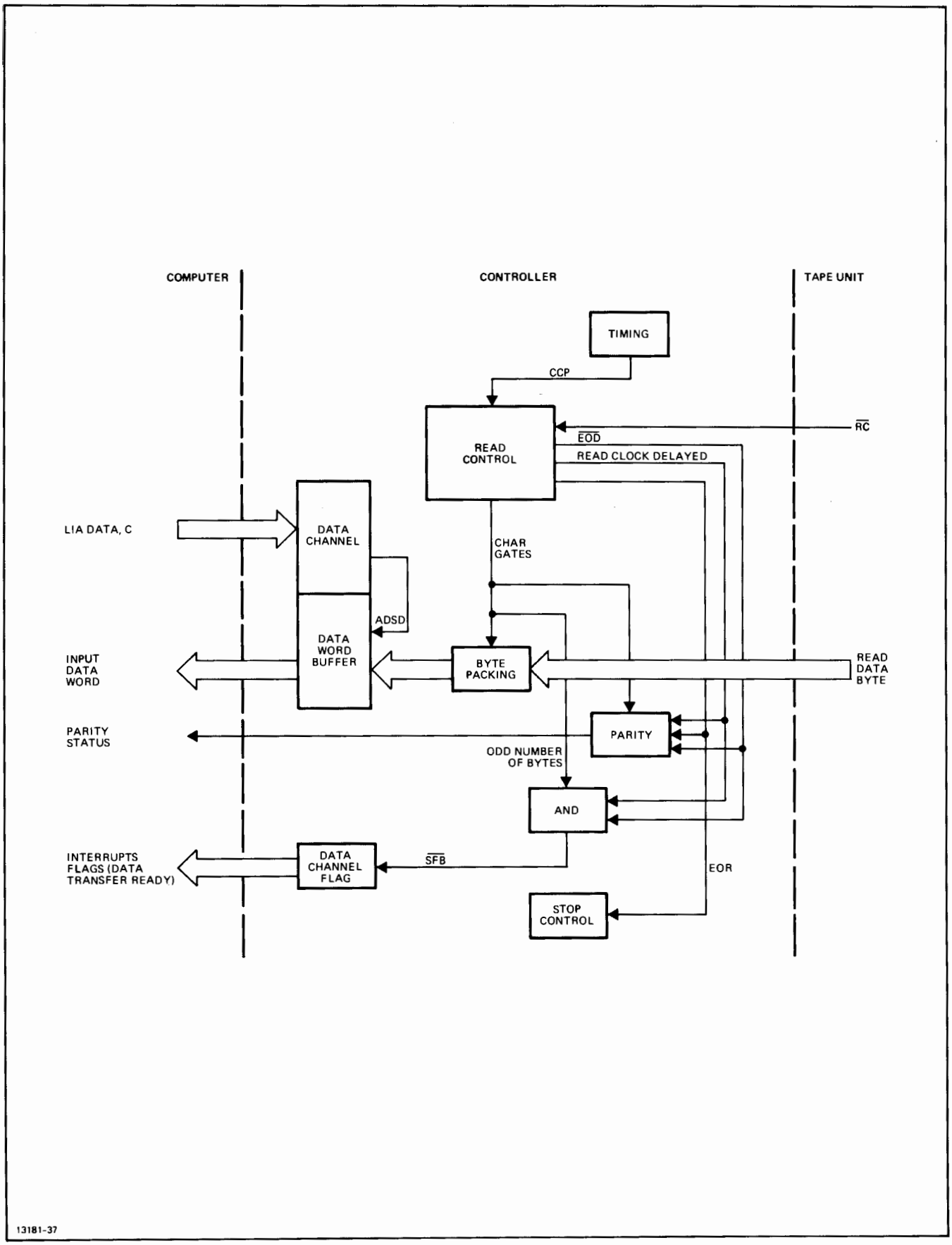
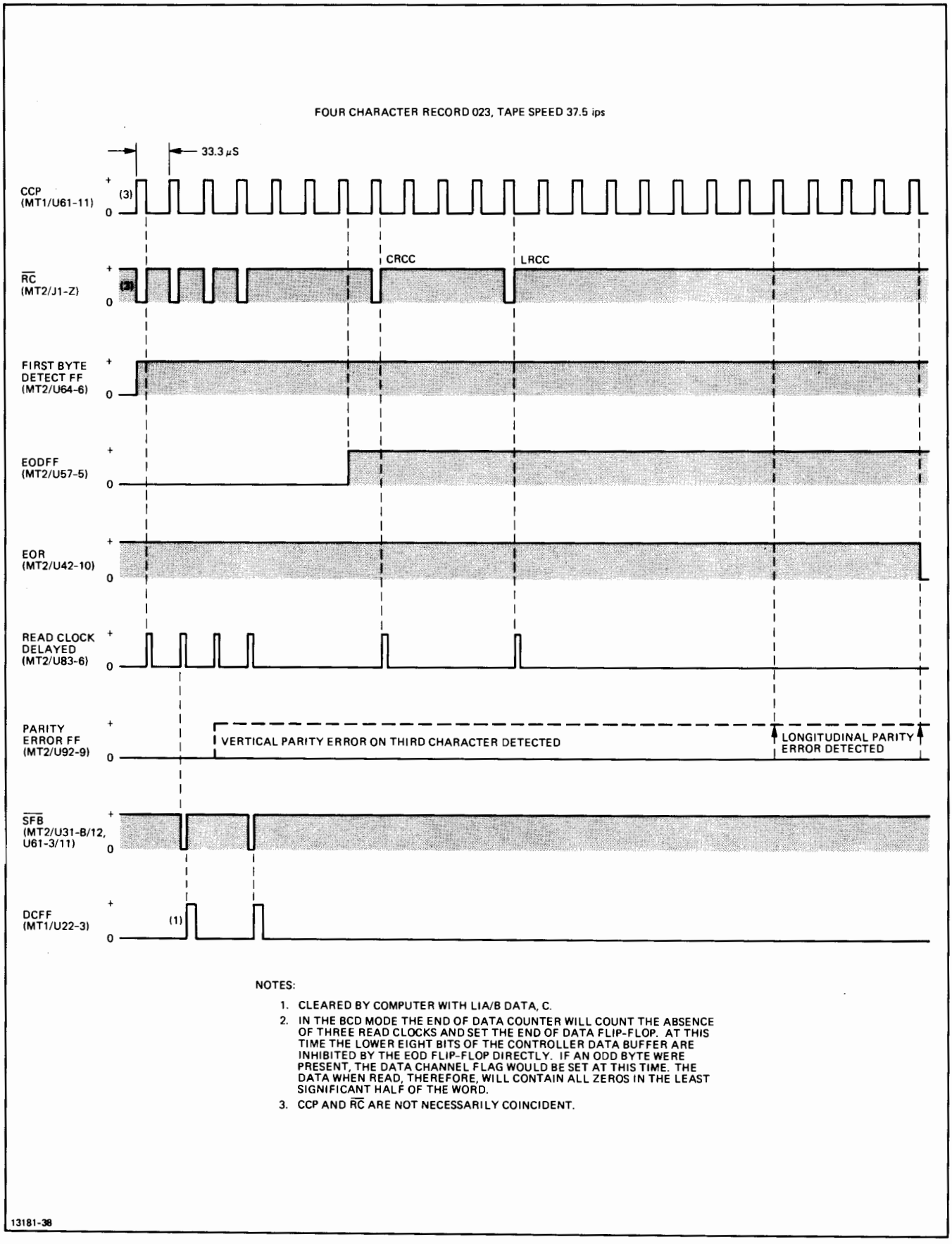


Figure 4-9. Read Data Control Block Diagram



NOTES:

1. CLEARED BY COMPUTER WITH LIA/B DATA, C.
2. IN THE BCD MODE THE END OF DATA COUNTER WILL COUNT THE ABSENCE OF THREE READ CLOCKS AND SET THE END OF DATA FLIP-FLOP. AT THIS TIME THE LOWER EIGHT BITS OF THE CONTROLLER DATA BUFFER ARE INHIBITED BY THE EOD FLIP-FLOP DIRECTLY. IF AN ODD BYTE WERE PRESENT, THE DATA CHANNEL FLAG WOULD BE SET AT THIS TIME. THE DATA WHEN READ, THEREFORE, WILL CONTAIN ALL ZEROS IN THE LEAST SIGNIFICANT HALF OF THE WORD.
3. CCP AND $\overline{RC}$ ARE NOT NECESSARILY COINCIDENT.

Figure 4-10. Read Data Control Timing Diagram

SECTION V
MAINTENANCE

5-1. INTRODUCTION.

5-2. This section contains maintenance information for the tape unit interface kit.

5-3. PREVENTIVE MAINTENANCE.

5-4. Detailed preventive maintenance procedures and schedules are provided in the HP computer documentation for the computer. There are no separate preventive maintenance procedures for the interface kit.

5-5. DIAGNOSTICS.

5-6. Procedures for running the interface kit diagnostic test are contained in the Diagnostic Program Procedure, part number 13181-90040, in the Manual of Diagnostics. The diagnostic test should be run after installation of the interface kit and periodically as a confidence check of the system operation.

5-7. TROUBLESHOOTING.

5-8. Troubleshooting for the interface assemblies is accomplished by performing the diagnostic test (paragraph 5-5) and analyzing the error halts that occur as the test is being run. To further isolate the trouble, refer to the schematic and parts location diagrams in figures 5-2 thru 5-5.

5-9. Figure 5-1 is the interconnection diagram for the tape unit to computer interface. Tables 5-1 and 5-2 list mnemonics definitions for the tape unit and controller, respectively.

Table 5-1. Tape Unit Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
CF	Forward Command	SL	On-Line Status
CL	Off-Line Command	SLP	Load Point Status
CR	Reverse Command	SR	Ready Status
CRW	Rewind Command	SRW	Rewind Status
CS0-CS3	Select Unit 0 thru 3	WC	Write Clock
RC	Read Clock	WDP	Write Data, Channel P
RDP	Read Data, Channel P	WD0	Write Data, Channel 0
RD0	Read Data, Channel 0	WD1	Write Data, Channel 1
RD1	Read Data, Channel 1	WD2	Write Data, Channel 2
RD2	Read Data, Channel 2	WD3	Write Data, Channel 3
RD3	Read Data, Channel 3	WD4	Write Data, Channel 4
RD4	Read Data, Channel 4	WD5	Write Data, Channel 5
RD5	Read Data, Channel 5	WD6	Write Data, Channel 6
RD6	Read Data, Channel 6	WD7	Write Data, Channel 7
RD7	Read Data, Channel 7	WRS	Write Reset
SET	End-of-Tape Status	WSW	Set Write Command
SFP	File Protect Status		

Table 5-2. Controller Mnemonics

MNEMONIC	DEFINITION	MNEMONIC	DEFINITION
ACI	Address Command Input	RC	Read Clock
ADSC	Address Command Channel	RE	Read Enable
ADSD	Address Data Channel	REV	Reverse
BOT	Beginning of Tape (Load Point)	SCP	Spacing Clock Pulse
CCP	Control Clock Pulse	SFB	Set Flag Buffer
CLR	Clear (Controller)	SRE	Set Read Enable
DTF	Data Transfer Latch	SRS	Start Reset
DFL	Data Flag	TIM	Timing Error
EOC	Even-Odd Clock	TWAS	Time, Write After Start
EOR	End-of-Record	WCC	Write Character Command
FM	File Mark	WFM	Write File Mark
FWD	Forward	WRS	Write Reset
LRC	Longitudinal Redundancy Character	WRT	Write
		FILE	File Operation

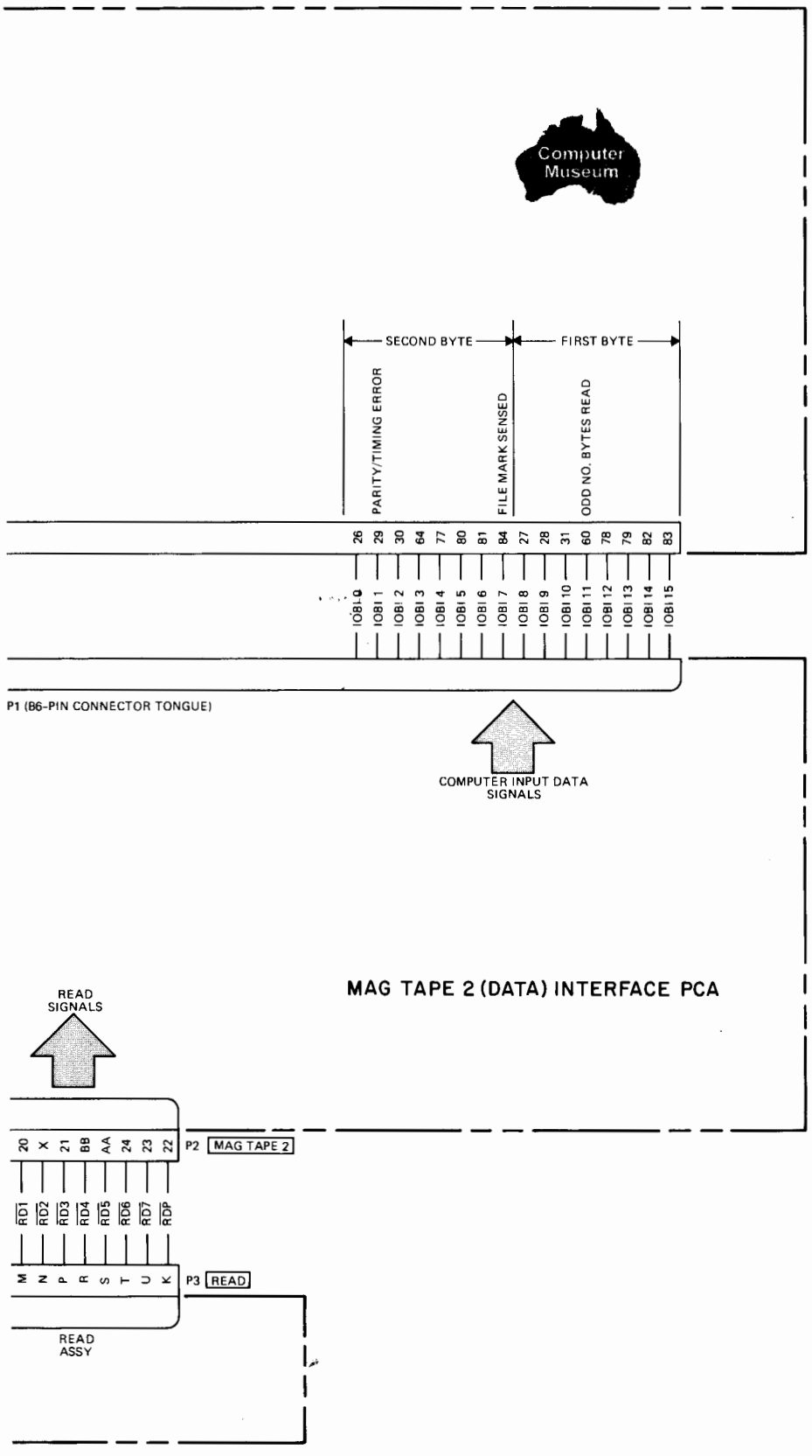
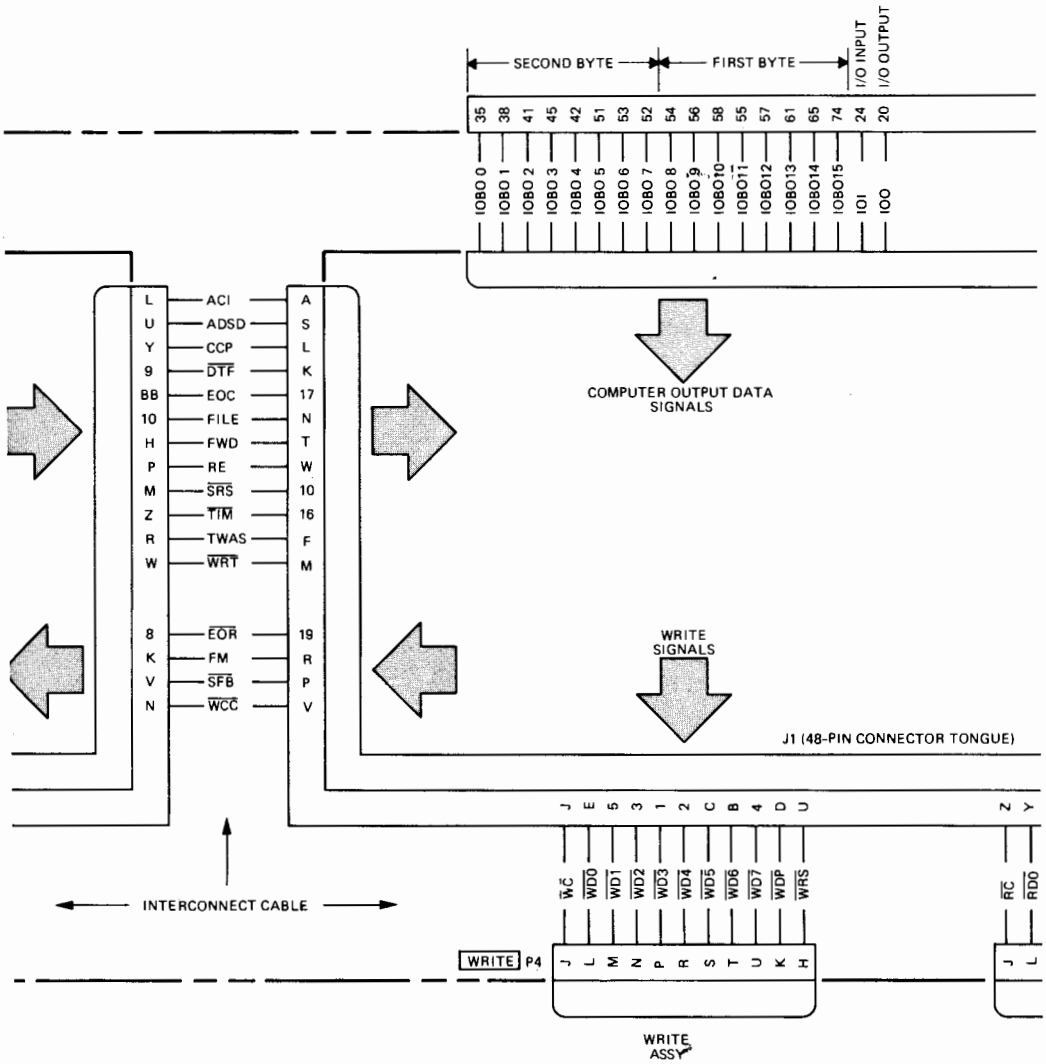
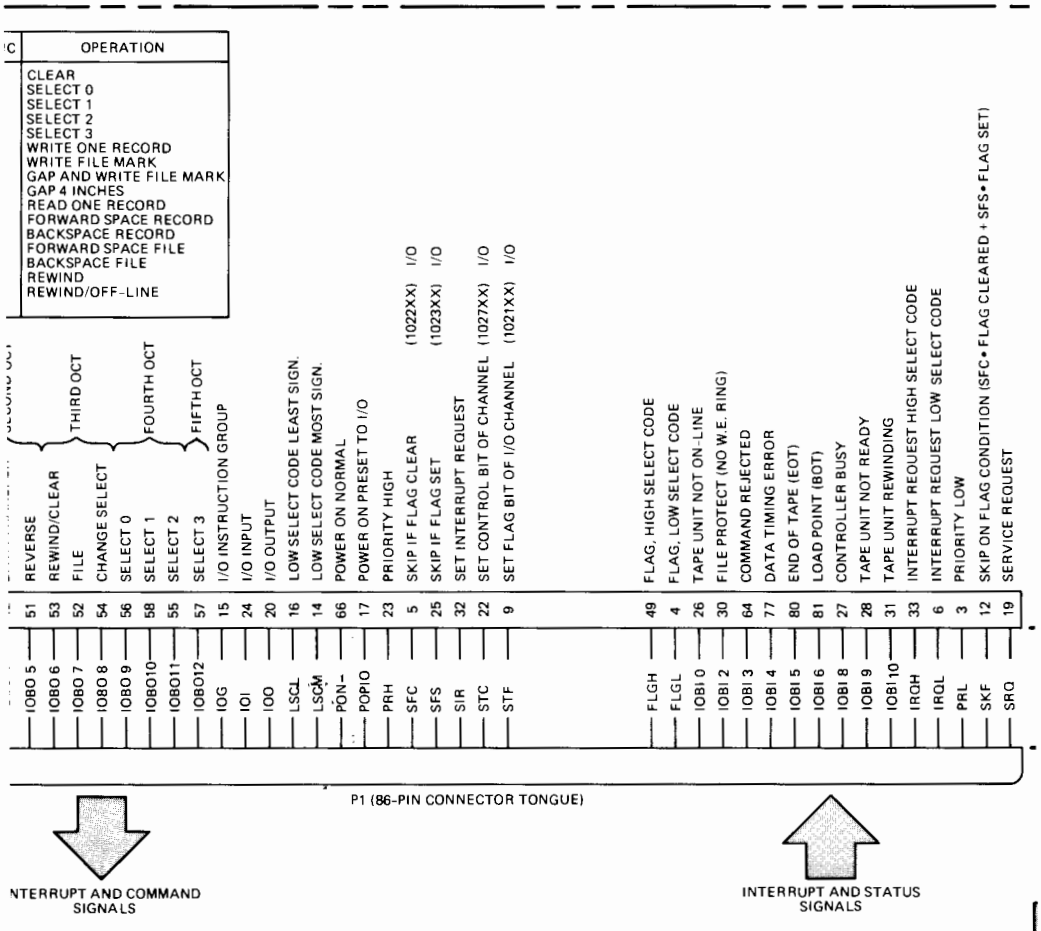


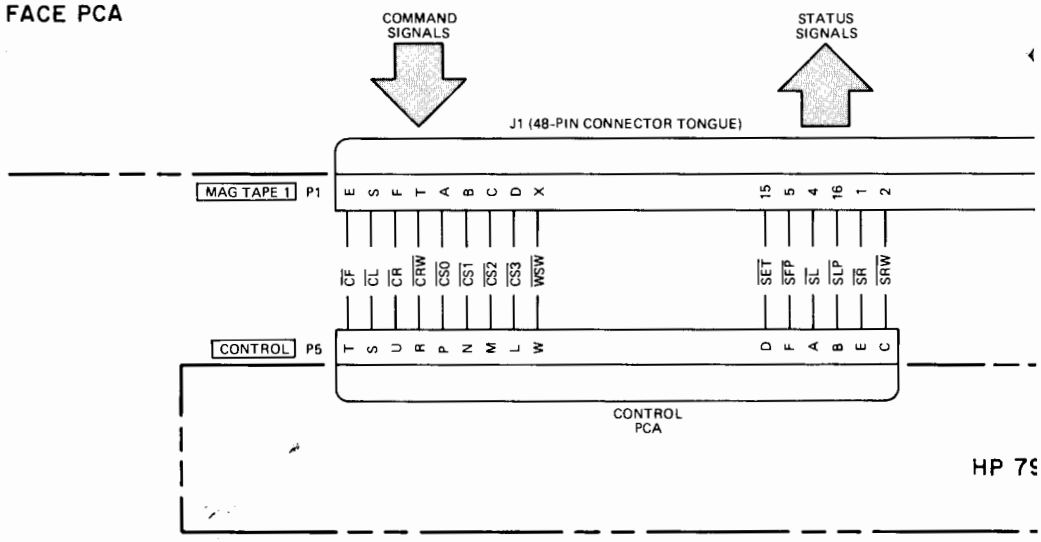
Figure 5-1. Interface Kit Interconnection Diagram

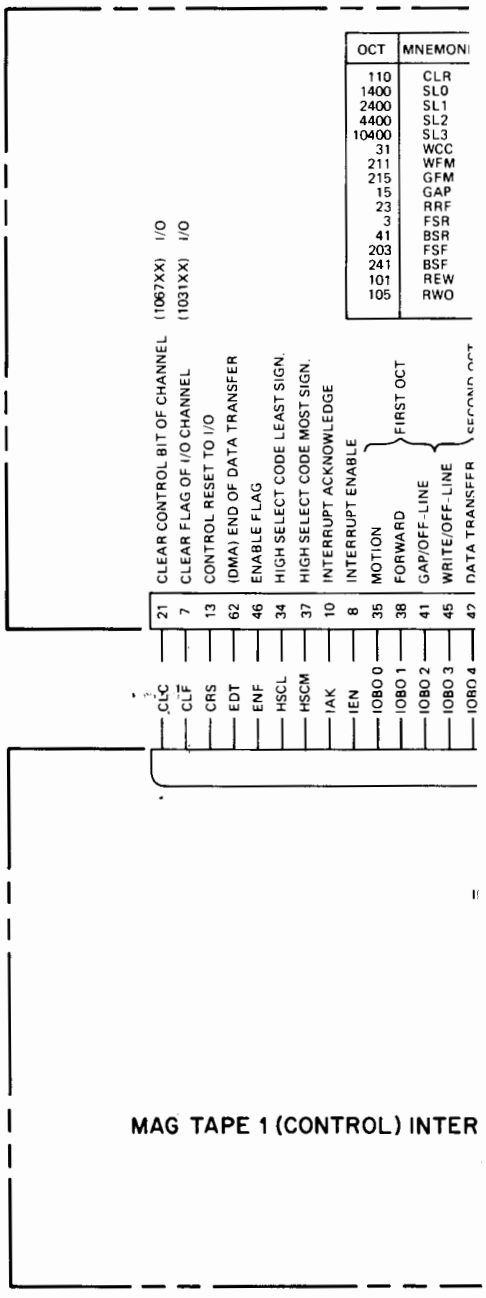
HP 2100 SERIES COMPUTER



70 SERIES DIGITAL MAGNETIC TAPE UNIT


OPERATION
CLEAR
SELECT 0
SELECT 1
SELECT 2
SELECT 3
WRITE ONE RECORD
WRITE FILE MARK
GAP AND WRITE FILE MARK
GAP 4 INCHES
READ ONE RECORD
FORWARD SPACE RECORD
BACKSPACE RECORD
FORWARD SPACE FILE
BACKSPACE FILE
REWIND
REWIND/OFF-LINE
THIRD OCT
FOURTH OCT
FIFTH OCT
REVERSE
REWIND/CLEAR
FILE
CHANGE SELECT
SELECT 0
SELECT 1
SELECT 2
SELECT 3
I/O INSTRUCTION GROUP
I/O INPUT
I/O OUTPUT
LOW SELECT CODE LEAST SIGN.
LOW SELECT CODE MOST SIGN.
POWER ON NORMAL
POWER ON PRESET TO I/O
PRIORITY HIGH
SKIP IF FLAG CLEAR (1022XX) I/O
SKIP IF FLAG SET (1023XX) I/O
SET INTERRUPT REQUEST
SET CONTROL BIT OF CHANNEL (1027XX) I/O
SET FLAG BIT OF I/O CHANNEL (1021XX) I/O
FLAG, HIGH SELECT CODE
FLAG, LOW SELECT CODE
TAPE UNIT NOT ON-LINE
FILE PROTECT (NO W.E. RING)
COMMAND REJECTED
DATA TIMING ERROR
END OF TAPE (EOT)
LOAD POINT (BOT)
CONTROLLER BUSY
TAPE UNIT NOT READY
TAPE UNIT REWINDING
INTERRUPT REQUEST HIGH SELECT CODE
INTERRUPT REQUEST LOW SELECT CODE
PRIORITY LOW
SKIP ON FLAG CONDITION (SFC • FLAG CLEARED + SFS • FLAG SET)
SERVICE REQUEST
51 53 52 54 56 58 55 57 15 24 20 16 14 66 17 23 5 25 32 22 9 49 4 26 30 64 77 80 81 27 28 31 33 6 3 12 19
IOBO 5 IOBO 6 IOBO 7 IOBO 8 IOBO 9 IOBO10 IOBO11 IOBO12 IOG IOI IOO LSCL LSCM PON- POPIO PRH SFC SFS SIR STC STF FLGH FLGL IOBI 0 IOBI 2 IOBI 3 IOBI 4 IOBI 5 IOBI 6 IOBI 8 IOBI 9 IOBI10 IRQH IRQL PRL SKF SRQ
P1 (86-PIN CONNECTOR TONGUE)
INTERRUPT AND COMMAND SIGNALS
INTERRUPT AND STATUS SIGNALS

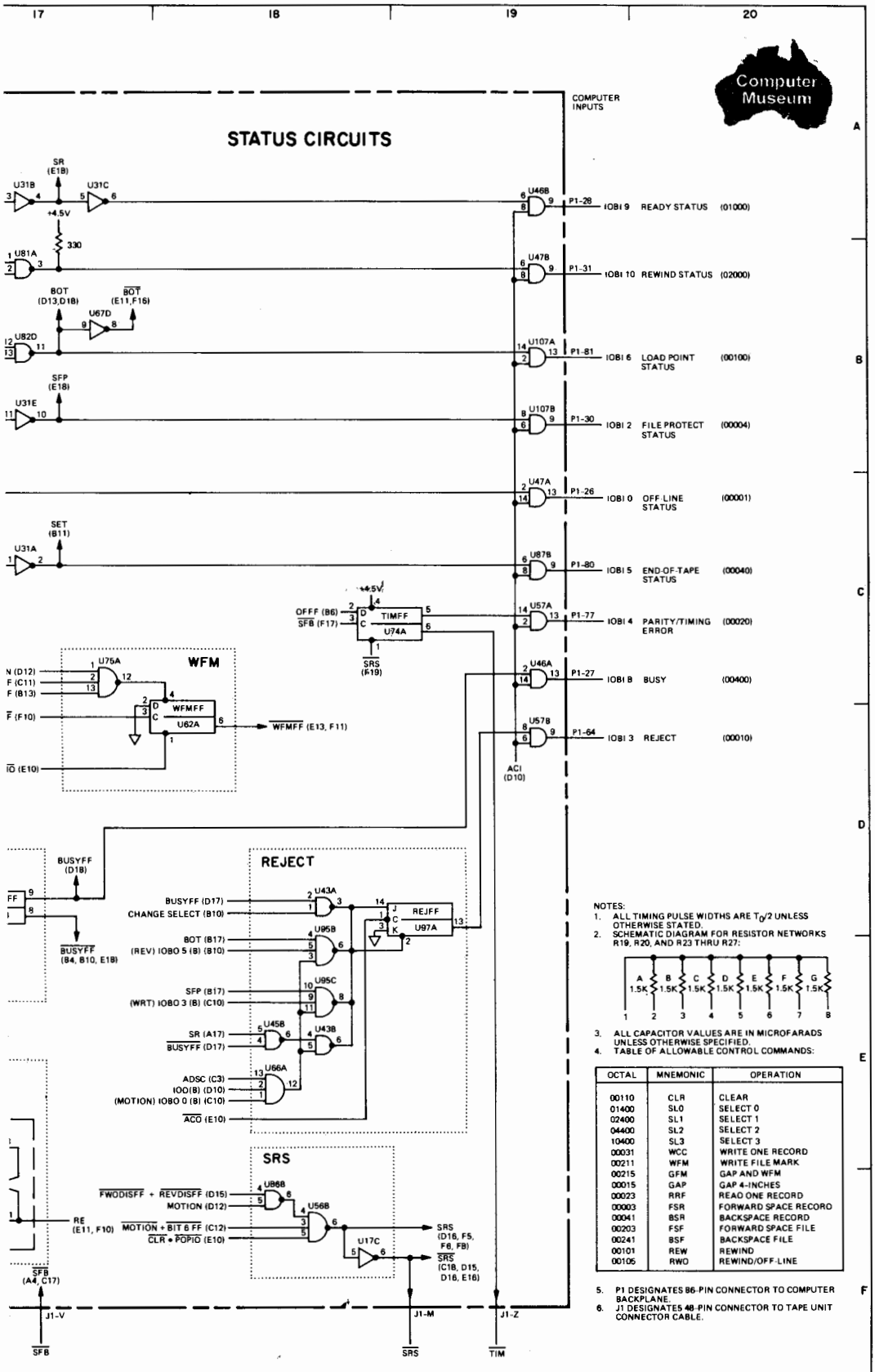

FACE PCA
COMMAND SIGNALS
STATUS SIGNALS
J1 (48-PIN CONNECTOR TONGUE)
MAG TAPE 1 P1
E S F T A B C D X 15 5 4 16 1 2
CF CL CR CRW CS0 CS1 CS2 CS3 WSW SET SFP SL SLP SR SRW
CONTROL P5
T S U R P N M L W D F A B E C
CONTROL PCA
HP 7


OCT
MNEMONI
110 CLR
1400 SL0
2400 SL1
4400 SL2
10400 SL3
31 WCC
211 WFM
215 GFM
15 GAP
23 RRF
3 FSR
41 BSR
203 FSF
241 BSF
101 REW
105 RWO
CLEAR CONTROL BIT OF CHANNEL (1067XX) I/O
CLEAR FLAG OF I/O CHANNEL (1031XX) I/O
CONTROL RESET TO I/O
(DMA) END OF DATA TRANSFER
ENABLE FLAG
HIGH SELECT CODE LEAST SIGN.
HIGH SELECT CODE MOST SIGN.
INTERRUPT ACKNOWLEDGE
INTERRUPT ENABLE
MOTION
FORWARD
GAP/OFF-LINE
WRITE/OFF-LINE
DATA TRANSFER
FIRST OCT
21
7
13
62
46
34
37
10
8
35
38
41
45
CLC
CLF
CRS
EDT
ENF
HSCL
HSCM
IAK
IEN
IOBO 0
IOBO 1
IOBO 2
IOBO 3
IOBO 4
MAG TAPE 1 (CONTROL) INTER

13181-21A

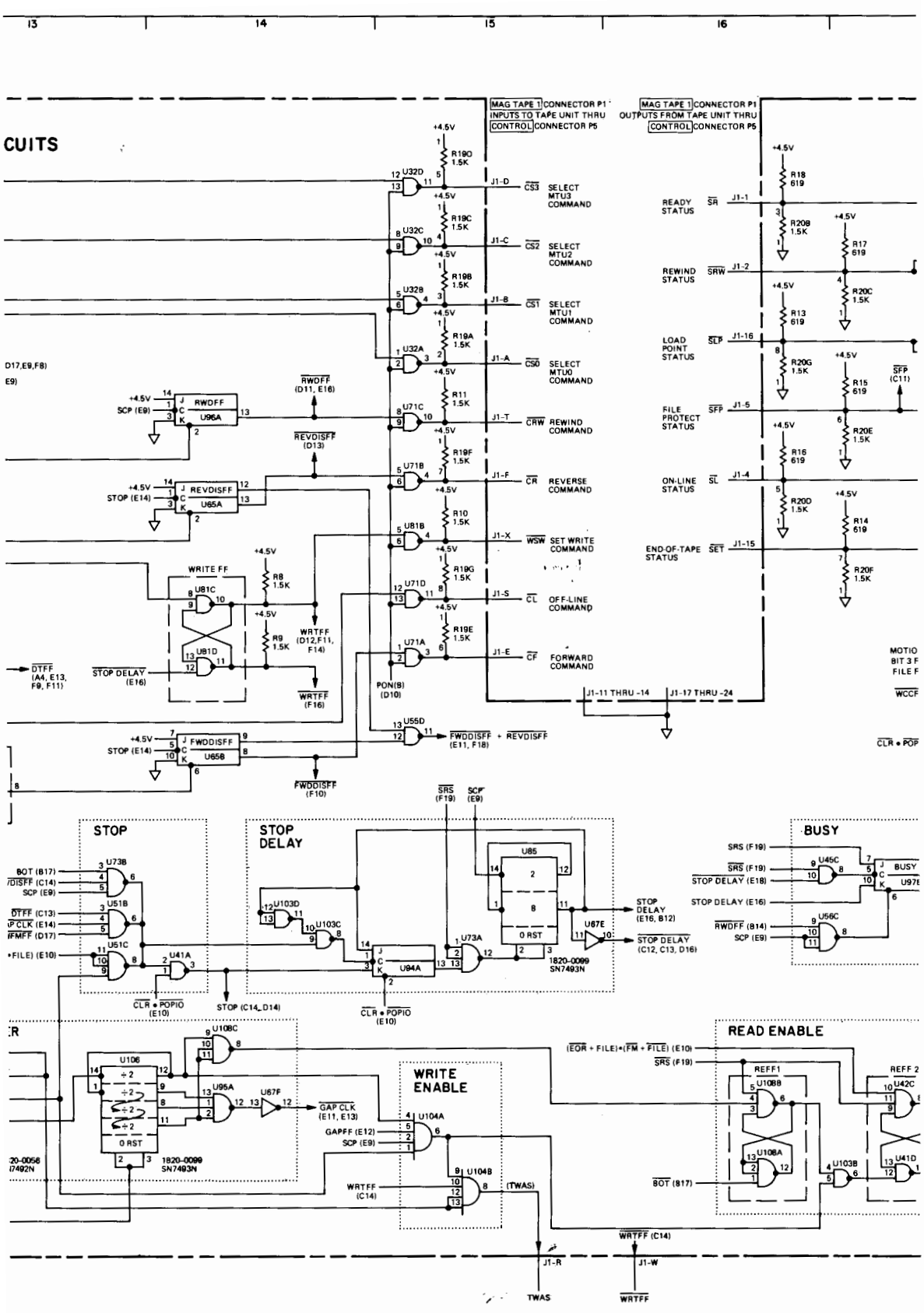
Table 5-3. Mag Tape 1 Printed-Circuit Assembly (13181-60040, -60070) Replaceable Parts

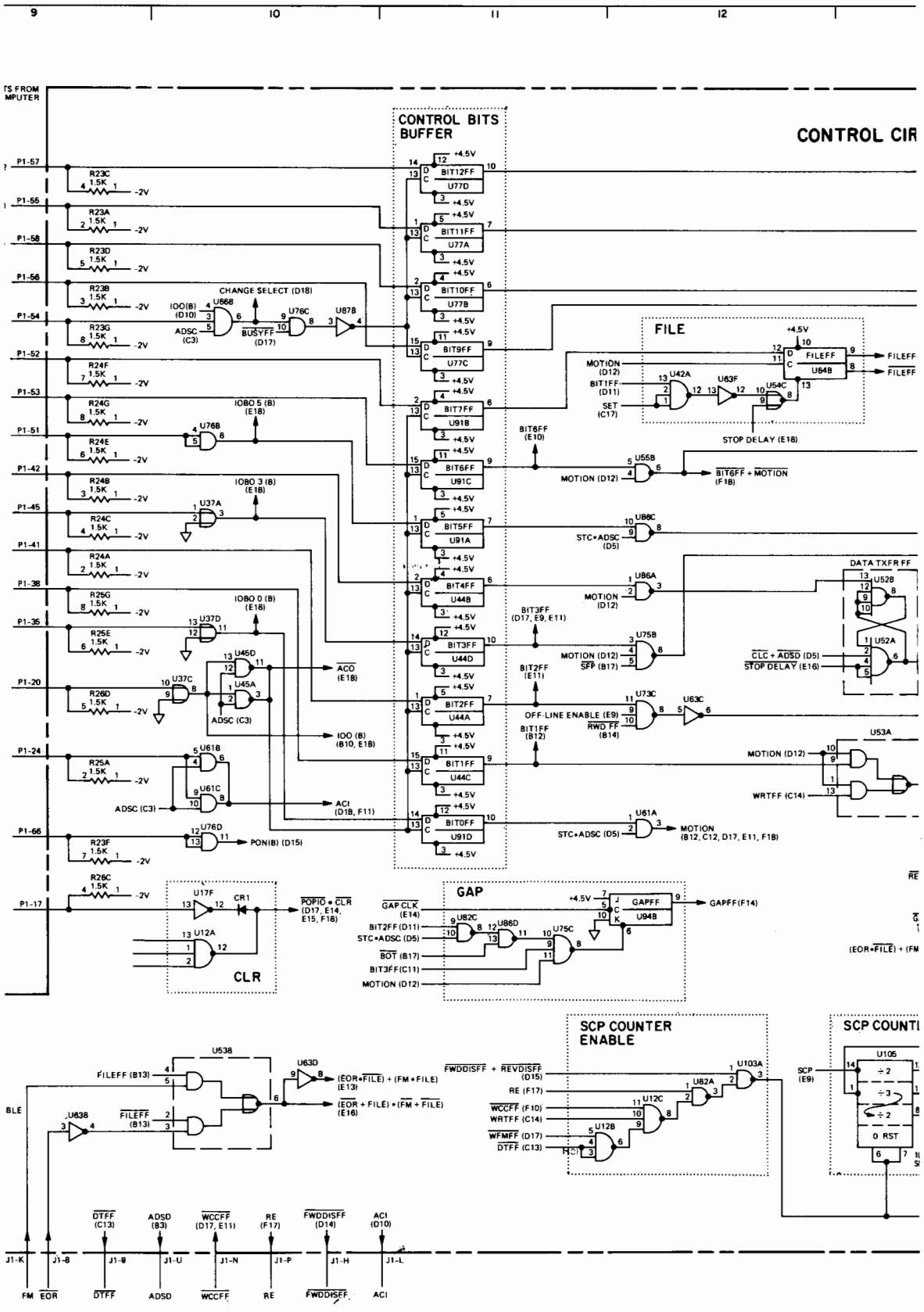
REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0160-2265	CAPACITOR, fxd, cer, 22 pF, 5%, 500 WVDC	72982	301-000 COGO 220J
C2	0150-0050	CAPACITOR, fxd, cer, 100 pF, -20%+80%, 1000 VDCW	56289	C067B102E102ZS26-CDH
C3	0160-2202	CAPACITOR, fxd, mica, 75 pF, 5%	28480	0160-2202
C4 thru 14, 16	0160-2055	CAPACITOR, fxd, cer, 10 nF, 100 VDCW	56289	C023F101F103ZS22
C15	0160-0153	CAPACITOR, fxd, cer, 1000 pF, 10%, 200 VDCW	56289	092P10292-PTS
C17 thru C21	0180-0100	CAPACITOR, fxd, Ta, 4.7 µF, 10%	28480	0180-0100
C22 thru C32	0160-2055	CAPACITOR, fxd, cer, 0.01 µF, 10%	28480	0160-2055
CR1	1910-0016	DIODE, ger, 60V	28480	1901-0016
Q1,2	1854-0215	TRANSISTOR, NPN, Si	04713	SPS3611
R1	0683-1535	RESISTOR, fxd, comp, 15k, 5%, 1/4W	01121	CB1535
R2	0683-2225	RESISTOR, fxd, comp, 2.2k, 5%, 1/4W	01121	CB2225
R3,4	0683-8215	RESISTOR, fxd, comp, 820 ohms, 5%, 1/4W	01121	CB8215
R5	0683-4725	RESISTOR, fxd, comp, 4.7k, 5%, 1/4W	01121	CB4725
R6,7	0683-3925	RESISTOR, fxd, comp, 3.9k, 5%, 1/4W	01121	CB3925
R8 thru 11	0683-1525	RESISTOR, fxd, comp, 1.5k, 5%, 1/4W	01121	CB1525
R12,22	0683-3315	RESISTOR, fxd, comp, 330 ohms, 5%, 1/4W	01121	CB3315
R13 thru 18	0757-0418	RESISTOR, fxd, comp, 619 ohms, 1%, 1/8W	28480	0757-0418
R19,20,23 thru 27	1810-0020	RESISTOR ARRAY, 7-res, fxd, film, 1.5k	56289	200C 1098-CRR
R21,28	0683-6805	RESISTOR, fxd, comp, 68 ohms, 5%, 1/4W	01121	CB6805
R29	0683-6815	RESISTOR, fxd, comp, 680 ohms, 5%, 1/4W	01121	CB6815
U12,56,75,108	1820-0068	INTEGRATED CIRCUIT, TTL	01295	SN7410N
U15,22,24,34,41,45, 55,82,86,103	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7400N
U16,26,27,46,47, 57,87,107	1820-0956	INTEGRATED CIRCUIT, CTL	07263	CTµL9956
U17,31,63,67	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U23	1820-0069	INTEGRATED CIRCUIT, TTL	01295	SN4344
U25,66,83	1820-0372	INTEGRATED CIRCUIT, TTL	01295	SN74H11N
U32,71,81	1820-0256	INTEGRATED CIRCUIT, DTL	04713	MC8558P
U33,42,51,73,95	1820-0310	INTEGRATED CIRCUIT, DTL	04713	MC862P
U35,53	1820-0063	INTEGRATED CIRCUIT, TTL	01295	SN4348
U36,43	1820-0094	INTEGRATED CIRCUIT, DTL	04713	SC6903PK
U37	1820-0205	INTEGRATED CIRCUIT, TTL	04713	MC3003P
U44,77,91	1920-0437	INTEGRATED CIRCUIT, TTL	04713	MC4015P
U52	1820-0086	INTEGRATED CIRCUIT, DTL	01295	SN4498
U54	1820-0239	INTEGRATED CIRCUIT, TTL	04713	MC3002P
U61,76	1820-0141	INTEGRATED CIRCUIT, TTL	04713	SC7514PK
U62,64,74	1820-0077	INTEGRATED CIRCUIT, TTL	01295	SN7474N
U65,94,96,97	1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN7473N
U72,84	1820-0055	INTEGRATED CIRCUIT, TTL	01295	SN7490N
U85,106	1820-0099	INTEGRATED CIRCUIT, TTL	01295	SN7493N
U93,105	1820-0056	INTEGRATED CIRCUIT, TTL	01295	SN7492N
U104	1820-0374	INTEGRATED CIRCUIT, TTL	01295	SN4482
W1,2,3	5080-0058	JUMPER CONNECTOR, printed-circuit board	28480	5080-0058
XY1	1200-0199	SOCKET, crystal	28480	1200-0199
Y1	0410-0163	CRYSTAL, quartz, 300 kHz (used on 13181-60040)	28480	0410-0163
Y1	0410-0431	CRYSTAL, quartz, 360 kHz (used on 13181-60070)	28480	0410-0431

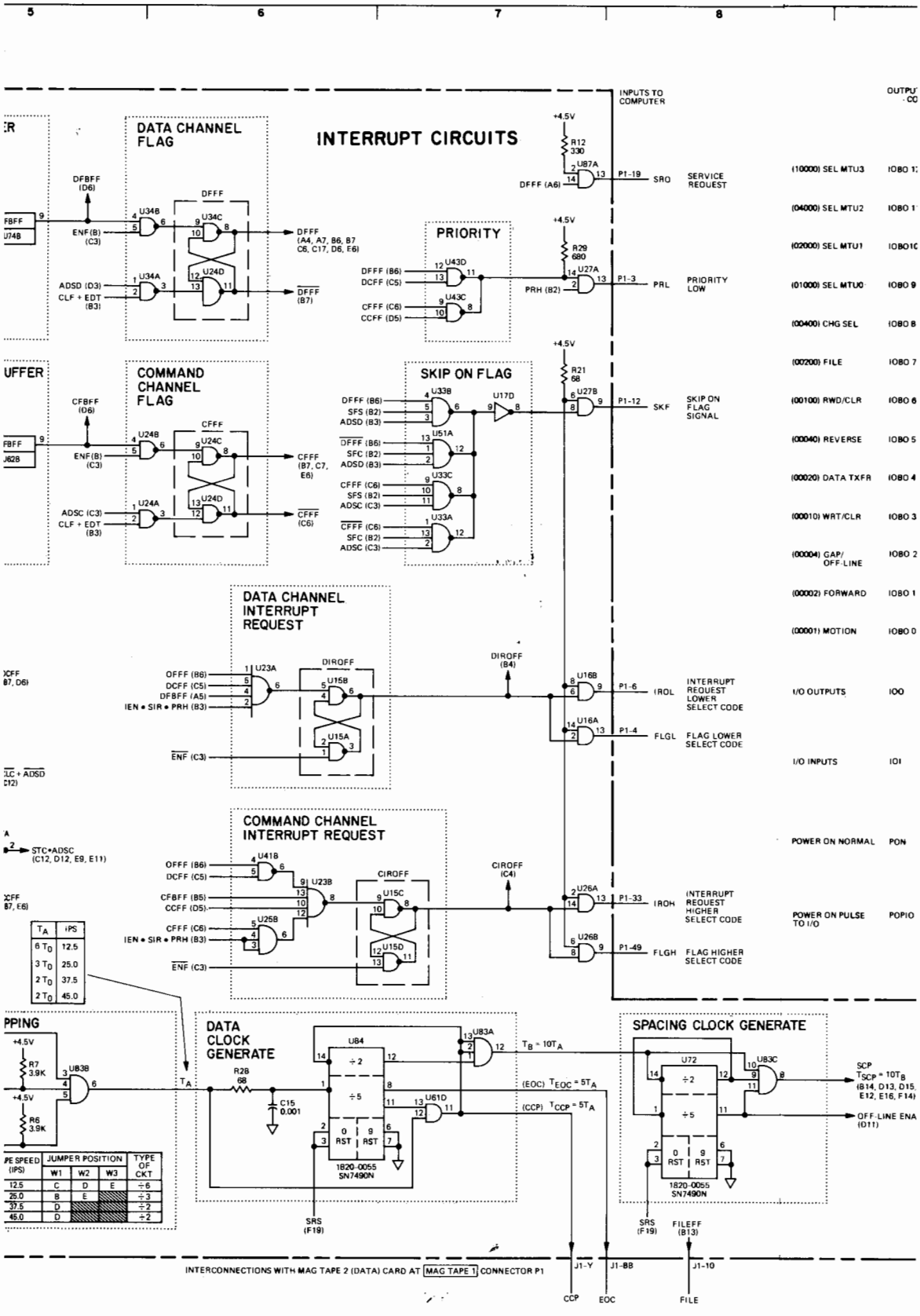


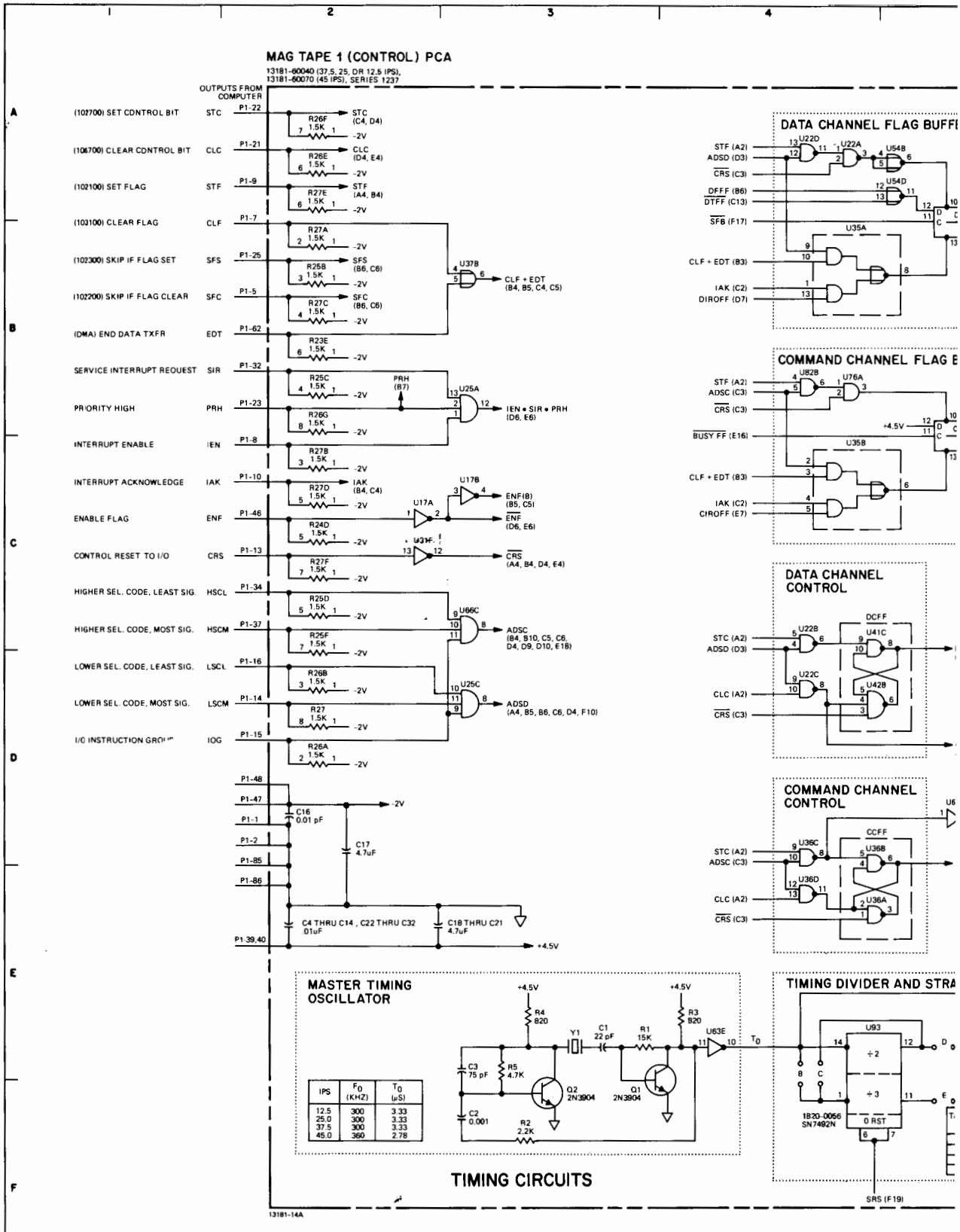
OCTAL	MNEMONIC	OPERATION
00110	CLR	CLEAR
01400	SL0	SELECT 0
02400	SL1	SELECT 1
04400	SL2	SELECT 2
10400	SL3	SELECT 3
00031	WCC	WRITE ONE RECORD
00211	WFM	WRITE FILE MARK
00215	GFM	GAP AND WFM
00015	GAP	GAP 4-INCHES
00023	RRF	READ ONE RECORD
00003	FSR	FORWARD SPACE RECORD
00041	BSR	BACKSPACE RECORD
00203	FSF	FORWARD SPACE FILE
00241	BSF	BACKSPACE FILE
00101	REW	REWIND
00105	RWO	REWIND/OFF-LINE

Figure 5-3. Mag Tape 1 Assembly Schematic Diagram


13
14
15
16
CUITS
MAG TAPE 1 CONNECTOR P1
INPUTS TO TAPE UNIT THRU
CONTROL CONNECTOR P5
MAG TAPE 1 CONNECTOR P1
OUTPUTS FROM TAPE UNIT THRU
CONTROL CONNECTOR P5
+4.5V
R19D 1.5K
U32D
J1-D
CS3
SELECT MTU3 COMMAND
R19C 1.5K
U32C
J1-C
CS2
SELECT MTU2 COMMAND
R19B 1.5K
U32B
J1-B
CS1
SELECT MTU1 COMMAND
R19A 1.5K
U32A
J1-A
CS0
SELECT MTU0 COMMAND
R11 1.5K
U71C
J1-T
CRW
REWIND COMMAND
R19F 1.5K
U71B
J1-F
CR
REVERSE COMMAND
R10 1.5K
U81B
J1-X
WSW
SET WRITE COMMAND
R19G 1.5K
U71D
J1-S
CL
OFF-LINE COMMAND
R19E 1.5K
U71A
J1-E
CF
FORWARD COMMAND
RWDFF
U96A
REVDISFF
U65A
FWDDISFF
U65B
U55D
FWDDISFF + REVDISFF
(E11, F18)
WRITE FF
U81C
U81D
R8 1.5K
R9 1.5K
WRTFF (D12,F11, F14)
WRTFF (F16)
STOP DELAY (E16)
DTFF (A4, E13, F9, F11)
PON(8) (D10)
J1-11 THRU -14
J1-17 THRU -24
READY STATUS
SR
J1-1
R18 619
R208 1.5K
REWIND STATUS
SRW
J1-2
R17 619
R20C 1.5K
LOAD POINT STATUS
SLP
J1-16
R13 619
R20G 1.5K
FILE PROTECT STATUS
SFP
J1-5
R15 619
SFP (C11)
ON-LINE STATUS
SL
J1-4
R16 619
R20E 1.5K
END-OF-TAPE STATUS
SET
J1-15
R20D 1.5K
R14 619
R20F 1.5K
MOTIO
BIT 3 F
FILE F
WCCF
CLR • POP
STOP
STOP DELAY
BUSY
U73B
U51B
U51C
U41A
U84A
U103D
U103C
U85
U73A
U87E
STOP DELAY (E16, B12)
STOP DELAY (C12, C13, D16)
1820-0099 SN7493N
CLR • POPIO (E10)
STOP (C14_D14)
U45C
U56C
U97E
BUSY
READ ENABLE
WRITE ENABLE
U106
U108C
U95A
U67F
GAP CLK (E11, E13)
U104A
U104B
GAPFF (E12)
WRTFF (C14)
(TWAS)
(EOR + FILE)•(FM + FILE) (E10)
REFF1
REFF 2
U108B
U108A
U103B
U42C
U41D
BOT (B17)
J1-R
J1-W
TWAS
WRTFF


9
10
11
12
CONTROL BITS BUFFER
CONTROL CIR
P1-57
P1-55
P1-58
P1-56
P1-54
P1-52
P1-53
P1-51
P1-42
P1-45
P1-41
P1-38
P1-35
P1-20
P1-24
P1-66
P1-17
R23C 1.5K
R23A 1.5K
R23D 1.5K
R23B 1.5K
R23G 1.5K
R24F 1.5K
R24G 1.5K
R24E 1.5K
R24B 1.5K
R24C 1.5K
R24A 1.5K
R25G 1.5K
R25E 1.5K
R26D 1.5K
R25A 1.5K
R23F 1.5K
R26C 1.5K
-2V
+4.5V
BIT12FF U77D
BIT11FF U77A
BIT10FF U77B
BIT9FF U77C
BIT7FF U91B
BIT6FF U91C
BIT5FF U91A
BIT4FF U44B
BIT3FF U44D
BIT2FF U44A
BIT1FF U44C
BIT0FF U91D
CHANGE SELECT (D18)
IOO(B) (D10)
ADSC (C3)
BUSYFF (D17)
U66B
U76C
U87B
IOBO 5 (B) (E18)
IOBO 3 (B) (E18)
IOBO 0 (B) (E18)
U76B
U37A
U37D
U45D
U45A
U37C
U61B
U61C
U76D
U17F
CR1
U12A
ACO (E18)
IOO (B) (B10, E18)
ACI (D1B, F11)
PON(B) (D15)
POPIO • CLR (D17, E14, E15, F18)
CLR
FILE
+4.5V
FILEFF U84B
MOTION (D12)
BIT1FF (D11)
SET (C17)
U42A
U63F
U54C
STOP DELAY (E18)
BIT6FF (E10)
U55B
MOTION (D12)
BIT6FF • MOTION (F18)
U86C
STC•ADSC (D5)
DATA TXFR FF
U52B
U52A
U86A
MOTION (D12)
BIT3FF (D17, E9, E11)
U75B
SFP (B17)
CLC • ADSD (D5)
STOP DELAY (E16)
BIT2FF (E11)
U73C
U63C
OFF-LINE ENABLE (E9)
RWD FF (B14)
BIT1FF (B12)
U53A
MOTION (D12)
WRTFF (C14)
U61A
STC•ADSC (D5)
MOTION (B12, C12, D17, E11, F18)
GAP
GAP CLK (E14)
BIT2FF (D11)
STC•ADSC (D5)
BOT (B17)
BIT3FF (C11)
MOTION (D12)
U82C
U86D
U75C
GAPFF U94B
GAPFF (F14)
(EOR•FILE) + (FM
U538
U638
U63D
FILEFF (B13)
(EOR•FILE) + (FM•FILE) (E13)
(EOR + FILE) • (FM + FILE) (E16)
SCP COUNTER ENABLE
FWDDISFF + REVDISFF (D15)
RE (F17)
WCCFF (F10)
WRTFF (C14)
WFMFF (D17)
DTFF (C13)
U103A
U82A
U12C
U12B
SCP (E9)
SCP COUNTI
U105
÷2
÷3
÷2
0 RST
DTFF (C13)
ADSD (B3)
WCCFF (D17, E11)
RE (F17)
FWDDISFF (D14)
ACI (D10)
J1-K
J1-8
J1-9
J1-U
J1-N
J1-P
J1-H
J1-L
FM
EOR
DTFF
ADSD
WCCFF
RE
FWDDISFF
ACI


INTERRUPT CIRCUITS
DATA CHANNEL FLAG
COMMAND CHANNEL FLAG
PRIORITY
SKIP ON FLAG
DATA CHANNEL INTERRUPT REQUEST
COMMAND CHANNEL INTERRUPT REQUEST
DATA CLOCK GENERATE
SPACING CLOCK GENERATE
INPUTS TO COMPUTER
OUTPUT
SERVICE REQUEST
PRIORITY LOW
SKIP ON FLAG SIGNAL
INTERRUPT REQUEST LOWER SELECT CODE
FLAG LOWER SELECT CODE
INTERRUPT REQUEST HIGHER SELECT CODE
FLAG HIGHER SELECT CODE
(10000) SEL MTU3
(04000) SEL MTU2
(02000) SEL MTU1
(01000) SEL MTU0
(00400) CHG SEL
(00200) FILE
(00100) RWD/CLR
(00040) REVERSE
(00020) DATA TXFR
(00010) WRT/CLR
(00004) GAP/ OFF-LINE
(00002) FORWARD
(00001) MOTION
I/O OUTPUTS
I/O INPUTS
POWER ON NORMAL
POWER ON PULSE TO I/O
1820-0055 SN7490N
INTERCONNECTIONS WITH MAG TAPE 2 (DATA) CARD AT MAG TAPE 1 CONNECTOR P1


MAG TAPE 1 (CONTROL) PCA
13181-60040 (37.5, 25, OR 12.5 IPS),
13181-60070 (45 IPS), SERIES 1237
OUTPUTS FROM COMPUTER
(102700) SET CONTROL BIT
STC
P1-22
R26F 1.5K
STC (C4, D4)
-2V
(106700) CLEAR CONTROL BIT
CLC
P1-21
R26E 1.5K
CLC (D4, E4)
(102100) SET FLAG
STF
P1-9
R27E 1.5K
STF (A4, B4)
(103100) CLEAR FLAG
CLF
P1-7
R27A 1.5K
(102300) SKIP IF FLAG SET
SFS
P1-25
R25B 1.5K
SFS (B6, C6)
(102200) SKIP IF FLAG CLEAR
SFC
P1-5
R27C 1.5K
SFC (B6, C6)
U37B
CLF + EDT (B4, B5, C4, C5)
(DMA) END DATA TXFR
EDT
P1-62
R23E 1.5K
SERVICE INTERRUPT REQUEST
SIR
P1-32
R25C 1.5K
PRH (B7)
PRIORITY HIGH
PRH
P1-23
R26G 1.5K
U25A
IEN • SIR • PRH (D6, E6)
INTERRUPT ENABLE
IEN
P1-8
R27B 1.5K
INTERRUPT ACKNOWLEDGE
IAK
P1-10
R27D 1.5K
IAK (B4, C4)
U17B
ENF(8) (B5, C5)
U17A
ENABLE FLAG
ENF
P1-46
R24D 1.5K
ENF (D6, E6)
CONTROL RESET TO I/O
CRS
P1-13
R27F 1.5K
CRS (A4, B4, D4, E4)
HIGHER SEL. CODE, LEAST SIG.
HSCL
P1-34
R25D 1.5K
U66C
HIGHER SEL. CODE, MOST SIG.
HSCM
P1-37
R25F 1.5K
ADSC (B4, B10, C5, C6, D4, D9, D10, E18)
LOWER SEL. CODE, LEAST SIG.
LSCL
P1-16
R26B 1.5K
U25C
LOWER SEL. CODE, MOST SIG.
LSCM
P1-14
R27 1.5K
ADSD (A4, B5, B6, C6, D4, F10)
I/O INSTRUCTION GROUP
IOG
P1-15
R26A 1.5K
P1-48
P1-47
P1-1
P1-2
P1-85
P1-86
C16 0.01 pF
-2V
C17 4.7uF
C4 THRU C14, C22 THRU C32 .01uF
C18 THRU C21 4.7uF
P1-39,40
+4.5V
DATA CHANNEL FLAG BUFFI
STF (A2)
ADSD (D3)
CRS (C3)
DFFF (B6)
DTFF (C13)
SFB (F17)
U22D
U22A
U54B
U54D
U35A
CLF + EDT (B3)
IAK (C2)
DIROFF (D7)
COMMAND CHANNEL FLAG E
U82B
U76A
BUSY FF (E16)
U35B
CIROFF (E7)
DATA CHANNEL CONTROL
STC (A2)
ADSD (D3)
CLC (A2)
DCFF
U22B
U41C
U22C
U42B
COMMAND CHANNEL CONTROL
CCFF
U36C
U36B
U36D
U36A
MASTER TIMING OSCILLATOR
IPS
F0 (KHZ)
T0 (μS)
12.5 300 3.33
25.0 300 3.33
37.5 300 3.33
45.0 360 2.78
R4 820
R3 820
Y1
C1 22 pF
R1 15K
U63E
C3 75 pF
R5 4.7K
Q2 2N3904
Q1 2N3904
C2 0.001
R2 2.2K
TIMING DIVIDER AND STRA
U93
÷2
÷3
1B20-0056 SN7492N
0 RST
SRS (F19)
TIMING CIRCUITS
13181-14A

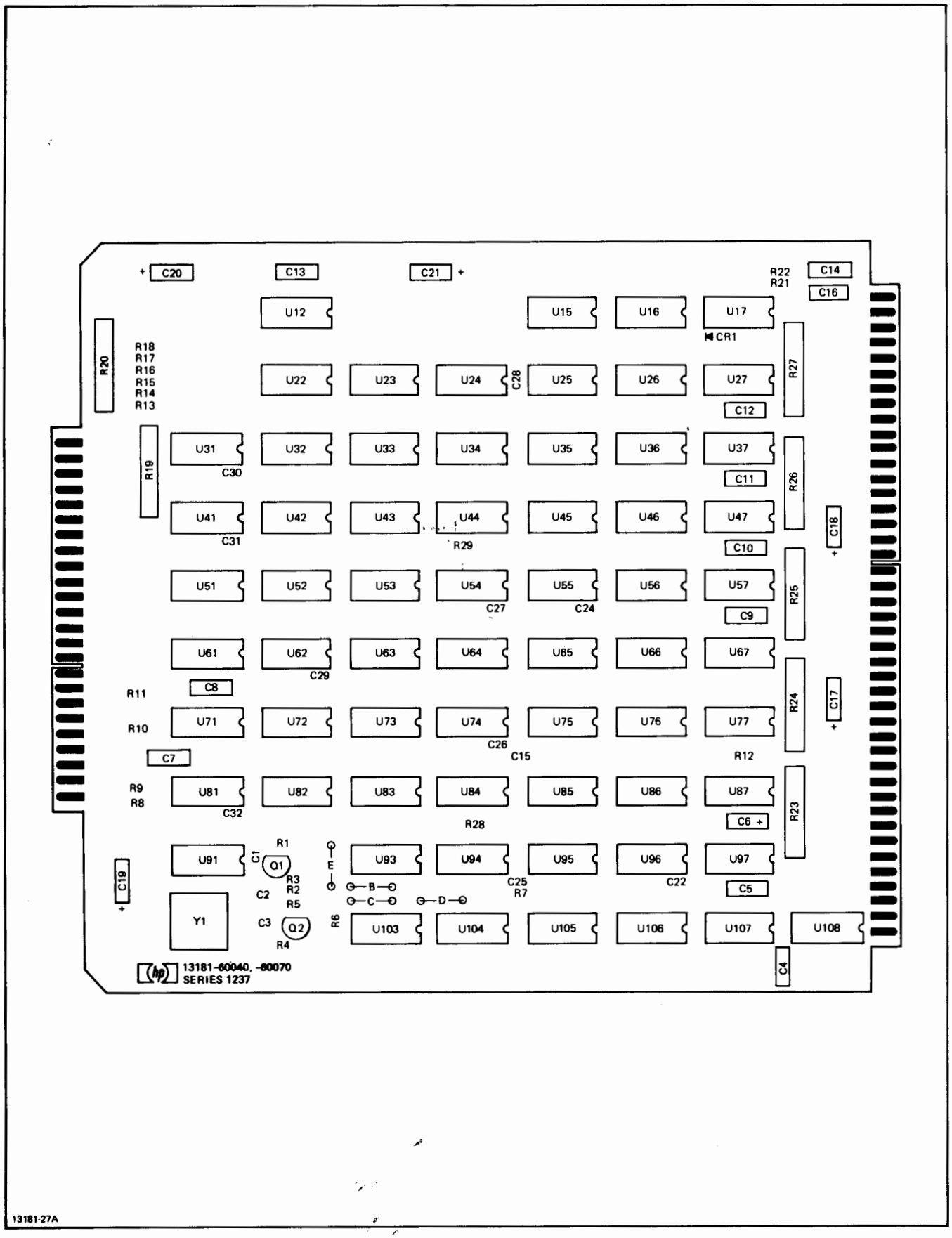


Figure 5-2. Mag Tape 1 Assembly Parts Location Diagram

Table 5-4. Mag Tape 2 Printed-Circuit Assembly (13181-60010) Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1 thru 7,9, 11 thru 15, 21, C22 thru C45	0160-2055	CAPACITOR, fxd, cer, 10 nF, 100 VDCW	56289	C023F101F103ZS22
C8	0160-0153	CAPACITOR, fxd, My, 0.001 μF, 10%, 200 WVDC	56289	192P10292-PTS
C17	0160-3572	CAPACITOR, fxd, cer, 330 pF, 20%, 200 WVDC	56289	C007F501F331K522-CDH
C18	0140-0191	CAPACITOR, fxd, mica, 56 pF, 5%	28480	0140-0191
C19	0160-0297	CAPACITOR, fxd, My, 1200 pF, 10%, 200 WVDC	56289	192P12292-PTS
C20	0160-3573	CAPACITOR, fxd, My, 680 pF, 20%, 200 WVDC	56289	2DF-M1
C49 thru C52	0180-0100	CAPACITOR, fxd, Ta, 4.7 μF, 10%	28480	0180-0100
CR1	1901-0450	DIODE, Si	09019	S156/DHD125
R1 thru 4, 26 thru 30	0683-1525	RESISTOR, fxd, comp, 1.5k, 5%, 1/4W	01121	CB1525
R5,7,24,25,31	1810-0020	RESISTOR ARRAY, 7-res, fxd, film, 1.5k	56289	200C1098-CRR
R6	0683-6805	RESISTOR, fxd, comp, 68 ohms, 5%, 1/4W	01121	CB6805
R14 thru 23	0757-0418	RESISTOR, fxd, comp, 619 ohms, 1%, 1/8W	28480	0757-0418
R34 thru 37	0683-1035	RESISTOR, fxd, comp, 10k, 5%, 1/4W	01121	CB1035
U11,84	1820-0376	INTEGRATED CIRCUIT, TTL	01295	SN74H40N
U12,22,32,34,43	1820-0256	INTEGRATED CIRCUIT, DTL	04713	MC858P
U13,15,25,56	1820-0282	INTEGRATED CIRCUIT, TTL	01295	SN7486N
U14,17,24,27,37, 47	1820-0437	INTEGRATED CIRCUIT, TTL	04713	MC4015P
U16,26,36,46,61	1820-0094	INTEGRATED CIRCUIT, DTL	04713	MC846P
U21,45,62,63,71	1820-0054	INTEGRATED CIRCUIT, TTL	01295	SN7400N
U23,35,73,83,93	1820-0174	INTEGRATED CIRCUIT, TTL	01295	SN7404N
U31	1820-0310	INTEGRATED CIRCUIT, DTL	04713	MC862P
U33,65	1820-0435	INTEGRATED CIRCUIT, TTL	01295	SN74180N
U41,53,72	1820-0099	INTEGRATED CIRCUIT, TTL	01295	SN7493N
U42	1820-0307	INTEGRATED CIRCUIT, DTL	07263	MC836P
U44,57	1820-0077	INTEGRATED CIRCUIT, TTL	01295	SN7474N
U51,52,94,95, 104,105	1820-0075	INTEGRATED CIRCUIT, TTL	01295	SN7473N
U54,81,82	1820-0068	INTEGRATED CIRCUIT, TTL	01295	SN7410N
U55	1820-0372	INTEGRATED CIRCUIT, TTL	01295	SN74H11N
U64,66	1820-0239	INTEGRATED CIRCUIT, TTL	04713	MC3002P
U67,76,77,86,87, 96,97,106,107, 117	1820-0956	INTEGRATED CIRCUIT, CTL	07263	CTμL9956
U74	1820-0070	INTEGRATED CIRCUIT, TTL	01295	SN7430N
U75,85	1820-0301	INTEGRATED CIRCUIT, TTL	01295	SN7475N
U91,92	1820-0515	INTEGRATED CIRCUIT, TTL	07263	SL50099
U103	1820-0454	INTEGRATED CIRCUIT, DTL	04713	MC1805P

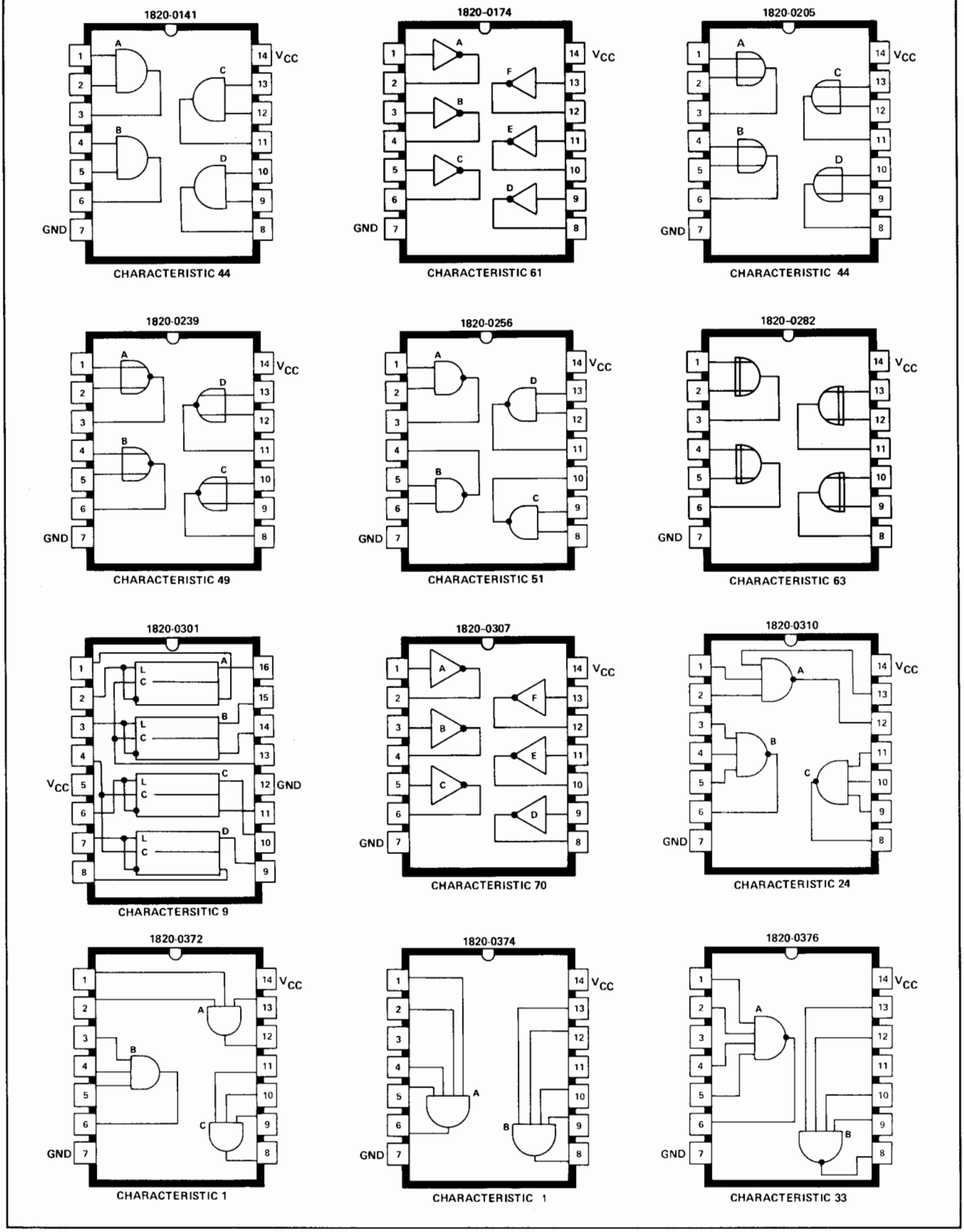


Figure 5-6. Integrated Circuit Pack Diagrams (Sheet 2 of 3)

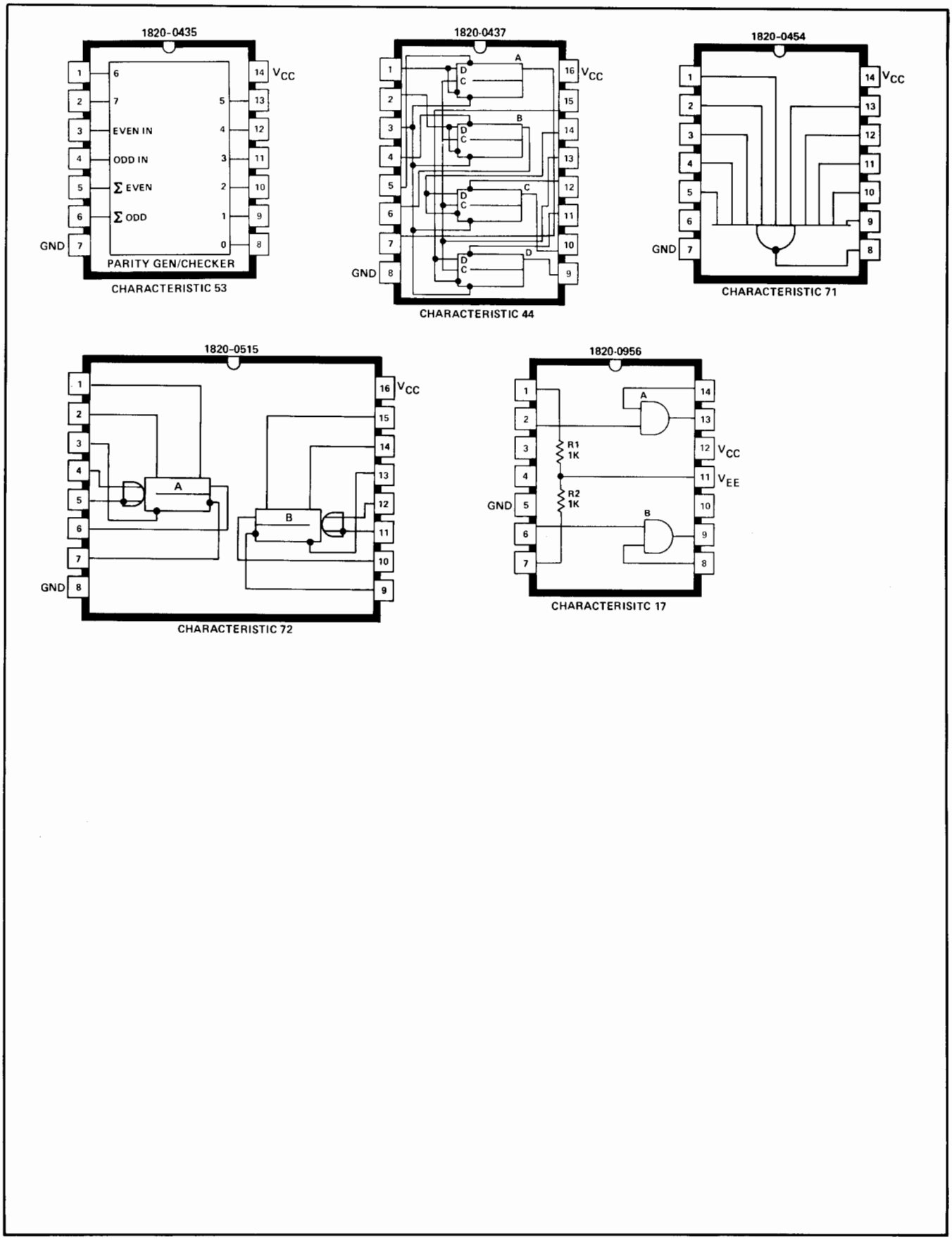


Figure 5-6. Integrated Circuit Pack Diagrams (Sheet 3 of 3)

Table 5-5. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS,MIN)	LOGIC 0 (VOLTS,MAX)	LOGIC 1 (VOLTS,MIN)	LOGIC 0 (VOLTS,MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
1	2.0	0.8	2.4	0.4	Logic 1	15	15
2	2.0	0.8	2.4	0.4	Logic 1	29	15
7	2.0	0.8	2.4	0.4	Logic 1	50(1)	50
8	2.0(2)	0.8	2.4	0.4	Logic 1	35	50
9	2.0(3)	0.8	2.4	0.4	Logic 1	40	25
24	2.0	0.9	2.6	0.5	Logic 1	80	30
28	2.0	0.9	2.6	0.5	Logic 1	80	40
29	2.0(4)	0.8(5)	2.4	0.4	Logic 1	135	135
33	2.0	0.8	2.4	0.4	Logic 1	11	11
39	2.0(6)	0.8	2.4	0.4	---	100	100
44	1.8	1.1	2.5	0.4	Logic 1	15	15
49	1.8	1.1	2.5	0.4	Logic 1	10	10
51	1.8	1.1	(7)	0.45	Logic 1	50	35
53	2.0	0.8	2.5	0.4	Logic 1	60	68
61	2.0	0.8	2.4	0.4	Logic 1	22	15
63	2.0	0.8	2.4	0.4	Logic 1	23 and 30	17 and 22
70	1.9	1.1	2.6	0.45	Logic 1	80	30
71	1.9	1.1	2.6	0.45	Logic 1	60	35
72	1.9	0.85	2.4	0.45	Logic 1	27	27

NOTES:

(1) Required clock pulse width 20 ns min; set-clear 25 ns min.

(2) Required pulse widths 30 ns min.

(3) Required pulse widths: clock 30 ns min; data 75 ns min.

(4) +2.2V for pin 1.

(5) +0.6V for pin 1.

(6) Required input pulse width 50 ns min.

(7) Level depends on load.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts for the HP 13181A Tape Unit Interface Kit. Table 6-1 lists the replaceable parts for the interface kit. Parts location diagrams for the printed-circuit assemblies in the kit are in section V of this manual. Tables 5-3 and 5-4 list the replaceable parts for these assemblies. The parts in tables 5-2 and 5-3 are listed in alphanumeric order by reference designation.

6-3. Tables 5-3, 5-4, and 6-1 list the following information for each part:

a. Circuit reference designation (if applicable).

b. Hewlett-Packard part number.

c. Description of the part. (Refer to table 6-2 for an explanation of abbreviations used in the DESCRIPTION column.)

d. Manufacturer of the part as a five-digit code. (Refer to table 6-3 for a listing of the manufacturers that correspond to the codes.)

e. Manufacturer's part number.

6-4. ORDERING INFORMATION.

6-5. To order replacement parts, address the order or inquiry to the local HP Sales and Service Office. (Refer to the list at the back of this manual.) Specify the following information for each part ordered.

a. Kit model number.

b. HP stock number for each part.

c. Description of each part.

d. Circuit reference designation (if applicable).

Table 6-1. HP 13181A Tape Unit Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
13181-60030	INTERCONNECT CABLE	28480	13181-60030	1
13181-60040	MAG TAPE 1 PRINTED-CIRCUIT ASSEMBLY, 37.5, 25 ips (option 001), and 12.5 ips (option 002) (Refer to table 5-3.)	28480	13181-60040	1
13181-60070	MAG TAPE 1 PRINTED-CIRCUIT ASSEMBLY, 45 ips (option 003 only) (Refer to table 5-3.)	28480	13181-60070	1
13181-60010	MAG TAPE 2 PRINTED-CIRCUIT ASSEMBLY (Refer to table 5-4.)	28480	13181-60010	1
13181-90000	OPERATING AND SERVICE MANUAL	28480	13181-90000	1

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A = assembly	K = relay	TB = terminal board
B = motor, synchro	L = inductor	TP = test point
BT = battery	M = meter	U = integrated circuit, non-repairable assembly
C = capacitor	P = plug connector	V = vacuum tube, photocell, etc.
CB = circuit breaker	Q = semiconductor device other than diode or integrated circuit	VR = voltage regulator
CR = diode	R = resistor	W = jumper wire
DL = delay line	RT = thermistor	X = socket
DS = indicator	S = switch	Y = crystal
E = Misc electrical parts	T = transformer	Z = tuned cavity, network
F = fuse		
FL = filter		
J = receptacle connector		

ABBREVIATIONS

A = amperes	gra = gray	PCA = printed-circuit assembly
ac = alternating current	grn = green	PWB = printed-wiring board
Ag = silver		phh = phillips head
Al = aluminum	H = henries	pk = peak
ar = as required	Hg = mercury	p-p = peak-to-peak
adj = adjust	hr = hour(s)	pt = point
assy = assembly	Hz = hertz	prv = peak inverse voltage
	hdw = hardware	PNP = positive-negative-positive
b = base	hex = hexagon, hexagonal	pwv = peak working voltage
bp = bandpass		porc = porcelain
bpi = bits per inch	ID = inside diameter	posn = position(s)
blk = black	IF = intermediate frequency	pozi = pozidrive
blu = blue	in. = inch, inches	
brn = brown	I/O = input/output	rf = radio frequency
brs = brass	int = internal	rdh = round head
Btu = British thermal unit	incl = include(s)	rms = root-mean-square
Be Cu = beryllium copper	insul = insulation, insulated	rwv = reverse working voltage
	impgrg = impregnated	rect = rectifier
cpi = characters per inch	incand = incandescent	r/min = revolutions per minute
coll = collector	ips = inches per second	RTL = resistor-transistor logic
cw = clockwise		
ccw = counterclockwise	k = kilo (10^3), kilohm	s = second
cer = ceramic		SB, TT = slow blow
com = common	lp = low pass	Se = selenium
crt = cathode-ray tube		Si = silicon
CTL = complementary-transistor logic	m = milli (10^{-3})	scr = silicon controlled rectifier
cath = cathode	M = mega (10^6), megohm	sst = stainless steel
Cd pl = cadmium plate	My = Mylar	stl = steel
comp = composition	mfr = manufacturer	spcl = special
conn = connector	mom = momentary	spdt = single-pole, double-throw
compl = complete	mtg = mounting	spst = single-pole, single-throw
	misc = miscellaneous	
dc = direct current	met. ox. = metal oxide	
dr = drive	mintr = miniature	Ta = tantalum
DTL = diode-transistor logic		td = time delay
depc = deposited carbon	n = nano (10^{-9})	Ti = titanium
dpdt = double-pole, double-throw	nc = normally closed or no connection	tgl = toggle
dpst = double-pole, single-throw	Ne = neon	thd = thread
	no. = number	tol = tolerance
em = emitter	n.o. = normally open	TTL = transistor transistor logic
ECL = emitter-coupled logic	np = nickel plated	
ext = external	NPN = negative-positive-negative	
encap = encapsulated	NPO = negative-positive zero (zero temperature coefficient)	U(μ) = micro (10^{-6})
elctlt = electrolytic	NSR = not separately replaceable	
	NRFR = not recommended for field replacement	V = volt(s)
F = farads		var = variable
FF = flip-flop		vio = violet
flh = flat head	OD = outside diameter	Vdcw = direct current working volts
flm = film	OBD = order by description	
fxd = fixed	orn = orange	W = watts
filh = fillister head	ovh = oval head	ww = wirewound
	oxd = oxide	wht = white
G = giga (10^9)		WIV = working inverse voltage
Ge = germanium	p = pico (10^{-12})	
gl = glass	PC = printed circuit	yel = yellow
gnd = ground(ed)		

Table 6-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wisconsin
01295	Texas Instruments Inc. Semiconductor Components Division	Dallas, Texas
04713	Motorola Semiconductor Prod. Inc.	Phoenix, Arizona
07263	Fairchild Camera & Inst. Corp. Semiconductor Division	Mountain View, California
09019	General Electric Co. Semiconductor Products Dept.	Lynchburg, Virginia
19701	Electra Manufacturing Compnay	Mineral Wells, Texas
28480	Hewlett-Packard Company	Palo Alto, California
56289	Sprague Electric Company	N. Adams, Massachusetts
72982	Erie Technological Prod. Inc.	Erie, Pennsylvania

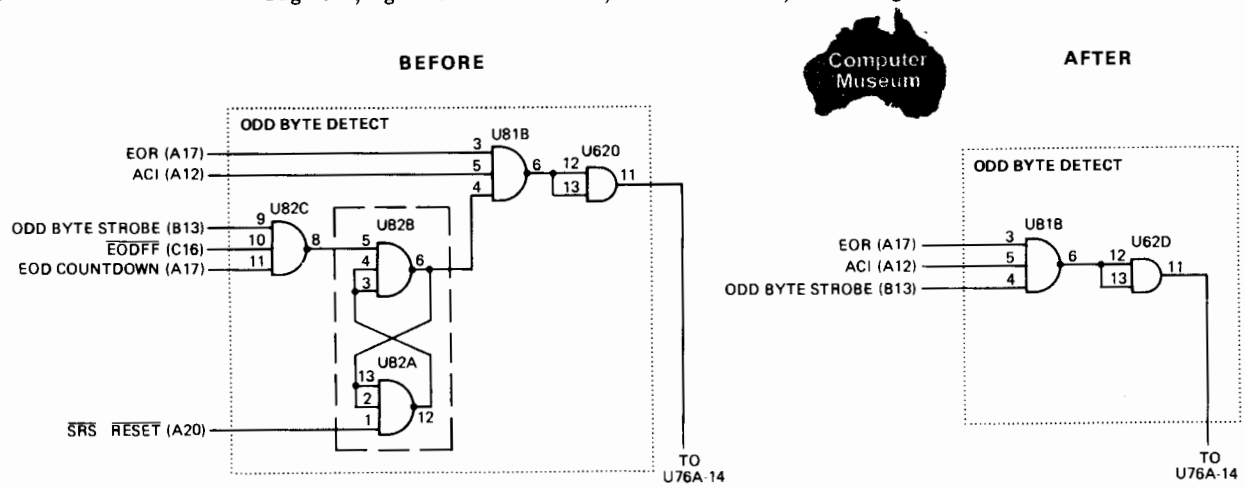
APPENDIX A
BACKDATING INFORMATION

This backdating appendix provides information for making this manual applicable to earlier configurations of HP 13181A Interface Kits. Changes are identified numerically in this appendix. Refer to the following table to determine which changes are associated with particular series-numbered printed-circuit assemblies. To backdate a manual to correctly represent a given interface kit, perform the changes in reverse sequence (highest numbered change first).

Description	Part Number	Series		Changes
		From	To	
Mag Tape 1 PCA	13181-60020	1034	1025	1 and 2
Mag Tape 1 PCA	13181-60040	1034	1025	1 and 2
Mag Tape 1 PCA	13181-60050	1034	1025	1 and 2
Mag Tape 1 PCA	13181-60060	1034	1025	1 and 2
Mag Tape 1 PCA	13181-60020	1037	1034	3 and 4
Mag Tape 1 PCA	13181-60040	1037	1034	3 and 4
Mag Tape 1 PCA	13181-60050	1037	1034	3 and 4
Mag Tape 1 PCA	13181-60060	1037	1034	3 and 4
Mag Tape 2 PCA	13181-60010	1039	1025	5 thru 7
Mag Tape 2 PCA	13181-60010	1042	1039	8 thru 10
Mag Tape 1 PCA	13181-60070	No change		11 thru 18
Mag Tape 1 PCA	13181-60020	1049	1037	19
Mag Tape 1 PCA	13181-60040	1049	1037	19
Mag Tape 1 PCA	13181-60050	1049	1037	19
Mag Tape 1 PCA	13181-60060	1049	1037	19
Mag Tape 1 PCA	13181-60070	1049	1037	19
Mag Tape 2 PCA	13181-60010	1103	1042	20 thru 22
Mag Tape 2 PCA	13181-60010	1139	1103	23 and 24
Mag Tape 1 PCA	13181-60040	1141	1049	25 and 26
Mag Tape 1 PCA	13181-60050	1141	1049	25 and 26
Mag Tape 1 PCA	13181-60060	1141	1049	25 and 26
Mag Tape 1 PCA	13181-60070	1141	1049	25 and 26
Mag Tape 2 PCA	13181-60010	1149	1139	27 thru 29
Mag Tape 1 PCA	13181-60050	No change		30 and 31
Mag Tape 1 PCA	13181-60060	No change		30 and 31
Mag Tape 1 PCA	13181-60040	1213	1141	32
Mag Tape 1 PCA	13181-60070	1213	1141	32
Mag Tape 2 PCA	13181-60010	1237	1149	33
Mag Tape 1 PCA	13181-60040	1237	1213	34
Mag Tape 1 PCA	13181-60070	1237	1213	34

CHANGE	DESCRIPTION
1	Page 5-5, figures 5-2 and 5-3. Change series code from 1034 to 1025.
2	Page 5-5, figure 5-3. Delete U67B (zone B10) and connect U76C-8 direct to U77D-13, U77A-13, U77B-13, and U77C-13.
3	Page 5-4, table 5-3. a. Add part number 13181-60020 to table title. b. Delete R29.
4	Page 5-5, figures 5-2 and 5-3. a. Change series code from 1037 to 1034. b. Delete resistor R29. c. Add part number 13181-60020 to the PCA identification.
5	Page 5-7, figures 5-4 and 5-5. Change series code from 1039 to 1025.
6	Page 5-7, figure 5-5. Delete the following wiring connections: a. J1-17 (zone A9) to U51B-5 (B3). b. U51A-12 (A5) to U51B-6 (B3). c. U51B-9 (B3) to U66A-2 (A3) and U66B-5 (B3). d. U51B-9 (B3) to U33-3 (B4). e. U51B-8 (B3) to U33-4 (B4). f. U41-8 (B9) to U32B-5 (B7), U32D-12 (B7), U34B-5 (B7), U34D-12 (C7), U12B-5 (C7), U12D-12 (C7), U22B-5 (D7), U22D-12 (D7), and U43B-6 (E7). g. U71C-8 (B8) to U71B-5 (B8). h. U41-11 (C9) to U31B-5 (D8). i. U42C-6 (B9) to U31B-4 (D8). j. U42B-4 (D9) to U43D-13 (D9). k. U51A-12 (A5) to U41-2, 3 (C9).
7	Page 5-7, figure 5-5. Add the following wiring connections: a. U51A-12 (A5) to U51B-5 (B3). b. U41-12 (B9) to U66A-2 (A3) and U66B-5 (B3). c. U71C-8 (B8) to U51B-6 (B3). d. U51B-9 (B3) to U71B-5 (B8). e. U51B-8 (B3) to U41-2, 3 (C9). f. U41-11 (C9) to U43D-13 (D9). g. U41-8 (B9) to U81C-11 (C8). h. U42D-8 (A9) to U31B-4 (D8). i. U42B-4 (D9) to U32B-5 (B7), U32D-12 (B7), U34B-5 (B7), U34D-12 (C7), U12B-5 (C7), U12D-12 (C7), U22B-5 (D7), U22D-12 (D7), and U43B-6 (E7).
8	Page 5-6, table 5-4. Delete U82.
9	Page 5-7, figure 5-4. Delete U82 and change series code from 1042 to 1039.

CHANGE	DESCRIPTION
10	Page 5-7, figure 5-5. Delete U82, as shown below, and change series code from 1042 to 1039.



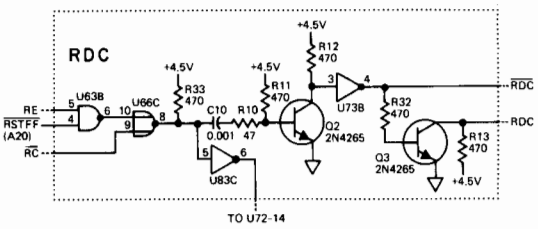
11	Page 1-1, paragraph 1-4, line 7. Delete the sentence "DMA is always required for 45 ips configurations."
12	Page 1-1, paragraph 1-6a. Delete reference to part number 13181-60070.
13	Page 1-1, paragraph 1-12, line 4, 7, and 8. Delete references to option 003 (45 ips).
14	Page 1-2, tables 1-1 and 1-2. Delete the references to 45 ips tape speed.
15	Page 3-1, paragraph 3-4, line 8. Delete reference to 45 ips tape speed.
16	Page 3-1, paragraph 3-5, line 4. Delete reference to 45 ips tape speed.
17	Page 5-4, table 5-3. Delete reference to part number 13181-60070 from table title.
18	Page 5-5, figures 5-2 and 5-3. Delete reference to part number 13181-60070 and 45 ips tape speed.
19	No change to equipment.
20	Page 5-6, table 5-4. a. Delete C16, C17, C18, CR1, R34, R35, and U92. b. Add Q2 and Q3 to the Q1 entry (all three transistors are the same type). c. Add C10 to the C8 entry (C10 and C8 are the same type capacitor). d. Add the following components:

R11,R12,R13 R32,R33	0683-4715	RESISTOR, fxd, 470 ohm, 5%, 1/4 W	01121	CB 4715
R10	0683-4705	RESISTOR, fxd, 47 ohm, 5%, 1/4 W	01121	CB 4705

21	Page 5-7, figures 5-4 and 5-5. Delete C16, C17, C18, CR1, R34, R35, and U92. (RDC circuit) and change series code from 1103 to 1042.

CHANGE	DESCRIPTION

22 Page 5-7, figure 5-5. Replace the RDC circuit (deleted in the preceding step) with the following circuit.



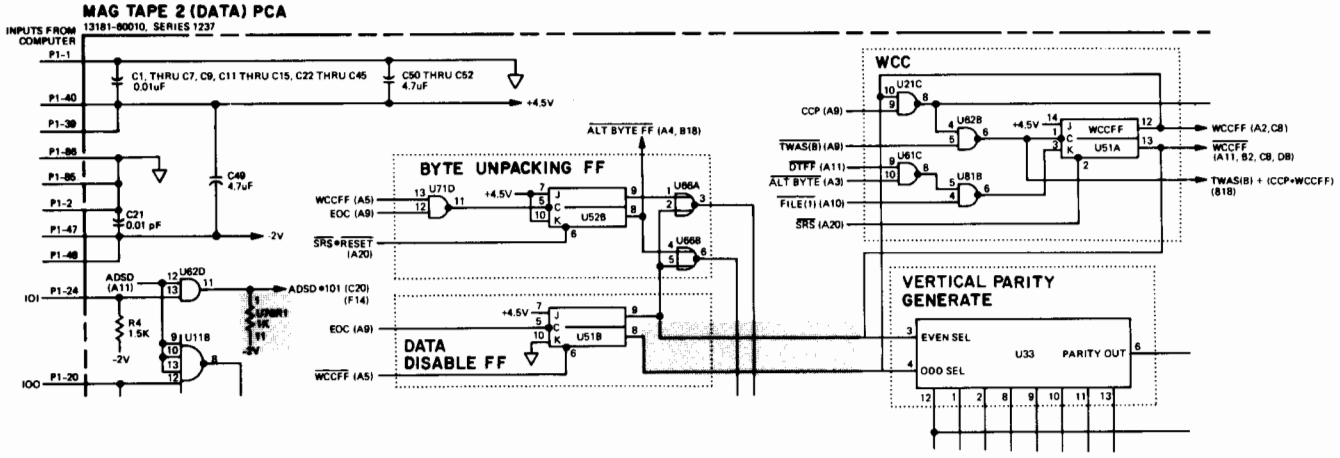
23 Page 5-6, table 5-4.

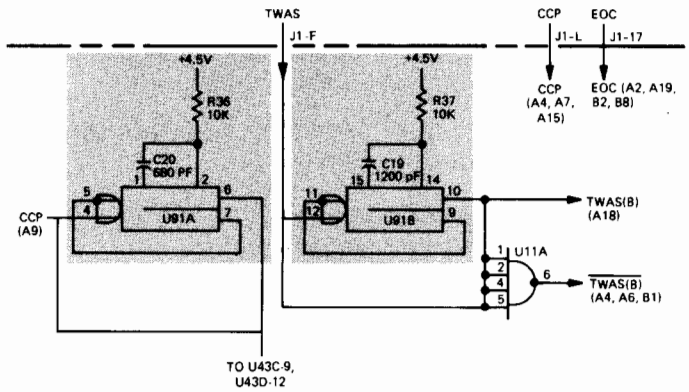
a. Delete C19, C20, R34, R35, U91, and U117.

b. Add the following entries:

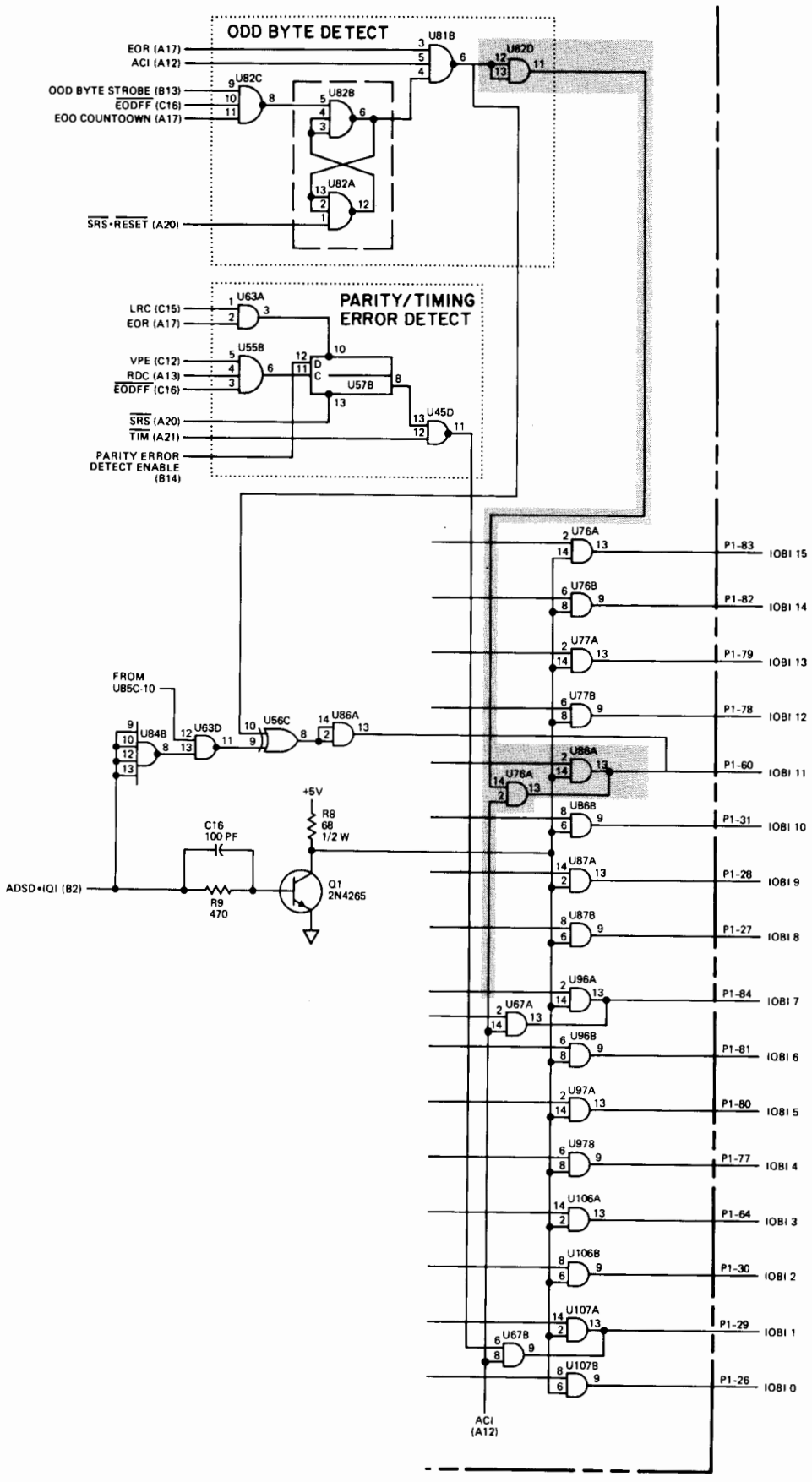
C16	0160-2204	CAPACITOR, fxd, mica, 100 pF, 5% 300 WVDC	28480	0160-2204
Q1	1854-0274	TRANSISTOR, NPN, sil, 1 W	04713	55384
R8	0686-6805	RESISTOR, fxd, 68 ohms, 5%, 1/2 W	01121	EB 6805
R9	0683-4715	RESISTOR, fxd, 470 ohms, 5%, 1/4 W	01121	CB 4715
R34,R35	0757-0442	RESISTOR, fxd, 10K, 1%, 1/8 W	91637	CMF-55-1, T-1

24 Page 5-7, figure 5-5. Change figure 5-5 as shown on the following three partial schematics (shaded areas indicate deletions).





CHANGE	DESCRIPTION
24 (cont.)	



CHANGE	DESCRIPTION
25	Page 5-4, table 5-3. Replace plug-in jumper 5040-1485 with jumper wire 8159-0005.
26	Page 5-5, figures 5-2 and 5-3. Change series code from 1141 to 1049.
27	Page 5-6, table 5-4. Delete entry for part number 0160-2055 (C1 thru 7, 9, 11 thru 15, 21) and associated note "†Series 1149 only" at bottom of page.
28	Page 5-7, figures 5-4 and 5-5. a. Delete C21. b. Change series code from 1149 to 1139.
29	Page 5-7, figure 5-5. Change value of C1 thru C7, C9, and C11 thru C15 from 0.01 μF to 1.0 μF.
30	Page 5-4, table 5-3. a. Add part numbers 13181-60050 and 13181-60060 to the table title. b. Delete entry for C4 thru C14 and C16 (part number 0160-2055) and associated note at bottom of page.
31	Page 5-5, figures 5-2 and 5-3. a. Add part numbers 13181-60050 and 13181-60060 to the Mag Tape 1 PCA and change the series code from 1213 to 1141. b. Delete capacitor C16.
32	Page 5-5, figure 5-3. a. Disconnect U42C-10 (zone F17) from U53B-6 (E10). b. Disconnect U52A-4 (D13) from U52A-5 (D13). c. Connect U53B-6 (E10) to U52A-5.
33	Pages 5-6 and 5-7, table 5-4 and figures 5-4 and 5-5. Delete capacitors C22 thru C45 and C49 thru C52 and change series code to 1149.
34	Pages 5-4 and 5-5, table 5-3 and figures 5-2 and 5-3. Delete capacitors C17 thru C32 and change series code to 1213.

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CERTIFICATION

The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.

MANUAL PART NO. 13181-90000
MICROFICHE PART NO. 13181-90091

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