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12920-16002

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12920 A/B ASYNCHRONOUS MULTIPLEXER INTERFACE DIAGNOSTIC

reference manual

FOR HP 2100 Series Computers

HEWLETT PACKARD

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Section I

INTRODUCTION

1-1. GENERAL

This diagnostic test program confirms proper operation of the HP 12920A or 12920B Asynchronous Multiplexer Interface. The basic I/O portion of the cards which includes the Flag and Control circuits will be tested. The status, control, receive and transmit features will be tested. This testing will use the test cable(s) in conjunction with the communications multiplexer panel.

Two absolute binary tapes are used to test the data and control boards. Binary tape number 12920-16001 tests the data boards. Binary tape number 12920-16002 tests the control board.

1-2. REQUIRED HARDWARE

The following hardware is required:

a. HP 2100 series computer with a minimum 4K memory.
b. An HP 12920B Asynchronous Multiplexer Interface consisting of:
    (1) 12920-60001 Upper Select Code Data Board
    (1) 12920-60002 Lower Select Code Data Board
    (1) 12922-60001 Control Board
    or an HP 12920A Asynchronous Multiplexer consisting of:
    (1) 12921-60001 Upper Select Code Data Board
    (1) 12921-60002 Lower Select Code Data Board
    (1) 12922-60001 Control Board
c. A test cable (HP 30062-60003).
d. A communication multiplexer panel (30062-60002).
e. A console teleprinter device for message reporting (recommended but not required).
f. A paper tape reading device (for loading only).

1-3. REQUIRED SOFTWARE

The following software is required:

a. Diagnostic Configurator Product No. 24296 used for equipment configuration and as a console device driver. The product includes the following part no.:
    Binary object tape Part No. 24296-60001
    Manual Part No. 02100-90157
b. HP 12920 Async. Mux. Diagnostic binary object tape, Part Nos. 12920-16001 and 12920-16002.

The Diagnostic serial number (DSN) is contained in memory location 126_8 of the program. The DSN for the Data Board is 103010_8 and the DSN for the Control Board is 103011_8.

Section II

PROGRAM ORGANIZATION

2-1. ORGANIZATION

This diagnostic program is divided into two absolute binary tapes: (1) 12920 Data Board Tape, consisting of eight tests; (2) 12922 Control Board Tape, consisting of six tests.

Each tape has a control and an initialization section which prepares the diagnostic by accepting the select code and options required by the tests. In addition to that, each tape has a basic I/O test which consists of seven subtests.

The Data Board tape includes tests which verify the operation of the send and receive data paths along with BREAK, PARITY, DIAGNOSE, ECHO, SYNC and CHARACTER LOST circuits.

The Control Board tape includes tests on the ADDRESS REGISTER, COMMAND, STATUS, COMMAND REGISTER ADDRESSING, STATUS INTERRUPT and SCAN circuits.

These tests are called into execution by the control section as sequential or selectable subroutines.

2-2. TEST CONTROL AND EXECUTION

The program outputs a title message to the console device if present for operator information then executes the tests according to the options selected on the switch register by the operator. The control section mainly checks switch register bits 15, 13 and 12.

The control also keeps count of the number of passes that have been completed and will output the pass count at the completion of each pass (if switch register bit 10 is clear). The count will be reset only if the program is restarted.

Test sections are executed one after another in each diagnostic pass. User selection or default will determine which test sections will be executed. (See 2-3 of PROGRAM ORGANIZATION.)

2-3. SELECTION OF TESTS BY OPERATOR

The operator has the capability to select his own tests or sequence of tests with the help of bit 9 in the switch register. Paragraph 3-4 outlines the test selection.

2-4. MESSAGE REPORTING

There are two types of messages, error and information. Error messages are used to inform the operator of a failure of the card to respond to a given control or sequence. Information messages are used to inform the operator of the progress

of the diagnostic or instruct the operator to perform some operation related to the interface's function. In this case an associated halt will occur to allow the operator time to perform the function, the operator must then press RUN.

If a console device is used, the printed message will be preceded by an E (error) or H (information) and a number (in octal). The number is also related to the halt code when a console device is not available.

Example - Error with halt
Message: EØ16 CLC CH ERROR
Halt Code: $1Ø2Ø16_8$ (T or Memory Data Register)

Example - Information with halt
Message: HØ24 PRESS PRESET (EXT & INT), RUN
Halt Code: $1Ø2Ø24_8$

Example - Information only
Message: HØ25 BI-0 COMP
Halt Code: None

Error messages can be suppressed by selection of the switch register bit 11 and error halts can be suppressed by switch register bit 14. This is useful when looping on a single section that has several errors.

Information messages are suppressed by Switch Register bit 10. Operator intervention is suppressed by setting Switch Register bit 8 (i.e., Preset Test in BI-0). When Switch Register bit 12 is set, the tests that are selected will be repeated. All operator intervention will be suppressed.

2-5. PROGRAM LIMITATIONS

2-6. PRIORITY STRING

The capability of the interface to receive, pass and deny priority is not completely checked by this diagnostic. If the interface does not receive priority (PRH from next lower select code) an error EØ14 NO INT will occur. To check this remove a board of a lower select code and run the Basic I/O test and the above mentioned error should occur. Checking the interface's ability to pass or deny priority is beyond the scope of this diagnostic.

Section III

OPERATING PROCEDURES

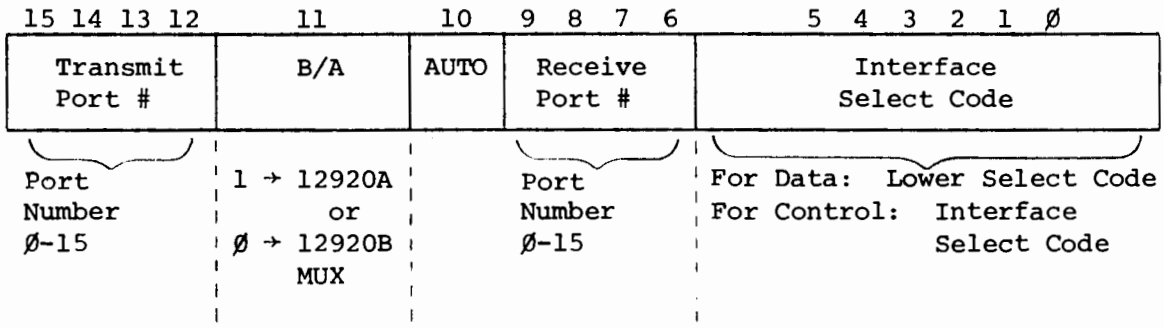
3-1. LOADING AND CONFIGURING

3-2. SINGLE COMPUTER ENVIRONMENT

Loading and configuring the diagnostic in a single computer environment should be done as follows:

1. Load Diagnostic Configurator into computer, if diagnostic has not been previously configured.
2. Configure the Diagnostic Configurator as described in M.O.D. (02100-90157).
3. At this time the user may optionally choose to dump a copy of the configured configurator. If so, set 'P' reg for ØX7677 ('X' will vary as to memory size) set bits Ø-5 of 'S' reg to select code of punch and press 'RUN'.
4. Load diagnostic into computer (Data or Control tape). Follow step 3 above if a configured paper tape is desired.
5. Set 'P' reg to 100_8 and set the switch reg as follows:
   (In case of restarting or reconfiguring set 'P' reg to 100_8 and continue with the new switch reg setting.)

Figure 3-1. Switch Register Settings



NOTE: If bits 12-15 and 6-9 are zero diagnostic will assume auto mode. A port is defined as one of the 16 connectors JØ-J15 on the connector panel No. 30062-60002.

6. Press 'RUN', computer will halt and display: 1Ø2Ø74. Follow step 3 above if a configured paper tape is desired.
7. Set switch register to desired options, as described in Table 3-3. Bit 12 is used to loop on the diagnostic if set. Bit 13 is used to loop on a given test that is running at the time. Bit 15, if set, will halt the computer at the completion of a test. Press RUN and the diagnostic will begin.

3-3. DIAGNOSTIC LOADING IN TWO COMPUTER ENVIRONMENT

When loading the diagnostic using two computers as in 2000C or 2000F systems, the following steps are followed:

1. Load Diagnostic Configurator into system computer.

2. Configure as previously described (refer Diagnostic Configurator 02100-90157). Be sure to configure to memory size, options and select codes of the I/O processor not the system processor.
3. Load Multiplexer diagnostic (Data or Control tape) into the system computer.
4. Using Diagnostic Configurator "Dump" routine as follows to transfer configured diagnostic from system computer to I/O processor.
   a. Set I/O processor "P" register to start of protected loader (Ø177ØØ for 8K), press: preset Int/External, loader Enable and Run.
   b. Set "P" register of SYSTEM computer to ØX7677 (Ø17677 if I/O processor is 8K). Set the switch register with the select code of the Processor Interconnect Card (12566) of the System Computer (1ØB for 2000C' and 2000F systems). Press preset EXT/INT, and RUN.
   c. I/O processor will display 1Ø2Ø77 when loaded. Halt system computer.
   d. Select "P" register 1ØØB in I/O processor and proceed in configuring diagnostic as previously described in paragraph 3-2 no. 5.

3-4. TEST SELECTION BY OPERATOR

The control portion of the program provides for the operator to select his own test or sequence of tests to be run. The operator sets switch register bit 9 to indicate he wants to make a selection and press RUN. The computer will come to a halt 102075 to indicate it is ready for the selection. If the program is running, that test will be completed and then the program will halt. Now the operator loads the A register with the tests desired. The A register bit Ø represents Test ØØ, bit 1 represents Test Ø1, and so on up to bit X which represents Test X*. The operator must then clear switch register bit 9 and press run. The operators selection will then be run. If the operator clears all bits then all the tests defined in Table 3-1, or 3-2 will be executed.

*Refer to Table 4-1.

Test Selection Summary

Table 3-1.

A-REGISTER BIT	IF SET WILL EXECUTE DATA BOARD
0	Test 00 BI-0 Test
1	Test 01 Send/Receive Test
2	Test 02 Break Test
3	Test 03 Parity Test
4	Test 04 Diagnostic
5	Test 05 Echo Test
6	Test 06 Sync Test
7	Test 07 Character Lost Test

Table 3-2.

A-REGISTER BIT	IF SET WILL EXECUTE CONTROL BOARD
0	Test 00 BI-0 Test
1	Test 01 Address Register Test
2	Test 02 Command and Register Test
3	Test 03 Command Register Addressing Test
4	Test 04 Status Interrupt Test
5	Test 05 Scan Test

Refer to Section IV for complete description of each test.

Table 3-3. Switch Register Options

BIT	MEANING IF SET
0	
1	Reserved
2	Reserved
3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Suppress tests requiring operator intervention.
9	Abort current diagnostic execution and halt (1Ø2Ø75); user may specify a new group of tests in the A register, clear bit 9 and then press RUN.
10	Suppress non-error messages.
11	Suppress error messages.
12	Repeat all selected tests after diagnostic run is complete without halting. Message "PASS XXXXXX" will be output before looping unless bit 1Ø is set or teletype is not present. Also those tests requiring operator intervention will be suppressed.
13	Repeat last test executed (loop on test).
14	Suppress error halts.
15	Halt (1Ø2Ø76) at the end of each test; the A register will contain the test number in octal.

Section IV

DIAGNOSTIC PERFORMANCE

4-1. TESTS DESCRIPTION

4-2. TEST Ø BASIC I/O CHECKS

Subtest 1 - Checks the ability to clear set and test the interrupt system. The following instruction combinations are tested:

CLF 0 - SFC 0
CLF 0 - SFS 0
STF 0 - SFC 0
STF 0 - SFS 0

Errors in the above sequences produce error messages EØØØ-EØØ3 as shown in Table 4-2.

Subtest 2 - Checks the ability to clear, set and test the card select code. The following instruction combinations are tested:

CLF CH - SFC CH
CLF CH - SFS CH
STF CH - SFC CH
STF CH - SFS CH

Errors in the above sequences produce error messages E005-E010 as shown in Table 4-2.

Subtest 3 - Checks that the test select code does not cause an interrupt with the flag and control set on the card and the interrupt system off. The sequence of instructions is shown below:

STF Ø
STF CH
STC CH
CLC Ø

The CLF Ø instruction should inhibit an interrupt from occurring. Error message EØØ4 occurs if CLF Ø fails.

Subtest 4 - Checks that the flag of the card under test is not set when all other select code flags are set. Error message EØ11 occurs if a flag is set incorrectly.

Subtest 5 - Checks the ability of the card to interrupt. With the flag and control set and the interrupt system on, there should be an interrupt on the I/O channel. If not, error message EØ14 occurs. Checks that the interrupt occurred where expected. The interrupt should not occur before a string of priority affecting instructions are executed. The following instructions are used to check the hold off operation:

```
STC 1
STF 1
CLC 1
CLF 1
JMP *+1,I
DEF *+1
JSB *+1,I
DEF *+1
NOP
```

Error messages EØ12 and EØ15 will occur if this is not true. Checks that another interrupt doesn't occur when the interrupt system is turned back on. Error message EØ13 will occur if this is not true. Checks that no instruction was missed during the interrupt (EØ26 INT EXECUTION ERROR).

Subtest 6 - Checks that with the interrupt system on and the CH control and flag set, there is no interrupt following a CLC CH instruction. The following sequence of instructions are used.

```
STC CH
STF CH
STF Ø
CLC CH
```

If the CLC CH fails to inhibit an interrupt, error message EØ16 will occur.

Checks that the CLC Ø instruction inhibits interrupts when the CH control and flag are set. The following sequence of instructions is used.

```
CLF CH
STC CH
STF CH
STF Ø
CLC Ø
```

If the CLC Ø fails to inhibit an interrupt, error message EØ17 will occur.

Subtest 7 - Checks that the PRESET (EXTERNAL and INTERNAL if applicable) buttons on the front panel performs the following actions:

1. Sets I/O flag (EXTERNAL).
2. Clears control (EXTERNAL).
3. Turns off the interrupt system (INTERNAL).
4. Clears the I/O data lines (EXTERNAL).

4-3. DESCRIPTION OF 12920 MUX Data Tests

4-4. TEST 1 SEND/RECEIVE TEST

This test sends and receives an alternate 1's and Ø's pattern on the two ports specified during the configuration routine. The send and receive ports are

configured for six different BAUD rate (2400, 1200, 600, 300, 150 and 110) and the largest character size (nine data bits plus two stop bits). The test is then repeated with the complement data pattern. In each send and receive test the flag is checked for operation complete, and the port number is checked to see if the correct port has interrupted.

4-5. TEST 2 BREAK TEST

Sends and receives a non-zero test character on a port and checks the Break bit (bit 2) of the status word after each send and receive to see that it is set to zero.

Sends and receives a break character (all zeros) on a port; and checks the Break bit of the status word after each send and receive to see that it is set to one.

4-6. TEST 3 PARITY TEST

Sends and receives odd ASCII parity. Checks bit 15 (parity check bit) of the receive word for a one.

Sends and receives even ASCII parity. Check bit 15 (parity check bit) of the receive word for a zero.

4-7. TEST 4 DIAGNOSE TEST

Tests the ability to route send data to the auxiliary ports 16-20 when bit 11 (diagnose bit) of send parameter word is set to a one.

4-8. TEST 5 ECHO TEST

Receives a test character on each port with bit 12 (echo bit) of the receive parameter word set to a one. Tests the ability to echo character back on the corresponding send port.

4-9. TEST 6 SYNC TEST

Tests the ability to send an all mark (all ones) character when bit 11 (sync bit) of the output data word is a one.

4-10. TEST 7 CHARACTER LOST TEST

Tests the ability to detect the reception of two characters on a receive port without the computer responding, and to flag this condition by setting bit 1 of the status word to a one.

4-11. DESCRIPTION OF 12922 MUX CONTROL TESTS

4-12. TEST 1 ADDRESS REGISTER

Test (ART) - The address register test sends an address to the interface board then reads back the address for verification. This check is made for all 16 addresses. Also the address register is set to zero and then incremented through all 16 addresses by executing LIA instructions. After each LIA the address is verified.

4-13. TEST 2 COMMAND AND STATUS TEST

Test (CST) - This program sends command word to the command registers. The command register outputs are connected to the EIA line drivers. The test cable routes the signals to the EIA line receivers. The line receiver inputs are routed through the multiplexer into the IOBI bus. The input status is checked against the expected status.

4-14. TEST 3 COMMAND REGISTER ADDRESSING TEST

Test (CRAT) - This program checks for proper addressing to the command registers and checks for an address being mapped to more than one address at a time.

4-15. TEST 4 STATUS INTERRUPT TEST

Test (SIT) - This program tests the ability to set the flag when input status does not compare with the stored status.

4-16. TEST 5 SCAN TEST

Test (SCAN) - The program sets up a port with a control word such that an interrupt will occur when the address register reaches that port number minus one. The I/O flag is cleared and the interface board is set in the SCAN mode. The next ENF signal from the computer should increment the address register to the port where the interrupt will occur. This sets the flag and stops the address register from incrementing. The flag is checked for a one and the address is verified.

Table 4-1. Halt Code Summary

HALT	DIAGNOSTIC	MEANING
TESTS $\emptyset_8$ to 7_8		
1Ø2ØØØ-1Ø2Ø56	12920	Error (E) information (H) messages 00-56_8.
TESTS $\emptyset_8$ to 5_8		
1Ø2ØØØ-1Ø2Ø4Ø	12922	Error (E) information (H) messages 00-40_8.
CONTROL		
1Ø2Ø72		Port number input error.
1Ø2Ø73		Select code input error.
1Ø2Ø74		Select code input complete.
1Ø2Ø75		User selection request.
1Ø2Ø76		End of Test (A = Test number).
1Ø2Ø77		End of diagnostic run.
1Ø6Ø77		Trap cell halts in location 2-77_8.

NOTE: See Table 4-2 for complete explanation of individual halts.

Table 4-2. Error, Information Messages and Halts
for Data and Control Boards

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102072	START	None	The port numbers entered during the configuration are invalid. Set the correct values in the switch register and press RUN.
102073	Configuration	None	I/O select code entered at configuration invalid. Must be greater than 7_8. Re-enter a valid select code and press RUN.
102074	Configuration	None	Select code entered during configuration valid. Enter program option bits in switch register and press RUN.
102075	Test Control	None	Test selection request resulting from switch register bit 9 being set. Enter in A register the desired group of tests to be executed, clear bit 9 and press RUN.
102076	Test Control	None	End of test halt resulting from switch register bit 15 being set (A register has the test number). To continue press RUN.
102077 AREG=PASS COUNT	Test Control	PASS XXXXXX	Diagnostic run complete. Switch register options may be changed. To continue press RUN.
106077	Test Control	None	Halt stored in location $2\text{-}77_8$ to trap interrupts which may occur unexpectedly because of hardware malfunctions. M register contains the I/O slot which interrupted. Diagnostic may be partially destroyed if halt occurs. The program may have to be reloaded; the problem should be corrected before proceeding.
NONE	Test Control	ASYNC MULTIPLEXER DATA BOARD DIAGNOSTIC ASYNC MULTIPLEXER CONTROL BOARD DIAGNOSTIC	
NONE	Test Control	Test XX	Information message before error message (XX = test number). Message occurs only once within a test but is suppressed for any subsequent messages within the same test.

Table 4-2. Error, Information Messages and Halts for Data and Control Boards (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102000	Test Ø	E000 CLF Ø-SFC Ø ERROR	CLF/SFC Ø combination failed. CLF did not clear flags or SFC caused no skip with flags clear.
102001	Test Ø	E001 CLF Ø-SFS Ø ERROR	CLF/SFS Ø combination failed. CLF did not clear flags or SFS caused skip with flags clear.
102002	Test Ø	E002 STF Ø-SFC Ø ERROR	STF/SFC Ø combination failed. STF did not set flags or SFC caused skip with flags set.
102003	Test 0	E003 STF Ø-SFS Ø ERROR	STF/SFS Ø combination failed. STF did not set flags or SFS caused no skip with flags set.
102004	Test 0	E004 CLF Ø DID NOT INHIBIT INT	With card flag and control set, CLF Ø did not turn off interrupt system.
102005	Test 0	E005 CLF CH-SFC CH ERROR	CLF/SFC CH combination failed. CLF did not clear flag or SFC caused no skip with flag clear.
102006	Test 0	E006 CLF CH-SFS CH ERROR	CLF/SFS CH combination failed. CLF did not clear flag or SFS caused skip with flag clear.
102007	Test 0	E007 STF CH-SFC CH ERROR	STF/SFC CH combination failed. STF did not set flag or SFC caused skip with flag set.
102010	Test 0	E010 STF CH-SFS CH ERROR	STF/SFS CH combination failed. STF did not set flag or SFS caused no skip with flag set.
102011 AREG = XX_8	Test 0	E011 STF XX SET CARD FLAG	Select code screen test failed. XX = select code that caused that card flag to set.
102012	Test 0	E012 INT DURING HOLD OFF INSTR	Interrupt occurred during an I/O instruction or a JMP/JSB indirect instruction.
102013	Test 0	E013 SECOND INT OCCURRED	Card interrupt a second time after initial interrupt was processed.

Table 4-2. Error, Information Messages and Halts
for Data and Control Boards (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102014	Test 0	E014 NO INT	No interrupt occurred with card flag and control set and the interrupt system on.
102015	Test 0	E015 INT RTN ADDR ERROR	Interrupt did not occur at the correct location in memory.
102016	Test 0	E016 CLC CH ERROR	CLC CH did not clear card control with the interrupt system on.
102017	Test 0	E017 CLC 0 ERROR	CLC 0 did not clear control with the interrupt system on.
102020	Test 0	E020 PRESET (EXT) DID NOT SET FLAG	PRESET (EXT) did not set the card flag.
102021	Test 0	E021 PRESET (INT) DID NOT DISABLE INTS	PRESET (INT) did not disable the interrupt system.
102022	Test 0	E022 PRESET (EXT) DID NOT CLEAR CONTROL	PRESET (EXT) did not clear control.
102023	Test 0	E023 PRESET (EXT) DID NOT CLEAR I-O LINES	PRESET (EXT) did not clear I/O data lines.
102024	Test 0	H024 PRESS PRESET (EXT & INT),RUN	Press PRESET (External, Internal), RUN.
NONE	Test 0	H025 BI-O COMP	Basic I/O Tests completed.
102026	Test 0	E026 INT EXECUTION ERROR	Interrupt was not processed correctly.

Table 4-3. Messages and Error Halts for Data Board Diagnostic

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102030	SEND/REC	E030 SEND PORT XX DID NOT INTERRUPT	Send port XX did not cause an external interrupt within timeout period of 300 milliseconds. A-Register contains the value of XX.
102031	SEND/REC DIAG	E031 RECEIVE PORT XX DID NOT INTERRUPT	Receive port XX did not cause an external interrupt within time-out period of 300 milliseconds. A-Register contains the value of XX.
102032	SEND/REC	E032 SEND PORT NUMBER IS XX SHOULD BE YY	Data was sent out on a port different than the one intended. A-Register contains value XX and B-Register contains value YY.
102033	SEND/REC	E033 RECEIVE PORT NUMBER IS XX SHOULD BE YY	Data was received on a port different than the one intended. A-Register contains value XX and B-Register contains value YY.
102034	SEND/REC	E034 DATA RECEIVED ON PORT XX IS XXXX SHOULD BE YYYY	Data sent did not compare with data received. A-Register contains value XXXX and B-Register contains value YYYY.
106034	SEND/REC		Press RUN the A-Register will contain port number XX. Press RUN to continue.
102035	SEND/REC	E035 S-R BIT SHOULD BE SET	When data was transmitted the send/receive status bit indicated received data.
102036	SEND/REC	E036 S-R BIT SHOULD BE RESET	When data was received the send/receive status bit indicated send data.
102037	BREAK	E037 BREAK BIT SHOULD NOT BE SET	A non-zero character is followed by a null character. The status is obtained during the transmission of the null. This test verifies that the break condition is buffered.

Table 4-3. Messages and Error Halts for Data Board Diagnostic (Continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102040	BREAK	E040 BREAK BIT SHOULD NOT BE SET	A non-zero test character was sent but bit 2 of the status word was not set to a zero.
102041	BREAK	E041 BREAK BIT SHOULD BE SET	A zero test character was sent but bit 2 of status word was not set to a one.
102042	PARITY	E042 PARITY BIT SHOULD BE SET	Odd ASCII parity sent but bit 15 of received word was not set to a one.
102043	PARITY	E043 RAW PARITY BIT 7 ERROR	Odd ASCII parity sent. A check is made on bit 7 of the received data. This bit is generated in the parity generator of the send section and not modified by the receive position.
102044	PARITY	E044 PARITY BIT SET	Even ASCII parity sent but bit 15 of received word was not set to a zero.
102045	PARITY	E045 RAW PARITY BIT 7 ERROR	Even ASCII parity sent. Similar to E043 except for even parity.
102046	DIAGNOSE	E046 SEND DATA NOT ON AUXILIARY PORT XX	Bit 11 (diagnose) of send parameters was set but data was not routed to auxiliary port XX. A-Register contains value XX.
102047	DIAGNOSE	E047 RECEIVED DATA NOT ON AUXILIARY PORT XX	Bit 11 (diagnose) of received parameters was set but data received was not routed to auxiliary port XX. A-Register contains value XX.
102050	ECHO	E050 NO ECHO ON PORT XX	Bit 12 (echo) of receive parameters was set but data was not echoed back on port XX. A-Register contains value XX.
102051	SYNC	E051 SYNC TEST FAILED	Failed to send an all mark (all ones) character when sync bit was set to a one and all data bits were ones.

Table 4-3. Messages and Error Halts for Data Board Diagnostic (continued)

HALT CODE	PROGRAM SECTION	MESSAGE	COMMENTS
102052	SYNC	E052 SYNC TEST FAILED (PTY=1)	Failed to receive an all mark (all ones) character when sync bit was set to a one and data bits plus parity were ones.
102053	CHAR-LOST	E053 CHARACTER LOST FAILED	Bit 1 (character lost) of status word should be set to a one to indicate character-lost condition.
102054	ANY	E054 SEEK BIT IS A ONE SHOULD BE A ZERO	During a seek operation the seek bit (bit 15) failed to reset within time-out period of 300 milliseconds.
102055	ANY	E055 SEEK STAYED SET	After issuing a CLC Ø to clear the interface the SEEK remained a one for more than 100 ms.
102056	ANY	E056 SEEK FAILED TO SET AFTER CLC Ø	A CLC Ø instruction is given to clear the interface. The SEEK bit should go to a one then to a zero.

Table 4-4. Error Messages and Halts for Control Board Diagnostic

HALT CODE	SECTION	MESSAGE	COMMENTS
102027	Test 0	E027 PRESET DID NOT CLEAR STATUS ON PORT XX	The status register was not cleared on port XX after preset.
102030	Test 1	E030 THE PORT ADDRESS IS XX SHOULD BE YY	The program selected port YY but the board returned with port XX. The A-Register contains XX and B-Register contains YY.
102031	Test 1	E031 THE PORT ADDRESS IS XX SHOULD BE YY	The LIA instruction failed to increment the address register. The actual port XX did not compare with the expected port YY. The A-Register contains XX and B-Register contains YY.
102032 106032	Test 2 Test 2	E032 STATUS ON PORT XX IS XXXXXX SHOULD BE YYYYYY	The status on port XX didn't compare with the expected status. For non teleprinter option A-Register contains actual status XXXXXX. B-Register contains expected status YYYYYY. Press RUN the A-Register will contain port number XX. Press RUN to continue.
102033	Test 3	E033 OUTPUT ON PORT XX CHANGES PORT YY	An output was made to 15 ports (XX). After each output, port YY was tested to see if it was altered. B-Register contains XX. A-Register contains YY.
102034	Test 4	E034 STORED STATUS #1 FAILED TO INTERRUPT	A control word sets up stored status #1 to cause an interrupt and no interrupt occurred.
102035	Test 4	E035 STORED STATUS #2 FAILED TO INTERRUPT	A control word sets up stored status #2 to cause an interrupt and no interrupt occurred.
102036	Test 4	E036 I-O FLAG FAILS TO CLEAR. SIT ABORTED.	Cannot clear I/O flag. The Status Interrupt Test (SIT) was aborted.

Table 4-4. Error Messages and Halts for Control Board Diagnostics (continued)

HALT CODE	SECTION	MESSAGE	COMMENTS
102037	Test 5	E037 SCAN TEST FAILED	During an SCAN operation the I/O flag failed to set.
102040	Test 5	E040 SCAN TEST INTERRUPT OCCURRED ON PORT XX SHOULD BE PORT YY	An interrupt occurs during the SCAN operation the port number is XX should be YY. A-Register contain XX, B-Register contains YY.

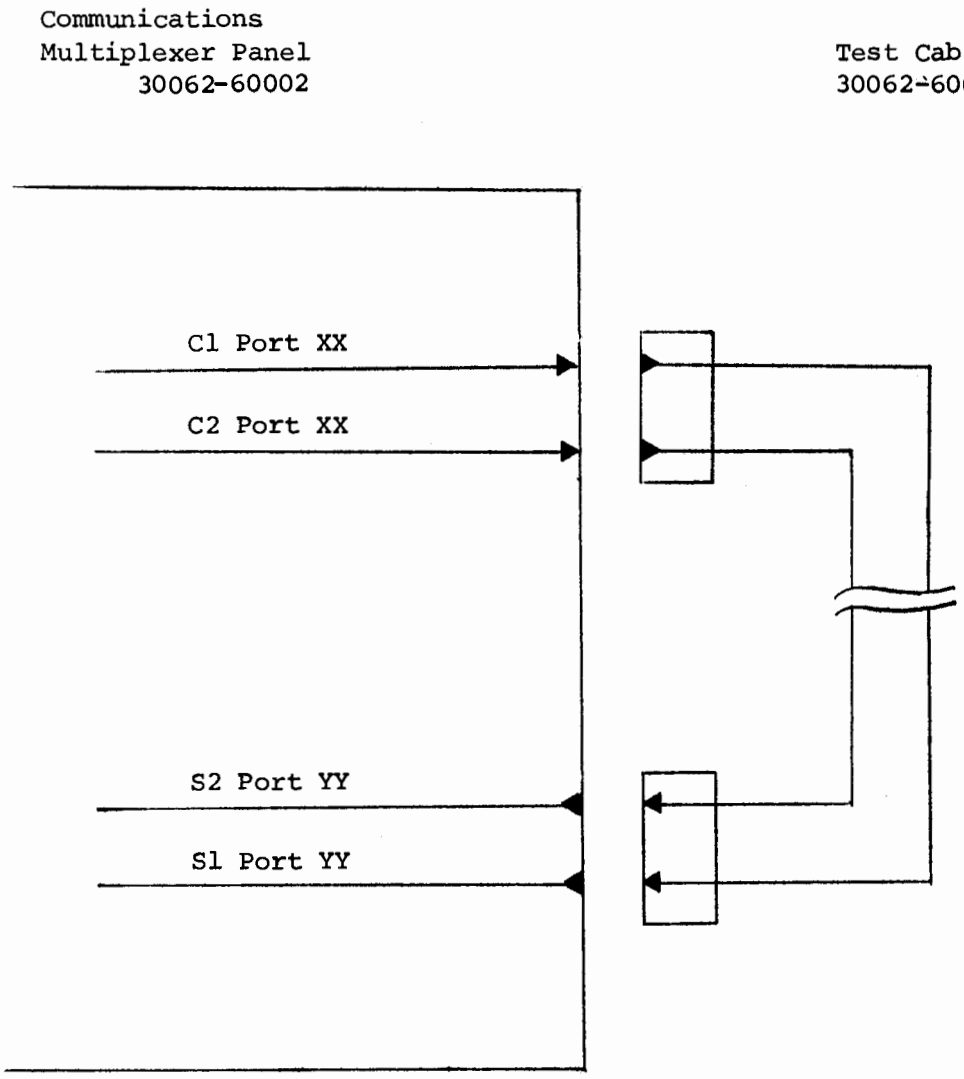


Figure 4-1. Test connector scheme for routine command (Cn) output and status (S_n) input signal lines.

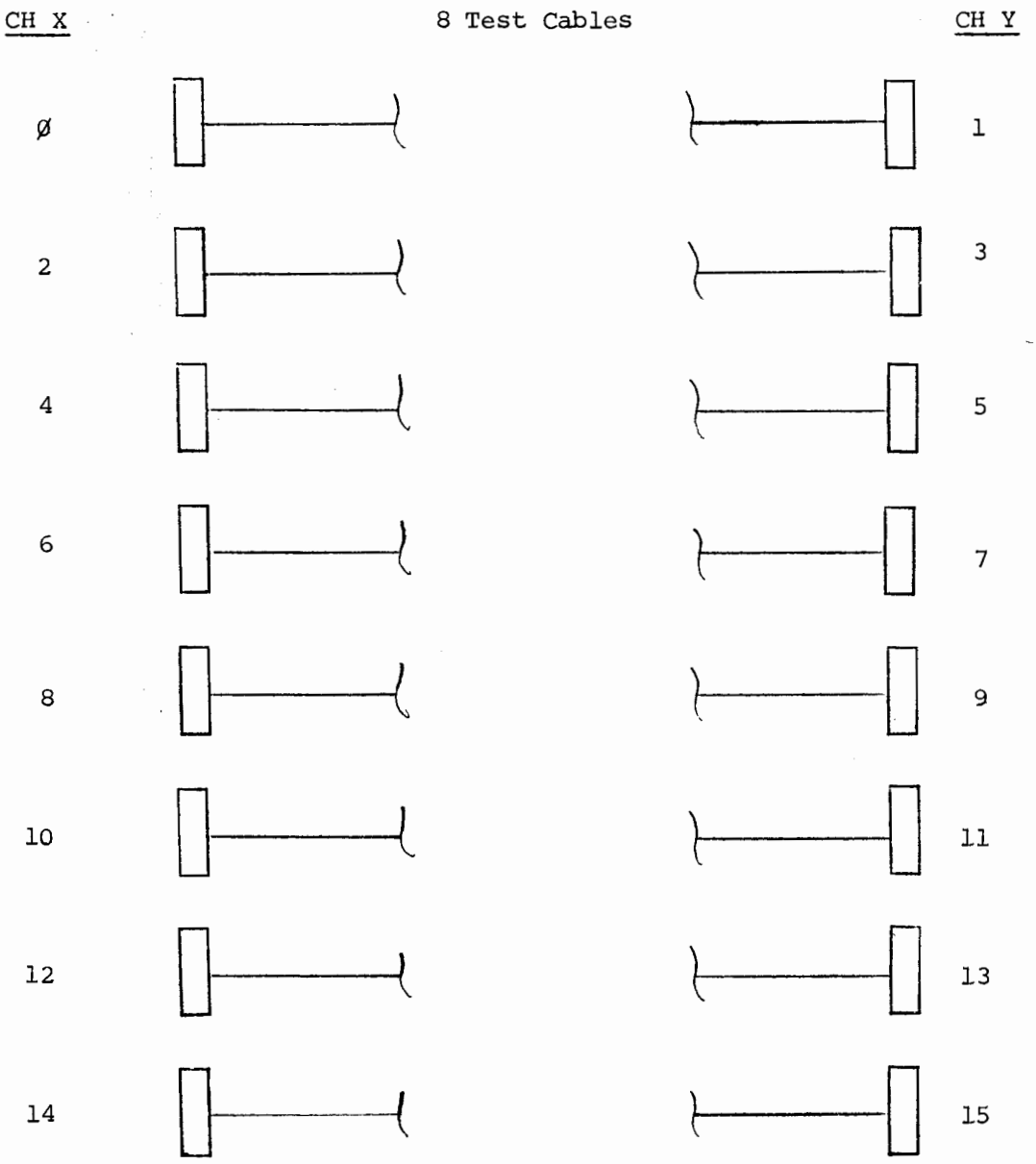


Figure 4-2. Test cables scheme for automatic mode.

NOTE: Only one test cable is furnished with the diagnostic. To run all 16 ports in sequential order the operator must obtain 7 additional test cables and connect them as shown. Bit10 must be set during the configuration.