HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12880A
12880A–001

KEYBOARD-DISPLAY TERMINAL INTERFACE KIT

(FOR 2100-SERIES COMPUTERS)

Card Assembly
12880-60001, Rev. 1017, 1411, and 1432

Note

This manual should be retained with the applicable computer documentation.

12880-90001

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LIST OF EFFECTIVE PAGES

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts information for the Hewlett-Packard 12880A Keyboard-Display Terminal Interface Kit. (See figure 1-1.)

1-3. GENERAL DESCRIPTION.

1-4. The standard HP 12880A Interface Kit provides the necessary equipment to interface the HP 2600A Keyboard-Display Terminal or the HP 2615A Terminal with an HP 2100-Series Computer. The kit contains the following items:

a. 12880-60001 Keyboard-Display Terminal Interface Card.
b. 12880-60003 Cable Assembly.
c. 12880-90001 Operating and Service Manual.

1-4A. The option 001 kit includes the items provided with the standard kit except 12880-60003 Cable Assembly is replaced by 02640-60058 Cable Assembly. The option 001 cable is designed to typically connect to certain terminals in the 2640 family of terminals.

1-5. The interface card contains control and interrupt logic for both input and output computer functions and a shift register for temporary storage of data between the computer and the terminals. Eight data bits are transferred in parallel between the interface card and the computer; an 11-bit word in American Standard Code for Information Interchange (ASCII) is transferred in serial between the interface card and the terminals. The interface card can provide automatic readback to the terminals without computer intervention. The cable assembly connects the interface card to the terminals.

1-6. CARD IDENTIFICATION.

1-7. Printed-circuit card revisions are identified by a letter, a date code, and a division code stamped on the card (e.g., A-1005-22). The letter code identifies the version of the etched trace pattern on the unloaded card. The date code (four middle digits) refers to the electrical characteristics of the loaded card. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the card. If the date code stamped on the printed-circuit card does not agree with the date code shown on the title page of this manual, there are differences between your card and the card described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-8. SPECIFICATIONS.

1-9. Specifications for the keyboard-display terminal interface kit are listed in table 1-1.

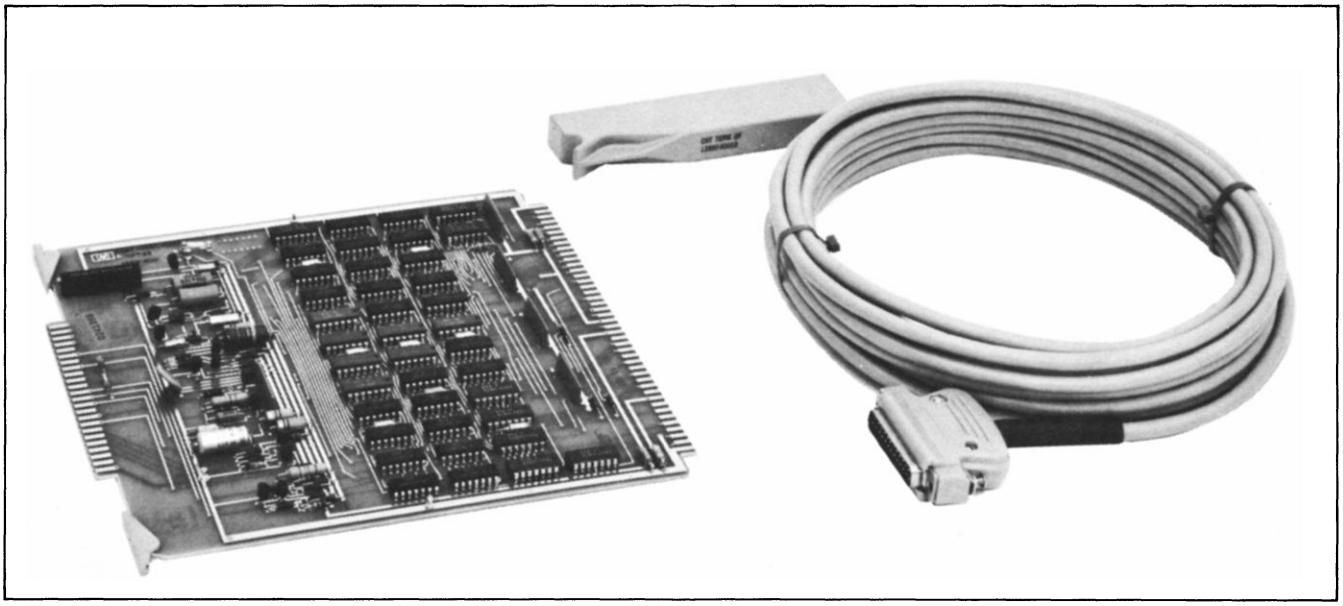

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Figure 1-1. HP 12880A Keyboard-Display Terminal Interface Kit

Table 1-1. Interface Kit Specifications

CURRENT REQUIRED FROM COMPUTER:		
+12-volt supply:	0.24 ampere	
+4.5-volt supply:	0.76 ampere	
-2-volt supply:	0.05 ampere	
-12-volt supply:	0.01 ampere	
DATA TRANSFER RATE:	10 to 960 characters per second (110 to 9600 baud). Actual value depends upon external clock input from terminals.	
EXTERNAL CLOCK FREQUENCY REQUIRED:	Eight times the selected baud rate to and from the terminals.	
TYPES OF CODES USED:	ASCII between interface card and terminals. HP Character Set between interface card and computer.	
LOGIC VOLTAGE LEVELS:	LOGIC 1	LOGIC 0
To and from terminals:	-3V dc to -12V dc	+3V dc to +12V dc
Signal condition:	Marking	Spacing
To and from computer:	+4.5V dc	0V dc

Note: Data transfer via the direct memory access (DMA) option is not recommended with the HP 12880A Keyboard Display Terminal Interface Kit when used in conjunction with the HP 2100 series computers. The results of such data transfers are unspecified.

SECTION II
INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, reshipment, and programming for the HP 12880A Keyboard-Display Terminal Interface Kit.

Note: Data transfer via the direct memory access (DMA) option is not recommended with the HP 12880A Keyboard Display Terminal Interface Kit when used in conjunction with the HP 2100 series computers. The results of such data transfers are unspecified.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping container is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit contents for damage (cracks in circuit card, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. JUMPER WIRE W1.

2-7. The interface card is shipped with jumper wire W1 in position B to allow the terminal to provide an external clock that controls the data transfer rate. Inspect the card and verify that the jumper wire is in the correct position. See the parts location view in figure 4-1 to determine the physical location of the jumper.

2-8. CARD INSTALLATION.

2-9. Install the interface card and cable assembly as follows:

a. Determine if the computer power supplies will provide the additional current required for operation of the interface card. Refer to the Hewlett-Packard computer documentation for a listing of current available from the computer power supplies.

b. Turn off computer and terminal power.

CAUTION

Make certain that power is off at the computer before installing the interface kit, or damage to the interface card or the computer may result.

c. Open computer for access to I/O card slots.

d. Plug interface card into I/O slot assigned for the particular computer system. Make certain that all higher priority slots have either another I/O card or a priority jumper card installed.

e. Pass interface card connector of the cable assembly through opening at rear of computer. Slide connector onto interface card and close computer.

f. Connect other end of cable assembly to mating connector on terminal.

g. Run diagnostic test to verify that the interface card is functioning properly. See paragraph 4-6.

2-10. RESHIPMENT.

2-11. If an item of the interface kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-12. Package the item in the original factory packaging material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-13. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 Cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J. and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Note

In any correspondence, identify the interface kit by model number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-14. PROGRAMMING.

2-15. The following paragraphs provide information for programming the interface card and the terminals. This information consists of the HP 2600A terminal characteristics, status and timing considerations, and a sample assembly language program. Additional programming information is available in the HP 2615A Terminal Operating and Service Manual, part no. 02615-90004, the HP 2640A Terminal Owner's Manual, part no. 02640-90011, and in software manuals supplied with the computer. It should be noted that the ASCII character sets for the terminals are not completely compatible.

2-16. HP 2600A TERMINAL CHARACTERISTICS.

2-17. The terminal contains a keyboard, cathode-ray tube display, character generator, memory, and interface components. Keyboard operation is similar to operation of a teleprinter keyboard in that characters are generated by typing. Generated characters are either of two types: graphic characters that are displayed on the CRT screen, or control characters that cause some action to occur such as positioning of the displayed characters. When any character is generated, a signal representing an equivalent ASCII character is generated at the same time. By programming, these generated signals are sent through the interface card to computer memory. The computer also outputs ASCII character signals through the interface card for display by the terminal. Data bits that make up each ASCII character are transferred serially between the terminal and the interface card data register and in parallel between the data register and computer memory. Figure 2-1 shows the ASCII character set used by the terminal.

BIT NUMBER 4	3	2	1	7	6	5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0	0	0	0						SP	0	@	P		
0	0	0	1					X on	!	1	A	Q		
0	0	1	0						"	2	B	R		
0	0	1	1					X off	#	3	C	S		
0	1	0	0						$	4	D	T		
0	1	0	1				WRU		%	5	E	U		
0	1	1	0				F^{cs}		&	6	F	V		
0	1	1	1				BELL		'	7	G	W		
1	0	0	0					c →	(	8	H	X		
1	0	0	1					c ←	)	9	I	Y		
1	0	1	0				LINE FEED	c ↑	*	:	J	Z		
1	0	1	1				c ↓	ESC	+	;	K	[		
1	1	0	0					HOME DOWN	,	<	L	\		
1	1	0	1				RE-TURN	HOME UP	-	=	M	]		
1	1	1	0				SPOW LATCH	ERASE EOL	.	>	N	↑		
1	1	1	1				SPOW UN-LATCH	ERASE EOF	/	?	O	←		RUB OUT

NOTE: C = CURSOR

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Figure 2-1. HP 2600A Terminal ASCII Character Set

2-18. HP 2600A SPECIAL CONSIDERATIONS.

2-19. The data transmission and receiving rate, as expressed in bits per second, is selectable through a BAUD RATE switch at the rear of the terminal. Because the time required to execute commands is sometimes greater than the data transfer rate, it is necessary to compensate for the command delays through programming. Most special programming considerations are concerned with the cursor. The cursor indicates the next character position on the CRT screen by flashing at the indicated position. To move the cursor requires a displayed character, which automatically moves the cursor to the next position, or a cursor direction arrow command. The cursor is also moved by erase EOF, erase EOL, home up, and home down commands. Special programming information required to ensure proper execution of cursor commands is provided in the following paragraphs.

a. The cursor direction arrow command moves the cursor one increment in the direction of the arrow: either up, down, right, or left. These cursor direction arrow commands are given at any time. However, special filler characters must be given with the cursor command to provide a total filler and cursor character time of 16.67 milliseconds. Filler characters are non-functioning control characters such as control-shift with the "F" character. (See figure 2-1 for the ASCII equivalent of F^{cs}.) The number of filler characters required depends on the BAUD RATE switch position as follows: no fillers required for positions 110 through 600; one filler required for position 880; two fillers required for positions 1200 and 1760; and three fillers required for position 2400.

b. The erase EOF and erase EOL commands clear portions of the CRT screen. Erase EOF clears from the cursor position to the end of the frame while erase EOL clears from the cursor position to the end of the line. To properly execute these commands, the commands should be sent in multiples that provide a total time of 16.67 milliseconds for either command. The number of commands required therefore depends on the BAUD RATE switch position as follows: one command for positions 110 through 600; two commands for positions 880 and 1200; three commands for position 1700; and four commands for position 2400.

c. The home up and home down commands move the cursor to the top left and bottom left, respectively, on the CRT screen. Home up commands have no restriction and work at any data transfer rate. Home down commands, however; cannot be used at BAUD RATE switch positions above 300 because of logic restrictions. To reach the home down position at faster data transfer rates, program a home up command followed by 25 down cursor direction arrow commands.

d. The terminal provides an automatic carriage return and line feed after 72 characters are displayed on any line. If a carriage return and line feed is also programmed after 72 characters, a double space will occur between lines of the display.

e. Line feed commands are also restricted at BAUD RATE switch positions above 600 when the cursor is at the home down (bottom line) position. If the line feed command is then followed by a different command or a

printing character, the terminal speed buffer falls behind. The first two sequences (a sequence is one line feed command followed by any different command or a character) are not restricted. However, before programming the third successive sequence, four filler characters must be programmed to prevent data from being lost. This restriction does not apply when any number of line feed commands are programmed successively without intermixing other commands or characters.

2-20. HP 2615A TERMINAL CHARACTERISTICS AND SPECIAL CONSIDERATIONS.

2-21. Characteristics and programming information for the HP 2615A Terminal are contained in the HP 2615A Terminal Operating and Service Manual, part no. 02615-90004. It should be noted that the HP 2615A Terminal ASCII character set differs from the HP 2600A Terminal ASCII character set.

2-21A. HP 2640A TERMINAL CHARACTERISTICS AND SPECIAL CONSIDERATIONS.

2-21B. Characteristics and programming information for the HP 2640A Terminal are contained in the Owner's Manual, part no. 02640-90011. It should be noted that the HP 2640A Terminal ASCII character set differs from the HP 2600A Terminal ASCII character set.

2-22. STATUS CHECK.

2-23. A method for checking status is shown in table 2-1. These program steps check bit 15 to determine if the terminal is transferring a character to the computer. Bit 15 is set true by the first input bit to the interface card and remains true until the tenth input bit. This allows time for the full character to be transferred before bit 15 is set to logic 0. Bit 15 remains set to logic 0 when the computer is transferring data to the interface card.

Table 2-1. Status Check

OPCODE	OPERAND	REMARKS
LIA	CRT	Put buffered data into A-register
SSA		Busy?
JMP	*-2	Yes, jump back two instructions.
---		No, program continuation.

2-24. TIMING.

2-25. The terminal operation is synchronized by a clock signal provided by the terminal. This clock signal is always available when the terminal is turned-on and is connected to a pulse counter (divider) on the interface card. During input operations the counter starts counting clock pulses when the first input bit is received from the terminal. For output operations, the counter starts counting clock pulses when an STC instruction is issued. In either case, the counter provides one bit count output for every eighth clock pulse and one character count output for every tenth bit count output. As each bit count occurs, the data register is clocked so that the ASCII character bits are serially transferred either in or out of the data register. On the tenth bit count the character count output clears the counter to inhibit further counting and also signals the computer by setting the Flag FF. Setting the Flag FF provides either an Interrupt Request or Skip Flag signal, depending on the method of data transfer, which indicates that the serial data transfer is complete.

2-26. Computer input and output operations are controlled by program control words and the STC instruction. The program control words are listed in table 2-2 along with other program constants that are useful in programming the terminal. Timing diagrams for input and output operations are provided in figures 3-3 and 3-4, respectively and flow diagrams showing the sequence of input and output operations are provided in figures 3-6 and 3-7, respectively.

2-27. ASSEMBLY LANGUAGE PROGRAM.

2-28. Table 2-3 provides an assembly language program that indicates the operations and instructions required to transfer data between the terminals and the computer. Computer input and output operations are both shown. This program, when assembled on an object tape, transfers data to and from the terminals using the noninterrupt (skip-if-flag-set) method of data transfer. The interrupt method of data transfer can also be used; however, the program is more complex because of subroutine requirements.

Table 2-2. Program Control Words

LABEL	OPCODE	OPERAND	REMARKS
TERM	EQU	nn	Where nn is the select code.
DOPR	OCT	120000	Data out (computer to terminal).
DINP	OCT	140000	Data in (terminal to computer).
DINPR	OCT	160000	Data in (with return to terminal for display).
CHAR1	OCT	000000	Temporary data.
CHAR2	OCT	000000	Storage locations.

Table 2-3. Assembly Language Program

```
0001                    ASMB,A,L,B,T
0002*  SAMPLE PROGRAM FOR HP2600A KEYBOARD DISPLAY
0003*  TERMINAL
0004*
0005  01000                 ORG 1000B
0006  01000 102511          LIA TRM         CHECK TERMINAL BUSY STATUS B15
0007  01001 002020          SSA              REMAIN IN WAIT CHECK UNTIL
0008  01002 025000          JMP *-2           B15=0
0009*
0010  01003 061077          LDA DOUT        SEND OUTPUT CONTROL WORD
0011  01004 102611          OTA TRM          TO TERMINAL
0012  01005 061132  TRM02 LDA HU           MOVE CURSOR TO TOP OF DISPLAY
0013  01006 015051          JSB CHOUT        SO SCREEN CAN BE CLEARED WHEN
0014  01007 061104          LDA M4           THE ERASE EOF CHARACTER IS
0015  01010 065127          LDB EEOFA         SENT TO TERMINAL. SEND 4-EEOF
0016  01011 015032           JSB OUT           CHARACTERS FOR 2400 BAUD
0017  01012 061106          LDA M22         CALLING SEQUENCE FOR
0018  01013 065107          LDB MSG1A        MESSAGE OUTPUT TO DISPLAY
0019  01014 015032          JSB OUT          'INPUT PRINT CHARACTER DESIRED
0020  01015 015057          JSB CHIN        INPUT KEYBOARD CHARACTER
0021  01016 061103          LDA LF          OUTPUT LINE-FEED
0022  01017 015051          JSB CHOUT        AND
0023  01020 061102          LDA CR           CURSOR RETURN
0024  01021 015051          JSB CHOUT         TO DISPLAY
0025*
0026*    OUTPUT 21 CHARACTERS DIAGIONALLY ACROSS THE
0027*    SCREEN AS INPUT FROM THE KEYBOARD
0028  01022 061106          LDA M22         INITIALIZE COUNTER TO REPEAT
0029  01023 071135          STA RPT          INPUT CHARACTER 22-TIMES
0030  01024 061105  TRM01 LDA M6           PREPARE CALLING SEQUENCE TO
0031  01025 065123          LDB MSG2A        OUTPUT CHARACTER AND CURSOR
0032  01026 015032          JSB OUT         CONTROLS AT 2400 BAUD
0033  01027 035135          ISZ RPT
0034  01030 025024          JMP TRM01
0035  01031 025005          JMP TRM02       REPEAT PROGRAM SEQUENCE
0036*
0037*    SUBROUTINE TO OUTPUT MESSAGE
0038  01032 000000  OUT   NOP
0039  01033 071134          STA CHCT        SAVE OUTPUT CHARACTER COUNT
0040  01034 075133          STB BUFF        SAVE MESSAGE BUFFER ADDRESS
0041  01035 065100          LDB ULFL        UPPER/LOWER FLAG
0042  01036 161133  OUT01 LDA BUFF,I      GET WORD CONTAINING CHARACTER
0043  01037 006021          SSB,RSS         IF UPPER/LOWER FLAG SAYS UPPER
0044  01040 001727          ALF,ALF          (SIGN=0) ROTATE TO LOWER
0045  01041 011101          AND M377        REMOVE UPPER CHARACTER
0046  01042 015051          JSB CHOUT       OUTPUT CHARACTER IN A(07-00)
0047  01043 006020          SSB             IF CHARACTER OUTPUT WAS LOWER
0048  01044 035133          ISZ BUFF         CHARACTER ADD 1 TO BUFF ADDRESS
0049  01045 005200          RBL             SET UPPER/LOWER FLAG;NEXT CHAR
0050  01046 035134          ISZ CHCT        INDEX CHARACTER COUNTER
0051  01047 025036          JMP OUT01       NOT ZERO; MORE TO OUTPUT
0052  01050 125032          JMP OUT,I       RETURN
0053*
0054*    SUBROUTINE TO OUTPUT CHARACTER
0055  01051 000000  CHOUT NOP
0056  01052 102611          OTA TRM         OUTPUT CHARACTER TO I/O BUFFER
0057  01053 103711          STC TRM,C       SEND ENCODE AND CLEAR FLAG
0058  01054 102311          SFS TRM         WAIT UNTIL TERMINAL
0059  01055 025054          JMP *-1          ACCEPTS CHARACTER
0060  01056 125051          JMP CHOUT,I     RETURN
```

Table 2-3. Assembly Language Program (Continued)

```
0061*
0062*   SUBROUTINE TO INPUT CHARACTER FROM TERMINAL
0063  01057 000000  CHIN  NOP
0064  01060 061076        LDA DIN        SEND INPUT CONTROL WORD
0065  01061 102611        OTA TRM         TO TERMINAL
0066  01062 103711        STC TRM,C      SEND ENCODE TO TERMINAL
0067  01063 102311        SFS TRM        WAIT FOR CHARACTER TO BE INPUT
0068  01064 025063        JMP *-1         FROM KEYBOARD
0069  01065 106511        LIB TRM        GET CHARACTER FROM BUFFER AND
0070  01066 005727        BLF,BLF         PREPARE FOR MESSAGE INSERTION
0071  01067 061077        LDA DOUT       SEND  OUTPUT CONTROL WORD
0072  01070 102611        OTA TRM         TO TERMINAL
0073  01071 061124        LDA MSG2       INSERT
0074  01072 011101        AND M377        INPUT
0075  01073 030001        IOR B            CHARACTER INTO
0076  01074 071124        STA MSG2           MESSAGE
0077  01075 125057        JMP CHIN,I     RETURN
0078*
0079*   DATA
0080  00011         TRM   EQU 11B
0081  00001         B     EQU 1
0082  01076 160000  DIN   OCT 160000
0083  01077 120000  DOUT  OCT 120000
0084  01100 052525  ULFL  OCT 52525
0085  01101 000377  M377  OCT 377
0086  01102 000015  CR    OCT 15
0087  01103 000012  LF    OCT 12
0088  01104 177774  M4    DEC -4
0089  01105 177772  M6    DEC -6
0090  01106 177752  M22   DEC -22
0091  01107 001110  MSG1A DEF MSG1
0092  01110 044516  MSG1  ASC 11,INPUT PRINT CHARACTER
      01111 050125
      01112 052040
      01113 050122
      01114 044516
      01115 052040
      01116 041510
      01117 040522
      01120 040503
      01121 052105
      01122 051040
0093  01123 001124  MSG2A DEF MSG2
0094  01124 000006  MSG2  OCT 12,3006,14013
      01125 003006
      01126 014013
0095  01127 001130  EEOFA DEF EEOF
0096  01130 017437  EEOF  OCT 15510,15512,15512
      01131 017437
0097  01132 000035  HU    OCT 35
0098  01133 000000  BUFF  BSS 1
0099  01134 000000  CHCT  BSS 1
0100  01135 000000  RPT   BSS 1
0101                      END
**  NO ERRORS*
```

SECTION III
THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief functional description of the interface card followed by a detailed circuit description. As an aid in following the discussions given in the paragraphs below, refer to the interface card flow diagrams in figures 3-5 through 3-7 and the logic diagram in figure 4-1.

3-3. FUNCTIONAL DESCRIPTION.

3-4. DATA CODES.

3-5. American Standard Code for Information Interchange (ASCII) is the data code generated by the terminal. Character transfer between the interface card and the terminal is in ASCII (11-bit serial) format. Character transfer between the interface card and the computer is in HP Character Set (least significant 8 bits parallel) format. Only seven bits are used in the HP Character Set. Whether bit 8 is a logic 1 or 0 during input operations, depends on the parity functions of the terminal being used. Programming masks bit 8 before placing the data in memory; therefore, the logic level of bit 8 is immaterial. During output operations, standard HP software furnished with the computer automatically sets bit 8 to a logic 1.

3-6. CHARACTER LENGTH.

3-7. For each character transferred between the interface card and the terminal, either 10 or 11 bits of information are required. The interface card transfers 11 bits serially to the terminal and receives either 10 or 11 bits serially depending upon the bit transfer rate of the terminal. (Refer to the terminal manual for transfer rates and number of bits.) Since the bits are transferred one at a time, the basic data unit is a bit. Figure 3-1 shows a simplified block diagram of data transfer. Of the 10 or 11 bits, one is a start bit, eight are character bits, and one or two are stop bits. If the terminal transfers 11 bits per character, the interface card ignores the second stop bit (bit 10). The 11-bit format for transfer of the letter M is shown in figure 3-2.

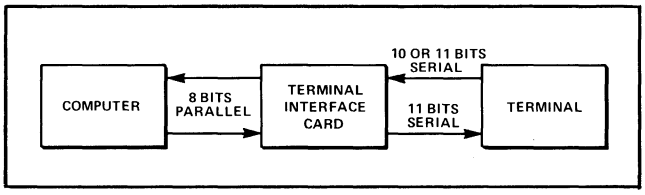

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Figure 3-1. Data Transfer, Simplified Block Diagram

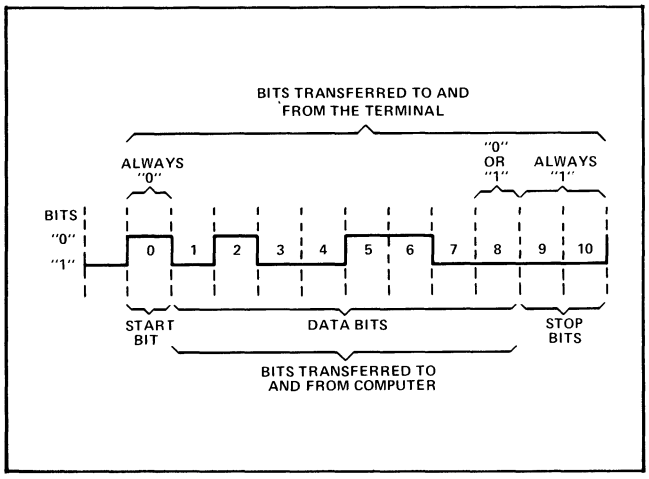

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Figure 3-2. Data Bits for Transfer of the Letter "M"

3-8. BASIC CIRCUITS OF THE INTERFACE CARD.

3-9. The interface card contains standard flag and interrupt logic circuits, control-word decoding circuits, data register, clock divider circuits, and level converter circuits. The standard flag and interrupt logic circuits permit operation under the skip-flag method or the interrupt method. The control-word decoding circuits prepare the card for an input or output operation. The data register provides serial-to-parallel and parallel-to-serial conversion of data for transfer between the terminal and the computer. The clock divider circuits divide the external clock signal from the terminal to provide the proper clock rate for the data register. The clock divider circuit also counts the bits during data transfer to and from the terminal to determine when the last bit of a character is transferred. The level converter circuits are in the data lines to and from the terminal to provide conversion between the signal levels used by the terminal and the signal levels used by the computer.

3-10. DETAILED CIRCUIT DESCRIPTION.

3-11. POWER ON.

3-12. When computer power is initially turned on, the POPIO and CRS signals are applied simultaneously to the interface card to establish initial conditions on the card. (See figure 3-5.) The POPIO signal sets the Flag Buffer FF, which in turn sets the Flag FF at time T2 (ENF true). The CRS signal clears the Control FF, Clock Enable FF, and the Read FF; direct sets the In/Out FF; and direct clears the Print FF, Punch FF, and Divider FFs.

3-13. The true clear-side outputs from the Print and Punch FFs hold transistor Q4 off, which in turn holds Q9 off. (The output of Q4 is coupled to the input of Q9 by jumper wires in the interconnecting cable.) This ensures that the output data line to the terminal is held in a mark condition (about -12 volts) while an input or output operation is not being performed.

3-14. The false set-side output of the Clock Enable FF direct clears FF U85A and direct sets FF U85B of the Data Register. The false clear-side output of FF U85B ensures that the output data line is held in the mark condition until the Data Register is clocked during an output operation. The false set-side output from FF U85A provides the start bit (space condition) when the Data Register receives the first clock pulse during an output operation.

3-15. The input data line from the terminal is maintained in a mark condition when data is not present on the line. This provides a logic 1 at the set input to FF U124B of the Data Register.

3-16. INPUT OPERATIONS.

3-17. To prepare the interface card for an input operation, control word bits 14 and 15 (both true) are transferred by an OTA/B instruction to the interface card. (See figure 3-6.) The LSCM, LSCL, and IOG(B) signals are "anded" to enable the instruction logic gates starting at time T3. The IOO signal, resulting from the OTA/B instruction, is "anded" with T3 to direct clear Data Register FFs U95B through U125A and to direct set FF U124B of the Data Register.

3-18. Control word bit 15 is "anded" with the IOO signal to clock the In/Out FF, Print FF, and Punch FF at time T5. The In/Out FF is set by control word bit 14. The true In signal from the In/Out FF performs the following functions:

a. Enables gate U94C to clock the Data Register FFs when the set-side output of the C FF of the Divider is true.

b. Enables gate U34A to set the Clock Enable FF when the first bit is received from the terminal.

c. Enables gate U24B to pass the input data through transistors Q4 and Q9 to the terminal for display when either the Print FF or the Punch FF is set by the control word.

3-19. Next, an STC,C instruction is issued from the computer program. The STC signal sets the Control FF to allow the interface card to cause an interrupt if the interrupt system is on. The CLF signal clears the Flag Buffer and Flag FFs. The true clear-side output of the Flag FF is applied to the skip flag logic and to gate U104C to enable the data bits to enter the data register.

3-20. Data bits from the terminal are applied through Q8 to the Schmitt trigger circuit (Q1,Q2). (Jumper wires in the interconnecting cable connect the output from Q8 to the Schmitt trigger circuit.) Transistor Q8 converts the positive and negative voltage levels of the true and false signals from the terminal to +12 volts and ground, respectively. The Schmitt trigger circuit shapes the leading edges of the data bits. Transistor Q3 converts the logic levels of the data bits to +4.5 volts (true) and ground (false).

3-21. The first data bit (bit 0), always false, is inverted and "anded" with the In signal to set the Clock Enable FF. The set-side output of the Clock Enable FF enables the External Clock signal from the terminal to enter the Divider FFs. The External Clock signal is divided by eight when the set-side output of the C FF becomes true. This matches the bit transfer rate of the terminal. Each time the C FF set-side output becomes true, it is "anded" with the In signal to clock the Data Register FFs. (See figure 3-3.)

3-22. After the 10 input data bits have been clocked into the data register, the divide-by-11 portion of the Divider FFs has counted to 10, which direct clears the Counter Reset FF at time T3. At time T5 (SIR true) the Divider FFs are direct cleared and the Flag Buffer FF is set. Also, the Clock Enable FF is cleared which prevents the External Clock signal from entering the Divider FFs. At time T2 of the following machine cycle, the Flag FF is set by the true ENF signal.

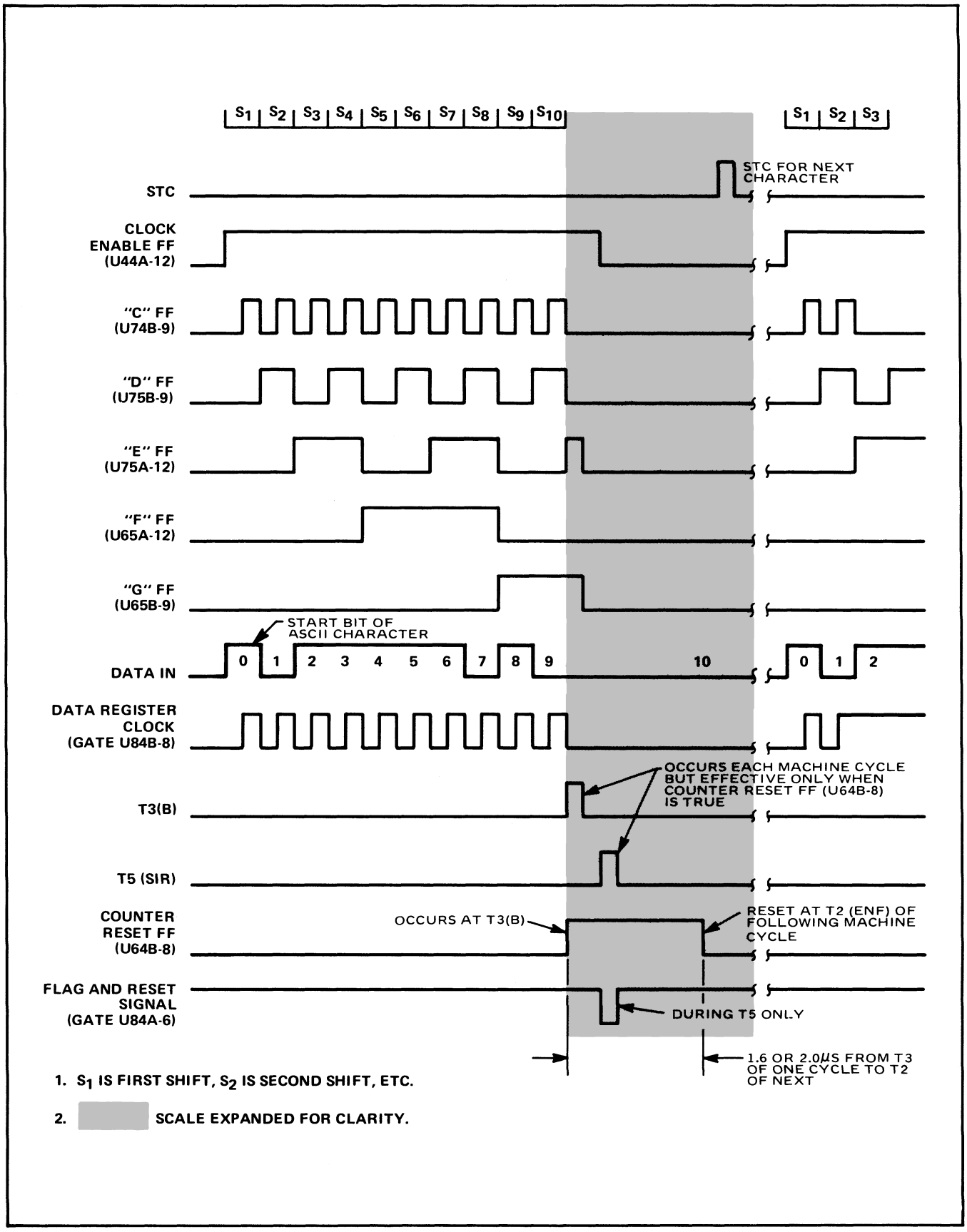
3-23. If the skip-flag method for determining data availability is used, the true set-side output of the Flag FF is "anded" with the SFS signal to generate the SKF signal.

3-24. If the interrupt method is used, the true set-side output of the Flag FF is "anded" with IEN, the Control FF set-side output, PRH, SIR, and the Flag Buffer FF set-side output signals to set the IRQ FF at time T5. The IRQ FF set-side output generates the FLGL and IRQL signals to cause an interrupt on the next available machine cycle.

3-25. During the fetch phase immediately following the interrupt phase, IAK becomes true and is "anded" with the IRQ FF set-side output to clear the Flag Buffer FF.

3-26. Data is input to the computer by an LIA/B instruction to the interface card select code. The resulting IOI signal strobes the data bits from the Data Register onto the IOBI lines.

3-27. If either the Print FF or the Punch FF was set by the control word during an input operation, the serial data from gate U104A is transferred to the terminal through gate U24B, Q4, and Q9. (Jumper wires in the interconnecting cable connect the output of Q4 to the input of Q9.)



2110-3A

Figure 3-3. Input Operation, Timing Diagram

3-28. OUTPUT OPERATIONS.

3-29. To prepare the interface card for an output operation, control word bits 13 and 15 must be true and bit 14 must be false. (See figure 3-7.) The control word bits are transferred to the card by an OTA/B instruction to the interface card. The LSCM, LSCL, and IOG(B) signals are "anded" to enable the instruction logic gates starting at time T3. The IOO signal, resulting from the OTA/B instruction, is "anded" with T3 to direct clear the Data Register FFs, and to direct set FF U124B of the Data Register.

3-30. Control word bit 15 is "anded" with the IOO signal to clock the In/Out FF, Print FF, and Punch FF at time T5. The In/Out FF is cleared by the false control word bit 14. The true Out signal of the In/Out FF performs the following:

a. Enables the Clock Enable FF to be set when an STC instruction is issued by the computer program.

b. Enables the Data Register to be clocked when the clear-side output from the C FF of the Divider is true.

c. Enables gate U24C at the output of the Data Register, along with the set state of the Print FF, to transfer the data bits to the terminal.

d. Allows the Divider FFs and the Clock Enable FF to be cleared and the Flag Buffer FF to be set when the divide-by-11 portion of the Divider reaches a count of 11.

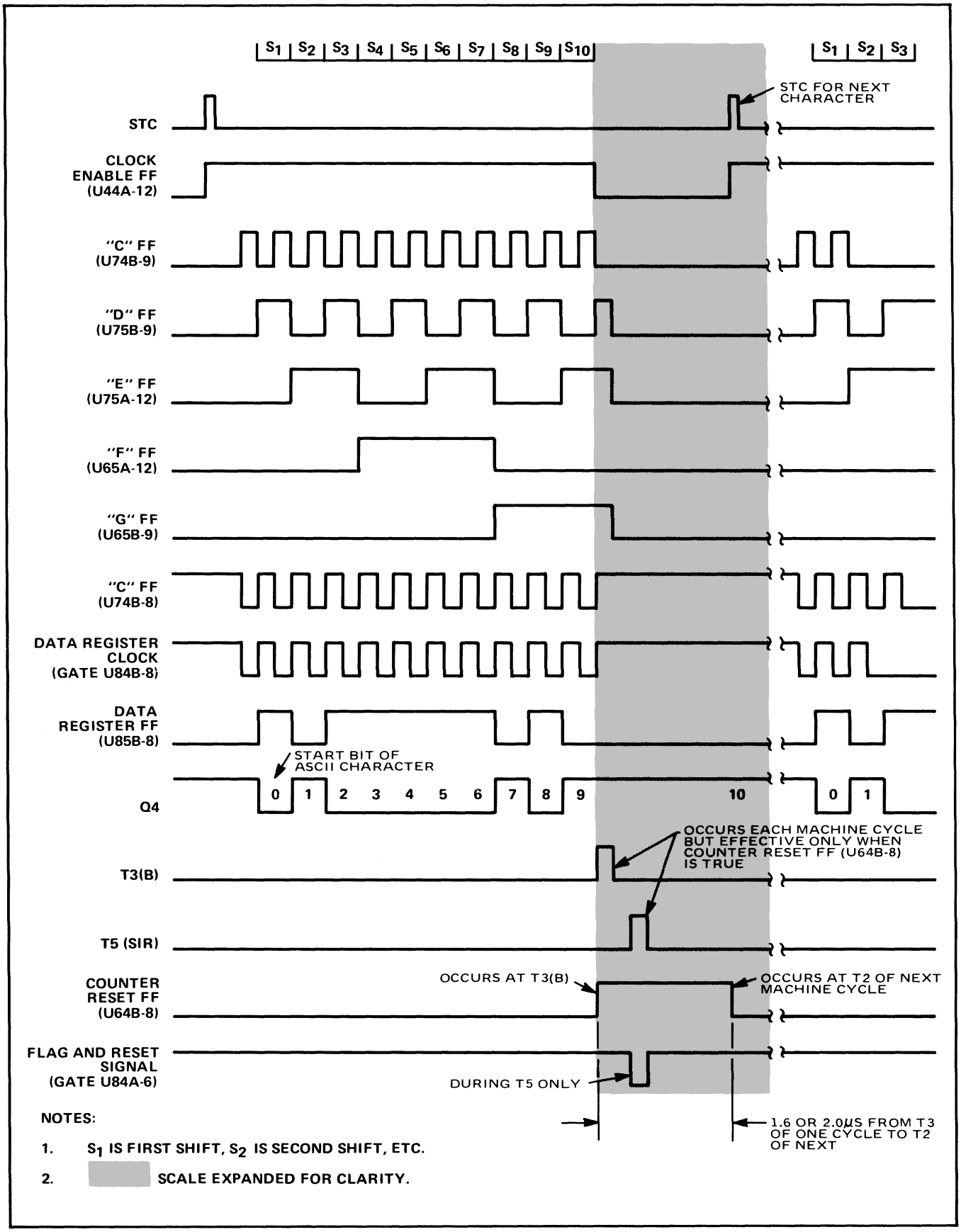
3-31. Next, an OTA/B instruction is issued to the interface card by the computer program to output the eight data bits to the Data Register. The resulting IOO signal enables the true IOBO bits to direct set the corresponding Data Register FFs at time T4.

3-32. An STC,C instruction to the interface card is issued by the computer program to set the Control FF and the Clock Enable FF. The true set-side output of the Control FF allows an interrupt, if the interrupt system is enabled (IEN signal true), after the data bits have been transferred to the terminal. The true set-side output of the Clock Enable FF allows the External Clock signal to enter the Divider circuit.

3-33. Each time the clear-side output of the C FF of the Divider goes true, the Data Register FFs are clocked. (See figure 3-4.) The clocking continues until all the inputs to gate U66B are true. At this point, the Data Register has been clocked 11 times. The Counter Reset FF is direct cleared at time T3 and stays cleared until the end of T2 on the following machine cycle. At time T5 the Divider FFs are direct cleared, the Clock Enable FF is cleared, and the Flag Buffer FF is set. This provides the necessary conditions for operation under the skip-flag method or the interrupt method, as discussed previously.

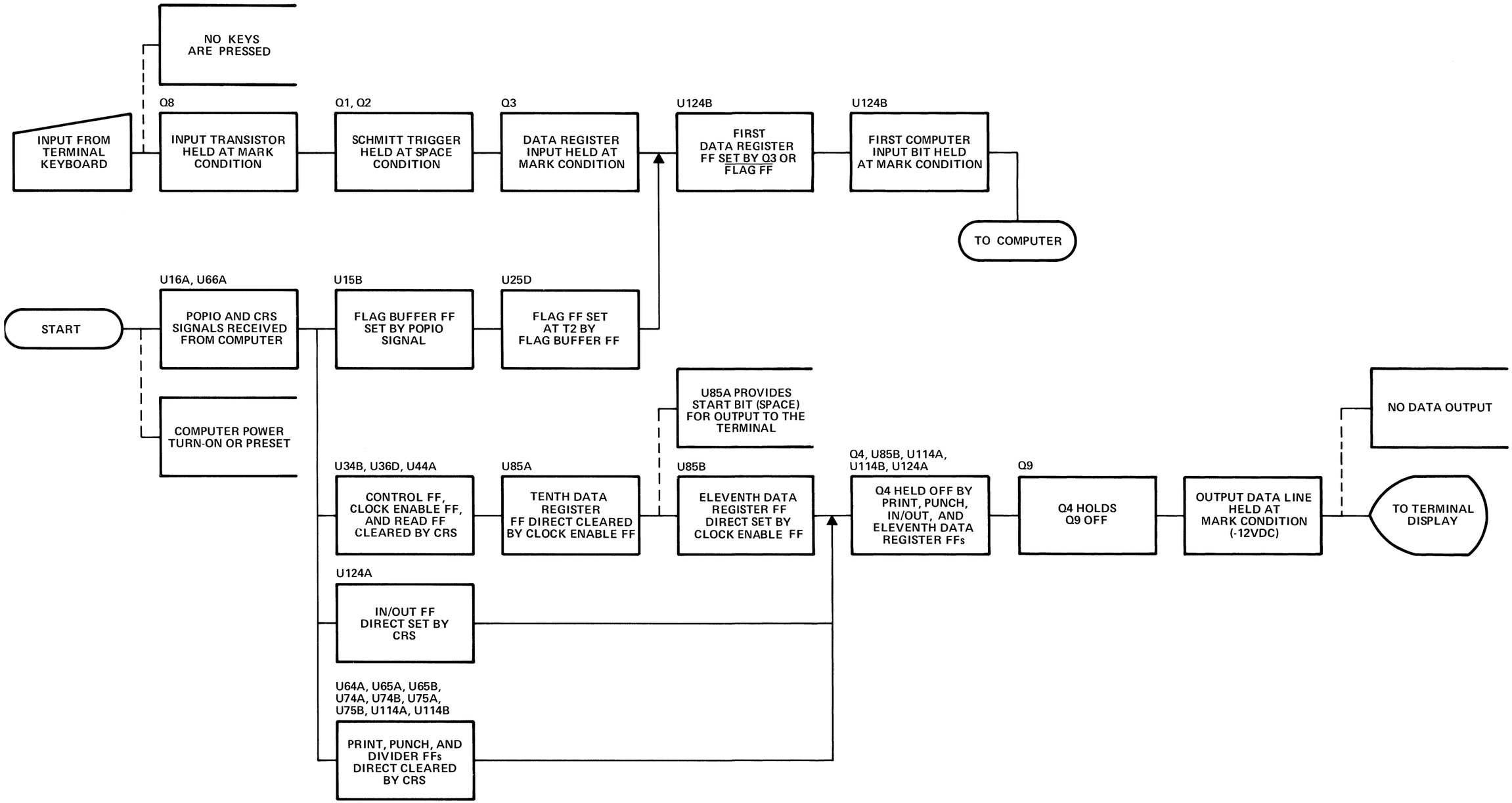
3-34. When the first clock pulse is received by the Data Register, the data is shifted down one FF. Since FF U85A was direct cleared when the Clock Enable FF was cleared after the previous operation, a false set-side output of FF U85A is clocked into FF U85B. The true clear-side output of FF U85B provides the start bit, or space condition, to the terminal. The next eight clock pulses shift the data bits stored in the Data Register from the IOBO lines out to the terminal. The last two clock pulses shift out the true, or mark condition, stop bits. The first stop bit was generated by direct setting FF U124B of the Data Register when the last OTA/B instruction was issued. This provided a logic 1 to the set input of FF U125A before the Data Register was clocked. The last stop bit was generated by the mark condition of the input data line which provided a true signal to the set input of FF U124B of the Data Register before the first clock pulse was received.

3-35. Clearing the Clock Enable FF at the end of the data transfer inhibits the External Clock signal from entering the Divider circuit, direct sets FF U85B of the Data Register to maintain the data output line in a mark condition, and direct clears FF U85A of the Data Register to provide the start bit for the next output operation.



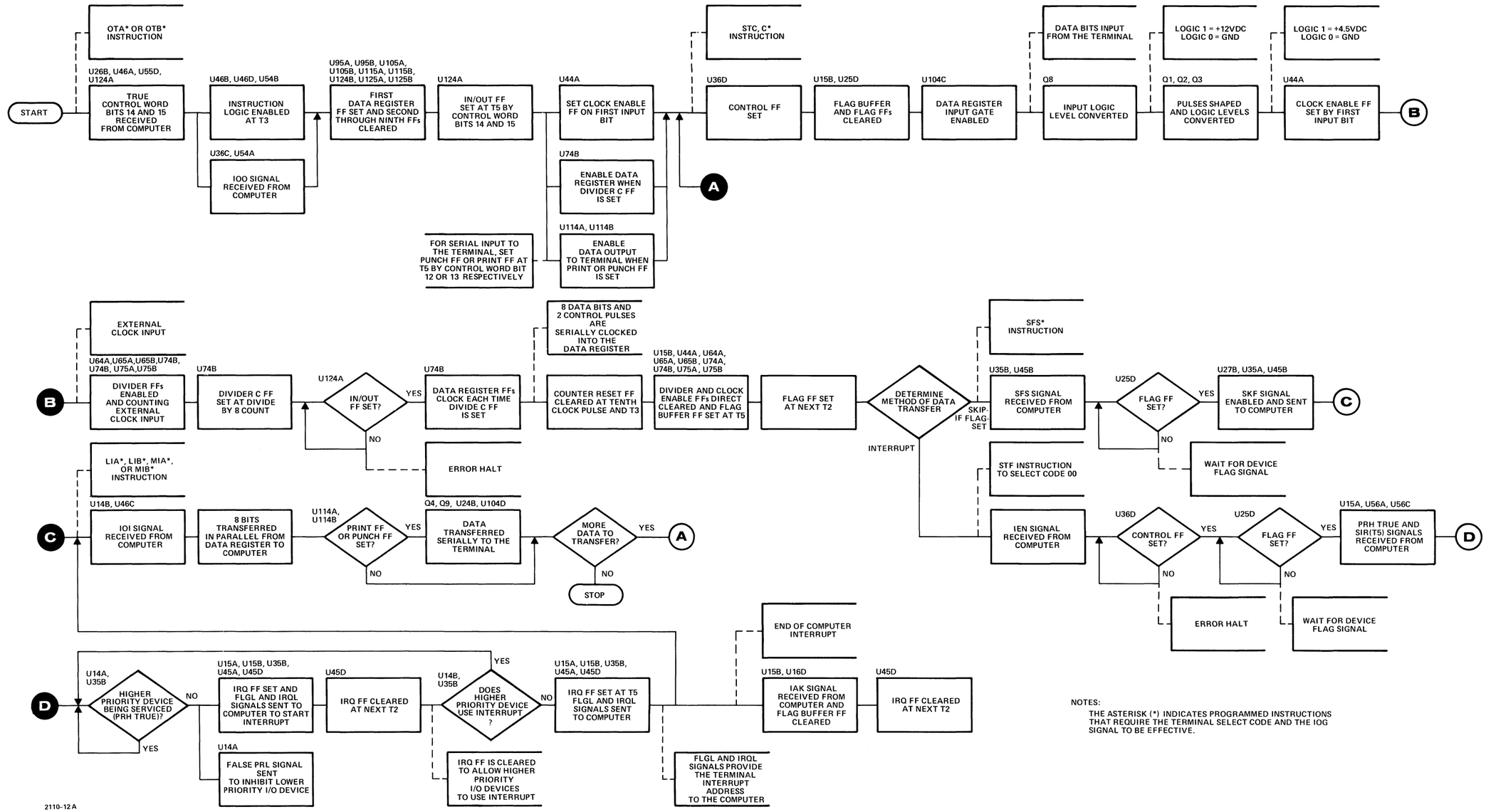
2110-4A

Figure 3-4. Output Operation, Timing Diagram



2110-11

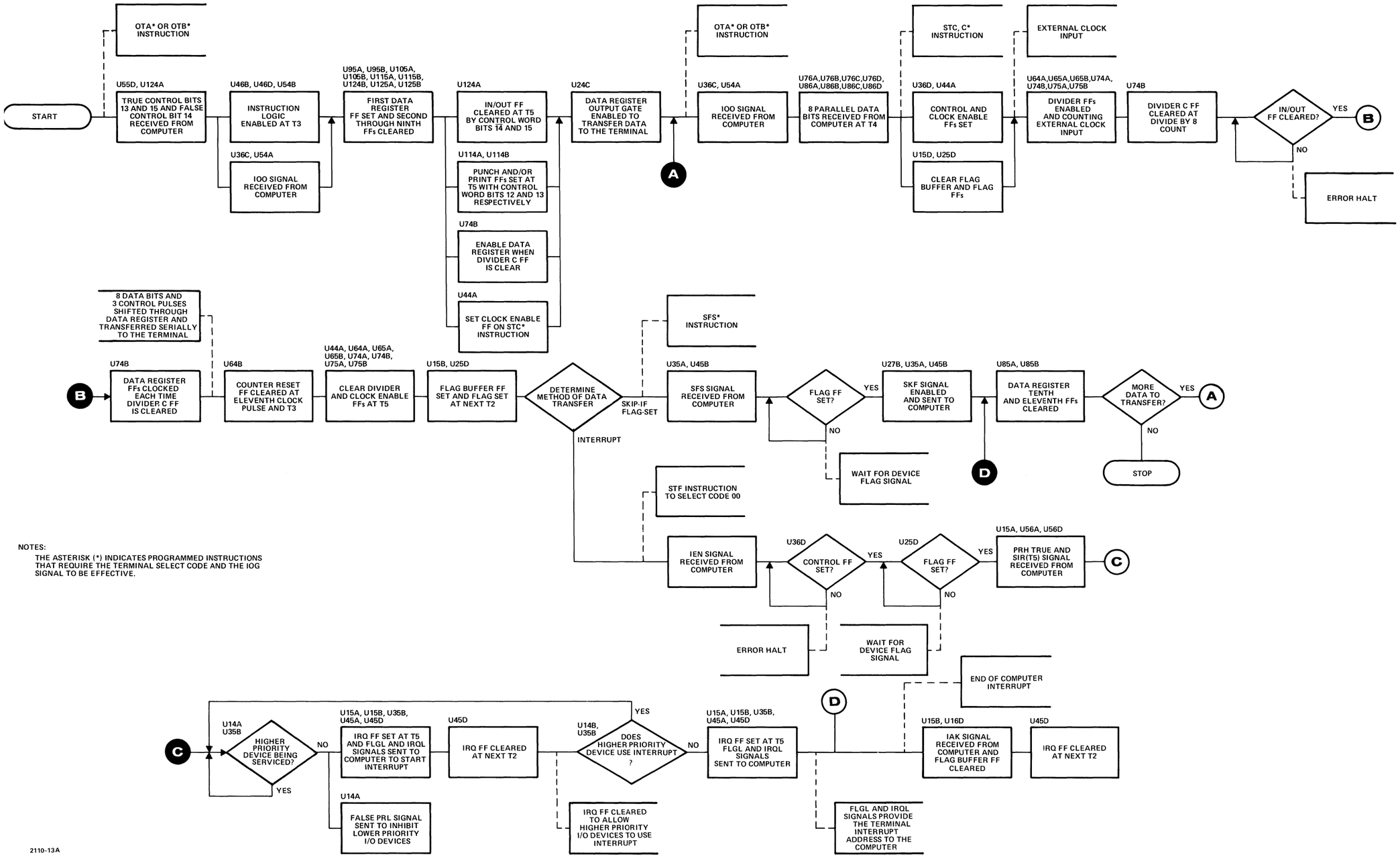
Figure 3-5. Initial Condition After Power Turn-On or Preset, Flow Diagram



NOTES:

THE ASTERISK (*) INDICATES PROGRAMMED INSTRUCTIONS THAT REQUIRE THE TERMINAL SELECT CODE AND THE IOG SIGNAL TO BE EFFECTIVE.

Figure 3-6. Interface Card Input Operation, Flow Diagram



NOTES:

THE ASTERISK (*) INDICATES PROGRAMMED INSTRUCTIONS THAT REQUIRE THE TERMINAL SELECT CODE AND THE IOG SIGNAL TO BE EFFECTIVE.

2110-13A

Figure 3-7. Interface Card Output Operation, Flow Diagram

SECTION IV
MAINTENANCE

4-1. INTRODUCTION.

4-2. This section contains information on diagnostics and troubleshooting for the HP 12880A Keyboard-Display Terminal Interface Kit.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are provided in the applicable computer documentation. There are no separate preventive maintenance procedures to be performed on the interface kit.

4-5. DIAGNOSTICS.

4-6. The interface card may be checked with a terminal using the diagnostic described in the following appropriate diagnostic reference manual: part no. 24200-90002 for HP 2600A; part no. 02615-90002 for HP 2615A; part no. 02640-90020 for HP 2640; and part no. 02644-90012 for HP 2644.

4-7. TROUBLESHOOTING.

4-8. Troubleshooting for the interface card is accomplished by performing the diagnostic tests in the diagnostic program and analyzing the error halts that occur as the test is being run. Continuity checks of the interconnecting cable may be performed by using table 4-1. To further isolate the trouble, refer to logic diagram and parts location view in figure 4-1. Table 4-2 contains a parts list for the interface card with the parts listed in alphanumeric order by reference designation. Logic and pin location diagrams for the integrated circuits used on the interface card are contained in figure 4-2. Table 4-3 gives the integrated circuit input levels, output levels, and delay times which correspond to the integrated circuit characteristic number shown below each diagram in figure 4-2.

4-9. CABLE ASSEMBLY CONNECTOR PIN FUNCTIONS.

4-10. Table 4-1 contains a list of cable assembly pin assignments for the interface card connector and the terminal connector.

Table 4-1. Wiring List for Interconnecting Cables

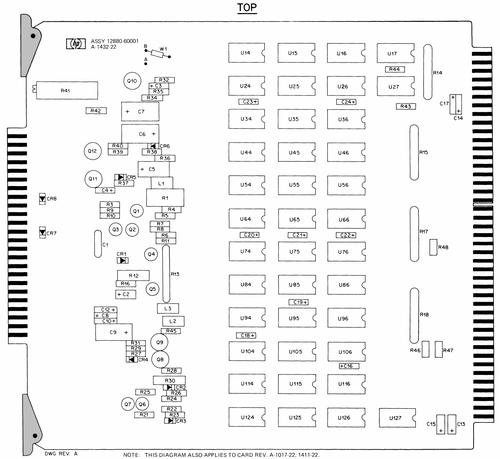
INTERFACE CARD CONNECTOR PINS	TERMINAL CONNECTOR PINS	WIRE COLOR	FUNCTION
INTERCONNECTING CABLE ASSY 12880-60003 (STANDARD)			
L	16	Orange	External clock from terminal
W	3	Brown	Data output to terminal
X	2	White	Data input from terminal
BB	1	Shield	Ground
17	6	Red	(Not used)
24	7	Black	Ground
INTERCONNECTING CABLE ASSY 02640-60058 (OPTION 001)			
U	E,J	Orange	+12 volts/clear to send
W	C	Red	Data output to terminal
X	B	Brown	Data input from terminal
L	K	Yellow	External clock from terminal
24	H	Green/Shield	Ground

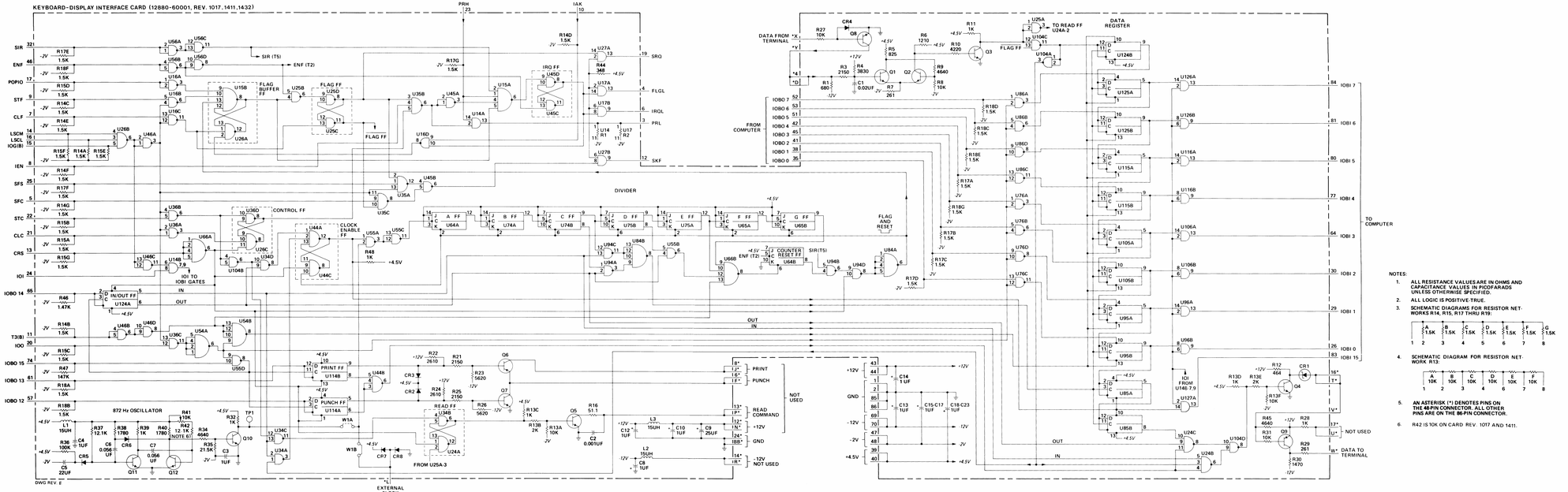
Notes: Jumpers within both interface card connector hoods tie the following pins together:
a. D, 4, and Y.
b. T, 16, and V.

Table 4-2. Interface Card Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1	0160-2146	Capacitor, Fxd, Cer, 0.025 uF, +80 -20%, 100 VDCW	28480	0160-2146
C2	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C3,4,8,10, C12 thru C24	0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X 9035A2
C5	0180-0228	Capacitor, Fxd, Elect, 22 uF, 10%, 15 VDCW	28480	0180-0228
C6,7	0160-0165	Capacitor, Fxd, My, 0.056 uF, 10%	28480	0160-0165
C9	0180-0338	Capacitor, Fxd, Elect, 25 uF, +75 -10%, 25 VDCW	28480	0180-0338
CR1	1902-0022	Diode, Breakdown, 2.67V	28480	1902-0022
CR2,3*	1910-0030	Diode, Ge, 100 mA, 0.65V	28480	1910-0030
CR4,5	1910-0022	Diode, Ge, 5 WIV	28480	1910-0022
CR6,7,8*	1901-0040	Diode, Si, 30 mA, 30 WV	07263	FDG1088
L1 thru L3	9140-0082	Coil, Fxd, RF, 15 uH	28480	9140-0082
Q1 thru Q3, Q10 thru Q12	1854-0094	Transistor, Si, NPN	28480	1854-0094
Q4,5	1854-0215	Transistor, Si, NPN	28480	1854-0215
Q6,7	1853-0036	Transistor, Si, PNP	28480	1853-0036
Q8,9	1853-0058	Transistor, Si, PNP	07263	2N3644
R1	0698-3635	Resistor, Fxd, Met Ox, 680 ohms, 5%, 2W	28480	0698-3635
R3,21,25	0698-0084	Resistor, Fxd, Flm, 2.15k, 1%, 1/8W	28480	0698-0084
R4	0698-3153	Resistor, Fxd, Flm, 3.83k, 1%, 1/8W	28480	0698-3153
R5	0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421
R6	0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274
R7,29	0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132
R8,27,31,42*	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442
R9,34,45	0698-3155	Resistor, Fxd, Flm, 4.64k, 1%, 1/8W	28480	0698-3155
R10	0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154
R11,28,32,39,48	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280
R12	0698-0090	Resistor, Fxd, Flm, 464 ohms, 1%, 1/2W	28480	0698-0090
R13	1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008
R14,15,17,18	1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020
R16	0757-0394	Resistor, Fxd, Flm, 51.1 ohms, 1%, 1/8W	28480	0757-0394
R22,24	0698-0085	Resistor, Fxd, Flm, 2.61k, 1%, 1/8W	28480	0698-0085
R23,26	0757-0200	Resistor, Fxd, Flm, 5.62k, 1%, 1/8W	28480	0757-0200
R30	0757-1078	Resistor, Fxd, Flm, 1.47k, 1%, 1/2W	28480	0757-1078
R35	0757-0199	Resistor, Fxd, Flm, 21.5k, 1%, 1/8W	28480	0757-0199
R36	0757-0465	Resistor, Fxd, Flm, 100k, 1%, 1/8W	28480	0757-0465
R37	0757-0444	Resistor, Fxd, Flm, 12.1k, 1%, 1/8W	28480	0757-0444
R38,40	0757-0278	Resistor, Fxd, Flm, 1.78k, 1%, 1/8W	28480	0757-0278
R41	2100-1660	Resistor, Var, WW, 10k, 10%, 1W	28480	2100-1660
R43	0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440
R44	0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445
R46,47	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
U14,17,27	1820-0956	Integrated Circuit, CTL	07263	U6A995679X
U15	1820-0069	Integrated Circuit, TTL	01295	SN7420N
U16,25,34,36,45,46,55,56,76, 86,94,104	1820-0054	Integrated Circuit, TTL	01295	SN7400N
U24,26,35,44	1820-0068	Integrated Circuit, TTL	01295	SN7410N
U54,66,84	1820-0071	Integrated Circuit, TTL	01295	SN7440N
U64,65,74,75	1820-0075	Integrated Circuit, TTL	01295	SN7473
U85,95,105,114,115,124,125	1820-0077	Integrated Circuit, TTL	01295	SN7474N
U96,106,116,126,127	1820-0974	Integrated Circuit, CTL	28480	1820-0974
W1	8159-0005	Jumper Wire	28480	8159-0005

*NOTE: CR7 and CR8 are part no. 1901-0040 on card rev. 1411 and above.
CR7 and CR8 are part no. 1910-0030 on card rev. 1017 and below.
R42 is part no. 0757-0444 for card rev. 1432 and above.





NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES IN PICOFARADS UNLESS OTHERWISE SPECIFIED.
2. ALL LOGIC IS POSITIVE-TRUE.
3. SCHEMATIC DIAGRAMS FOR RESISTOR NETWORKS R14, R15, R17 THRU R19:

4. SCHEMATIC DIAGRAM FOR RESISTOR NETWORK R13:

5. AN ASTERISK (*) DENOTES PINS ON THE 86-PIN CONNECTOR. ALL OTHER PINS ARE ON THE 96-PIN CONNECTOR.
6. R42 IS 10K ON CARD REV. 1017 AND 1411.

Figure 4-1. Interface Card Logic Diagram and Parts Location View

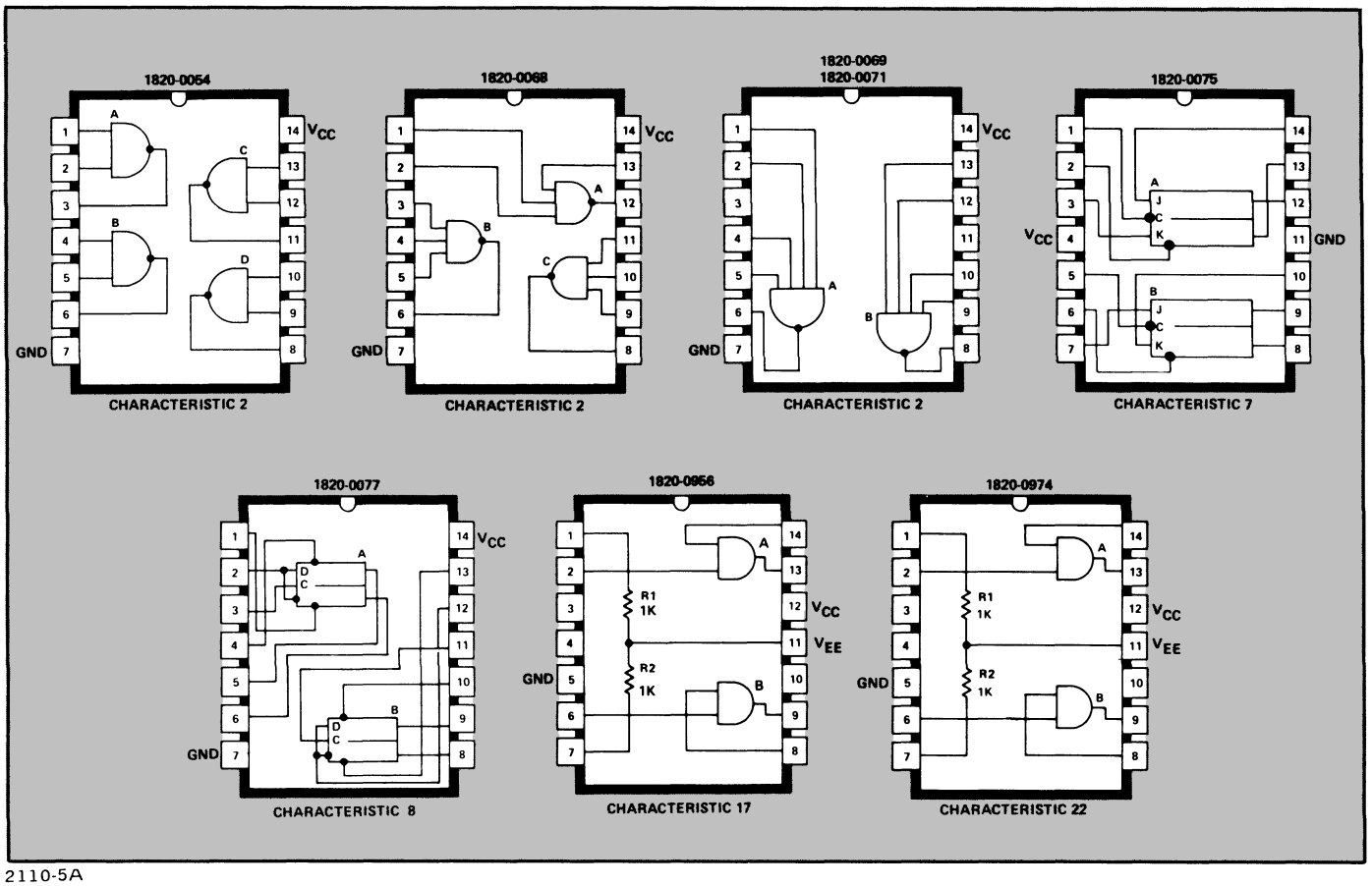


Figure 4-2. Integrated Circuit Diagrams

Table 4-3. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	MAXIMUM PROPAGATION DELAY	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECOND)	TO LOGIC 0 (NANOSECOND)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
7 (See note 1)	+2.0	+0.8	+2.4	+0.4	Logic 1	50	50
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
22	+1.5	+0.4	+2.2	-0.3	Logic 0	24	24

Note: 1. Required clock pulse width is 20 ns minimum; required direct-clear input is 25 ns minimum.

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the HP 12880A Keyboard-Display Terminal Interface Kit. Table 5-1 lists parts in numeric order by HP part number and lists the following information for each part:

a. Description of the part. (Refer to table 5-3 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-2.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. A separate parts list is provided along with the parts location view for the interface card in section IV of this manual. This parts list presents the parts in alpha-numeric order by reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Interface kit model and serial number.
b. Hewlett-Packard part number for each part.
c. Description of each part.
d. Circuit reference designation.

Table 5-1. HP 12880A Keyboard-Display Terminal Interface Kit
Numeric Parts List

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	1
0160-0165	Capacitor, Fxd, My, 0.056 uF, 10%	28480	0160-0165	2
0160-2146	Capacitor, Fxd, Cer, 0.025 uF, +80 -20%, 100 VDCW	28480	0160-2146	1
0180-0228	Capacitor, Fxd, Elect, 22 uF, 10%, 15 VDCW	28480	0180-0228	1
0180-0291	Capacitor, Fxd, Elect, 1 uF, 10%, 35 VDCW	56289	150D105X 9035A2	17
0180-0338	Capacitor, Fxd, Elect, 25 uF, +75 -10%, 25 VDCW	28480	0180-0338	1
0698-0084	Resistor, Fxd, Flm, 2.15k, 1%, 1/8W	28480	0698-0084	3
0698-0085	Resistor, Fxd, Flm, 2.61k, 1%, 1/8W	28480	0698-0085	2
0698-0090	Resistor, Fxd, Flm, 464 ohms, 1%, 1/2W	28480	0698-0090	1
0698-3132	Resistor, Fxd, Flm, 261 ohms, 1%, 1/8W	28480	0698-3132	2
0698-3153	Resistor, Fxd, Flm, 3.83k, 1%, 1/8W	28480	0698-3153	1
0698-3154	Resistor, Fxd, Flm, 4.22k, 1%, 1/8W	28480	0698-3154	1
0698-3155	Resistor, Fxd, Flm, 4.64k, 1%, 1/8W	28480	0698-3155	3
0698-3440	Resistor, Fxd, Flm, 196 ohms, 1%, 1/8W	28480	0698-3440	1
0698-3445	Resistor, Fxd, Flm, 348 ohms, 1%, 1/8W	28480	0698-3445	1
0698-3635	Resistor, Fxd, Met Ox, 680 ohms, 5%, 2W	28480	0698-3635	1
0757-0199	Resistor, Fxd, Flm, 21.5k, 1%, 1/8W	28480	0757-0199	1
0757-0200	Resistor, Fxd, Flm, 5.62k, 1%, 1/8W	28480	0757-0200	2
0757-0274	Resistor, Fxd, Flm, 1.21k, 1%, 1/8W	28480	0757-0274	1
0757-0278	Resistor, Fxd, Flm, 678k, 1%, 1/8W	28480	0757-0278	2
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	28480	0757-0280	5
0757-0394	Resistor, Fxd, Flm, 51.1 ohms, 1%, 1/8W	28480	0757-0394	1
0757-0421	Resistor, Fxd, Flm, 825 ohms, 1%, 1/8W	28480	0757-0421	1
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	28480	0757-0442	4**
0757-0444	Resistor, Fxd, Flm, 12.1k, 1%, 1/8W	28480	0757-0444	1**
0757-0465	Resistor, Fxd, Flm, 100k, 1%, 1/8W	28480	0757-0465	1
0757-1078	Resistor, Fxd, Flm, 1.47k, 1%, 1/2W	28480	0757-1078	1
0757-1094	Resistor, Fxd, Flm, 647k, 1%, 1/8W	28480	0757-1094	2
1480-0116	Pin, Grooved	28480	1480-0116	2
1810-0008	Resistor Network (6 fxd flm resistors)	28480	1810-0008	1
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	4
1820-0054	Integrated Circuit, TTL	01295	SN7400N	12
1820-0068	Integrated Circuit, TTL	01295	SN7410N	4
1820-0069	Integrated Circuit, TTL	01295	SN7420N	1
1820-0071	Integrated Circuit, TTL	01295	SN7440N	3
1820-0075	Integrated Circuit, TTL	01295	SN7473	4
1820-0077	Integrated Circuit, TTL	01295	SN7474N	7
1820-0956	Integrated Circuit, CTL	07263	U6A995679X	3
1820-0974	Integrated Circuit, CTL	28480	1820-0974	5
1853-0036	Transistor, Si, PNP	28480	1853-0036	2
1853-0058	Transistor, Si, PNP	07263	2N3644	2
1854-0094	Transistor, Si, NPN	28480	1854-0094	6
1854-0215	Transistor, Si, NPN	28480	1854-0215	2
1901-0040	Diode, Si, 30 mA, 30 WV	28480	1901-0040	3*
1902-0022	Diode, Breakdown, 2.67V	28480	1902-0022	1
1910-0022	Diode, Ge, 5 WIV	28480	1910-0022	2
1910-0030	Diode, Ge, 100 mA, 0.65V	28480	1910-0030	2*
2100-1660	Resistor, Var, WW, 10k, 10%, 1W	28480	2100-1660	1
8159-0005	Jumper Wire	28480	8159-0005	1
9140-0082	Coil, Fxd, RF, 15 uH	28480	9140-0082	3

Table 5-1. HP 12880A Keyboard-Display Terminal Interface Kit
Numeric Parts List (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
5040-6065	PC Extractor	28480	5040-6065	2
02640-60058	Cable Assy (Option 001 only)	28480	02640-60058	1
12880-60001	Circuit Card, Keyboard-Display Terminal Interface	28480	12880-60001	1
12880-60003	Cable Assembly	28480	12880-60003	1
12880-90001	12880A Operating and Service Manual	28480	12880-90001	1

NOTE: *TQ for card rev. 1017 and below is 1 for part no. 1901-0040 and 4 for part no. 1910-0030. Quantities shown are for card rev. 1411.
**TQ for card rev. 1432 and above is 3 for part no. 0757-0442 and 2 for part no. 0757-0444.

Table 5-2. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and the latest supplements.

Code No.	Manufacturer	Address
01295	Texas Instruments, Inc. Transistor Products Division	Dallas, Texas
07263	Fairchild Camera & Inst. Corp., Semiconductor Division	Mt. View, Cal.
28480	Hewlett-Packard Co.	Palo Alto, Cal.
56289	Sprague Electric Co.	North Adams, Mass.

Table 5-3. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit
C	= capacitor	MC	= microcircuit	V	= vacuum tube, neon bulb, photocell, etc.
CR	= diode	P	= plug connector		
DL	= delay line	Q	= transistor	VR	= voltage regulator
DS	= indicator (lamp)	R	= resistor	W	= cable, jumper
E	= misc hardware	RT	= thermistor	X	= socket
F	= fuse	S	= switch	Y	= crystal
FL	= filter	T	= transformer	Z	= tuned cavity, network
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gnd	= ground(ed)	ph	= Phillips head
ac	= alternating current	gra	= gray	pk	= peak
ad	= anode	grn	= green	p-p	= peak-to-peak
Al	= aluminum			pt	= point
AR	= as required	H	= henries	PIV	= peak inverse voltage
adj	= adjust	Hg	= mercury	PNP	= positive-negative-positive
Assy	= assembly	hr	= hour(s)	PWV	= peak working voltage
		Hz	= hertz	porc	= porcelain
B	= base	hdw	= hardware	posn	= position(s)
bp	= bandpass	hex	= hexagon, hexagonal	pozi	= pozidrive
bfo	= beat frequency oscillator			ph brz	= phosphor bronze
blk	= black	ID	= inside diameter		
blu	= blue	IF	= intermediate frequency	rf	= radio frequency
brn	= brown	in.	= inch, inches	rdh	= round head
brs	= brass	I/O	= input/output	rmo	= rack mount only
Btu	= British thermal unit	int	= internal	rms	= root-mean-square
bwc	= backward wave oscillator	incl	= include(s)	RWV	= reverse working voltage
Be Cu	= beryllium copper	insul	= insulation, insulated	rect	= rectifier
		impgrg	= impregnated	r/min	= revolutions per minute
C	= collector	incand	= incandescent		
cw	= clockwise			s	= second
ccw	= counterclockwise	k	= kilo (10^3), kilohm	SB	= slow-blow
cer	= ceramic			Se	= selenium
cmo	= cabinet mount only	lp	= low pass	Si	= silicon
com	= common			scr	= silicon-controlled rectifier
crt	= cathode-ray tube	m	= milli (10^{-3})	sil	= silver
CTL	= capacitor-transistor logic	M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
Comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous	semicond	= semiconductor
		met ox	= metal oxide		
dc	= direct current	mintr	= miniature	Ta	= tantalum
dr	= drive			td	= time delay
DTL	= diode-transistor logic	n	= nano (10^{-9})	Ti	= titanium
depc	= deposited carbon	nc	= normally closed or no connection	tgl	= toggle
dpdt	= double-pole, double-throw			thd	= thread
dpst	= double-pole, single-throw	Ne	= neon	tol	= tolerance
		no.	= number or normally open	TTL	= transistor-transistor logic
E	= emitter	np	= nickel plated	term	= terminal
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative positive zero (zero temperature coefficient)	U (μ)	= micro (10^{-6})
elctlt	= electrolytic				
		NSR	= not separately replaceable	V	= volt(s)
F	= farads	NRFR	= not recommended for field replacement	var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head			VDCW	= direct current working volts
flm	= film	OD	= outside diameter		
fxd	= fixed	OBD	= order by description	W	= watts
filh	= fillister head	orn	= orange	ww	= wirewound
		ovh	= oval head	wht	= white
G	= giga (10^9)	oxd	= oxide	WIV	= working inverse voltage
Ge	= germanium				
gl	= glass	p	= pico (10^{-12})	yel	= yellow
		PC	= printed circuit		

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CERTIFICATION

Products, materials, parts, and services furnished on this order have been provided in accordance with all applicable Hewlett-Packard specifications. Actual inspection and test data pertaining to this order is on file and available for examination.

Hewlett-Packard's calibration measurements are traceable to the National Bureau of Standards to the extent allowed by the Bureau's calibration facilities.

The Hewlett-Packard Quality Program satisfies the requirements of MIL-Q-9858, MIL-I-45208, and MIL-C-45662.

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