HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

12845B

LINE PRINTER INTERFACE KIT

(FOR THE HP 2100-SERIES COMPUTERS)

Printed-Circuit Assembly:

12845-60005, Series 1423, 1506, 1715

12845-90011

HEWLETT-PACKARD COMPANY
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GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This installation and service manual covers general information installation, programming, theory of operation, maintenance, and replaceable parts for the HP 12845B Line Printer Interface Kit.

1-3. GENERAL DESCRIPTION.

1-4. The HP 12845B Line Printer Interface Kit provides the necessary equipment to interface Hewlett-Packard line printers with an HP 2100-series computer. The kit contains the following items:

a. One interface printed-circuit assembly, part no. 12845-60005.

b. One interface cable, part no. 12845-60006.

c. One installation and service manual, part no. 12845-90011

1-5. The line printer interface kit uses a printed circuit assembly (PCA) which contains the circuitry required to control the transfer of data and status information between the computer and line printer. The interface PCA contains register circuits for output from the computer to the line printer and buffer circuits for status input from the line printer to the computer. Seven data bits are transferred from the computer to the line printer and up to five status bits are transferred from the line printer to the computer. The interface PCA also contains control, interrupt, and service request logic circuits that permit programming of the I/O functions.

1-6. IDENTIFICATION.

1-7. Printed-circuit assembly revisions are identified by a letter, a series code, and a division code marked beneath the part number on the PCA. The letter identifies the revision of the etched-trace pattern on the unloaded PCA. The four-digit series code pertains to the electrical chacteristics of the loaded PCA and the positions of the components. The two-digit division code identifies the division of Hewlett-Packard that manufactured the PCA. If the series number does not correspond exactly with the series number on the title page of this manual, the PCA differs from the one described in this manual. These differences are covered in manual supplements available at the nearest HP Sales and Service Office listed at the back of this manual.

1-8. SPECIFICATIONS.

1-9. Specifications for the line printer interface kit are given in table 1-1.

Table 1-1. Specifications

CURRENT REQUIRED FROM COMPUTER:	
+4.5 Volt Supply	1.13 amperes
-2 Volt Supply	.04 ampere
DATA TRANSFER RATE	2 microseconds per character
TYPE OF CODE USED	ASCll (7 bits per character)
LOGIC VOLTAGE LEVELS:	
Logic 1	+2.4 volts dc (minimum)
Logic 0	+0.4 volts dc (maximum)
CARD DIMENSIONS:	
Width	7-3/4 inches (196.8mm)
Height	8-11/16 inches (220.7mm)
WEIGHT:	
Net	18 oz (510gm)
Shipping	2 lb (908gm)

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, reshipment, and programming for the HP 12845B Line Printer Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. Before installing the interface PCA in the computer, ensure that the additional power consumed by the PCA will not overload the computer power supply. Power requirements of the PCA are given in table 1-1; instructions for calculating available power are given in the applicable computer manual. If sufficient power is available, install the interface kit as follows:

a. Ensure that jumper STR is positioned properly (paragraph 2-4lb).

b. Turn off power at the computer and line printer.

c. Gain access to the computer I/O card cage and insert the interface PCA in the slot corresponding to the desired select code.

d. Connect the 100-pin connector (P1) of the interconnecting cable to the 100-pin edge connector of the interface PCA.

e. Connect the other end of the cable assembly (P2) to the mating connector on the line printer.

f. Verify proper operation by performing the appropriate diagnostic test. Instructions for performing the diagnostic test are contained in the *Manual of Diagnostics*.

2-7. RESHIPMENT.

2-8. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-9. Package the item in the original factory packing material, if available. If the original material is not available, standard factory packaging material can be obtained from a local Hewlett-Packard Sales and Service Office.

2-10. If standard factory packaging material is not used, wrap the item in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corp., Hawthorne, N.J., and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

Note: In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-11. PROGRAMMING.

2-12. The following paragraphs provide general information for programming the operation of the line printer interface. This information consists of line printer characteristics, computer data output and control signals to the line printer, and control and status signals from the line printer. A sample program and information on DMA operation are also included.

2-13. LINE PRINTER CHARACTERISTICS.

2-14. Hewlett-Packard line printers control the paper movement and printing of 132- column lines by receiving character words, format control words and control signals from the interface. Control and status signals are sent from the line printer to the interface.

2-15. The line printer accepts ASCII coded data over seven pairs of lines from the interface. Each character word contains the code for one printed character. Line printer character sets consist of 64, 96, or 128 characters as shown by table 2-1.

2-16. The same seven pairs of lines used to transfer characters to the line printer are used to transfer format control words which control vertical line spacing. A prepunched tape, located inside the line printer, is used for controlling the vertical format of the printed page. The perforations in the tape are arranged in eight or twelve channels depending on the model line printer, each of which, when selected by a format contol word, cause the line printer to advance a specified number of lines. The standard VFU tape supplied by Hewlett-Packard is coded for 11-inch forms at six lines per inch.

2-17. COMPUTER OUTPUT.

2-18. CHARACTER WORD. Characters are received in the form of 7-bit ASCII coded words. Bits 0 through 6 of the 16-bit computer word (see figure 2-1) are used; therefore, if the characters are stored "packed" in memory, they must be unpacked and right-justified before being output to the line printer interface. Bit 15 of the computer word is a definition bit and must be "0" when transferring a character word. Character words are transferred to the interface via an OTA or OTB instruction addressed to the interface or by DMA output cycles. An STC,C (Set Control, Clear Flag) instruction addressed to the interface causes the line printer to accept the character word and enables the flag logic so the line printer can respond when ready for another word.

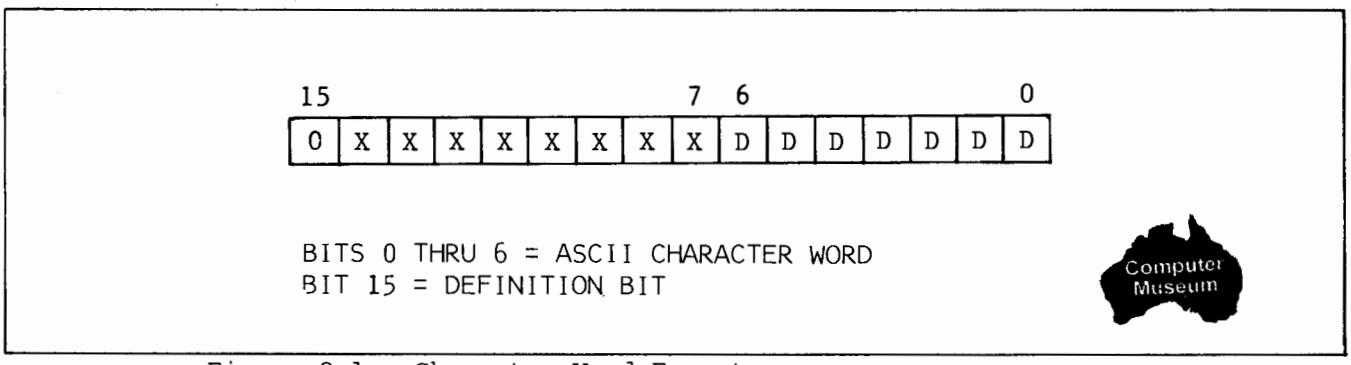


Figure 2-1. Character Word Format

2-19. Table 2-1 is a listing of the various Hewlett-Packard line printer character codes and characters. Line printer models not specifically noted on the table use the characters described in the STANDARD columns.

2-20. FORMAT CONTROL WORD. The format control word is also a 7-bit word using bits 0 through 6 of the computer word (see figure 2-2). The definition bit (bit 15) must be a "1". This definition bit, when a "1", causes the line printer to initiate a print cycle printing the content of its character buffer. This takes place befor the format control word is executed. Format control words are transferred to the interface via an OTA or OTB instruction addressed to the line printer interface or by a DMA output cycle. An STC,C instruction addressed to the line printer interface causes the line printer to accept and execute the format control word and enables the interface flag logic so that the line printer can respond when ready for another word.

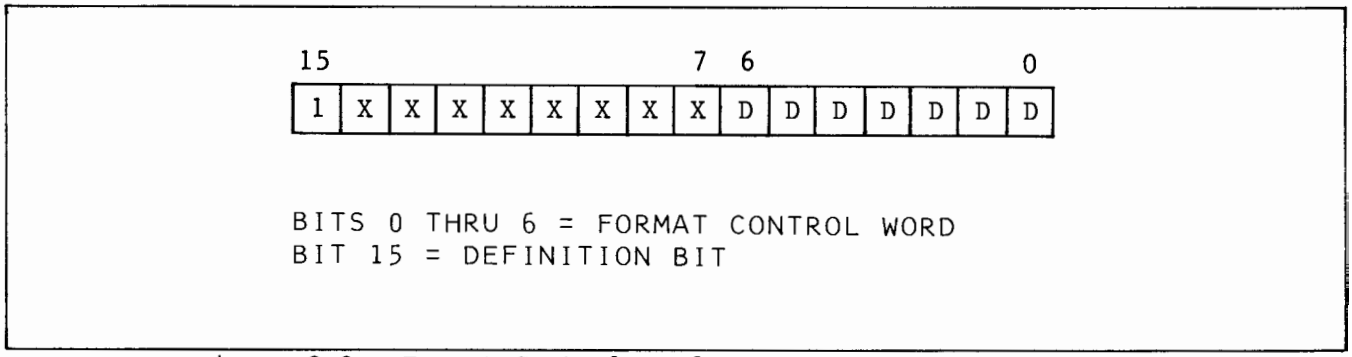


Figure 2-2. Format Control Word Format

2-21. Table 2-2 lists the format control words and their functions. Note that there are some differences between line printers in format control capabilities.

2-22. CONTROL SIGNALS TO LINE PRINTER.

2-23. Control signals transferred from the interface to the line printer are as follows:

a. Master Clear Signal.
b. Paper Instruction Signal.
c. Strobe Signal.

Table 2-1. Character Codes and Symbols

CODE (OCTAL)	2607A 2607A-002	2607A-001	2607A-003	CODE (OCTAL)	STANDARD	2607A-002 2607A-003	CODE (OCTAL)	STANDARD	2607A-002 2607A-003	CODE (OCTAL)	STANDARD (64 CHAR)	STANDARD (96 CHAR)	2607A-002	2607A-003
0xx000				0xx040	(blank)		0xx100	@		0xx140	@	`		ü
0xx001				0xx041	!		0xx101	A		0xx141	A	a		
0xx002				0xx042	"		0xx102	B		0xx142	B	b		
0xx003				0xx043	#	£	0xx103	C		0xx143	C	c		
0xx004				0xx044	$		0xx104	D		0xx144	D	d		
0xx005				0xx045	%		0xx105	E		0xx145	E	e		
0xx006				0xx046	&		0xx106	F		0xx146	F	f		
0xx007				0xx047	'		0xx107	G		0xx147	G	g		
0xx010				0xx050	(		0xx110	H		0xx150	H	h		
0xx011				0xx051	)		0xx111	I		0xx151	I	i		
0xx012				0xx052	*		0xx112	J		0xx152	J	j		
0xx013				0xx053	+		0xx113	K		0xx153	K	k		
0xx014				0xx054	'		0xx114	L		0xx154	L	l		
0xx015				0xx055	-		0xx115	M		0xx155	M	m		
0xx016				0xx056	.		0xx116	N		0xx156	N	n		
0xx017				0xx057	/		0xx117	O		0xx157	O	o		
0xx020				0xx060	0		0xx120	P		0xx160	P	p		
0xx021				0xx061	1		0xx121	Q		0xx161	Q	q		
0xx022				0xx062	2		0xx122	R		0xx162	R	r		
0xx023				0xx063	3		0xx123	S		0xx163	S	s		
0xx024				0xx064	4		0xx124	T		0xx164	T	t		
0xx025				0xx065	5		0xx125	U		0xx165	U	u		
0xx026				0xx066	6		0xx126	V		0xx166	V	v		
0xx027				0xx067	7		0xx127	W		0xx167	W	w		
0xx030				0xx070	8		0xx130	X		0xx170	X	x		
0xx031				0xx071	9		0xx131	Y		0xx171	Y	y		
0xx032				0xx072	:		0xx132	Z		0xx172	Z	z		
0xx033				0xx073	;		0xx133	[	Ä	0xx173	{	{	Ä	ä
0xx034				0xx074	<		0xx134	\	Ö	0xx174	|	|	Ö	ö
0xx035				0xx075	=		0xx135	]	Å	0xx175	}	}	Å	å
0xx036				0xx076	>		0xx136	^		0xx176	~	~		
0xx037				0xx077	?		0xx137	_		0xx177	_	▒		

Table 2-2. Format Control Codes and Functions

CODE (OCTAL)	FUNCTION		
	2610A/2614A	2607A	2613A/2617A/2618A
lxx000	Suppress line advance	Advance 1 line	Suppress line advance
lxx001 thru lxx077	Advance 1 line thru Advance 63 lines	Advance 1 line thru Advance 15 lines (codes lxx020 thru lxx077 not used)	Advance 1 line thru Advance 15 lines (codes lxx020 thru lxx077 not used)
lxx100	Select VFU channel 1 (top of form)	Select VFU channel 1 (top of form)	Select VFU channel 1 (top of form)
lxx101	Select VFU channel 2 (bottom of form)	Select VFU channel 2 (bottom of form)	Select VFU channel 2 (bottom of form)
lxx102	Select VFU channel 3 (single space)	Select VFU channel 3 (single space)	Select VFU channel 3 (single space)
lxx103	Select VFU channel 4 (double space)	Select VFU channel 4 (double space)	Select VFU channel 4 (double space)
lxx104	Select VFU channel 5 (triple space)	Select VFU channel 5 (triple space)	Select VFU channel 5 (triple space)
lxx105	Select VFU channel 6 (half page)	Select VFU Channel 6 (half page)	Select VFU channel 6 (half page)
lxx106	Select VFU channel 7 (quarter page)	Select VFU channel 7 (quarter page)	Select VFU channel 7 (quarter page)
lxx107	Select VFU channel 8 (sixth page)	Select VFU channel 8 (sixth page)	Select VFU channel 8 (sixth page)
lxx110	NOT USED	NOT USED	Select VFU channel 9 (bottom of form)
lxx111	NOT USED	NOT USED	Select VFU channel 10 *
lxx112	NOT USED	NOT USED	Select VFU channel 11 *
lxx113	NOT USED	NOT USED	Select VFU channel 12 *

* VFU channels 10,11, and 12 are blank and can be punched to meet the user's requirements.

2-24. MASTER CLEAR SIGNAL. The Master Clear signal is caused by the computer preset function when computer power is turned on, when external preset is enabled on the computer control panel, or when a programmed CLC (Clear Control) instruction addressed to select code 00 is executed. The Master Clear signal, which has a duration of five microseconds, clears the printer line buffer and on all line printers except the 2613A, aborts any paper advance in progress. The Master Clear signal will not abort a print cycle in progress.

2-25. PAPER INSTRUCTION SIGNAL. The Paper Instruction signal is derived from bit 15 of the computer output word (definition bit). When bit 15 is "0", the Paper Instruction signal is false and signifies that the interface output data register contains an ASCII coded character word. When bit 15 is "1", Paper Instruction is true and signifies that the output data register contains a format control word.

2-26. STROBE SIGNAL. The Strobe signal is caused by the computer executing an STC instruction addressed to the line printer interface. When true it causes the line printer to load the content of the output data register into its print line buffer. The strobe signal occurs once for every character or format control word transferred to the line printer.

2-27. CONTROL AND STATUS SIGNALS FROM LINE PRINTER.

2-28. Control and status signals transferred from the line printer to the interface are as follows:

a. Demand signal.
b. Buffer Ready signal
c. Ready signal.
d. On-Line signal.
e. VFU Channels 9 and 12.

2-29. Two of these signals (Demand and Buffer Ready) are used by the interface as control signals. All of them are made available to the computer program in the form of a status word as shown by figure 2-3. Status word bits are described by table 2-3.

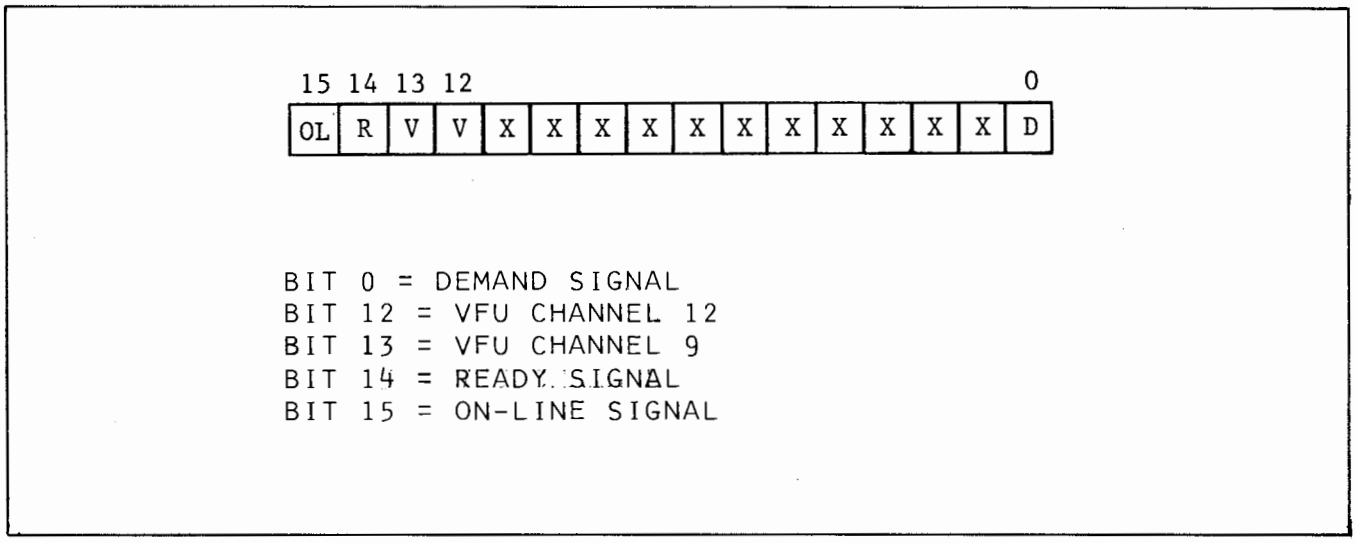


Figure 2-3. Status Word Format

Table 2-3. Status Word Description

BIT	LINE PRINTER MODEL	MEANING
0	2610A/2614A/2613A/ 2617A/2618A	"0"= line printer busy loading a character or printing a line.
		"1"= line printer is idle.
	2607A	"0"= line printer is busy loading a character.
		"1"= line printer is idle
12	2613A/2617A/2618A	"0"= VFU channel 12 ="0"
		"1"= VFU channel 12 ="1"
	2610A/2614A/2607A	NOT USED
13	2613A/2617A/2618A	"0"= VFU channel 9="0"
		"1"= VFU channel 9="1"
	2607A/2610A/2614A	NOT USED
14	ALL *	"1"= Not Ready
		"0"= Ready
15	ALL *	"1"= On-Line
		"0"= Not On-Line

* Refer to the appropriate line printer documentation for details

2-30. DEMAND SIGNAL. The Demand signal (in conjunction with the Buffer Ready signal) controls the state of status word bit 0 and triggers the interface flag logic. The Demand signal is false (status word bit 0 = "0") when the line printer is busy, and true (status word bit 0 = "1") when the line printer is idle. If the interface flag logic is enabled (cleared), the transition from busy to idle sets the flag logic (if Buffer Ready is true) which signals the computer program (or DMA) that another data word can be transferred. A transition from idle to busy terminates the Strobe signal.

2-31. BUFFER READY SIGNAL. The Buffer Ready signal also controls the state of bit 0 of the status word. Its purpose is to indicate when the line printer is performing a print operation and cannot accept data. The Buffer Ready signal is used by all Hewlett-Packard line printers except the HP 2607A.

2-32. The Buffer Ready signal is true and status word bit 0 is "1" (if Demand is also true) when the line printer is not performing a print operation. When the line printer is performing a print operation,Buffer Ready is false and status word bit 0 is "0". Because the HP 2607A Line Printer can accept characters while it is printing a line, it does not require a Buffer Ready signal. When operating with an HP 2607A Line Printer, the Buffer Ready line at the interface is always true.

2-33. READY SIGNAL. The Ready signal controls the state of status word bit 14. When Ready is true, status word bit 14 is "0"; when false bit 14 is "1". Refer to the line printer documentation for specific information regarding the line printer "ready" condition.

2-34. ON-LINE SIGNAL. The On-Line signal controls the state of status word bit 15. When the On-Line signal is true, bit 15 is "1"; when false, bit 15 is "0". Refer to the line printer documentation for specific information regarding the line printer "on-line" condition.

2-35. VFU CHANNELS 9 AND 12. The HP 2613A, 2617A, and 2618A Line Printers have the capability of sending back to the interface the content of the VFU tape channels 9 and 12. This allows the computer program to monitor the line printer position on the paper form.

2-36. Channel 9 of the VFU tape is punched by Hewlett-Packard to indicate "bottom of form". When the line printer is at "bottom of form" the VFU CH9 signal is true and bit 13 of the status word is a "1"; otherwise, VFU CH9 is false and bit 13 is "0".

2-37. Channel 12 of the VFU tape is blank and can be punched by the user for any special application. If one or more positions of channel 12 are punched and when the tape reaches a punched position, the VFU CH12 signal is true and status word bit 12 is "1"; otherwise, VFU CH12 is false and bit 12 is "0".

2-38. SAMPLE PROGRAM.

2-39. Table 2-4 is a sample program showing typical operation of the line printer interface. The program prints one line using skip-flag and one using interrupt. The program is not intended as a test program for the interface; it is simply an example of the assembly language requirements for status checking, transferring data, and commanding the operation of the line printer.

2-40. DIRECT MEMORY ACCESS OPERATION.

2-41. The HP 12845B Line Printer Interface is capable of operating under control of DMA (Direct Memory Access). This can be an advantage when interfacing high speed line printers such as the HP 2618A. Programming the operation of DMA is described in applicable DMA or computer manuals depending on the Hewlett-Packard model computer in use. The following are considerations required for operation of the line printer interface under control of DMA.

a. Set control. The DMA channel must be programmed during initialization to issue an STC signal to the interface during each DMA output cycle. This initiates a Strobe signal to the line printer

b. Strobe delay. During a DMA output operation, data is transferred and the Strobe signal is initiated during the same computer cycle. With the 2607A, 2610A, and 2614A Line Printers, this does not allow sufficient time for data to settle at the printer line buffer. To accomodate these line printers, jumper STR on the interface PCA must be in position 2. This delays the Strobe signal for one computer cycle. For DMA operations with other line printers and for all non-DMA operations, STR must be in position 1.

c. Set Flag instruction. After DMA is initialized, it is turned on by an STC (Set Control) instruction addressed to the DMA channel. Just prior to this, an STF (Set Flag) instruction must be issued to the line printer interface. This forces the interface to request service (SRQ signal) of DMA. For the remainder of the DMA data block transfer, Service Request is issued automatically each time the line printer becomes idle.

Table 2-4. Sample Program

```
0001                    ASMB,A,B,L
0002*
0003*
0004*
0005  00000                    ORG 0
0006  00011            CH      EQU 11B         PRINTER SELECT CODE
0007  00100                    ORG 100B
0008  00100 000000     START   NOP             START OF CALLING PROGRAM
0009*
0010*                       SKIP-FLAG MODE
0011*

0013  00101 014120             JSB INIT
0014  00102 160140     GETF    LDA BUFFC,I     SEND TEXT AND
0015  00103 014156             JSB OUTF          PRINT INSTRUCTION
0016  00104 034140             ISZ BUFFC
0017  00105 034142             ISZ COUNT
0018  00106 024102             JMP GETF
0019*
0020*                       INTERRUPT MODE
0021*
0022  00107 014120             JSB INIT
0023  00110 060143             LDA JMPI        GET TRAP CELL JUMP INSTRUCTION
0024  00111 070011             STA CH          STORE IN TRAP CELL
0025  00112 160140     GETI    LDA BUFFC,I     SEND TEXT AND
0026  00113 014145             JSB OUTI          PRINT INSTRUCTION
0027  00114 034140             ISZ BUFFC
0028  00115 034142             ISZ COUNT
0029  00116 024112             JMP GETI
0030  00117 024100             JMP START
0031*
0032*                       INITIALIZE BUFFER ACCESS
0033*
0034  00120 000000     INIT    NOP
0035  00121 060137             LDA BUFFS       INITIALIZE CURRENT
0036  00122 070140             STA BUFFC         BUFFER LOCATION
0037  00123 060141             LDA BUFFL       INITIALIZE BUFFER
0038  00124 003004             CMA,INA           LENGTH COUNTER
0039  00125 070142             STA COUNT
0040  00126 124120             JMP INIT,I      RETURN
0041*
0042*                       BUFFER, COUNTERS, AND CONSTANTS
0043*
0044  00127 020110     BUFF    ASC 7, H P   2 6 0 7
      00130 020120
      00131 020040
      00132 020062
      00133 020066
      00134 020060
      00135 020067
0045  00136 100001     PI      OCT 100001      PRINT INSTRUCTION
0046  00137 000127     BUFFS   DEF BUFF        BUFFER STARTING ADDRESS
0047  00140 000000     BUFFC   OCT 0           CURRENT BUFFER LOCATION
0048  00141 000010     BUFFL   DEC 8           BUFFER LENGTH
0049  00142 000000     COUNT   OCT 0
0050  00143 124144     JMPI    JMP *+1,I
```

Table 2-4. Sample Program (continued)

```
0051   00144 000154  JMPIL DEF OUTIC
0052*
0053*                      OUTPUT A-REGISTER VIA INTERRUPT MODE
0054*
0055   00145 000000  OUTI   NOP
0056   00146 014165         JSB RDY        CHECK PRINTER STATUS
0057   00147 102611         OTA CH         TRANSFER WORD
0058   00150 102100         STF 0          TURN ON INTERRUPT
0059   00151 103711         STC CH,C       SEND WORD
0060   00152 000000         NOP            DO SOMETHING
0061   00153 024152         JMP *-1          ELSE
0062   00154 103100  OUTIC  CLF 0          TRANSMISSION COMPLETED
0063   00155 124145         JMP OUTI,I     RETURN
0064*
0065*                      OUTPUT A-REGISTER VIA SKIP-FLAG MODE
0066*
0067   00156 000000  OUTF   NOP
0068   00157 014165         JSB RDY        CHECK PRINTER STATUS
0069   00160 102611         OTA CH         TRANSFER WORD
0070   00161 103711         STC CH,C       TRANSMIT WORD
0071   00162 102311         SFS CH         TRANSMISSION COMPLETED ?
0072   00163 024162         JMP *-1        NO
0073   00164 124156         JMP OUTF,I     EXIT
0074*
0075*                      CHECK LINE PRINTER STATUS, WAIT IF BUSY
0076*
0077   00165 000000  RDY    NOP
0078   00166 070201         STA RDY2       SAVE A-REGISTER
0079   00167 102511  RDY1   LIA CH         GET STATUS
0080   00170 002021         SSA,RSS        CHECK BIT 15
0081   00171 102001         HLT 01           NOT READY ACTION
0082   00172 002011         SLA,RSS        CHECK BIT 0
0083   00173 024167         JMP RDY1         BUSY ACTION
0084   00174 001200         RAL            CHECK
0085   00175 002020         SSA              BIT 14
0086   00176 102002         HLT 02           POWER-OFF ACTION
0087   00177 060201         LDA RDY2       RESTORE A-REGISTER
0088   00200 124165         JMP RDY,I      RETURN
0089   00201 000000  RDY2   OCT 0          SAVE A-REGISTER
0090                        END
**   NO ERRORS*
```

NOTE: The above program prints out one line of "HP 2607" via Skip-Flag, one line of "HP 2607" via interrupt, then loops back to start.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section provides a brief overall description of the line printer interface and a detailed description of the operation of the line printer interface functions.

3-3. OVERALL DESCRIPTION.

3-4. Figure 3-1 is a block diagram showing the relationship of the line printer interface to the computer and the line printer. The interface circuitry provides an output register, to transfer data from the computer to the line printer; control logic, to signal the line printer when data is available; flag logic, to signal the computer when more data can be sent; and input status buffers, to provide line printer status information to the computer. In addition, the line printer interface provides an auto-print feature which, for servicing purposes, allows the line printer to be operated independent of the computer. This feature is enabled by a switch on the line printer interface PCA.

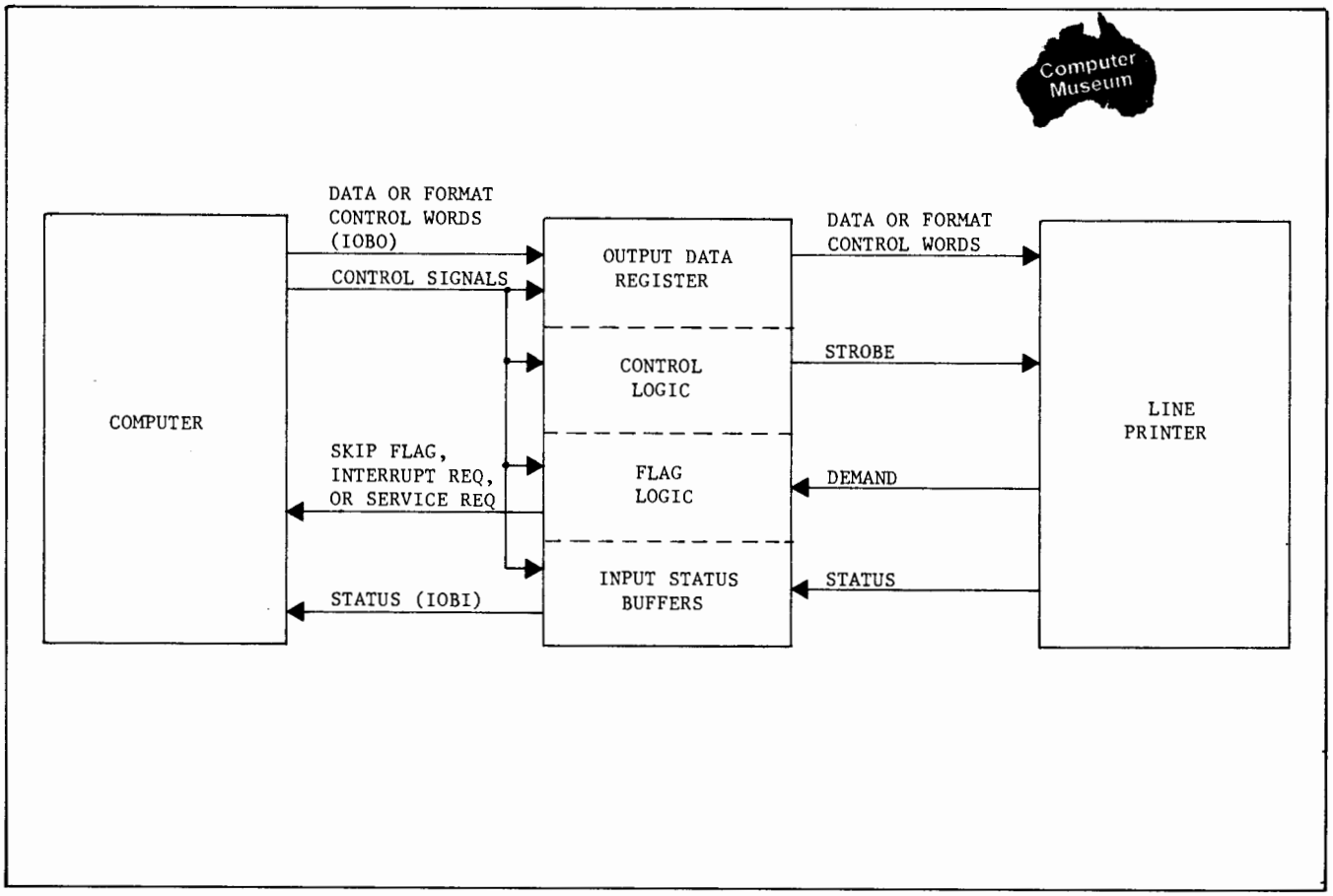


Figure 3-1. Simplified Block Diagram

3-5. Data is transferred from the computer to the interface in the form of 7-bit parrallel ASCII words. Each data word represents one character to be printed or one format control word. Programmed instructions executed by the computer cause a data or format control word to be put on the I/O output bus (IOBO) and provide control signals which cause the interface to load this word into its output register. Additional control signals from the computer set the interface control logic which in turn signals the line printer that a word is available. The line printer then accepts and stores the data word or executes the format control word.

3-6. When the line printer is ready for another word, it sets the interface flag logic initiating either a skip flag, interrupt request, or service request depending on the method programmed for data transfer.

3-7. Line printer status information is continuously available at the interface input status buffers. Control signals, again caused by programmed instructions, gate the status information onto the I/O input bus (IOBI) to be stored and evaluated by the computer.

3-8. DETAILED DESCRIPTION.

3-9. For the purpose of this discussion, the line printer interface is divided into the following functions:

a. Power-on and preset.
b. Select code detector.
c. Flag.
d. Control.
e. Interrupt request.
f. Service request.
g. Skip flag.
h. Output Register.
i. Input buffer.
j. Auto-print.

3-10. Figure 3-2 is a block diagram of the interface showing these functions and significant signals. The logic diagram for the interface is figure 4-2 in section IV of this manual.

3-11. POWER-ON AND PRESET.

3-12. The power-on and preset function establishes the initial operating conditions for the interface circuits. When computer power is turned on, signals CRS (Control Reset) and POPIO (Power On Preset I/O) are sent to the interface. The CRS signal clears the Control, Information Ready, and Printer FF's and, via the Master Clear one-shot, provides a five-microsecond Master Clear signal to the line printer. The POPIO signal clears the output data register and sets the Flag Buffer FF. At computer time T2, The Flag Buffer FF output gates the ENF (Enable Flag) signal to set the Flag FF. This is the initial operating state of the line printer interface. Signal CRS is also generated by the computer external preset function or by executing a CLC (Clear Control) instruction addressed to select code 00.

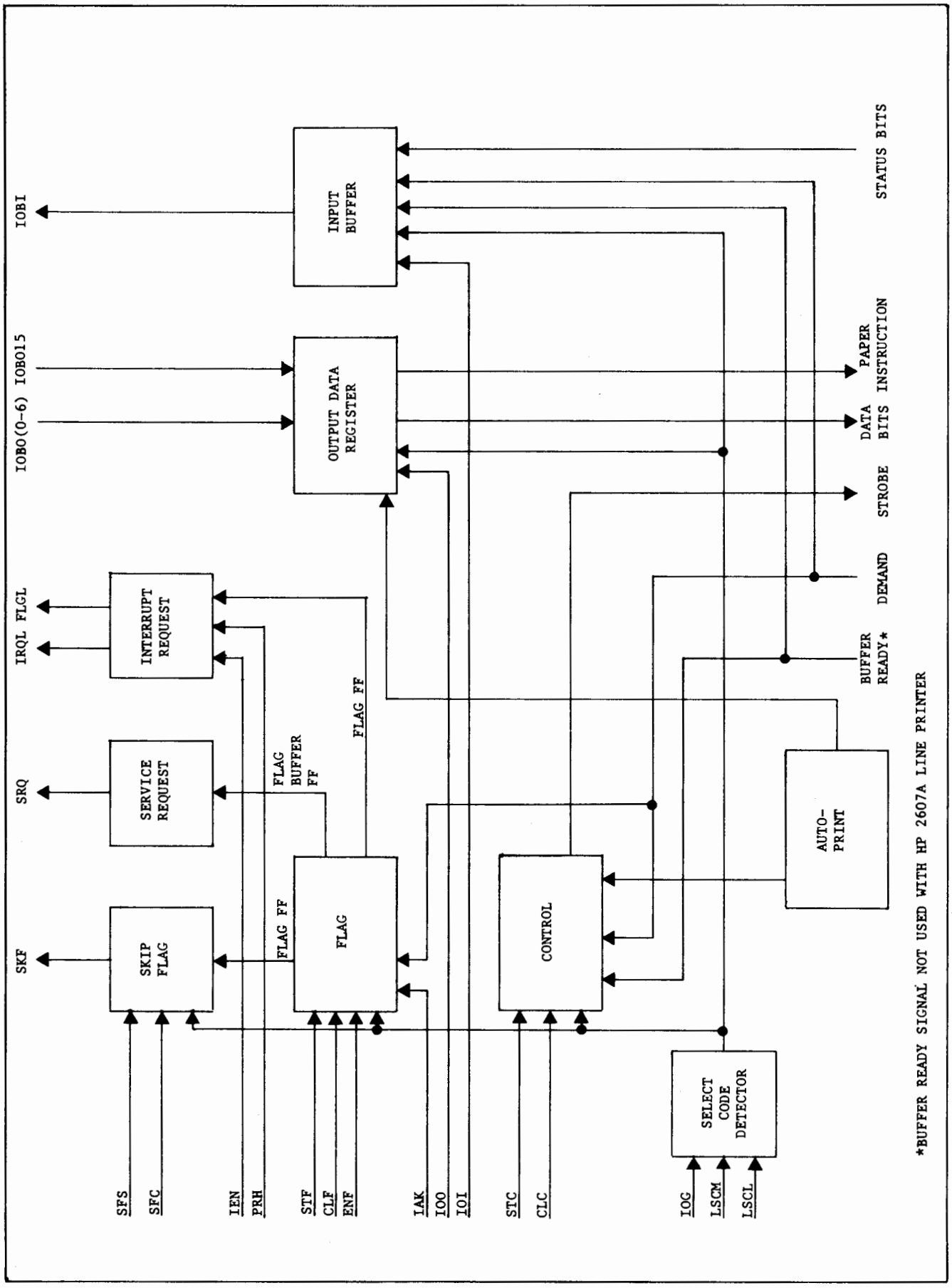


Figure 3-2. Functional Block Diagram

3-13. SELECT CODE DETECTOR.

3-14. The select code detector function allows the line printer interface to be exclusively addressed by computer instructions intended for the line printer. The select code number (address) of the line printer is dependent on the I/O PCA slot in which the interface is installed.

3-15. When a computer I/O group instruction is executed, a true IOG (Input/Output Group) signal is sent to all interface PCA's. If the instruction is addressed to the line printer interface, signals LSCM (Lower Select Code Most Significant) and LSCL (Lower Select Code Least Significant) at the interface are also true. The select code detector logically "ands" these signals to provide an enabling signal to the skip flag, flag, control, output register, and input buffer functions. All three signals (IOG, LSCM and LSCL) must be true for the interface to execute a programmed I/O instruction.

3-16. FLAG.

3-17. The flag function provides the initial indication to the computer that the interface is ready to accept data. This function consists of the Flag Buffer FF, the Flag FF, the Flag one-shot, and associated logic. The Flag Buffer FF is set by any one of three actions: during power-on or preset by the signal POPIO (paragraph 3-12); a programmed STF (set Flag) instruction addressed to the line printer interface by the signal STF; and by the output of the flag one-shot as described in the following paragraph.

3-18. When the line printer buffer is ready to accept a data word, signals Demand and Buffer Ready from the line printer are true. When these conditions are met (ie on the transition from "busy" to "idle") the Flag one-shot is triggered generating an 80-nanosecond pulse which, gated with the clear side output of the Flag FF, sets the Flag Buffer FF. If data transfers are under control of DMA (Direct memory access), the output of the Flag Buffer FF is sent to the DMA circuits as an SRQ (Service Request) signal.

3-19. At the next computer time T2, the Flag Buffer FF output gates signal ENF to set the Flag FF. The Flag FF output is used by the skip flag function or interrupt function to inform the computer that a data transfer is in order.

3-20. Both the Flag Buffer FF and the Flag FF are cleared by a programmed CLF (Clear Flag) instruction addressed to the line printer interface. When operating under control of DMA, the DMA circuits provide the CLF signal. The Flag Buffer FF is also cleared by an IAK (Interrupt Acknowledge) signal from the computer as described in paragraph 3-30.

3-21. CONTROL.

3-22. The control function provides signals to the line printer to indicate that data is in the output register and ready for transfer. The control function consists of the Control FF, the Information Ready FF, the Control one-shot, The Strobe Delay FF's and associated logic.

3-23. Both the Control and Information Ready FF's are set by a programmed STC (Set Control) instruction addressed to the line printer interface. When the Control FF is set, the output provides one condition for enabling the interrupt function (paragraph 3-26). The Control FF remains set until a programmed CLC (Clear Control) instruction addressed to the line printer interface is executed or a CRS signal is issued as described in paragraph 3-12.

3-24. The output of the Information Ready FF, when set, puts a high on the set input of the Strobe Delay 1 FF. At the end of the next computer cycle time T5, the trailing edge of signal SIR clocks the Strobe Delay 1 FF to the set state. If the jumper STR is in position 1, the output of the Strobe Delay 1 FF provides a Strobe signal to the line printer. One computer cycle later, again at the end of T5, the trailing edge of signal SIR clocks the Strobe Delay 2 FF to the set state. This provides a one-cycle delayed Strobe signal with jumper STR in position 2. This delay is required when operating HP 2607A, 2610A, and 2614A Line Printers under control of DMA. For all other operations, jumper STR should be in position 1.

3-25. When the line printer receives a Strobe signal, its Demand signal goes false indicating that it is busy. The negative-going Demand signal triggers the Control one-shot. After 80 nanoseconds the Control one-shot clears the Information Ready FF. The output of the Information Ready FF clears the Strobe Delay 1 and Strobe Delay 2 FF's removing the Strobe signal from the line printer.

3-26. INTERRUPT REQUEST.

3-27. The interrupt request function coupled with the computer interrupt logic allows the line printer interface to interrupt and direct the computer processor to a subroutine written to provide data to the line printer. The interrupt request function consists of the IRQ (Interrupt Request) FF and associated logic.

3-28. For the line printer interface to request an interrupt, the Control FF (paragraph 3-23), Flag Buffer FF, and Flag FF (paragraph 3-17) must be set and the IEN (Interrupt Enable) signal must be true. Signal IEN is true as a result of enabling the computer interrupt logic with an STF instruction addressed to select code 00. In addition, there must be no higher priority interface currently requesting an interrupt.

3-29. The set-side outputs of the Control and Flag FF's are gated with the IEN signal (U42C). The resulting signal forces signal PRL (Priority Low) false. This prevents any lower priority interfaces from generating an interrupt request. This condition remains until the Flag FF is cleared by a CLF instruction. The output of U42C gates signal SIR (U34C) to provide an input to "nand" gate U44A. If no higher priority interrupts are in progress, signal PRH (Priority High) will be true. This along with the set-side output of the Flag Buffer FF allows the gated SIR signal to set the IRQ FF. The IRQ FF generates true FLGL (Flag Low) and IRQL (Interrupt Request Low) signals which cause the computer to initiate an interrupt phase.

3-30. At the next time T2, an ENF signal clears the IRQ FF. If PRH is still true at T5, the IRQ FF again sets. FLGL and IRQL signals are sent to the computer where this time they indicate the address (select code) of the line printer interface. This address is used by the computer to fetch

and execute the contect of the line printer interface trap cell (usually a JSB instruction). The computer returns an IAK (Interrupt Acknowledge) signal during the first time period of the interrupt phase which clears the Flag Buffer FF.

3-31. At T2 during the interrupt phase signal ENF again clears the IRQ FF. The computer now fetches and executes the interrupt subroutine for the line printer. One of the last instructions in the subroutine is a CLF addressed to the line printer clearing the Flag FF. This allows signal PRL to go high, enabling lower priority interrupts, and resets the flag function so that the interface can again interrupt when the line printer is ready for more data.

3-32. SERVICE REQUEST.

3-33. The service request function is used when the interface is operating under control of DMA. The service request function consists of the SRQ signal which is the buffered set-side output of the Flag Buffer FF. If DMA is initialized to expect an SRQ from the line printer interface, a DMA cycle is initiated. The DMA circuits "freeze" the operation of the processor for one cycle and provide the control signals required for transfer of data to the interface. The Flag and IRQ FF's on the interface set as usual and are cleared by a CLF signal issued by DMA at time T3 during the DMA cycle. Additional information on DMA operation is provided in the computer installation and maintenance manual.

3-34. SKIP FLAG.

3-35. The skip flag function allows the computer program to test the state (set or clear) of the Flag FF and respond accordingly. The function generates an SKF (Skip Flag) signal depending on the state of the Flag FF. A programmed SFS (Skip If Flag Set) instruction addressed to the line printer interface results in a true SKF signal if the Flag FF is set. A programmed SFC (Skip If Flag Clear) instruction addressed to the line printer interface results in a true SKF signal if the Flag FF is clear. The SKF signal causes the computer to skip the instruction following the SFS or SFC instruction. This method of operation requires that the computer interrupt system be disabled by a CLF instruction addressed to select code 00.

3-36. OUTPUT REGISTER.

3-37. The output register function provides one-word storage for character and format control words transferred to the line printer. It consists of two 4-bit registers and eight differential line drivers. Data inputs to the register are bits 0 through 6 and bit 15 of the computer I/O output bus (IOBO0 throught IOBO6 and IOBO15). When sent to the line printer, I/O output bits 0 through 6 become Data Bits 0 through 6 and I/O output bit 15 becomes the Paper Instruction signal. The Paper Instruction signal when true, signifies that the data bits are a format control word.

3-38. An OTA (Output From A-Register) instruction, OTB (Output From B-Register) instruction or a DMA output cycle addressed to the line printer interface results in a true IOO (I/O Output) signal the trailing edge of which, when gated by the select code detector, clocks the I/O output bus bits into the output register. The output of this register is immediately available, via the differential line drivers, on the Paper Instruction and Data Bit lines.

The line printer accepts this output when it receives a Strobe signal as described in paragraph 3-24. The output data register is cleared by a POPIO signal (paragraph 3-12) and by the auto-print function when in the test mode.

3-39. INPUT BUFFER.

3-40. The input buffer function allows the computer to read the status of the line printer when programmed to do so. It consists of eight differential receivers and seven gated buffers. The input buffer provides a status word to the I/O input bus (IOBI) as follows:

a. IOBO 0. Logical "and" of line printer Demand and Buffer Ready signals. (HP2607A Line Printer provides Demand signal only.)

b. IOBI 1 through IOBI 11. Not used.

c. IOBI 12 and IOBI 13. Vertical format unit (VFU) tape channels 12 and 9 respectively for line printers having VFU readback capability.

d. IOBI 14. Line printer Ready signal.

e. IOBI 15. Line printer On Line signal.

3-41. An LIA (Load Into A-Register) instruction, LIB (Load Into B-Register) instruction, or a DMA input cycle addressed to the line printer interface results in a true IOI signal which, when gated by the select code detector, enables the status word to the I/O input bus.

3-42. TIMING.

3-43. Figure 3-3 shows the signal sequence between the interface and the line printer during normal operation. The signals shown are not drawn to scale. It is important to realize that signals from the interface to the line printer (ie Data Bits 0-6 and Strobe) are the result of the computer executing programmed I/O instructions and the exact timing is controlled by the computer and the computer program.

3-44. AUTO-PRINT.

3-45. Auto-print is a service function which allows the line printer to be operated by the interface without intervention from the computer. This function consists of the Printer FF, the Printer Control one-shot, the state register (U28A and U28B), and associated logic. Auto-printing is enabled by pressing the computer External Preset switch and putting switch S1 in the TEST position.

3-46. The operation of the auto-print function has four states which, in terms of the state register, are defined as follows:

a. State 0. Flip-flops U28A and U28B cleared.
b. State 1. Flip-flops U28A set and U28B cleared.
c. State 2. Flip-flops U28A cleared and U28B set.
d. State 3. Flip-flops U28A and U28B set.

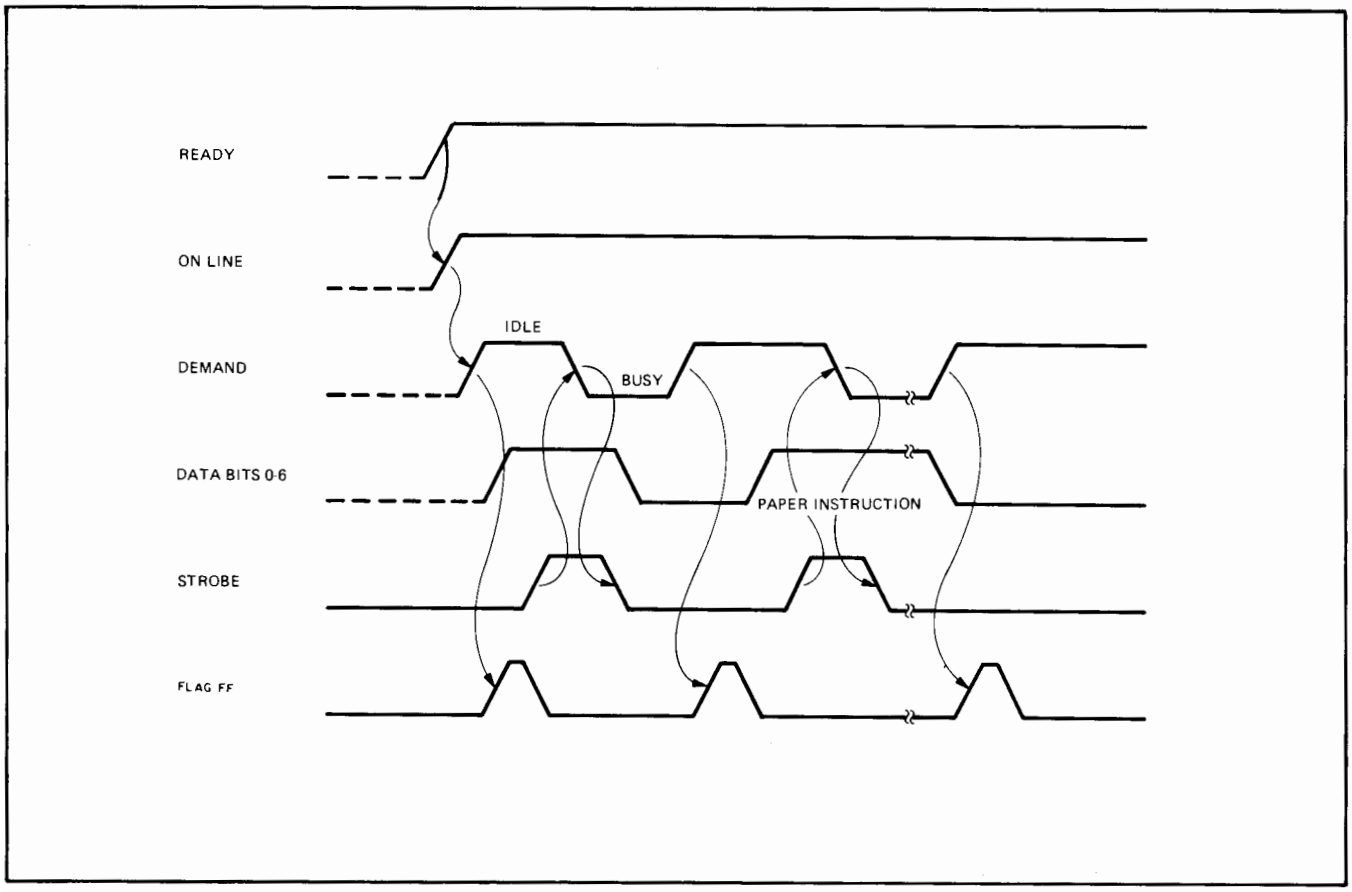


Figure 3-3. Timing Diagram

3-47. Initially, with switch S1 in the NORMAL position, the state register is held in state 0 and the auto-print function is disabled. When S1 is put in the TEST position, the Control one-shot is triggered. The output of the Control one-shot clocks the state register to state 1 which triggers the Flag one-shot. Switch S1, in TEST, also clears and holds clear the output data register and enables "nand" gate U37A.

3-48. In state 1, the output of the state register puts the ASCII code for the character "H" on the Data Bit lines. The output of the Flag one-shot, gated through U37A, sets the Information Ready FF which, via the Strobe Delay FF's,generates a Strobe signal to the line printer (paragraph 3-24). The line printer returns a false Demand signal indicating that it is busy and loads the character into its buffer. The Demand signal going false triggers the Control one-shot which clears the Information Ready FF and clocks the state register to state 2. The Information Ready FF direct clears the Strobe FF's causing the Strobe signal to go false.

3-49. In state 2, the output of the state register forces a true Paper Instruction signal and places the format control code for "advance one line" on the Data Bit lines. When the line printer returns a true Demand signal, the Flag one-shot is triggered, again setting the Information Ready FF and, via the Strobe Delay FF's. generating a true Strobe signal. The line printer then reads the Paper Instruction signal and the format control word initiates printing of the first line (single character "H" loaded during state 1), forces the Demand signal false, and, on all line printers except the HP 2607A, forces the Buffer Ready signal false.

3-50. At this point, the operation of the auto-print function with an HP 2607A Line Printer is different from other HP line printers. The following paragraphs describe operation with all line printers except the HP 2607A which is described by paragraphs 3-54 through 3-57.

3-51. The false Demand signal transition triggers the Control one-shot which clears the Information Ready FF and clocks the state register to state 3. The Information Ready FF clears the Strobe FF's causing the Strobe signal to go false. The false Buffer Ready signal from the line printer sets the Printer FF. The Printer FF when set, identifies the line printer as one that requires a Paper Instruction signal to print a line of characters. (The HP 2607A does not require a Paper Instruction signal as it automatically prints a line when its buffer is full.) Also, when the Printer FF is set, the ASCII character on the Data Bit lines becomes an "E".

3-52. When the line printer has completed printing the first line (paragraph 3-49), Its Demand and Buffer Ready signals become true. The true Demand signal transition triggers the Flag one-shot which sets the Information Ready FF and, via the Strobe Delay FF's, generates a true Strobe signal. The line printer then forces the Demand signal false and loads the character "E" into its buffer. The false Demand signal transition triggers the Control one-shot clearing the Information Ready FF (which clears the Strobe Delay FF's) and clocking the state register to state 1.

3-53. The action of the state register going from state 3 to state 1 triggers the Printer Control one-shot. This one-shot generates a 950-microsecond pulse which, for the duration, prevents any further changes in the state register. During this time the printer, via Demand and Strobe signals, fills its buffer with character "E's". When the Printer Control one-shot runs down, the state register is clocked to state 2 which clears the Printer FF and outputs a format control word and a Paper Instruction signal (paragraph 3-49). The state register then advances to state 3, sets the Printer FF (because the Buffer Ready signal is false), and waits for the line printer to print the content of its buffer. When this is done, the operation continues as described beginning with paragraph 3-52. The auto-print function remains in this loop until S1 is returned to the NORMAL position.

3-54. AUTO-PRINT WITH THE HP 2607A LINE PRINTER

3-55. As stated in paragraph 3-50, the operation of the auto-print function is somewhat different when using an HP 2607A Line Printer. This difference is caused primarily because the HP 2607A is "double buffered" and does not require a Buffer Ready signal. The signal line at the interface reserved for Buffer Ready will remain true at all times when operating an HP 2607A Line Printer.

3-56. The action described up to paragraph 3-51 is the same for the HP 2607A. At this point a single character "H" has been passed to the line printer and the line printer has been commanded to print that character as the first printed line. The resulting false Demand signal transition triggers the Control one-shot which clears the Information Ready FF and clocks the state register to state 3. The Buffer Ready line remains true, therefore the Printer FF will not set. The Data Bit lines continue to carry the ASCII character "H".

3-57. Since the Printer FF does not set, the state register cannot advance to state 1 and trigger the Printer Control one-shot; in fact, the state register remains in state 3 as long as S1 is in the TEST position. Through use of Demand and Strobe signals, the line printer continues to receive ASCII character "H's" and simply prints a line and single spaces automatically when its buffer is full.

SECTION IV

MAINTANANCE

4-1 INSTRODUCTION.

4-2. This section provides maintenance information for HP 12845B Line Printer Interface Kit. Included is an interconnecting cable wire list, integrated circuit descriptions and diagrams, schematic and parts location diagrams, and a replaceable parts list.

4-3. PREVENTIVE MAINTENANCE.

4-4. Detailed preventive maintenance procedures and schedules are given in the computer system documentation. There are no seperate preventive maintenance schedules for the line printer interface kit; however, it is good practice to remove dust and visually inspect the interface PCA and cable for damage whenever the interface PCA is removed from the computer.

4-5. TROUBLESHOOTING.

4-6. Troubleshooting the interface kit is accomplished by performing the tests in the diagnostic program and analyzing the errors that occur as the test is being run. Continuity checks of the interface cable can be made using table 4-1. To isolate troubles to a replaceable component, refer to the integrated circuit descriptions and diagrams (figure 4-1), the schematic and parts location diagrams (figure 4-2), and the replaceable parts list (table 4-2).

4-7. DIAGNOSTICS.

4-8. Diagnostic programs for the line printer interface are tailored to the particular model line printer used with the interface. These diagnostics test line printer functions as well as interface functions. For instructions on running the diagnostic tests, refer to the appropriate diagnostic operating procedure contained in the *Manual of Diagnostics* (MOD).

4-9. AUTO-PRINT.

4-10. The HP 12845B Line Printer Interface Kit provides an auto-print feature that is useful primarily to test the operation of the line printer. To enable the auto-print function, press EXTERNAL PRESET then put switch S1 (on the interface PCA) in the TEST position. The TEST position is the position closest to the center of the interface PCA. When enabled, the auto-print function will cause the line printer to print 132-column lines of the character "E" ("H" on the HP 2607A Line Printer).

4-11. For troubles within the auto-print function, a test point (TP1 on the parts location and schematic diagrams) is provided. An externally generated series of pulses applied to TP1 will alternately switch the auto-print function on and off allowing the operation of the auto-print circuitry to be observed with an oscilloscope or logic probe. The external pulse applied to TP1 should be a +5 volt pulse with a duration of approximately 2 milliseconds. Switch S1 must be in the TEST position.

4-12. REPLACEABLE PARTS.

4-13. Table 4-2 lists the replaceable parts for the HP 12845B Line Printer Interface Kit. Components located on the interface PCA are listed by reference designation.

4-14. When ordering replacement parts from Hewlett-Packard, address the order to the nearest HP Sales and Service Office (listed at the back of this manual) and specify the following information for each part ordered:

a. Identification of instrument, kit or assembly containing the part.

b. Hewlett-Packard part number for each part.

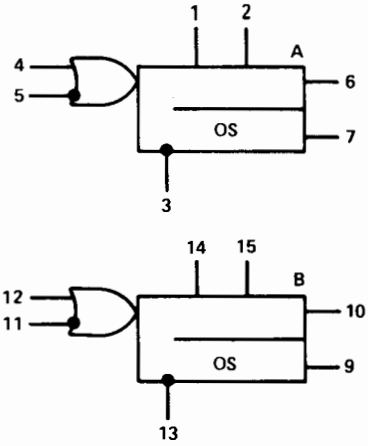
c. Description of each part.

d. Circuit reference designation for each part (if applicable).

Table 4-1. Cable Assembly Signal Index

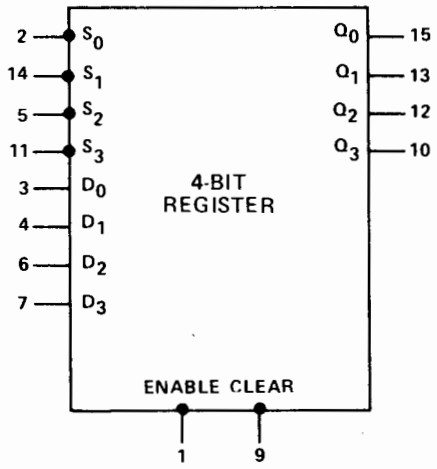
J1/P1	SIGNAL		P2
1A	(BRN)	PAPER INSTRUCTION	a
1B	(WHT)	$\overline{\text{PAPER INSTRUCTION}}$	b
10A	(RED)	DATA BIT 6	U
10B	(WHT)	$\overline{\text{DATA BIT 6}}$	V
11A	(ORN)	DATA BIT 5	S
11B	(WHT)	$\overline{\text{DATA BIT 5}}$	T
12A	(YEL)	DATA BIT 4	P
12B	(WHT)	$\overline{\text{DATA BIT 4}}$	R
13A	(GRN)	DATA BIT 3	M
13B	(WHT)	$\overline{\text{DATA BIT 3}}$	N
14A	(BLU)	DATA BIT 2	K
14B	(WHT)	$\overline{\text{DATA BIT 2}}$	L
15A	(VIO)	DATA BIT 1	H
15B	(WHT)	$\overline{\text{DATA BIT 1}}$	J
16A	(GRA)	DATA BIT 0	E
16B	(WHT)	$\overline{\text{DATA BIT 0}}$	F
21A	(WHT/BLK)	MASTER CLEAR	p
21B	(WHT)	$\overline{\text{MASTER CLEAR}}$	n
24A	(WHT/BRN)	STROBE	B
24B	(WHT)	$\overline{\text{STROBE}}$	A
26A	(WHT/BRN)	ON LINE	j
26B	(WHT)	$\overline{\text{ON LINE}}$	h
27A	(WHT/ORN)	$\overline{\text{READY}}$	s
27B	(WHT)	READY	r
28A	(WHT/YEL)	VFU CH9	v
28B	(WHT)	$\overline{\text{VFU CH9}}$	w
29A	(WHT/GRN)	VFU CH12	u
29B	(WHT)	$\overline{\text{VFU CH12}}$	t
30A	(WHT/GRA)	Spare	NC
30B	(WHT)	Spare	NC
31A	(WHT/BLK/BRN)	Spare	NC
31B	(WHT)	Spare	NC
48A	(WHT/BLU)	$\overline{\text{BUFFER READY}}$	k
48B	(WHT)	BUFFER READY	m
49A	(WHT/VIO)	$\overline{\text{DEMAND}}$	D
49B	(WHT)	DEMAND	C
50A	(BLK)	Common	x
50B	(WHT)	Common	x

1820-0515



When either input condition is met the one-shot will generate an output pulse. The pulse width is determined by an external RC network. The circuit may be initialized by a low clear input.

1820-0626

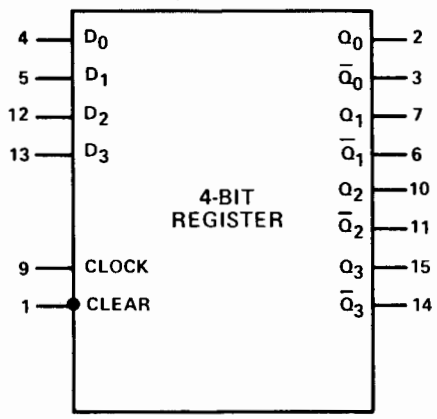


A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using the S input lines.

If the D inputs are used the S inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

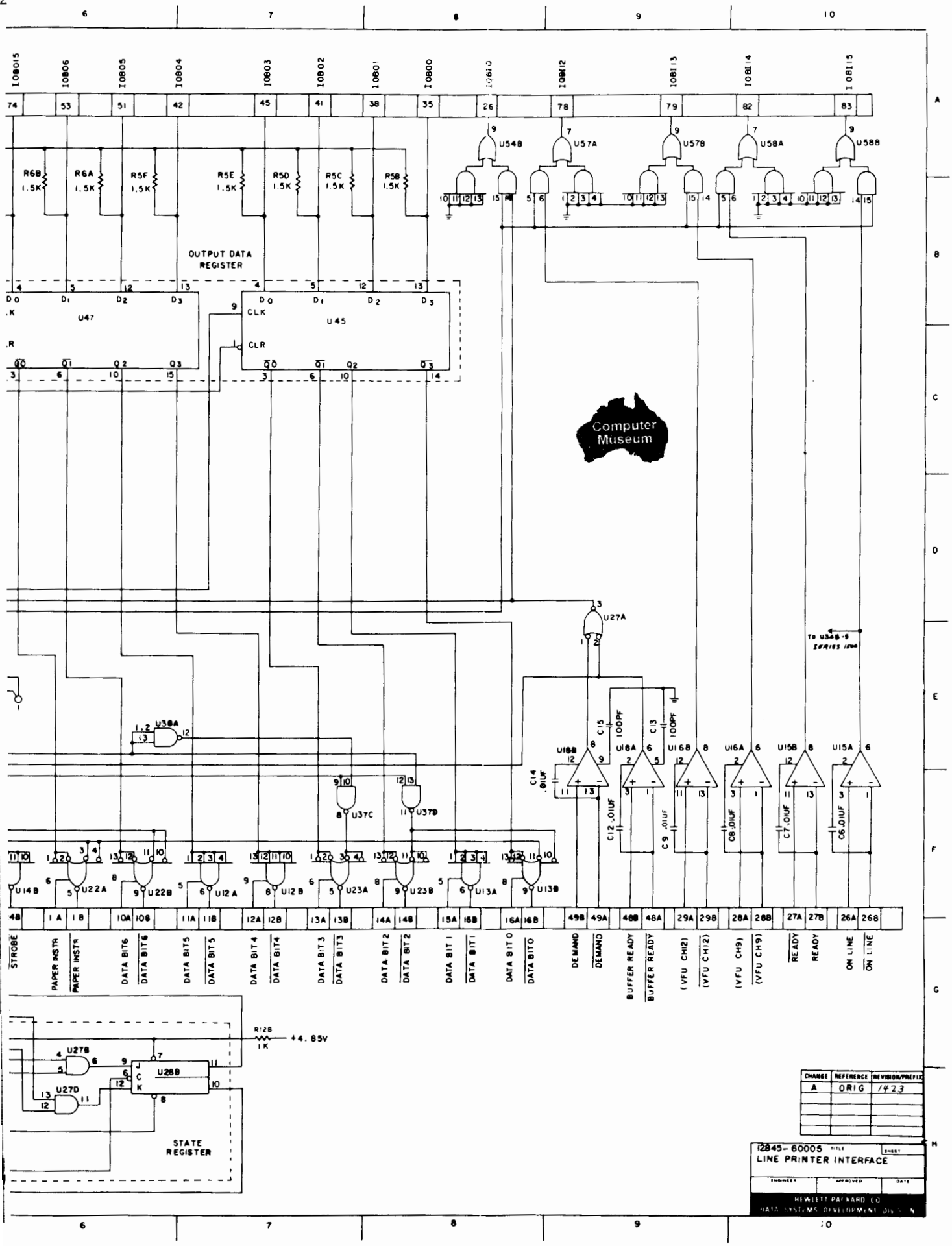
If the S inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the S line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and S modes of operation.

1820-0839



Data on the input lines (D_0 - D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

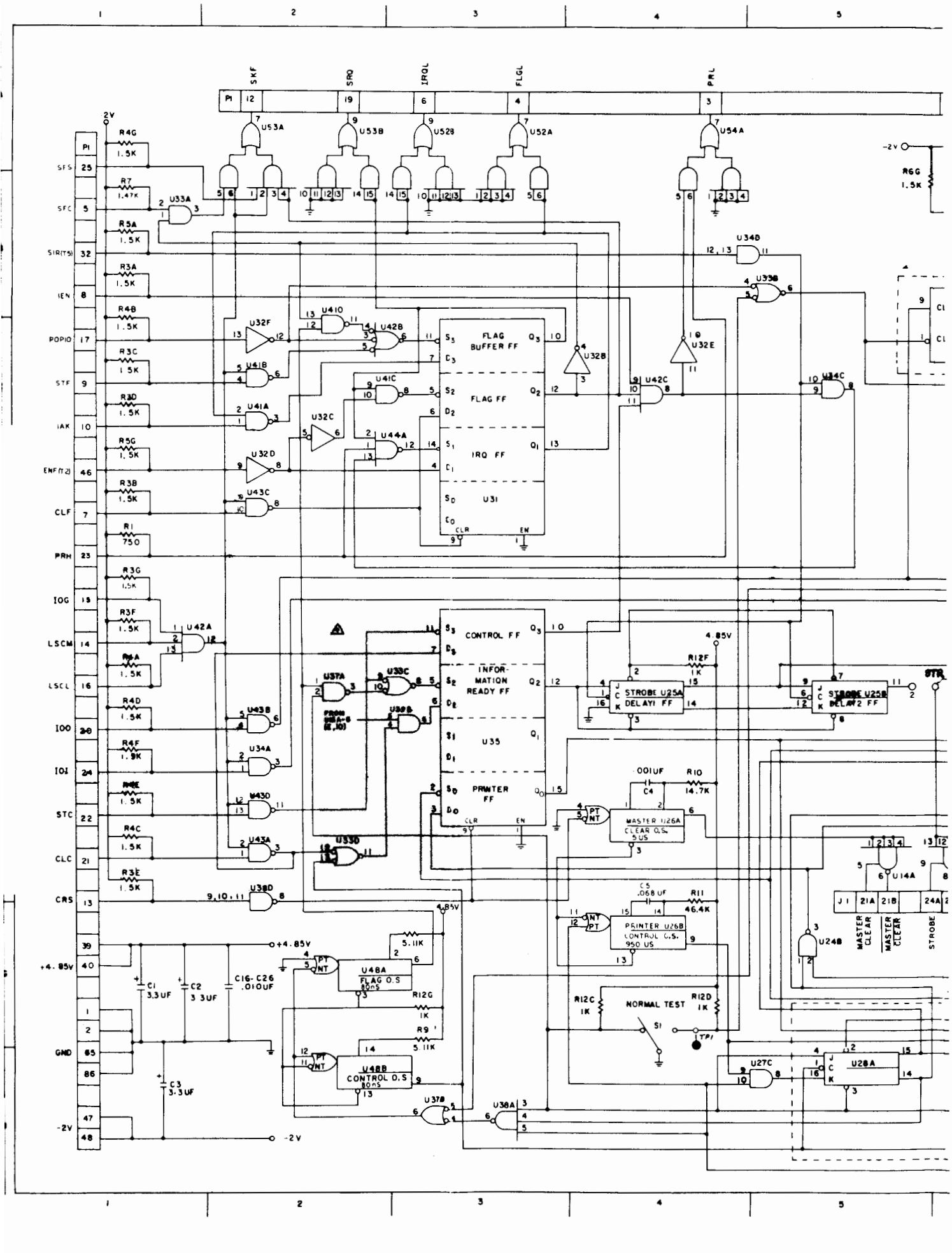
Figure 4-1. Integrated Circuit Descriptions and Diagrams

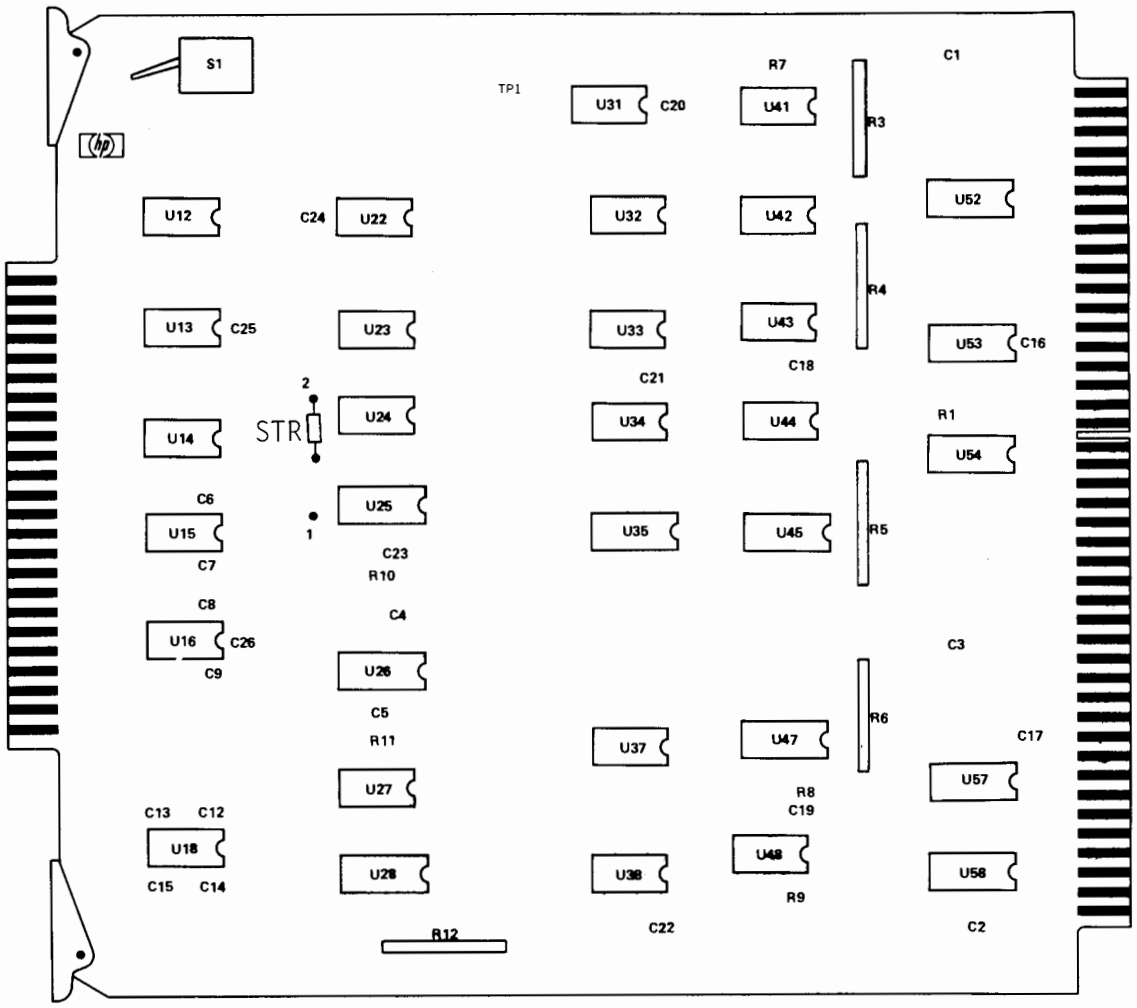


CHANGE	REFERENCE	REVISION/PREFIX
A	ORIG	/423

12845-60005 TITLE
LINE PRINTER INTERFACE
SHEET
ENGINEER | APPROVED | DATE
HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

Figure 4-2. Parts Location and Schematic Diagrams

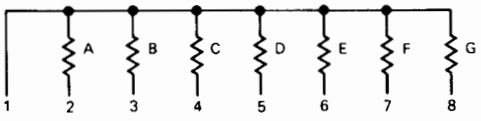

SKF
SRQ
IRQL
FLGL
PRL
U53A
U53B
U52B
U52A
U54A
R4G 1.5K
R7 1.47K
R5A 1.5K
R3A 1.5K
R4B 1.5K
R3C 1.5K
R3D 1.5K
R5G 1.5K
R3B 1.5K
R1 750
R3G 1.5K
R3F 1.5K
R4A 1.5K
R4D 1.5K
R4F 1.5K
R4E 1.5K
R4C 1.5K
R3E 1.5K
R6G 1.5K
SFS
SFC
SIR(TS)
IEN
POPIO
STF
IAK
ENF(T2)
CLF
PRH
IOG
LSCM
LSCL
IOO
IOI
STC
CLC
CRS
+4.85V
GND
-2V
FLAG BUFFER FF
FLAG FF
IRQ FF
U31
CONTROL FF
INFOR-MATION READY FF
U35
PRNTER FF
CLR
EN
U32F
U32C
U32D
U32E
U32B
U41C
U41A
U41B
U42B
U44A
U43C
U42A
U43B
U34A
U43D
U43A
U33D
U38D
U37A
U33C
U38B
U34B
U33B
U34C
U42C
STROBE U25A DELAY1 FF
STROBE U25B DELAY2 FF
MASTER U26A CLEAR O.S. 5 US
PRINTER U26B CONTROL O.S. 950 US
U48A FLAG O.S 80 NS
U48B CONTROL O.S 80 NS
NORMAL TEST
U14A
U24B
U27C
U28A
MASTER CLEAR
MASTER CLEAR
STROBE
C1 3.3 UF
C2 3.3 UF
C3 3.3 UF
C16-C26 .01 UF
C4 .001 UF
C5 .068 UF
R10 14.7K
R11 46.4K
R12C 1K
R12D 1K
R12F 1K
R12G 1K
R9 5.11K
5.11K
4.85V
-2V
TP1
S1



NOTES:

1. ALL RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN UF UNLESS OTHERWISE SPECIFIED.

2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS:



3. JUMPER STR:
   POSITION 1. DMA OPERATIONS WITH HP 2613A, 2617A, AND 2618A AND ALL NON-DMA OPERATION.
   POSITION 2. DMA OPERATIONS WITH HP 2607A, 2610A, AND 2614A.

4. SHADED AREA SHOWN BELOW FOR SERIES 1423 PCA.

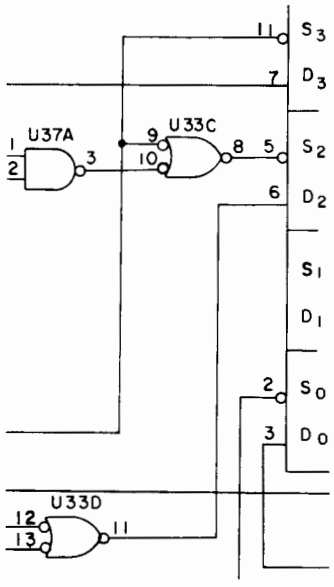


Table 4-2. Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION
C1 thru 3	0180-0210	CAPACITOR, fxd, elect, 3.3uF, 15 Vdcw
C4	0160-3456	CAPACITOR, fxd, cer, 1000 pF
C5	0160-0166	CAPACITOR, fxd, mylar, .068 uF
C6 thru 9, 12, 14, 16 thru 26	0160-2055	CAPACITOR, fxd, cer, .01 uF
R1, 7	0757-0420	RESISTOR, fxd, 750 ohms, 1%, .125W
R3 thru 6	1810-0020	RESISTOR NETWORK, 1.5k ohms, 5%, (7 resistors)
R8, 9	0757-0438	RESISTOR, fxd, 5.11k ohms, 1%, .125W
R10	0698-3156	RESISTOR, fxd, 14.7k ohms, 1%, .125W
R11	0698-3162	RESISTOR, fxd, 46.4k ohms, 1%, .125W
R12	1810-0030	RESISTOR NETWORK, 1k ohms, 5%, (7 resistors)
S1	3101-1213	SWITCH, toggle, DPST
U12 thru 14, 22, 23	1820-0720	INTEGRATED CIRCUIT
U15 thru 16, 18	1820-0721	INTEGRATED CIRCUIT
U24, 37, 41, 43	1820-0054	INTEGRATED CIRCUIT
U25, 28	1820-0715	INTEGRATED CIRCUIT
U26, 48	1820-0515	INTEGRATED CIRCUIT
U27, 33	1820-0511	INTEGRATED CIRCUIT
U31, 35	1820-0626	INTEGRATED CIRCUIT
U32	1820-0174	INTEGRATED CIRCUIT
U34	1820-0141	INTEGRATED CIRCUIT
U38, 44	1820-0068	INTEGRATED CIRCUIT
U42	1820-0372	INTEGRATED CIRCUIT
U45, 47	1820-0839	INTEGRATED CIRCUIT
U52, 53, 54, 57, 58	1820-1080	INTEGRATED CIRCUIT
	12845-60005	LINE PRINTER INTERFACE PCA
	12845-60006	CABLE ASSEMBLY
	12845-90011	OPERATING AND SERVICE MANUAL

HEWLETT hp PACKARD

MANUAL PART NO. 12845-90011
MICROFICHE PART NO. 12845-90012

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