

HP 12821A DISC INTERFACE



Installation and Service Manual

Card Assembly: 12821-60003
Date Codes: A-2323
 A-2424
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12821-90006

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SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

CAUTION

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a **CAUTION** sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged), while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000

volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and ultimate use. Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

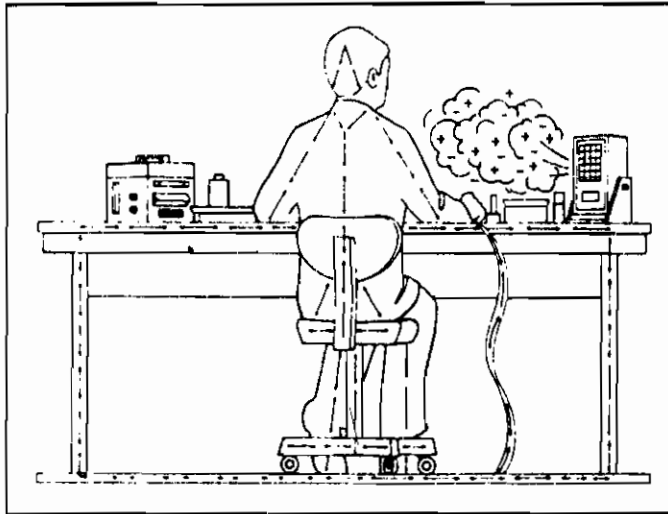
1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by 3M Company. Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top,

wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninteruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

This manual provides installation and service instructions for the HP 12821A Disc Interface (DI) Card. The 12821A card is used to interface H-Series and CS80-Series disc drives to the HP 1000 M/E/F-Series computers. In such applications these computers are running under the HP 92068A RTE-IVB operating system (using disc driver DVA32) or the HP 92084A RTE-6/VM operating system (using disc driver DVM/DVN33).

Other publications which should be available for reference when using this manual for the following purposes are:

GENERAL

1. Disc Loader ROM Installation and Service Manual, HP Part Number 12992-90001.
2. DVR/DVA 32 Reference Manual, HP Part Number 92068-90012 for H-Series disc drives.
3. DVM/DVN 33 Reference Manual, HP Part Number 92084-90025 for CS80 Series disc drives.

DIAGNOSTICS

1. 12821-90002, Diagnostic Reference Manual.
2. 91711B, Diagnostics and Verification Package, which includes the following:
 - * Diagnostics and Verification Reference Manual, HP Part Number 91711-90006 for System Processor, I/O Cards and Peripherals.
 - * Integrated Controller Disc Utilities Reference Manual, HP Part Number 5955-4355 for H-Series disc drives.
 - * CS80 External Exerciser Reference Manual, HP Part Number 5955-3462, for CS80-Series disc drives.

TABLE OF CONTENTS

SAFETY	iii
PREFACE	v
GLOSSARY	ix
1. INTRODUCTION	
1.1 Description	1-1
1.2 Multi-Disc Configurations	1-1
1.3 Interconnection Disc Cabling	1-1
1.4 Product Contents	1-2
1.5 Related Items	1-3
1.6 Identification	1-3
1.6.1 Product	1-3
1.6.2 Circuit Card	1-3
1.7 Power and Environmental Requirements	1-4
1.8 Operation	1-4
1.9 Functional Description	1-6
1.10 Output Modes	1-7
1.10.1 Data Mode (Control Flip-Flop Set)	1-7
1.10.2 Configure Mode (Control Flip-Flop Clear)	1-8
1.11 Input Modes	1-10
1.11.1 Data Mode (Control Flip-Flop Set)	1-10
1.11.2 Status Mode (Control Flip-Flop Clear)	1-10
1.12 Master Reset	1-12
1.12.1 Master Reset Functions	1-12
1.12.2 Rules Concerning MR	1-12
2. INSTALLATION	
2.1 General	2-1
2.2 Unpacking and Inspection	2-1
2.3 Checkout	2-1
2.4 Storage and Reshipment	2-1
2.5 System Controller Address DIP Switch Block	2-2
2.5.1 Setting the SRQ Control Jumper	2-2
2.6 Installation	2-3
2.7 Interconnecting Cables	2-4
2.8 System or Subsystem Checkout	2-4
3. PRINCIPLES OF OPERATION	
3.1 Introduction	3-1
3.2 Signal Names and Locations	3-1
3.3 Channel Select Logic	3-1

3.4	Control Logic	3-1
3.4.1	Control Flip-Flop and Logic	3-1
3.4.2	Control Word Register	3-2
3.4.3	Bus Transceivers and Control Line Logic	3-2
3.5	Output Data Register	3-3
3.6	Input Byte Select Logic	3-3
3.7	Input Data Select	3-3
3.8	The FIFOs	3-3
3.8.1	Introduction	3-4
3.8.2	The FIFO Buffer Memory	3-4
3.8.3	The DI FIFO Buffers	3-5
3.9	Output Byte Select Logic	3-6
3.10	Output Data Select	3-7
3.11	Input Data Register	3-8
3.12	End of Data Detect Logic	3-8
3.13	Transmit Handshake Logic	3-8
3.14	Hooks for the Diagnostic	3-9
3.15	Receive Handshake Logic	3-11
3.16	The Last Byte In Logic	3-13
3.17	FIFO Load Logic	3-14
3.18	FIFO Unload Logic	3-15
3.19	Last Byte Out Logic	3-17
3.20	Interrupt Source, Mask Logic	3-19
3.21	Input Multiplexer	3-19
3.22	Input Multiplexer Enable Logic	3-19
3.23	Clear Flag Detect Flip-Flop	3-20
3.24	End of Data Transfer Flip-Flop	3-21
3.25	Service Request Logic	3-22
3.26	Flag Buffer Flip-Flop	3-23
3.27	Flag Logic	3-24
3.28	Interrupt Request Logic	3-26
3.29	Interface Clear 100 Microsecond Timer	3-27
3.30	Interface Clear Flip-Flop	3-27
3.31	Parallel Poll Conduct Logic	3-27
3.32	Bus Address Switch	3-28
3.33	Bus Address Comparator	3-28
3.34	Command Decode Logic	3-28
3.35	System Controller	3-28

4. MAINTENANCE

4.1	Introduction	4-1
4.2	Safety Precautions	4-1
4.3	Preventive Maintenance	4-1
4.4	Troubleshooting	4-1
4.5	Diagnostic Tests	4-2
4.6	Replacement Procedure	4-2

5. BACKDATING INFORMATION

5.1	Introduction	5-1
5.2	Conventions	5-1
5.3	Listing	5-1

LIST OF ILLUSTRATIONS

	Page
1-1. Multi-Disc Configuration	1-2
1-2. Block Diagram, Disc Interface Data Paths	1-5
1-3. Unpacked Data Output Format	1-7
1-4. Packed Data Output Format	1-7
1-5. Control Word Format	1-8
1-6. Unpacked Data Input Format	1-10
1-7. Packed Data Input Format	1-10
1-8. Status Word Format	1-11
3-1. The FIFO IC	3-4
3-2. Upper Byte FIFO Loading	3-5
3-3. Upper Byte FIFO Unloading	3-6
3-4. Function of Input Output Data Selectors	3-7
3-5. Transmit Handshake Logic Timing	3-9
3-6. Diagnostic Timing Logic	3-10
3-7. Receive Handshake Logic Timing	3-12
3-8. Last Byte In Logic	3-13
3-9. FIFO Load Logic (Packed Data Format Input from Bus)	3-14
3-10. FIFO Load Logic (Load Output Data Register into FIFOs)	3-15
3-11. FIFO Unload Logic (Packed Data Format Output to Bus)	3-16
3-12. FIFO Unload Logic (Packed Data Format, FIFOs to Input to Input Data Register)	3-17
3-13. Last Byte Out Logic	3-18
3-14. Input Multiplexer Enable Logic	3-20
3-15. Clear Flag Detect Flip-Flop (Assume Pack=1)	3-20
3-16. End Data Transfer Flip-Flop	3-21
3-17. Service Request Logic (Input Transfer Assume Control=1)	3-22
3-18. Flag Buffer Flip-Flop	3-24
3-19. Flag Flip-Flop	3-25
3-20. Skip Flag Logic	3-25
3-21. Interrupt Request Logic	3-26
3-22. Parallel Poll Logic	3-27
4-1. 12821-60003 Parts Location Diagram	4-3
4-2. Pin Connections for the Bus Cable 59310-60008	4-8
4-3. Schematic Diagrams	4-10/4-14
5-1. 12821-60001 Parts Location Diagram	5-3

LIST OF TABLES

1-1. Disc Cables	1-1
1-2. Power Requirements	1-4
3-1. Interrupt Source, Mask Logic	3-19
4-1. Reference Parts List for Card Assembly 12821-60003	4-4
4-2. Code List of Manufacturers	4-7
5-1. Reference Parts List for Card Assembly 12821-60001	5-4

This is a basic list of mnemonics and acronyms which will be helpful in using this manual. With your addition of an appropriate prefix or suffix (such as EN, IN, OUT, etc. to indicate enable, input, output) this basic list can be leveraged to cover those situations likely to arise in the use of this manual:

MNEMONIC	DESCRIPTION
ADD	Address Detected
ATNL	Attention, Low True
ATNEN	Attention Enable
ATNIN	Attention In
BSRQL	Backwards SRQ, Low True
CHSEL	Channel Select
CIC	Controller-In-Charge
CLCSCL	Clear Control Select Code, Low True
CLFSCL	Clear Flag Select Code, Low True
CONTROL	Control
CONTROLL	Control, Low True
CRSL	Control Reset, Low True
CWCLKL	Control Word Clock, Low True
CS80-Series	HP Model 7908x, 7911x, or 7935x disc drive using HP-IB controller
DACIN	Data Accepted In
DACOUTL	Data Accepted Out, Low True
DAVINL	Data Valid In, Low True
DAVL	Data Valid, Low True
DAVOUTL	Data Valid Out, Low True
DIAG	Diagnostic
DSEL	Data Word Selected
EDT	End Data Transmission
ENFL	Enable Flag, Low True
EOI	End or Identify
EOIIN	End or Identify IN
EOIL	End of Identify, Low True
EOILBO	End or Identify, Last Byte Out
EOR	End of Record
EORL	End of Record, Low True
EOT	End Data Transfer
5GENSRQL	5T5 Controlled Generate SRQ, Low True
FIFO	First In, First Out
FLAGL	Flag, Low True
GENSRQL	Generate SRQ, Low True
H-SERIES	HP Model 7906H, 7920H, 7925H, or 9895A disc drive using HP-IB controller
IBP	Input Byte Pointer
ICD	Another name for H-Series disc drives
IESL	Serial Input Enable, Low True
IFCEN	Interface Clear Enable
IFCIN	Interface Clear Input

IFCL	Interface Clear, Low True
IFCOUT	Interface Clear Output
IOI	I/O Input
IOISCDL	I/O Input of Data
IOO	I/O Output
IRHI	Input Register Full-Upper Byte, Low True
IRL	Input Register Loaded
IRLEN	Input Register Loaded Enable
IRLO	Input Register Full-Lower Byte, Low True
L	Listen
LBIFF	Last Byte In Flip-Flop
LBOFF	Last Byte Out Flip-Flop
LF	Line Feed
MR	Master Reset
NCLFL	No Clear Flag, Low True
NDACL	Not Data Accepted, Low True
NRFDL	Not Ready for Data, Low True
O/E	Odd-Even
OBCLKL	Output Byte Clock, Low True
OBP	Output Byte Pointer
ODDIN	Odd In
OR	Output Ready
OREL	Output Register Empty, Low True
ORHI	Output Register Full-Upper Byte FIFO
ORLL	Output Register Loaded, Low True
ORLO	Output Register FullLower Byte and Tag FIFOs
PACK	Enable Packing
PLHI	Parallel Load-Upper Byte
PLLO	Parallel Load-Lower Byte
PP	Parallel Poll
PPC	Parallel Poll Conduct
PPE	Parallel Poll Enable
PPRL	Parallel Poll Response Load, Low True Receive
RCV	Receive
RENL	Remote Enable, Low True
RFDIN	Ready for Data In
RFDOUTL	Ready for Data Out, Low True
RHSKL	Receive Handshake, Low True
RRDYL	Receive Ready, Low True
SETFLG	Set Flag
SRQL	Service Request, Low True
SSEL	Status Select
SYSCTL	System Controller
T	Talk
THSKL	Transmit Handshake, Low True
TOPHI	Transfer Out Parallel-Upper Byte FIFO
TOPLO	Transfer Out Parallel-Lower Byte and Tag FIFO
TRDYL	Transmit Ready, Low True
TTIRL	Transfer to Input Register, Low True
TTSL	Transfer to Stack, Low True
XMITL	Transmit, Low True

1.1 DESCRIPTION

The HP 12821A Disc Interface (DI) is HP's implementation of IEEE Standard 488-1978 conforming to the Higher Speed Operations Guidelines of paragraph 5.2.3 to provide high speed, bidirectional interchange of digital data between the computer and its disc drive.

Both the H-Series (7906H, 7920H, 7925H, 9895A) and the CS80-Series (7908x, 7911x, 7912x, 7935x) disc drives are supported on the 12821A. This compatibility extends to the integrated Cartridge Tape Unit found in certain models of the CS80-Series disc drives (7908x, 7911x, and 7912x). While both the H-Series and CS80-Series disc drives are supported under RTE-6/VM, only the H-Series discs are supported under RTE-IVB. See Figure 1-1 for representative Multi-Disc configuration.

1.2 MULTI-DISC CONFIGURATIONS

Each 12821A will support either two H-Series or four CS80-Series disc drives (maximum). However, when both series disc drives are interfaced to the same computer, each series must be configured on a separate interface, each with its own driver.

1.3 INTERCONNECTION DISC CABLING

The disc drive is supplied with a standard 4 meter cable used to connect the DI. Table 1-1 lists the HP supported interconnection cables used to connect additional disc drives (either series):

Table 1-1. Disc Cables

LENGTH	PART NUMBER
1 meter	10833A
2 meter	10833B

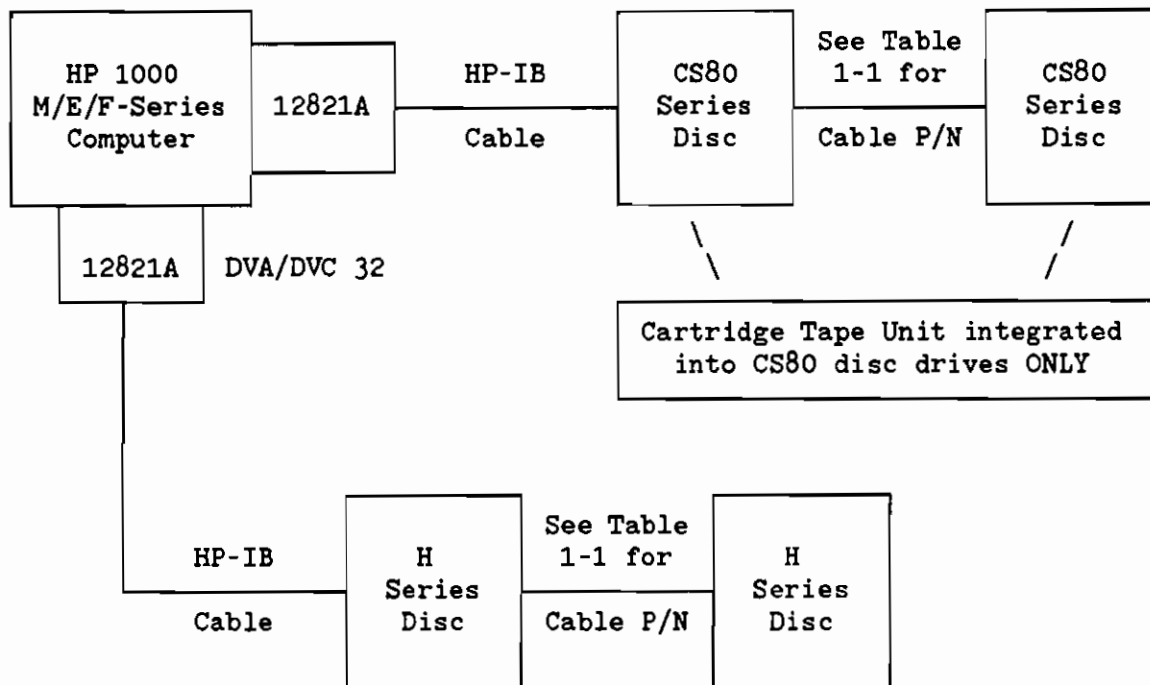


Figure 1-1. Multi-Disc Configuration

1.4 PRODUCT CONTENTS

The 12821A Disc Interface product consists of:

- 1) Disc Interface Card, HP Part Number 12821-60003.
- 2) HP-IB Cable Assembly, HP Part Number 59310-60008.
- 3) Disc Interface Installation and Service Manual, HP Part Number 12821-90006.
- 4) HP 12992 Loader ROM Installation Manual, HP Part Number 12992-90001.
- 5) HP 12992H Disc Loader ROM (for H-Series disc drive only).

- or -

- 6) For CS80-Series, Option 001 is ordered (deletes item 5) and 12992J Disc Loader ROM is ordered as a separate line item.

1.5 RELATED ITEMS

The following items are not included in 12821A component shipments but are included in HP 1000 Computer Systems shipments. When purchasing a component product or system or adding to or upgrading a previously purchased system, these items will be needed (as indicated) for typical system operation:

- 1) Software Driver DVA/DVC 32, HP Part Number 92067-16553, for H-Series disc drive. Included with the RTE-IVB (92068A) or the RTE-6/VM (92084) Operating System.
- 2) Software Driver DVM/DVN 33, HP Part Number 92084-16650, for CS80-Series disc drive. Included in the RTE-6/VM (92084A) Operating System.
- 3) HP-IB bus cables (see Table 1-1) for multi-disc installation.
- 4) HP 12992J Disc Loader ROM for CS80-Series disc drives (see item 6, section 1.4 Product Contents above).
- 5) 24998-14002, HP 1000 Computer System Diagnostic Library, supplied with shipments of HP 1000 Systems.
- 6) HP 91711B Diagnostics and Verification Package, supplied with current shipments of HP 1000 Systems.

1.6 IDENTIFICATION



1.6.1 Product

Five digits and a letter suffix (12821A in this case) are used to define and identify HP products used with HP computers. The five digits identify the product while the letter indicates the revision level of the product.

1.6.2 Circuit Card

The interface circuit card assembly is further identified by a part number marked on the card. In addition to this, a letter and a date code consisting of four digits are placed below the part number. The letter identifies the etched circuit on the card. The four-digit date code identifies the electrical characteristics of a loaded circuit card, such as:

12821-60001
A-1926

If the date code on the card does not exactly agree with the date code on the title page of this manual, there are differences between your circuit card and the one described in this manual. These differences are covered in manual supplements; these supplements either accompany this manual or are available through the nearest HP Sales and Support Office (listed in the back of this manual).

1.7 POWER AND ENVIRONMENTAL REQUIREMENTS

The 12821A operating temperature range is 0 to 55 degrees Celsius. Power requirements are:

Table 1-2. Power Requirements

SUPPLY VOLTAGE	MAX. CURRENT REQUIRED
+30	None
+12	None
+ 5	3.34A
- 2	0.10A
-12	None

1.8 OPERATION

The 12821A architecture has been optimized for DMA transfer. However, this does not inhibit the ease of interrupt-driven transfers of small data buffers. The DI operates under control of either RTE-IVB (92068A), or RTE-6/VM (92084) operating system drivers to make data transfers. The transfer rate can approach one megabyte per second without user intervention (user transparency). To achieve this high transfer rate, the DI is preloaded with seven unit resistive loads. Because drivers are device specific routines, the following drivers will be used with the indicated Series disc drives:

- * DVA/DVC 32 for H-Series disc drives
- * DVM/DVN 33 for CS80-Series disc drives

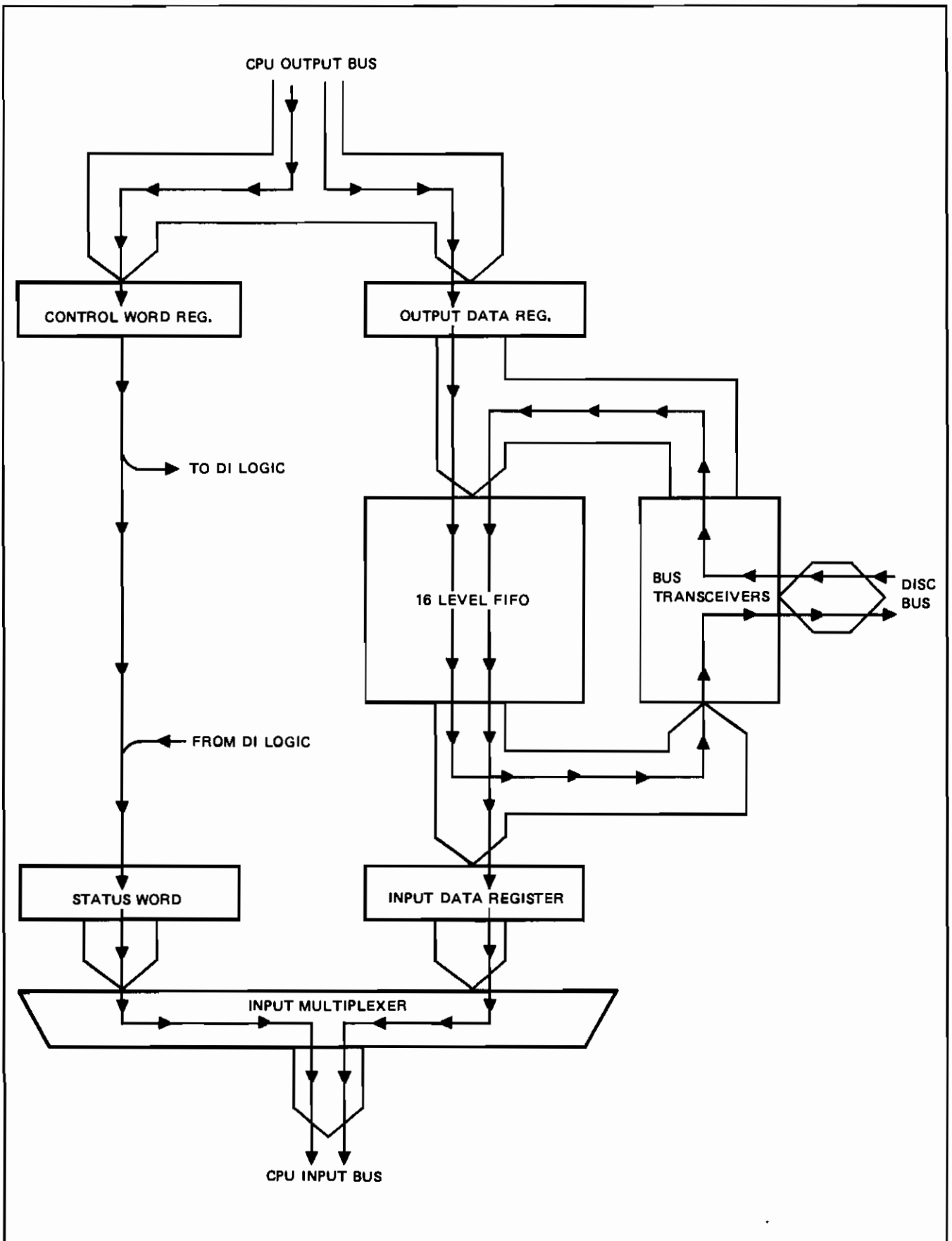


Figure 1-2. Disc Interface Data Paths Block Diagram

1.9 FUNCTIONAL DESCRIPTION

The Disc Interface (DI) in the Data Mode is bidirectional, data may be transferred from the CPU or memory to a disc or from a disc to the CPU or memory. The DI is defined to be a talker when transferring data from the computer to the disc and to be a listener when transferring data from the disc to the computer. In addition to the Data Mode, the CPU can place the DI in the Configure Mode, as a talker, or the Status Mode, as a listener.

Figure 1-2 is a functional block diagram showing the data paths within the DI. Information from the computer I/O bus can be seen to have two possible destinations, the Control Word Register (Configure Mode) or the Output Data Register (Data Mode). The Control Word sets up the DI logic and alerts the disc that data is to be transmitted. When the disc acknowledges the request and is ready to receive, the data is processed through the FIFO and the transceivers to the disc. To obtain data from the disc the DI must first be set up as a talker to inform the disc that data is going to be requested. When the disc acknowledges the commands the DI is then made a listener and the data transfer takes place through the Transceivers, FIFO, Input Data Register, and Input Multiplexer to the computer.

The key to the high transfer rate of the DI is the 16 word FIFO buffer. The FIFO can be loaded from the Output Data Register when the DI is a talker or from the transceivers when a listener. Data from the computer, being 16 bits wide, is loaded directly into the FIFO, while byte data from the disc can be packed two bytes per word.

Similarly, data out of the FIFO can be sent to the computer from the Input Data Register when DI is a listener, or to the disc from the transceivers when DI is a talker. FIFO words can be unpacked to form two 8-bit bytes. The routing of data into and out of the FIFO is done by Tri-state logic. If packing is used the upper byte of each FIFO word is the first to be sent or received. If no packing is specified, the lower byte FIFO is always selected.

Data for the computer is selected by the Input Multiplexer. The input mode will determine whether the Input Data Register or the Status Word will be read by the computer.

1.10 OUTPUT MODES

The formats for the Data Mode and the Configure Mode are shown in the following paragraphs. Data output to the DI will be received by Output Data Register or the Control Word Register depending on the previously selected mode. The Control Word Register (Configure Mode) is selected by clearing the Control Flip-Flop.

1.10.1 Data Mode (Control Flip-Flop Set)

Data can be output to the DI in two formats, packed or unpacked. In general, the unpacked format will be used when outputting less than 17 bytes of commands and/or data in a software controlled transfer. The packed format is most often used when outputting more than 17 bytes of data in a DMA transfer.

The unpacked data output format is shown in Figure 1-3.

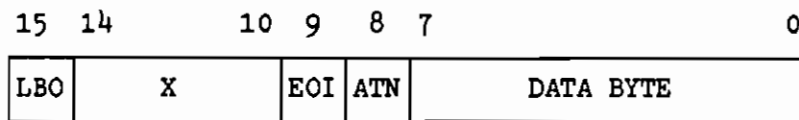


Figure 1-3. Unpacked Data Output Format

Bits 0-7 contain the data byte, while bits 8 and 9 contain the values of the disc ATN and EOI lines to be associated with this data. Note that this format allows disc commands (ATN=1) and data (ATN=0) to be mixed in any order within the FIFO.

Bits 10-14 are ignored by the DI in the unpacked format. Bit 15 signals to the DI that this is the last byte of the current output string. (See description of LBO.)

The packed data output format is shown in Figure 1-4.

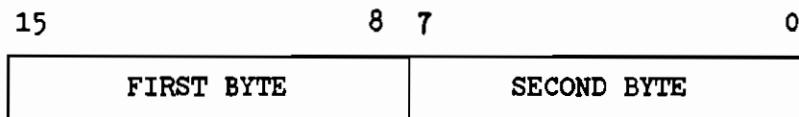


Figure 1-4. Packed Data Output Format

Here two 8-bit bytes are contained within the word. The values of ATN and EOI associated with each byte are determined by two bits of the Control Word Register (see section 1.10.2).

1.10.2 Configure Mode (Control Flip-Flop Clear)

The data format of the Control Word Register is shown in Figure 1-5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S R Q	I F C	R E N	I R L	L B O	L F	E O I	A T N	D I A G	N R F D	P P E	O / E	P	L	T	C I C

Figure 1-5. Control Word Format

Note that each bit has a specific function, and that no multibit encoding is used. The functions of each Control Word Register bit are as follows:

CIC (Controller⁵ in Charge, Bit 0) -- tells the DI that it is currently controlling the disc.

T (Talk, Bit 1) -- indicates that the DI is a talker to the disc.

L (Listen, Bit 2) -- indicates that the DI is a listener (from disc).

Pack (Enable Packing, Bit 3) -- indicates that the packed data format is to be used for input or output.

O/E (Odd-Even, Bit 4) -- if set, indicates that for the current Packed Output operation an odd number of bytes is to be output to the disc (i.e., the second byte of the last word will not be sent). For the definition of "last word" see the description of LBO control bit.

PPE (Parallel Poll Enable, Bit 5) -- sets ATN and EOI on the bus, indicating that a Parallel Poll is being conducted. T and L must also be set for a parallel poll. After 2 microseconds, the DI looks for a response. When the response occurs it is automatically loaded into the FIFO.

NRFD (Not Ready for Data, Bit 6) -- sets the corresponding line on the bus, indicating that the DI is not ready to receive data. This function is required when the DI has been receiving data from a disc and now wishes to untalk the device. NRFD will prevent the disc from placing any further data on the bus while the DI is being reconfigured to talk and the untalk command is being loaded into the FIFO.

DIAG (Diagnostic, Bit 7) -- This bit is used by the diagnostic program. When set, this bit enables the diagnostic program to circle data from the FIFOs through the transceivers back into the FIFOs.

ATN (Attention, Bit 8) -- in the Packed Output Mode, specifies the value of the bus Attention line. The CIC bit in the control register must also be set.

EOI (End or Identify, Bit 9) -- in the Packed Output Mode, specifies that the last byte sent will be tagged with EOI (see the following description of LBO).

When the DI is inputting, EOI specifies that reception of a byte tagged with EOI will be the EOR (End of Record) Flip-Flop. EOR will generate NRFD, indicating to the disc that the DI is no longer ready to receive data. A tag indicating that this is the last word of the current input transfer is placed in the FIFO with the data. When this word has been read by the CPU the DI flag will be set. Any byte signalling EOR will automatically be loaded into the lower byte of the FIFO. Thus if an odd number of bytes are received, the EOR byte will be put in both halves of the FIFO and appear twice in memory. This mechanism is necessary to insure that an odd-numbered byte tagged with EOI will be sent to the CPU. The possible ambiguity of a double last byte in memory can be resolved by reading the O/E bit in the DI Status word.

LF (Line Feed, Bit 10) -- enables the line feed detector to set EOR if the line feed is received by the DI. (The results of EOR are the same as described above).

LBO (Last Byte Output, Bit 11) -- causes the DI flag to be set when the last byte of the current output transfer has been accepted by the disc.

The last word of an output transfer is signalled to the DI in either of two ways. If a DMA transfer is occurring, the DCPC will automatically signal when the last word is output. This tag will be placed in the FIFO along with the data word.

If the data is being output via software (in the unpacked mode), Bit 15 of the data word will indicate to the DI that this word is the last of the current transfer. If the data is output in the packed format the last word is indicated by outputting the word with an OTA DI instruction rather than outputting with an OTA DI,C instruction.

If the output data format is packed, the last byte of the transfer will be the byte of the last word specified by the O/E bit of the Control Word Register (Bit 4). If the output data format is unpacked, the lower byte is automatically assumed to be the last byte.

IRL (Input Register Loaded, Bit 12) -- will cause the DI flag to be set when the Input Data Register is loaded. If packing is disabled, reception of one data byte from the disc will load the register; if packing is enabled, 2 bytes must be received. The IRL interrupt is useful for notifying the software that a Parallel Poll response has been received.

REN (Remote Enable, Bit 13) -- determines that state of the disc REN line. The system controller switch must be set on the DI for this signal to be output to the disc.

IFC (Interface Clear, Bit 14) -- the positive going transition of this bit will generate a 100 microsecond IFC signal to the disc. The System Controller switch must be set on the DI for this signal to be generated.

SRQ (Service Request, Bit 15) -- allows any SRQ received by the DI to set the DI flag. The DI must be Controller-In-Charge.

The Control Flip-Flop is cleared by the CPU backplane signal CRS, which occurs at power-up, or when the "PRESET" button is pressed and also when a CLC 0 instruction is executed.

1.11 INPUT MODES

Data input from the DI will come from either the Input Data Register or the Status Word, depending upon the previously selected mode. The Status Mode is selected by clearing the DI Control Flip-Flop; input will then be the Status Word. (Reading status will not change the mode of the DI.)

Similarly, when the DI Control Flip-Flop is set, the Data Mode is selected and data will be input from the Input Data Register.

1.11.1 Data Mode (Control Flip-Flop Set)

Data is input from the DI in two formats, packed or unpacked.

The unpacked data input format is shown in Figure 1-6.

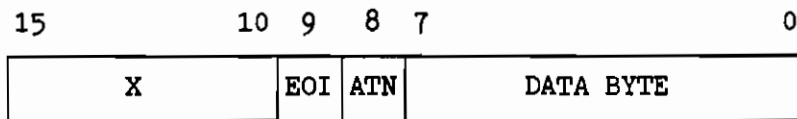


Figure 1-6. Unpacked Data Input Format

Bits 0-7 contain the data byte, while Bits 8 and 9 contain the values of the disc ATN and EOI line associated with the data. If the DI is conducting a Parallel Poll, the poll response will be in the data positions and both Bits 8 and 9 will be set, indicating the poll function. Bits 10-15 are undefined in the unpacked format, and should be masked by software.

The packed data input format is shown in Figure 1-7.

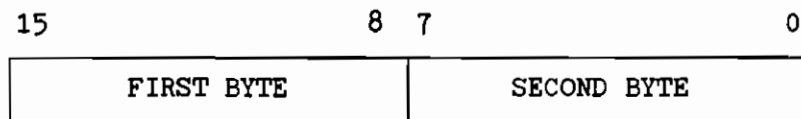


Figure 1-7. Packed Data Input Format

Here two 8-bit bytes are contained within the word. As described in "EOI" (section 1.10.2), an odd numbered byte signalling End of Record will appear in both bytes of the data word.

1.11.2 Status Mode (Control Flip-Flop Clear)

The data format of the Status Word is shown in Figure 1-8.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S R Q	I F C I	R E N	I R L	L B O	L B I	E O I	A T N	I F C O	X	X	O / E	S C Y T L	L	T		C I C

Figure 1-8. Status Word Format

The definition of each Status Bit is as follows:

CIC (Controller-in-Charge, Bit 0) -- indicates that the DI is currently controlling the disc.

T (Talk, Bit 1) -- indicates that the DI is currently a talker to the disc.

L (Listen, Bit 2) -- indicates that the DI is currently a listener to the disc.

SYSTL (System Controller, Bit 3) -- indicates the position of the System Controller Switch on the DI.

ODDIN (Bit 4) - if set, indicates that an odd number of bytes were received in the last (packed) input transfer. (In the unpacked mode, this bit is always set.)

IFCO (Interface Clear Output, Bit 7) -- indicates that the 100 microsecond IFC one-shot is still fired.

ATN (Attention, Bit 8) -- indicates that the instantaneous state of the disc ATN line. This may or may not be the same as the values of ATN stored in the FIFO for each data byte.

EOI (End or Identify, Bit 9) -- same as above for the disc EOI line.

LBI (Last Byte Input, Bit 10) -- indicates that the EOR Flip-Flop has been set.

LBO (Last Byte Output, Bit 11) -- indicates that the LBO Flip-Flop has been set.

IRL (Input Register Loaded, Bit 12) -- indicates that a byte (unpacked) or 2 bytes (packed) are valid in the Input Data Register.

REN (Remote Enable, Bit 13) -- indicates the state of the disc REN Line.

IFCI (Interface Clear Input, Bit 14) -- indicates that the IFC Flip-Flop has been set due to IFC asserted on the bus.

SRQ (Service Request, Bit 15) -- indicates the state of the disc SRQ line.

1.12 MASTER RESET

1.12.1 Master Reset Functions

The Master Reset signal is used to reset and/or initialize all data paths and Flip-Flops on the DI. MR will affect the following logic elements of the DI:

- (1) Clear the DI Control Flip-Flop
- (2) Clear the DI Flag Flip-Flop
- (3) Reset the DI FIFO
- (4) Clear the Input Data Register
- (5) Reset the LBO (Last Byte Output) Flip-Flop
- (6) Reset the LBI (Last Byte Input) Flip-Flop
- (7) Reset the IRL (Input Register Loaded) Flip-Flop
- (8) Set the input byte pointer to upper byte (if packed)
- (9) Set the output byte pointer to upper byte (if packed)
- (10) Reset the IFCI (Interface Clear) Flip-Flop

The MR signal is also generated by the CPU backplane signal CRS.

1.12.2 Rules Concerning MR

Two rules must be followed for generating MR prior to a data transfer:

- a) MR must be generated before the DI is made a Talker or a Listener. This will prevent "garbage" left in the FIFO from some previous transfer from either being transmitted to the bus or read into the DI Input Data Register.
- b) MR must also be generated after Packing is enabled but before the first data word is transferred.

This is necessary because, in the unpacked mode, the input and output byte pointers are held in the "lower byte" position and cannot be changed. When Packing is enabled, MR must then be sent to position these pointers are the "upper byte" position, to be ready for the first byte of data.

Thus, to make the DI a Talker in Packed output format, the proper sequence is:

- (1) MR (Rule 1)
- (2) Control Register = Talk, Packing
- (3) MR (Rule 2)
- (4) Output Data to DI

2.1 GENERAL

This section provides installation information needed to interface the 12821A Disc Interface (DI) to an HP compatible disc. The H-Series (7906H, 7920H, 7925H and 9895A) and the CS80-Series (7908x, 7911x, 7912x and 7935x) disc drives are compatible with the DI. This interface is supported only when installed on an HP 1000 M/E/F-Series CPU configured under either the RTE-IVB (92068A) or the RTE-6/VM (92084A) operating system. The user choice of operating system is supplied with an HP 1000 System or may be ordered separately under one of several options. Consult your local HP Sales and Support Office (listing in back of this manual) to determine which is most advantageous to you. Included in this section are installation requirements, DIP switch settings, cabling instructions and recommended packaging and shipping procedures for product reshipment.

2.2 UNPACKING AND INSPECTION

Inspect the product shipping container before opening. If there is external evidence of damage, request that the carrier's agent be present when the container is first opened. Carefully inspect each item for damage. If there is physical damage, immediately notify your local Hewlett-Packard Sales and Support Office (listing included in the back of this manual) and the common carrier. If the product fails to meet HP's published specifications or the diagnostics cannot be successfully run (see Installation Checkout, next section and Chapter 4), notify your local Hewlett-Packard Sales and Support Office.

Retain the shipping container and packing material for the carrier's and HP's inspection. The HP Sales and Support Office will arrange for the repair or replacement of your shipment, without waiting for your claim against the carrier to be resolved.

2.3 CHECKOUT

To verify operation of this product, perform the diagnostics included in the 24998-14002 Diagnostic Library, included in your HP 1000 Model 60 or 65 System.

2.4 STORAGE AND RESHIPMENT

If your local HP Sales and Support Office instructs you to return the shipment for repair, attach a tag identifying the owner and (if possible) the HP Sales Order Number. Indicate on the tag the service to be performed or the problem encountered with this shipment. If the original, factory packaging material is available and in reusable condition, it may be useful. Whether packaged for reshipment by your Traffic Department, or a third party, good grade commercial material should be used. Carefully follow the local HP Sales and Support Office's instructions for expeditious repair or replacement of your defective product.

2.5 SYSTEM CONTROLLER ADDRESS DIP SWITCH BLOCK

Before installation of the DI in the CPU backplane, the System Controller function must be enabled. The eight position DIP Switch located at position U13 (See Figure 4-1) on the PCA has switch eight (U13-S8) assigned to the system controller function. Set S8 to the OPEN (OPEN = 1) position to enable the system controller function. Switches 1 through 7 are used by the diagnostic and to set the DI's select code. Closing S1-S7 will provide an address of 0 which is recommended when running the diagnostic. See your HP 1000 Primary System Configuration Data Manual for more information on the select code.

WARNING

Hazardous voltages are present inside the computer mainframe. Before installing the DI or the loader ROM, set the POWER SWITCH TO OFF. Failure to observe this warning can result in serious injury.

2.5.1 Setting the SRQ Control Jumper

Jumper W1 must be installed in either the "A" or "B" position.

CAUTION

The Disc Interface may be damaged and errors in data can occur, if Jumper W1 is left out.

Jumper W1 is in the "A" position when it is installed across the "A" printed on the board. Likewise, W1 is in the "B" position when it is installed across the "B".

To change jumper W1's position, grasp the jumper with tweezers or small needle-nose pliers and pull straight up. Position the jumper across the desired letter, carefully align the jumper's pins with the holes in the board, and gently push the jumper until the plastic touches the printed circuit assembly.

NOTE

With the jumper in the "A" position the DI will fail the DMA portion of the diagnostics. This is due to the timing of the test, not necessarily an error by the DI.

Some devices will time-out and go off-line if they cannot access the CPU in a fixed time. Be sure W1 is in the "A" position to accommodate such devices. See Chapter 3 under the heading "Service Request Logic" for more information.

2.6 INSTALLATION

Install the DI as follows:

- 1) Set the computer POWER switch to OFF.
- 2) Remove the I/O card cage cover.
- 3) If you are installing the DI in an HP 1000 System, insert the DI into the I/O slot (select code) reserved for it (refer to Table 1 of your HP 1000 Primary System Configuration Data Manual) otherwise install it in any convenient I/O slot.
- 4) Install the HP 12992H Disc Loader ROM for H-Series disc drive operation using the instructions contained in the 12992 Loader ROM's Installation Manual, HP Part Number 12992-90001.

- OR -

- 5) If CS80-Series disc drivers are to be used, Option 001 was ordered to delete the H-Series Loader ROM and the 12992J CS80-Series Loader ROM was ordered as a separate line item. Install it using the instructions contained in the 12992 Loader ROM Installation Manual, HP Part Number 12992-90001.

NOTE

If the DI was purchased as part of an original HP 1000 System order, the DI and the loader ROM will have been installed. Refer to the decal on the inside of the cabinet front door to determine the DI and loader ROM location.

- 6) Turn OFF all disc drives before connecting cables to the DI or the disc drive.
- 7) Perform the disc installation and checkout procedures described in your Disc Installation and Service Manual before connecting the HP-IB cable (furnished with this interface) to the DI and the first disc drive.

NOTE

The DI will Fail the DMA portion of the diagnostic if Jumper W1 is in position "A". See "Setting SRQ Control Jumper", above.

CAUTION

All disc drives must be OFF before connecting cables.

2.7 INTERCONNECTING CABLES

- a) If you are installing the HP 1000 Model 60 or 65 System, attach the HP-IB cable (4 meters) from the DI to the first disc drive and interconnection cables to any additional disc drives (see Figure 1-1 and Table 1-1). Then perform the primary system tests described in your "Getting Started" manual.
- b) If you are installing an HP 1000 M/E/F-Series computer, run the 24998 diagnostics (refer to the Disc Interface Diagnostic Manual, 12821-90002). Then connect the HP-IB cable from the DI to the first disc drive, and the interconnecting cable to any additional disc drive.

2.8 SYSTEM OR SUBSYSTEM CHECKOUT

Refer to the HP 1000 Model 60/65 Installation and Service Manual, HP Part Number 5955-4359, for system checkout procedures, or to the diagnostic manual, 12821-90002, for DI checkout procedures. If a disc or system level problem is indicated, use the 91711B, Diagnostics and Verification Package to isolate.

NOTE

In order to prevent degraded operation, ALL disc drives cabled to the disc interface (DI) must be powered ON whenever your computer or system is operating.

3.1 INTRODUCTION

This section provides a brief description of the logical operation of the Disc Interface (DI). This theory is presented to aid in confirming that a problem exists on the DI rather than another component of the subsystem. The DI is a multilayer Printed Circuit Assembly (PCA) and should be returned to a Hewlett-Packard service center for repair. The warranty may be voided if the DI is repaired by unqualified personnel. Assembly and schematic diagrams to be used in conjunction with this discussion are located in Chapter 4.

3.2 SIGNAL NAMES AND LOCATIONS

Signal names are mnemonic identifiers usually chosen to be as close to the signal usage as possible. These signal identifiers may have a bar over them on the schematics to indicate the signal is active low. In text the same signal will contain an "L" at the end of the signal name to indicate the active low condition.

The DI logic diagram in Chapter 4 is printed on three fold-out pages, so during our discussion we have indicated sheet numbers and coordinates within brackets []. The coordinates will be those of an area of the schematic which contains the logic circuit described in the text. A reference to a particular component in those coordinates will usually be printed in parenthesis ().

Example: [2D-7] (U117-2) refers you to sheet 2 at coordinates D-7 and component U117's pin number 2.

3.3 CHANNEL SELECT LOGIC

The CHSEL signal (U117-12) [2D-7] results from a logical AND of IOG (I/O Group Instruction), LSCM (Lower Select Code, Most Significant Digit), and LSCL (Lower Select Code, Least Significant Digit). It is used to enable the Control, Flag Buffer, Flag, and Input Multiplexer Enable logic blocks when an I/O instruction is being executed and is directed to the DI's select code.

3.4 CONTROL LOGIC

3.4.1 Control Flip-Flop and Logic

The Control Flip-Flop Output signal CONTROLL [2D-7] (U126-4, low true) determines whether the DI is in Data Mode or in Configure/Status Mode. Data Mode is selected by executing an STC Configure/Status Mode. Data Mode is selected by executing an STC DI instruction. The CHSEL signal (U117-12) enables the STC signal [2D-8] (U127-5) to the Control Flip-Flop. STC is inverted through the NAND gate (U127) and resets the Control Flip-Flop (U126-1) so that CONTROLL is

low. CONTROLL is inverted and is input to the NAND gate which generates OBCLKL [2D-6] (U105-8) in addition to being input to the Flag logic and Input Mux Enable logic. OBCLKL is derived from IOO when CONTROLL is zero and CHSEL is one, i.e., when an I/O output instruction to the DI is executed and the card is in data mode. OBCLKL is used to clock the Output Data Register.

Similarly, a CLC DI instruction selects Configure/Status mode by setting the Control Flip-Flop (CONTROLL = 1). CONTROLL enables the NAND gate which generates CWCLKL [2D-6]. CWCLKL is derived from IOO when CONTROLL and CHSEL are one, i.e., when an I/O output instruction to the DI is executed and the card is in configure mode. CWCLKL is used to clock the Control Word Register [2C-4,5].

3.4.2 Control Word Register

The Control Word Register is made up of two Octal D-type flip-flops (U96, U56) with a common clock. The inputs are the IOBO (Input/ Output Bus Output) lines from the CPU. Data is latched on the rising edge of CWCLKL. The Control Word Register is cleared by the CRSL signal (Control Reset, low true) [2D-6] and not by Master Reset (MR).

3.4.3 Bus Transceivers and Control Line Logic

The bus transceivers are inverting quad tri-state party line transceivers [1C-6; 1C-3,2] and inverting quad unified bus transceivers (U51) [1C-5] with open collector drivers.

The open-collector drivers used for the NDA CL, NRF DL, SR QL and REN L control lines allow wired-OR connection of the lines. The drivers are always enabled so that any signal seen on the S inputs is sent to the bus and any signal seen on the bus is received at the R outputs.

In general, a signal to be sent to the disc will be called XXXOUT, and one received from the disc will be called XXXIN where XXX is the mnemonic of the appropriate control line (ATN, REN, NDAC etc.).

The other bus transceiver on the control lines has regular drivers. Its receivers are always enabled. Its drivers, however, are enabled only when the DI is controller-in-charge and the DI is a talker. The driver enable signal is generated by some of the combinational logic referred to as the Control Line Logic (U61-3, U61-6) [1C-6].

The driver enable signal is ORed with the PPC (Parallel Poll Conduct) signal to generate XMITL (U52-11) [1C-5]. XMITL is used to enable the drivers on the Data Line Bus Transceivers (U31,21) [1C-2,3] and also tells the transmit handshake logic that a data transfer is about to begin.

U102-6 [1C-7] allows RENL to go low if the DI is System Controller and the RENEN bit in the Control Register is set. Similarly, U53-8 [1C-7] allows SRQL to go low if the DI is not controller-in-charge and the SRQEN bit in the Control Register is set. The gates U122-6 [1C-7] and U32-11 [1C-7] are used to assert ATNL (DI must be Controller-in-Charge) or EOIL respectively, if ATNOUT

or EOIOU are asserted, or if a parallel poll is being conducted (PPC is high) by the DI.

The bus transceivers on the data lines (U31,21) have the FIFO and Output Byte Select logic outputs (OUTBUS1-8) [1B,C-1] as their driver inputs. The drivers are enabled whenever XMITL is low. Their receiver outputs (INBUS1-8) [3D-1] are input to the FIFOs and Input Byte Select logic [3D-3]. The receivers are enabled whenever RCVL is low.

The bus lines are loaded by seven equivalent HP-IB loads. The loading is done by resistors R4 and R5 [1D-5], and R2 and R3 [1C-1]. In their high state, the lines are at 3.7V with no external devices connected to the DI.

3.5 OUTPUT DATA REGISTER

The Output Data Register is made up of two octal latches (U86, U66) [2C-1,2,3] with common clock and enable. While OBCLKL is low, the latch outputs follow the IOBO lines. Data is latched when OBCLKL returns high. Typically the latch outputs are enabled. The outputs will be high impedance if RCV is a one indicating that the DI is a receiving data from the disc or if the DIAG bit of the Control Register [2C-4] is set (see the heading "Hooks for the Diagnostic" in this chapter). The register's outputs are input to the FIFOs and the Input Byte Select logic [3D-3].

3.6 INPUT BYTE SELECT LOGIC



The Input Byte Select logic [D3-3] is used to enable the INBUS to the Upper Byte FIFO when the DI is receiving data from the disc. A tri-state octal buffer (U76) is used with RCVL as the enable.

3.7 INPUT DATA SELECT

The Input Data Selector [3C-1] is a quad 2 to 1 data selector (U16). Its outputs are always enabled and are input to the TAG FIFO. RCV is used as the select. When the DI is receiving data from the disc (RCV = 1), the ATN (ATNIN) and EO1 (EOIIN) values associated with the current byte on the bus are selected. When the DI is transmitting data over the bus (RCV = 0) bits DI8 and DI9 are selected. Note that these bits correspond to ATN and EO1 when in unpacked data format.

3.8 THE FIFO's

3.8.1 Introduction

A First In First Out Buffer Memory is used as the basic building block for the DI FIFO Buffers [3C-2 to 5]. A general description of the FIFO Buffer Memory will be given first, then a more detailed description of how the DI utilizes this part. Consult the part manufacturer's data book for more information.

3.8.2 The FIFO Buffer Memory

The IC is organized as 16 four-bit words (Figure 3-1). It is capable of being expanded to any number of bits and may be loaded and unloaded asynchronously or in parallel. The outputs are tri-state.

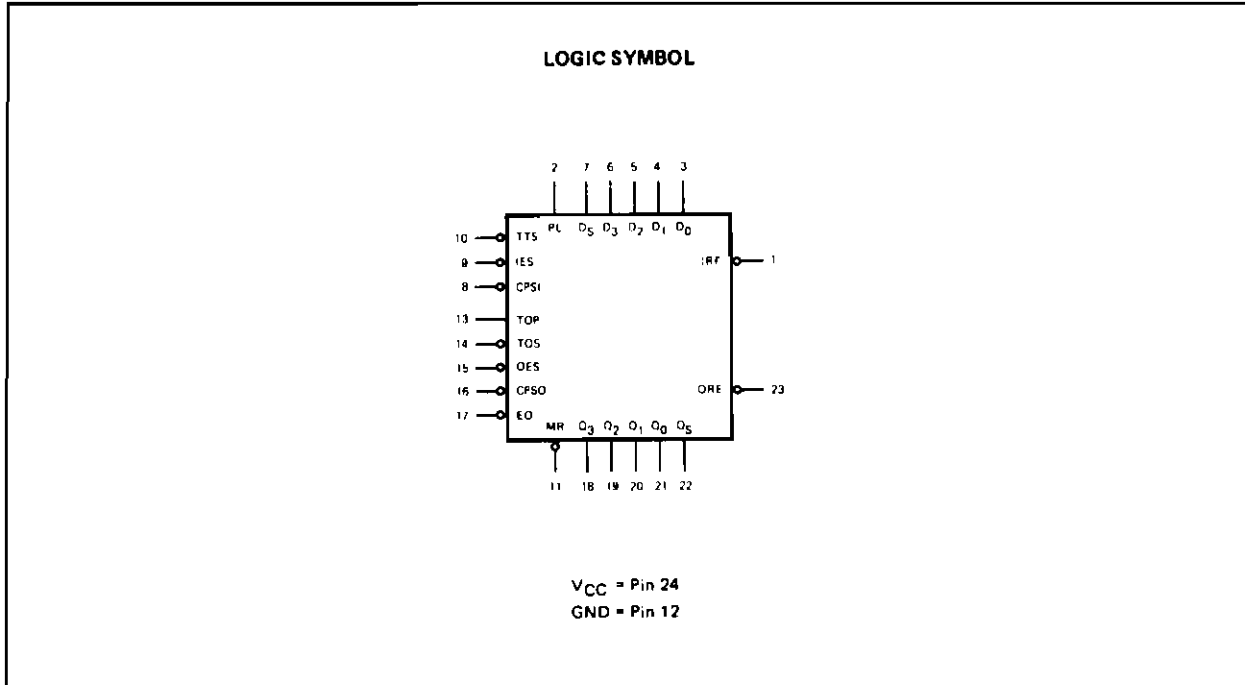


Figure 3-1. The FIFO IC

A high on PL (Parallel Load Input) parallel loads the D inputs into the input register internal to the FIFO, and IRFL (Input Register Full Output, low true) goes low indicating the register is full. NOTE: IESL (Serial Input Enable) must be low to enable parallel inputs. The input register feeds the FIFO stacks and if the top location of the stack is empty then when TTSL (Transfer to Stack input, low true) goes low, the data falls through to the stack automatically - pausing only when necessary to wait for the next location to empty. The input register is reinitialized when PL returns low. When the FIFO's input data register contents have been transferred to the stack IRFL returns high, assuming horizontal expansion is more than 4 bits in width. Automatic FIFO action is achieved by connecting the IRFL output of the right-most tip of a logical block to the TTSL input of all the FIFOs of that block.

After data has entered the IC and fallen through to the last stack location it is transferred into the FIFOs output data register if TOP (Transfer Out Parallel Input) is high. After this transfer, OREL (Output Register Empty Output, low true) goes high indicating there is valid data in the FIFO's output data register. If EOL (Output Enable, low true) is low, the output data register contents are seen at the FIFO outputs.

TOP is used to "clock" out such words. When TOP goes low, the data is latched in the output data register. OREL goes low to indicate that the data has been extracted. However, the data remains in the output data register until TOP returns high, allowing the next word to be transferred into the register.

3.8.3 The DI FIFO Buffers

The FIFO buffers are logically divided into two blocks; the Upper Byte FIFO, and the Lower Byte and Tag FIFOs. The Upper Byte FIFO consists of two FIFO ICs organized as a buffer sixteen levels deep, each level containing eight bits. The Lower Byte and Tag FIFO's are made up of 3 FIFO ICs organized as a buffer sixteen levels deep, each level containing twelve bits. Since the structure of each block is similar, the Upper Byte FIFO will be described and then the differences in the Lower Byte and Tag FIFO will be pointed out. The ICs which make up the Upper Byte FIFO have a common PL signal (PLHI) and TTSL signal. The IRFL output of the right-most FIFO provides the TTSL signal and is ultimately used to derive IRHI. The IRFL output of the left-most FIFO provides the right-most FIFO IESL input. The inputs are always enabled on the left-most FIFO. Thus for loading the upper byte, the sequence of events is as shown in Figure 3-2.

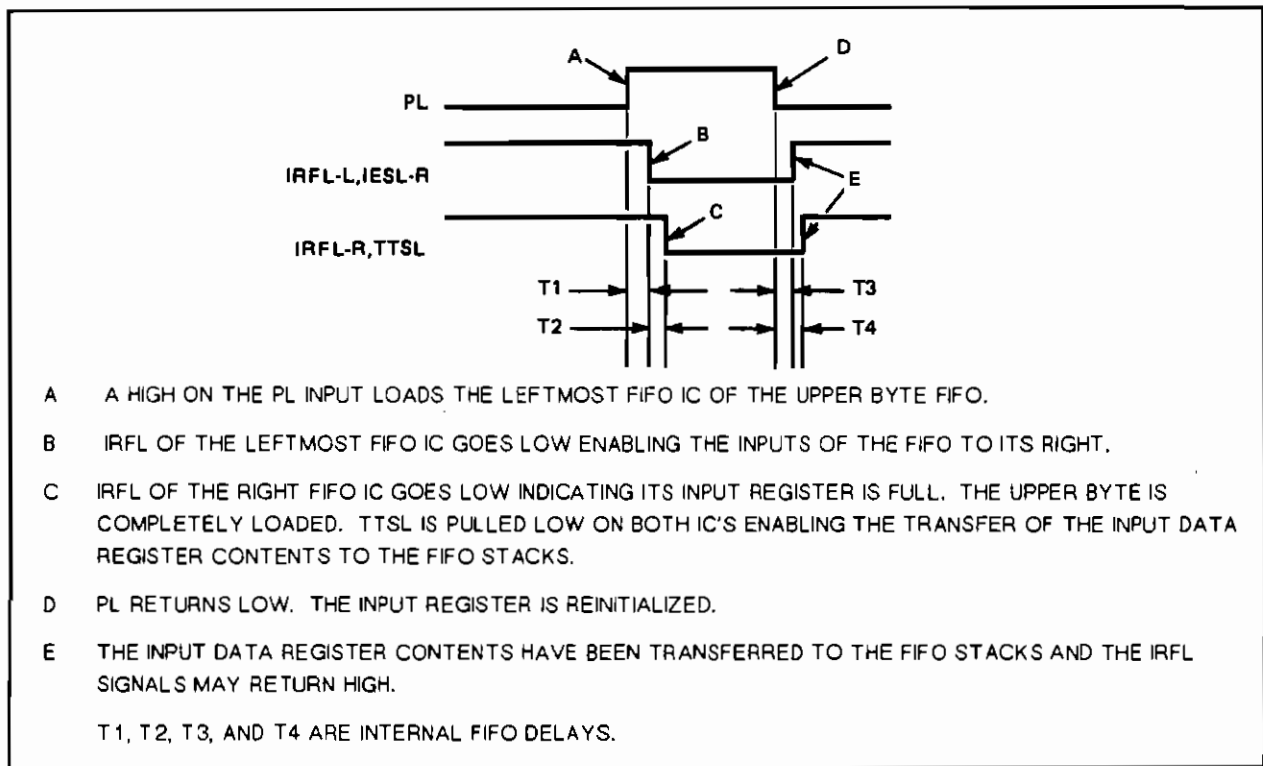


Figure 3-2. Upper Byte FIFO Loading

The FIFOs also have a common TOP signal. The outputs of the left-most FIFO are always enabled and its OREL output signal provides the output enable to the right-most FIFO. The right-most FIFO's OREL signal is used in deriving ORHI. The sequence of events for unloading the upper byte is as shown in Figure 3-3.

The Lower Byte and Tag FIFO's ICs are chained together and loaded in the same manner as in the Upper Byte FIFO. The PL signal is PLLO and the IRFL output of the right-most FIFO is IRLO.

Unloading the Lower Byte and Tag FIFOs differs from the Upper Byte only when the FIFO outputs are enabled. The Lower Byte FIFO's outputs are high impedance when the DI is not receiving data (RCV=0) and the Output Byte Pointer points to the Upper Byte (OBP=1). When the DI is transmitting over the bus, the Output Byte Select logic enables the Upper Byte to the OUTBUS lines when OBP is high. When OBP points to the lower byte, the Lower Byte outputs are enabled to the OUTBUS lines and the Output Byte Select logic outputs are high impedance.

The Tag outputs are always enabled. All five FIFO ICs have a common reset line, MRL.

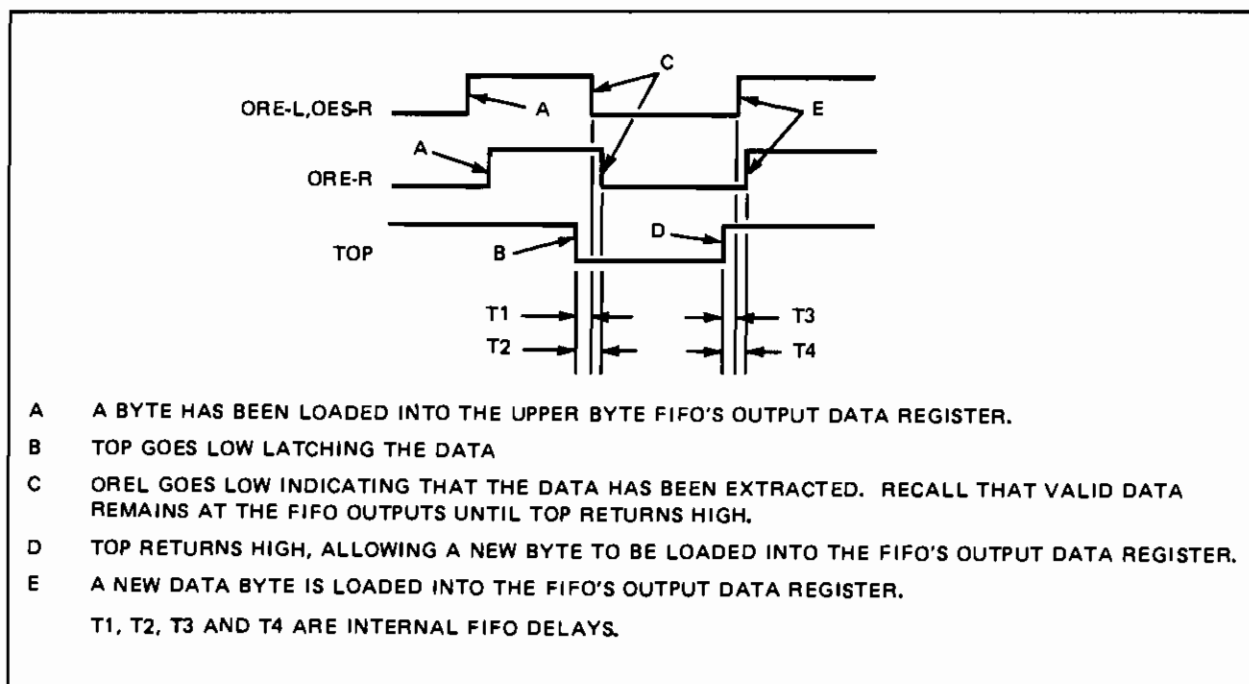


Figure 3-3. Upper Byte FIFO Unloading

3.9 OUTPUT BYTE SELECT LOGIC

The Output Byte Select Logic (U36) [3B-3] enables the Upper Byte FIFO's outputs to the OUTBUS lines when the DI is transmitting data to the disc in packed data format. As discussed above, U36's outputs are enabled when RCV is low and OBP is high. Otherwise the outputs are high impedance.

3.10 OUTPUT DATA SELECT

A Quad 2 to 1 multiplexer (U43) [3B-5] was used with the PACK bit of the Control Word Register as the select and its outputs always enabled. The outputs provide the ATNOUT and EOIOU signals sent to the bus transceivers and the values of bits 8 and 9 of the Input Data Register or Output Byte, depending on what type of transfer is taking place. Figure 3-4 summarizes the function of the Input and Output Data Selectors.

		PACK	
		0	1
RCV	0	D18 → ATNOUT O19 → EOIOU	D18 & 9 TO OUTPUT BYTE SELECT BITS 1 & 2 ATNEN → ATNOUT EOIL80 → EOIOU
	1	EOIN → INPUT DATA REGISTER, BIT 9 ATNIN → INPUT DATA REGISTER, BIT 8	D18 & 9 TO INPUT DATA REGISTER BITS 8 & 9

- (A) IBI TRANSMITTING DATA OVER THE HP-IB IN UNPACKED DATA FORMAT. D18 AND D19 CORRESPOND TO THE ATN AND EOI VALUES ASSOCIATED WITH THE DATA BYTE D17-0 AND ARE OUTPUT TO THE HANDSHAKE AND CONTROL LINE BUS TRANSCEIVERS AS THE DATA BYTE IS OUTPUT TO THE DATA TRANSCEIVERS.
- (B) IBI TRANSMITTING DATA OVER THE HP-IB IN PACKED DATA FORMAT. THE UPPER BYTE (D18-15) IS OUTPUT TO THE BUS INTACT. ATNOUT IS DETERMINED BY THE CONTROL WORD REGISTER, EOIOU BY THE CONTROL WORD REGISTER AND THE END-OF-DATA DETECT LOGIC.
- (C) IBI RECEIVING DATA FROM THE HP-IB IN UNPACKED DATA FORMAT. THE EOI AND ATN VALUES ASSOCIATED WITH EACH BYTE ARE LOADED INTO BITS 9 AND 8 OF THE INPUT DATA REGISTER AS THE DATA IS LOADED INTO BITS 0-7.
- (D) IBI RECEIVING DATA FROM THE HP-IB IN PACKED DATA FORMAT. THE UPPER BYTE IS LOADED INTO THE INPUT DATA REGISTER INTACT.

Figure 3-4. Function of Input/Output Data Selectors

3.11 INPUT DATA REGISTER

The Input Data Register [3B-3] consists of two 74LS273 Octal D Flip-Flops with a positive-edge-triggered clock and direct clear input. The clear signal is Master Reset and the clock is Input Register Loaded. Inputs come from the FIFOs and Output Data Select Logic (EOI and ATN during unpack input transfers). The register outputs are input to the Input Data Multiplexer [2A-3].

3.12 END OF DATA DETECT LOGIC

The End of Data Detect Logic [3B-1,2] examines the EORL and EDTFF tags from the Tag FIFO looking for the last byte in an input or output transfer, respectively. The EORL Tag is input to a D-type flip-flop (U114). The flip-flop is clocked by IRL as the data word the EORL Tag corresponds to is clocked into the Input Data Register. The flip-flop output EOR (End of Record Flip-Flop, low true) is input to the Interrupt Source, Mask Logic [3D-7]. This flip-flop is preset by Master Reset.

The EDTFF tag is input to an AND gate (U53-2) [3B-1] which is enabled when the Output Byte Pointer points to the lower byte (OBPL=1; unpacked format or packed format--even number of bytes) or the O/E bit of the Control Register is set (packed format--odd number of bytes). When EDTFF goes high, LEO is generated [3B-1]. If the EOIEN bit of the Control Word Register [2C-5] is set, EOILBO also goes high [3B-1].

3.13 TRANSMIT HANDSHAKE LOGIC

The Transmit Handshake Logic [1A-7] controls the handshake for output transfer. It generates DAVOUTL and monitors the NRFDL and NDAFL lines. It also generates THSKL, which is used as a clock by the FIFO load [3B-7] and Last Byte Out Logic [3A-7] blocks.

Figure 3-5 shows the timing and signal transitions within the Transmit Handshake Logic. The RC delay circuits provide the 1.0 microsecond delay before transfer of the first byte and the 350ns delay prior to each subsequent byte as required by the IEEE 488-1978 Standard. When the last byte has been transferred, TRDYL remains high, freezing the bus with DAVOUTL held high.

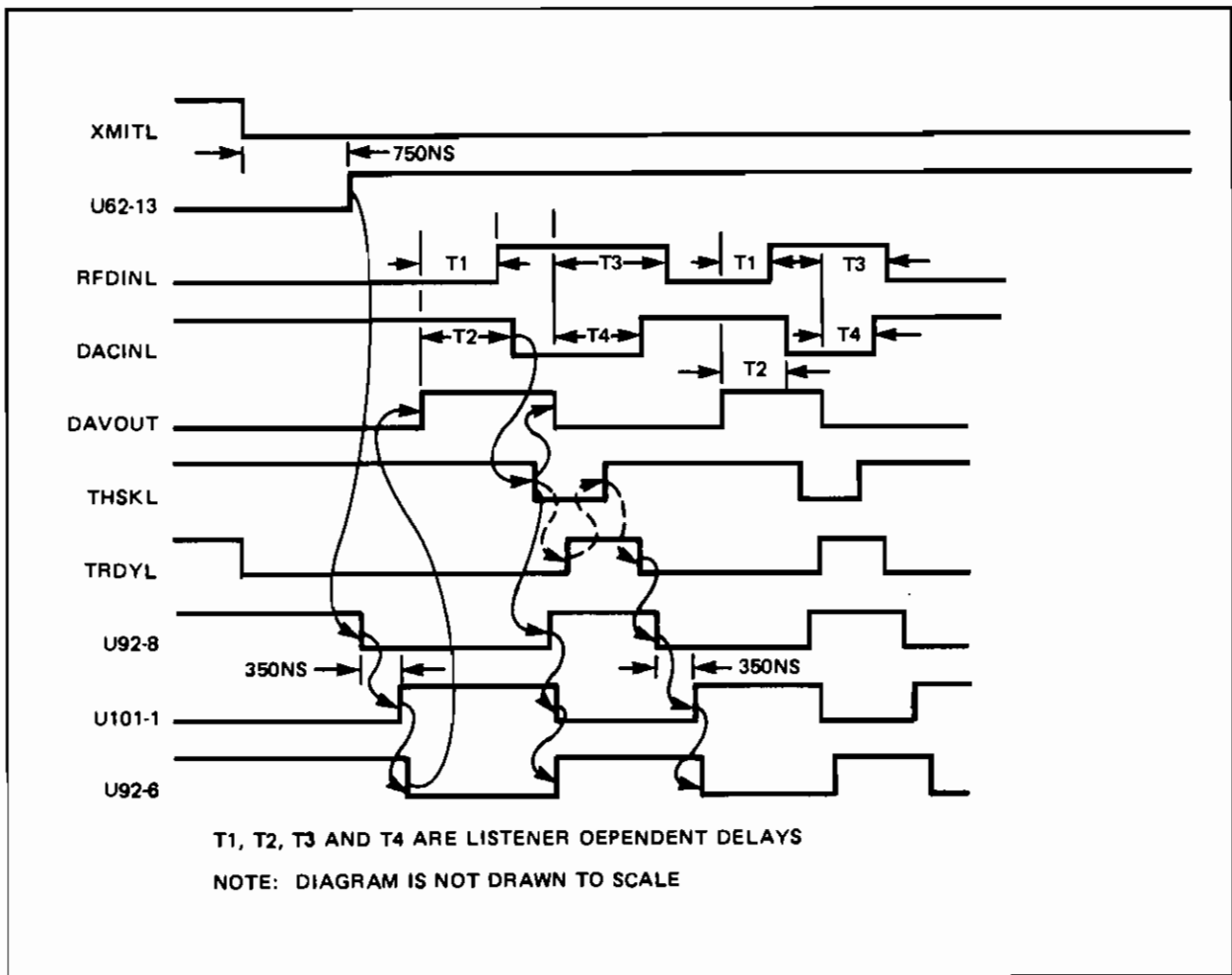


Figure 3-5. Transmit Handshake Logic Timing

3.14 HOOKS FOR THE DIAGNOSTIC

Included in the Transmit Handshake Logic [1A-7] and the Output Data Register [2C-2] is logic used by the diagnostic program to enable the DI To "talk to itself". This logic is enabled by setting bit 7 (DIAG) in the Control Word Register.

The test sequence loads the FIFOs with known data, cycles that data through the FIFO out to the bus transceivers and back into the FIFOs, and then reads the data back into the CPU to check its validity. The Receive Handshake, Transmit Handshake, FIFO Load and Unload logic is checked in addition to the FIFOs and the Bus Transceivers.

The diagnostic first fills the FIFOs with data, then the card is configured with the DIAG,T,L and CIC bits set. The card is then enabled to both receive and transmit data. The transceivers have their drivers enabled to their receivers so the OUTBUS and INBUS lines are tied together and DAVOUT is tied to DAVIN, RFDOUT to RFDIN, and DACOUT to DACIN. There is valid data on the OUTBUS/INBUS lines.

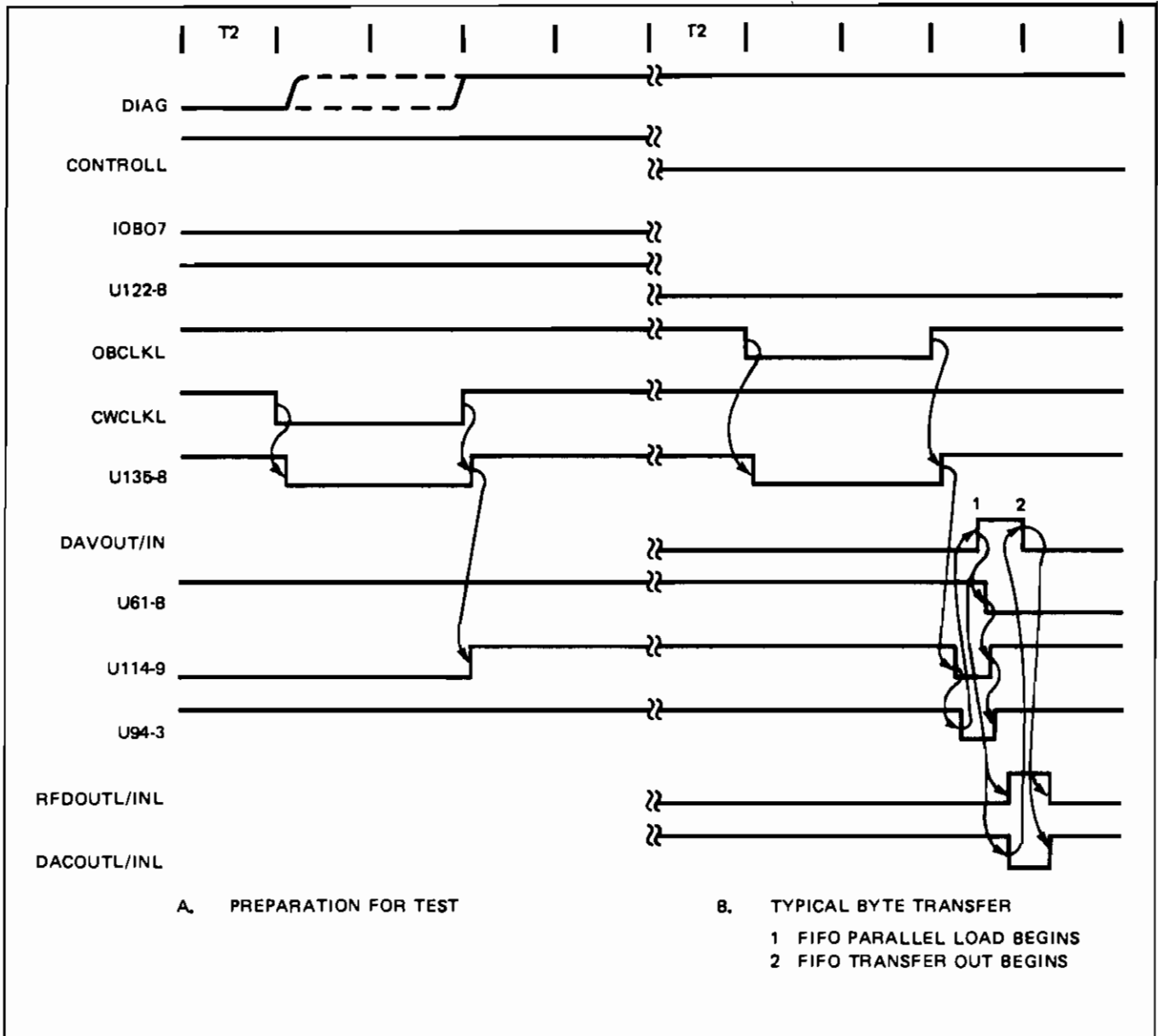


Figure 3-6. Diagnostic Timing Logic

When the card is configured with control word 207 (octal) the flip-flop U114-9 [1A-6] is set, disabling U94-3 [1A-6] (Figure 3-6). The card is placed in data mode and an OTA DI,C or OTB DI,C instruction is executed for each byte rotated. Recall that an OT* instruction results in the signal OBCLKL.

On the rising edge of OBCLKL U114-11 [1A-6] is reset and U94-3 [1A-6] goes low causing DAVOUT (and DAVIN) to be asserted. The FIFO load sequence begins. When the byte is loaded DACOUT (U42-13)[1B-6], DACIN, RFDOUT, and RFDIN are asserted. When DACINL goes low U72-9 [1A-5] is set and DAVOUT (and DAVIN) goes low. A new byte is now transferred to the FIFOs outputs. RFDOUT (RFDIN) and DACOUT (DACIN) return low but further transfers are inhibited until the next OT* DI,C instruction is executed (Figure 3-6).

Note that a DIAG bit value of one disables the Output Data Register (U52-6) [2D-2], causing its outputs to be high impedance. For all other transfers or tests the DIAG bit is clear and U114-9 [1A-6] is always a zero, enabling U94-3. Thus it is as if U92-6 [1A-6] was tied directly to U72-11 and U72-12 [1A-6].

3.15 RECEIVE HANDSHAKE LOGIC

The Receive Handshake Logic [1B-6] controls the bus handshake for input transfers. It monitors the DAVIN line and generates RFDOUTL and DACOUTL accordingly. RHSKL is also generated and serves as a clock input to the FIFO Load Logic and Last Byte In Logic [3C-7].

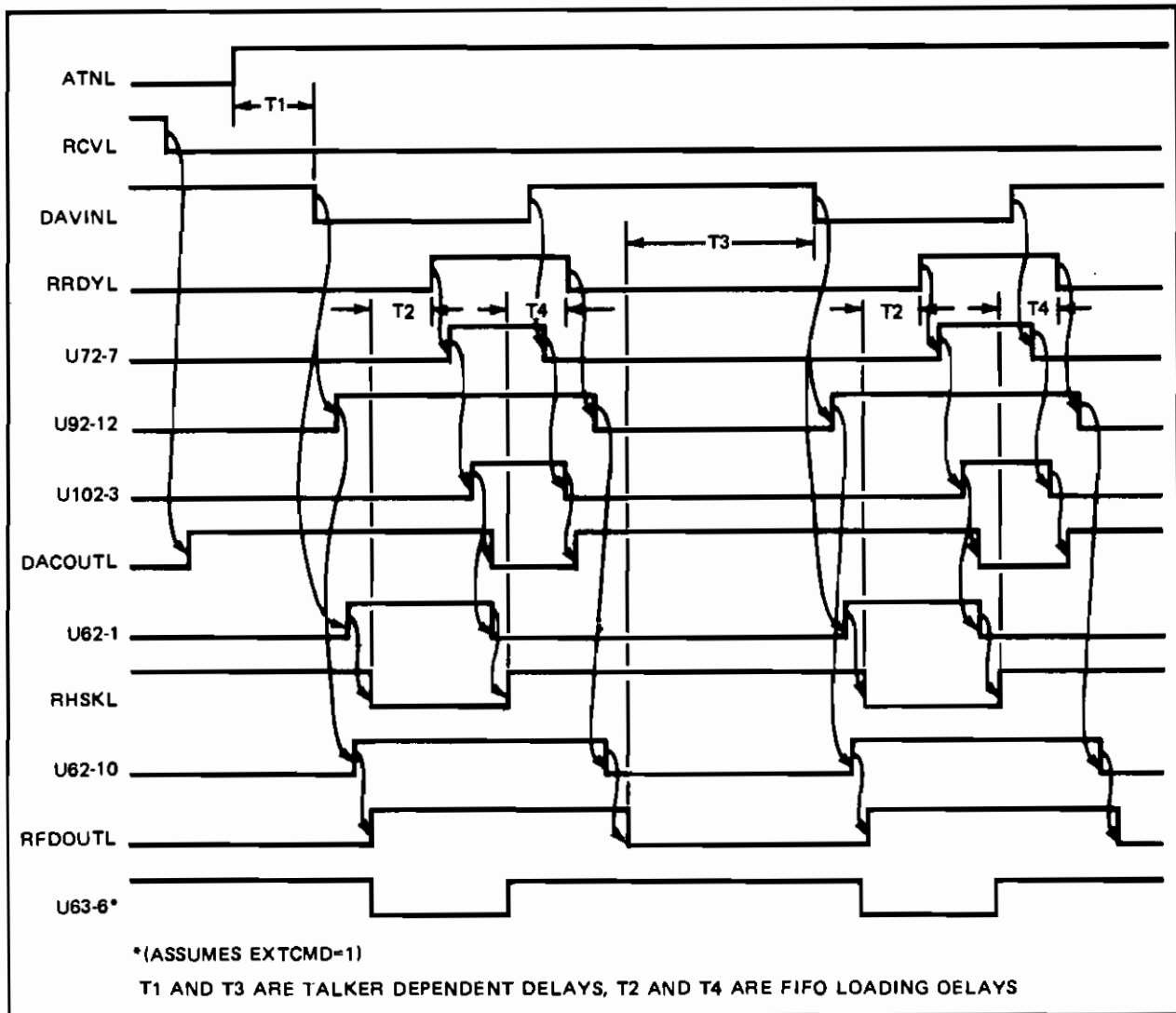


Figure 3-7. Receive Handshake Logic Timing

Figure 3-7 shows the timing in the RSHK logic. In a typical input transfer where the DI is CIC, RCVL goes low when the DI is made a listener.

When the last byte in a transfer is received, RRDYL remains high freezing the RSHK logic with RFDOUTL high. Note that RFDOUTL may also be asserted by setting the NRFD bit of the Control Register [2C-4,5] to one (U52-10)[1B-5]. DACOUTL will remain low until DAVL returns high at which time DACOUTL goes high.

3.16 THE LAST BYTE IN LOGIC

The Last Byte In Logic [3C-7] performs three distinct functions. During an output transfer, the LBI Logic generates ORLL used by the FIFO Load Logic to generate the FIFO loading signals PLHI and PLLO. The timing for this is shown in Figure 3-8.

Figure 3-8 also shows the timing for loading a parallel poll response. In this case the loading sequence is initiated by PPRLL [1C,D-4,3 and 3C-7,8]. Because PPRLL remains low, the ORLL signal is generated repeatedly until the FIFO fills. This feature is not disastrous since the FIFOs will be cleared after the PP response is read by the CPU; thus the multiple loading is ignored.

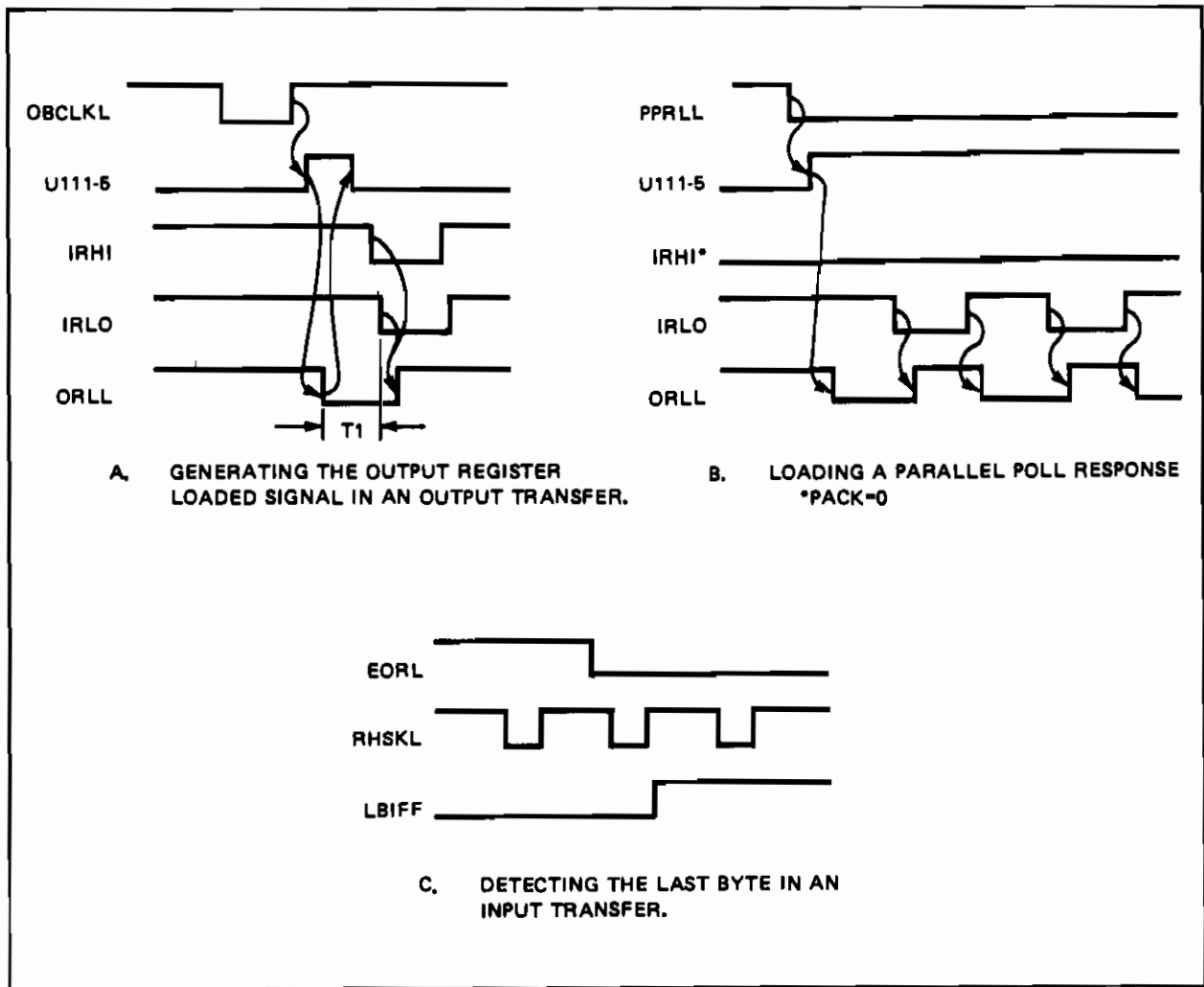


Figure 3-8. Last Byte In Logic

Lastly, the DI Logic detects the last byte in an input transfer. If the LFEN and/or the EOIEN bits of the Control Register are one, then EORL (END of Record, low true) from U113-6 [3C-7] will be generated when a LF or EOI is received by the DI. The Last Byte In Flip-Flop is then reset on the rising edge of RHSKL to assert LBIFF high.

3.17 FIFO LOAD LOGIC

The FIFO Load Logic [3B-7] generates the FIFO loading signals for all input and output transfers, and for loading parallel poll responses.

The timing for an input transfer is given in Figure 3-9. Packed data format and an odd number of bytes have been assumed. RHSKL causes the Input Byte Pointer to switch to select either PLHI or PLLO [3C-7]. A master reset is executed before a transfer in packed format to set the IBP to the upper byte.

For a transfer in unpacked data format, PACK is low and the IBP is held pointing to the lower byte (U121-4) [3C-7]. Thus PLHI remains low and PLLO is generated for each byte received.

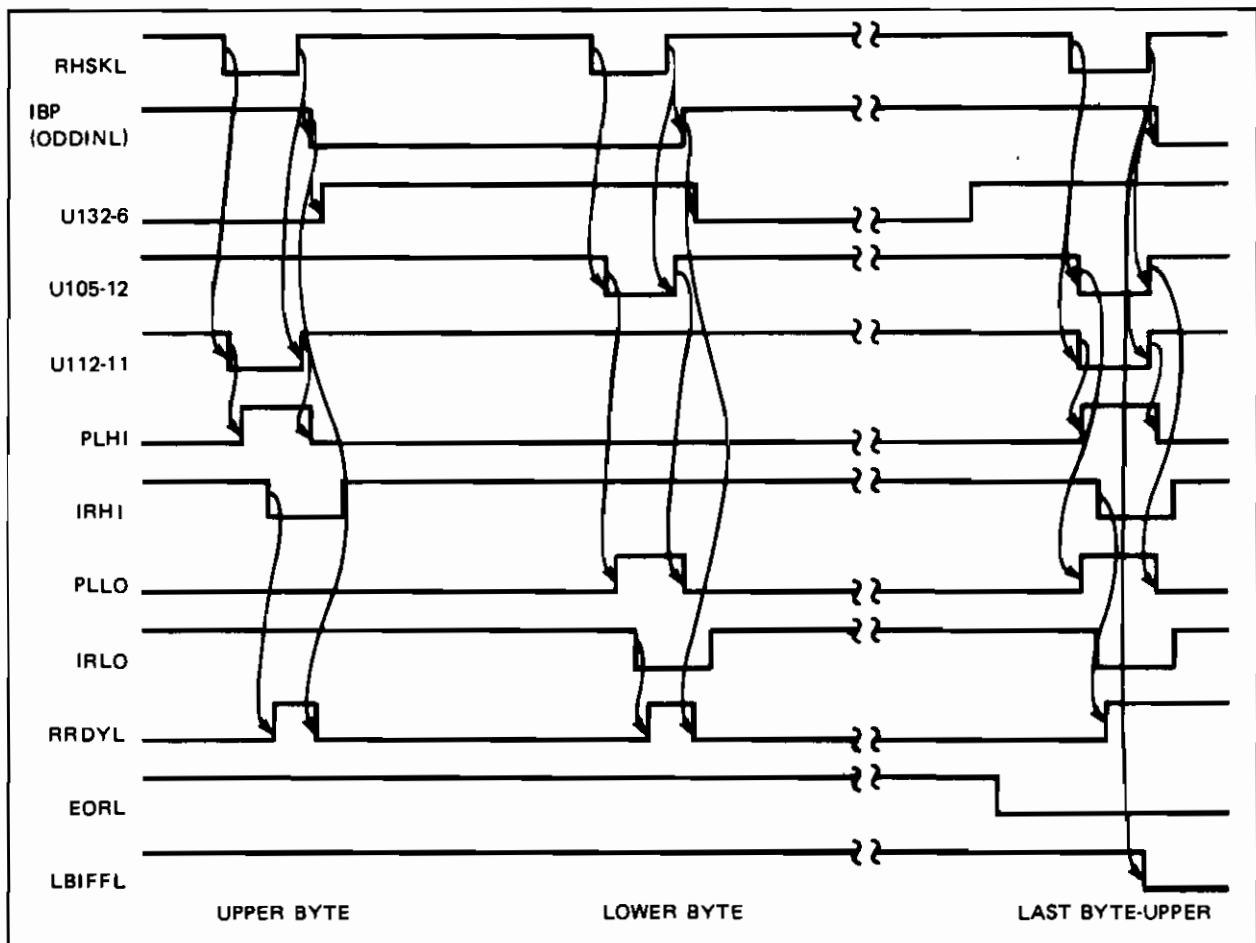


Figure 3-9. FIFO Load Logic (Packed Data Format Input From Bus)

Also shown in Figure 3-9 is the loading of an odd numbered last byte. When the last byte is received, EORL goes low forcing [3C-7] to a one. Thus U106-12 [3C-6] is enabled and both PLHI and PLL0 are generated. The odd numbered last byte is loaded into both the upper and lower byte FIFOs. On the rising edge of RHSKL the LBI Flip-Flop (U111) [3C-6] is set. LBIFFL (U111-9) disables the RRDYL line (U133-8) [3B-7] preventing further input transfers. The IBP pointer is set to the lower byte in anticipation of another byte. Thus ODDIN (U121-6)[3C-7], the complement of IBP, is high, indicating an odd number of bytes was input.

If the last byte is an even numbered byte, it is loaded into the lower byte FIFO and LBIFFL disables the RRDYL line as above. The IBP is set to the upper byte and ODDIN is low indicating that an even number of bytes was transferred.

When the FIFOs are being loaded with the Output Data Register contents or with a parallel poll response, only gates U112-6 and U112-8 [3C-7] of the FIFO Load Logic are used (Figure 3-10). Because RHSKL is high, the gate outputs U106-12 and U112-11 are also high enabling the above gates to generate PLHI and PLL0 each time ORLL is generated. If unpacked data format is used, IRHI (102-11) [3C-5] remains low and the Upper Byte FIFO is ignored.

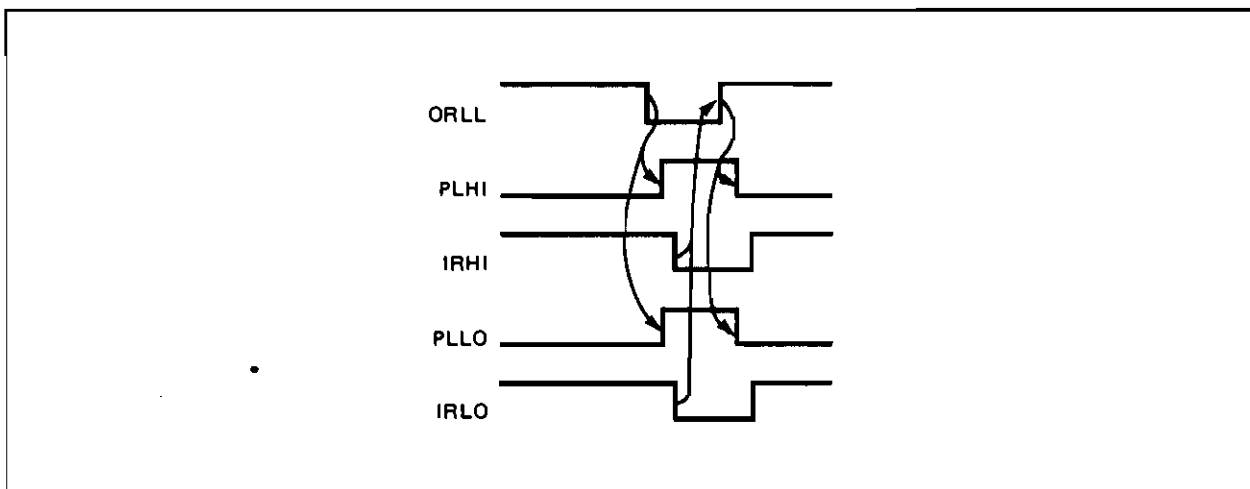


Figure 3-10. FIFO Load Logic (Load Output Data Register Into FIFOs)

3.18 FIFO UNLOAD LOGIC

The FIFO Unload Logic [3B-7] controls the FIFO unloading signals TOPHI (U122-3) and TOPLO (U122-11). Data is output to the disc or loaded into the Input Data Register [3B-3,4].

Figure 3-11 shows the timing for an output transfer in packed format. The Output Byte Pointer causes the logic to alternate between generating TOPHI and TOPLO from THSKL [3B-8]. A master reset before the transfer in packed format guarantees the OBP points to the upper byte first (U121-13) [3B-8].

If unpacked data format is used, PACK is low causing the OBP (U121-8) to point to the lower byte continuously. Thus, TOPHI remains high and ORHI remains low (U102-8) [3C-5] throughout the transfer. TOPLO is generated with each THSKL to load the Lower Byte FIFO.

Also shown in Figure 3-11 is the unloading of the last byte. If the last byte is the lower byte (OPB=0) or the last byte is the upper byte and the O/E bit in the Control Word Register is equal to one, then the Last Byte Out Flip-Flop is set on the rising edge of THSKL. LBOFFL inhibits further transfers by holding TRDYL high (U113-11,12) [3B-6].

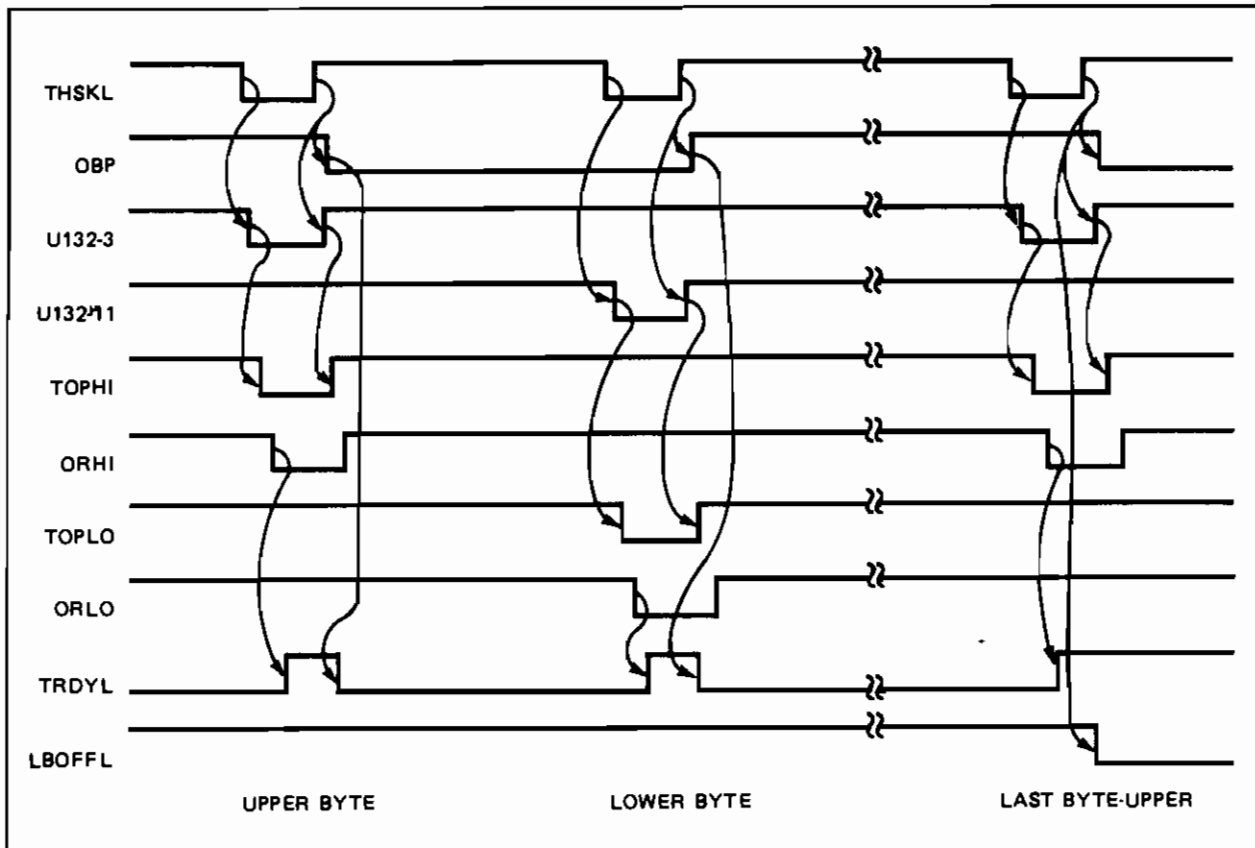


Figure 3-11. FIFO Unload Logic (Packed Data Format Output to Bus)

Figure 3-12 shows how the FIFO unloading signals are generated when the FIFOs are being unloaded into the Input Data Register. THSKL is high causing the outputs U132-3 and U132-11 [3B-7] to be high, enabling U122-11 and U122-3 respectively. The LBO Logic generates TTIRL (U123-9) (Transfer To Input Register, low true) each time a word is to be input. TOPHI and TOPLO are generated simultaneously from TTIRL. None of the other FIFO Unload Logic is used.

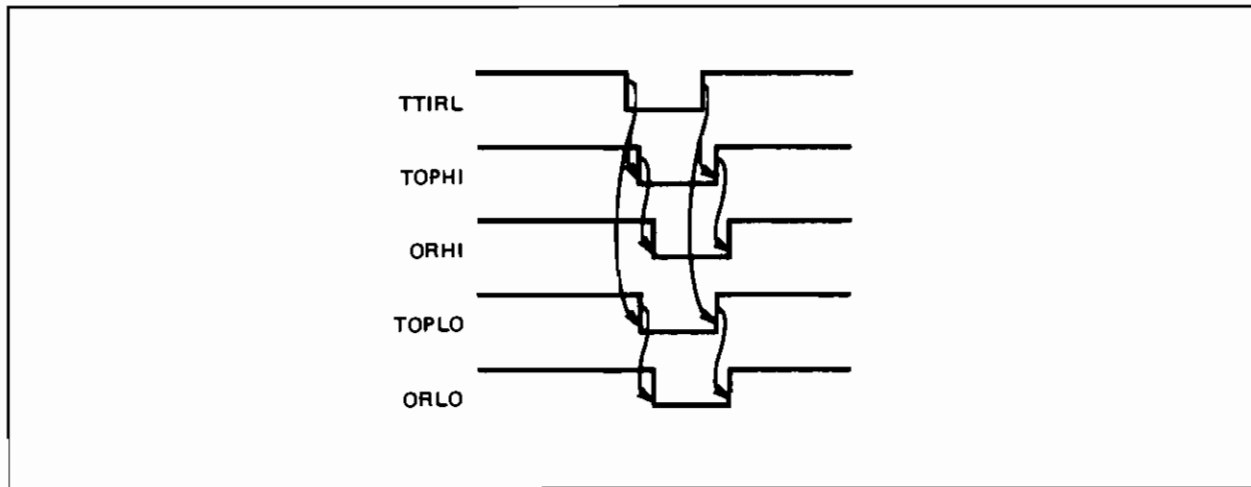


Figure 3-12. FIFO Unload Logic (Packed Data Format, FIFOs to Input Data Register)

3.19 LAST BYTE OUT LOGIC

The LBO Logic [3A-7] consists of four parts; the LBO Flip-Flop (U131-9), the Generate Service Request Logic (U133-6) [3A-6], 5GENSRQL logic (U33-3,U85,U62-4) [3A-5,6], and the Input Register Load Logic (U131) [3A-7].

Figure 3-13 shows the timing for the Input Register Load (U131-5) [3A-7] and 5GENSRQ logic [3A-4,5]. Transfer of the first word into the Input Data Register is initiated by Output Ready as soon as both ORHI and ORLO are high (U101-13) [3A-8]. Transfer of each succeeding word is initiated by IRL (3A-7), [U131-6], providing that the word is available at the FIFO outputs.

If unpacked data format is used, then Output Ready is equivalent to ORLO (3A-8). The LBO and IRL Flip-Flops are reset by the master reset signal. The IRL logic is enabled only when RCV is a one (U83-2) [3A-8], i.e., when the DI is inputting data from the disc.

After the last word is loaded into the Input Data Register, OR remains low, disabling further TTIRL signals. After the last word is read into the CPU, IRL remains low and GENSRL (5GENSRQL) remains high. See the discussion of GENSRL and 5GENSRQL under the heading "Service Request Logic".

The GENSRQ logic is also used during output transfers. GENSRQL (and 5GENSRQL if jumper W1 is in position "A") is generated when the DI is a talker and IRLO is high. Recall that as long as IRLO is high there is room for another word.

The LBO Flip-Flop is straightforward (U131-11) [3A-8]. The Flip-Flop is clocked on the rising edge of THSKL. Its input is the Last Byte Out Signal generated by the End of Data Detect Logic [3B-1, 3B-2]. When LBO is high, the Flip-Flop is set and LBOFF is high. LBOFF remains high until reset by a Master Reset signal.

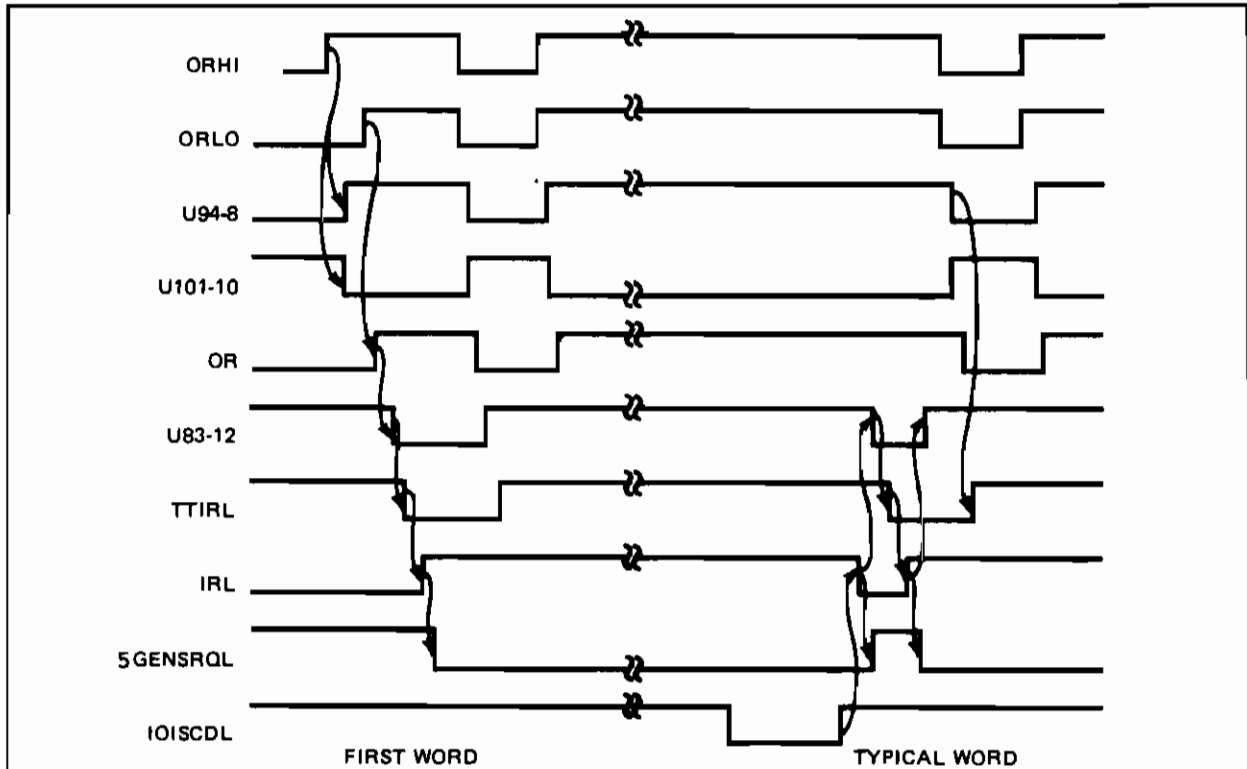


Figure 3-13. Last Byte Out Logic

3.20 INTERRUPT SOURCE, MASK LOGIC

Table 3-1 summarizes the function of the Interrupt Source, Mask Logic [3D-7]. The first column lists the signal which is to result in a "set flag" or an interrupt request. Column two lists the bits in the DI Control Register which must be set and other conditions which must be met so that the signal in column one can generate SETFLG. The third column is a brief discussion of the use of each interrupt. The SETFLG signal causes the DI Flag Flip-Flop (U126) [3C-7] to be set. Software can check for this condition or, if interrupts are enabled, the DI will assert IRQ and FLGL. For most cases an MR is required to disable the SETFLG signal.

Table 3-1. Interrupt Source, Mask Logic

SIGNAL	CONDITIONS	DESCRIPTION
IRL	IRLEN	Typically used for a software controlled input transfer. Interrupt request generated when data, command, or parallel poll response is in input data register.
IFCFF	IFCEN, SYSTL	The IFC flipflop is set whenever an interface clear is issued to the bus. An IFC can only be generated by the system controller, thus if the IBI is SYSTL then IFCFF is ignored.
RENIN	RENEN, SYSTL	Used to detect a remote enable signal on the bus. REN can only be generated by the system controller, thus if the IBI is SYSTL then RENIN is ignored.
EORFF	IRL	Typically used for a software controlled input transfer to detect the last byte. The EOR flipflop is set when the byte/word tagged with EOR or a LF is loaded into the input data register.
SRQIN	SRQEN, CIC	Used to detect a service request on the bus. The IBI must be controller in charge to acknowledge a SRQ. Note that the IBI can generate an SRQ only if it is not CIC.
LBOFF	LBOEN	Typically used in a software controlled output transfer to detect the end of transfer. The LBO flipflop is set when the last byte is output to the bus.

3.21 INPUT MULTIPLEXER

The DI's Input Multiplexer [2A-1 to 4] is made up of 16 dual line-drivers. Each line driver has a data bit from the Input Data Register [3B-2,3,4,5] as one input and a status bit as the other. The Input Mux Enable Logic [2A-6,7] provides the select signals which enable these inputs to the CPU Input Bus.

3.22 INPUT MULTIPLEXER ENABLE LOGIC

The Timing for the Input Mux Enable Logic [2A-6,7] is shown in Figure 3-14. When the Control Flip-Flop is set, IOI is used to generate the Data Select signal. The status word is selected when the Control Flip-Flop is cleared.

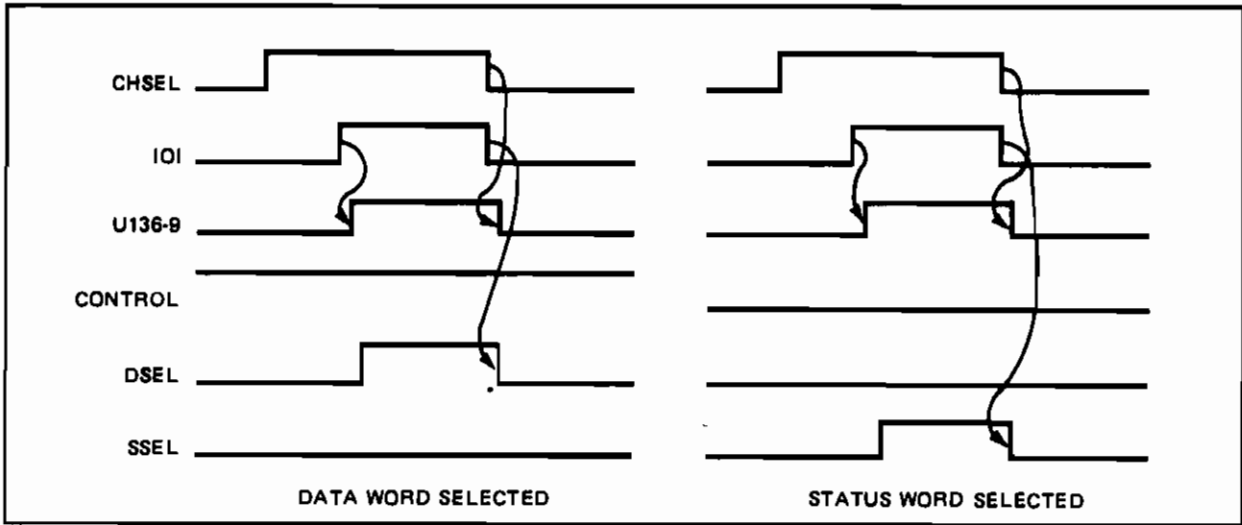


Figure 3-14. Input Multiplexer Enable Logic

3.23 CLEAR FLAG DETECT FLIP-FLOP

The Clear Flag Detect Logic [2B-6] is used to detect the last word of a software controlled output transfer in packed format. The flip-flop is reset at the beginning of each machine cycle. If a CLF [2D-8] is executed during that cycle, the flip-flop is set (see Figure 3-15); if not, NCLFL [2B-6] remains low. If unpacked data format is used, the flip-flop output remains high.

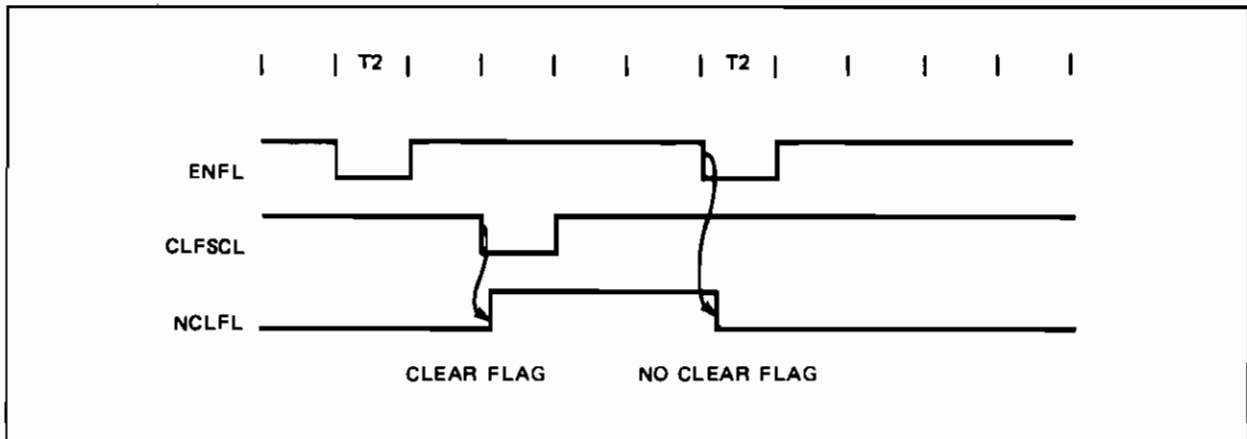


Figure 3-15. Clear Flag Detect Flip-Flop (Assume Pack=1)

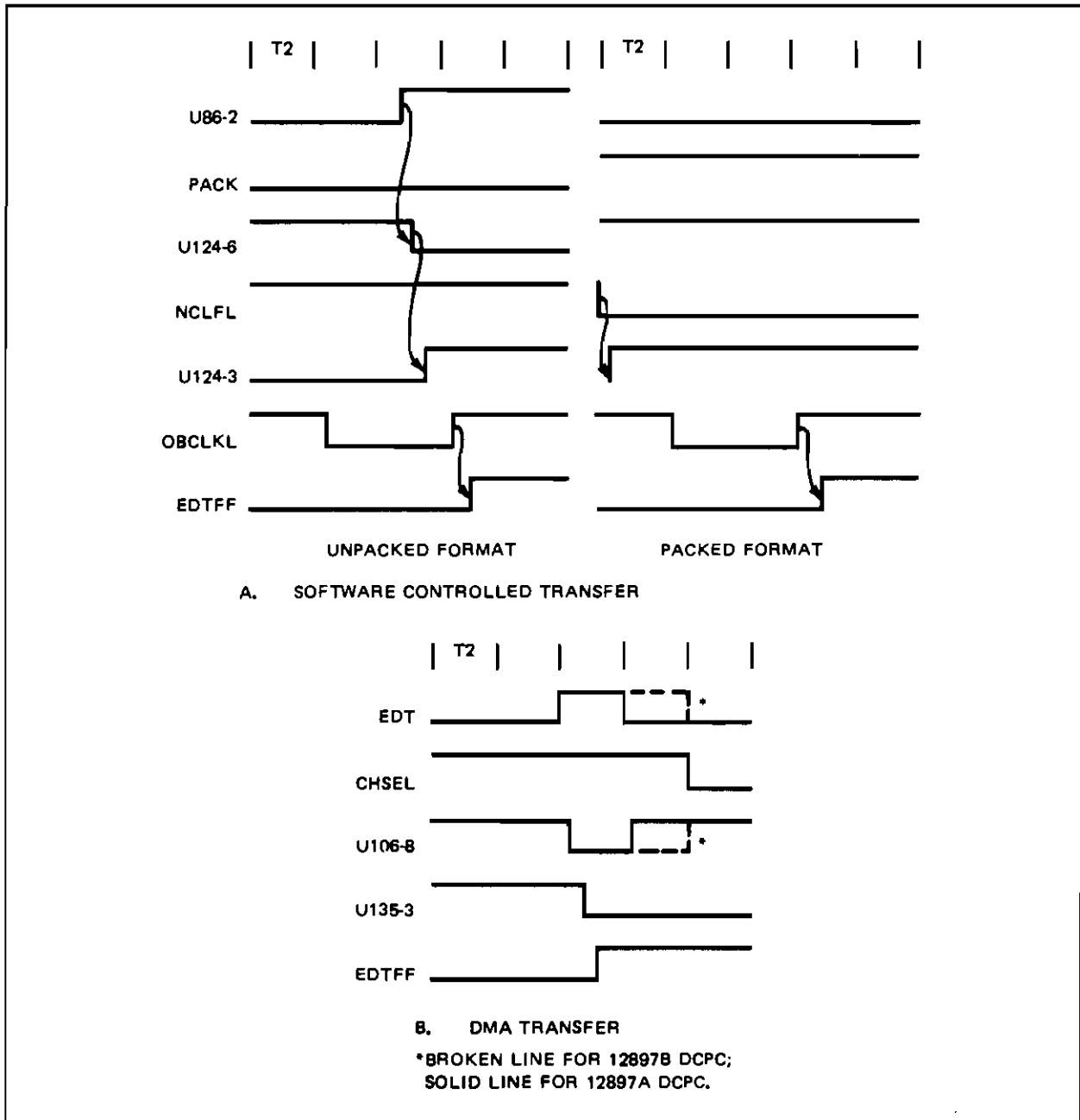


Figure 3-16. End Data Transfer Flip-Flop

3.24 END OF DATA TRANSFER FLIP-FLOP

The EDT Flip-Flop [2B-5] [U134] can be set three different ways, illustrated in Figure 3-16. In a software-controlled transfer in unpacked format U124-6 [2C-5] goes low when bit 15 of the Output Data Register [2C-3] is a one. U124-3 goes high and the EDT flip-flop is set on the rising edge of OBCLKL. In a software-controlled transfer in packed format, the last word is output without a CLF. NCLFL remains low and U124-3 is high. Again the flip-flop is set on the rising edge of OBCLKL. In a DMA transfer the flip-flop is set when the DCPC asserts EDT (U106-8) [2A-7].

The AND gate [2B-5] guarantees that once set, the EDT Flip-Flop will remain set until a Master Reset is generated. This prevents the flip-flop from being reset on the rising edge of OBCLKL [2D-6] during a DMA transfer.

3.25 SERVICE REQUEST LOGIC

The SRQ Logic includes the SRQ Flip-Flop (U136-6) [2B-5], the AOI gate used to generate SRQ (U137-7) [2A-7], and U124-11 (Figure 3-17). Notice in Figure 3-17 that the flip-flop is clocked (U136-6) by ENF at the beginning of each T2 time period. If 5GENSRQL (or GENSERQL, see information on Jumper W1, below) is low the flip-flop goes high. SRQ is then asserted if CONTROL (not shown in Figure 3-17) is high (data mode) and U124-11 is high.

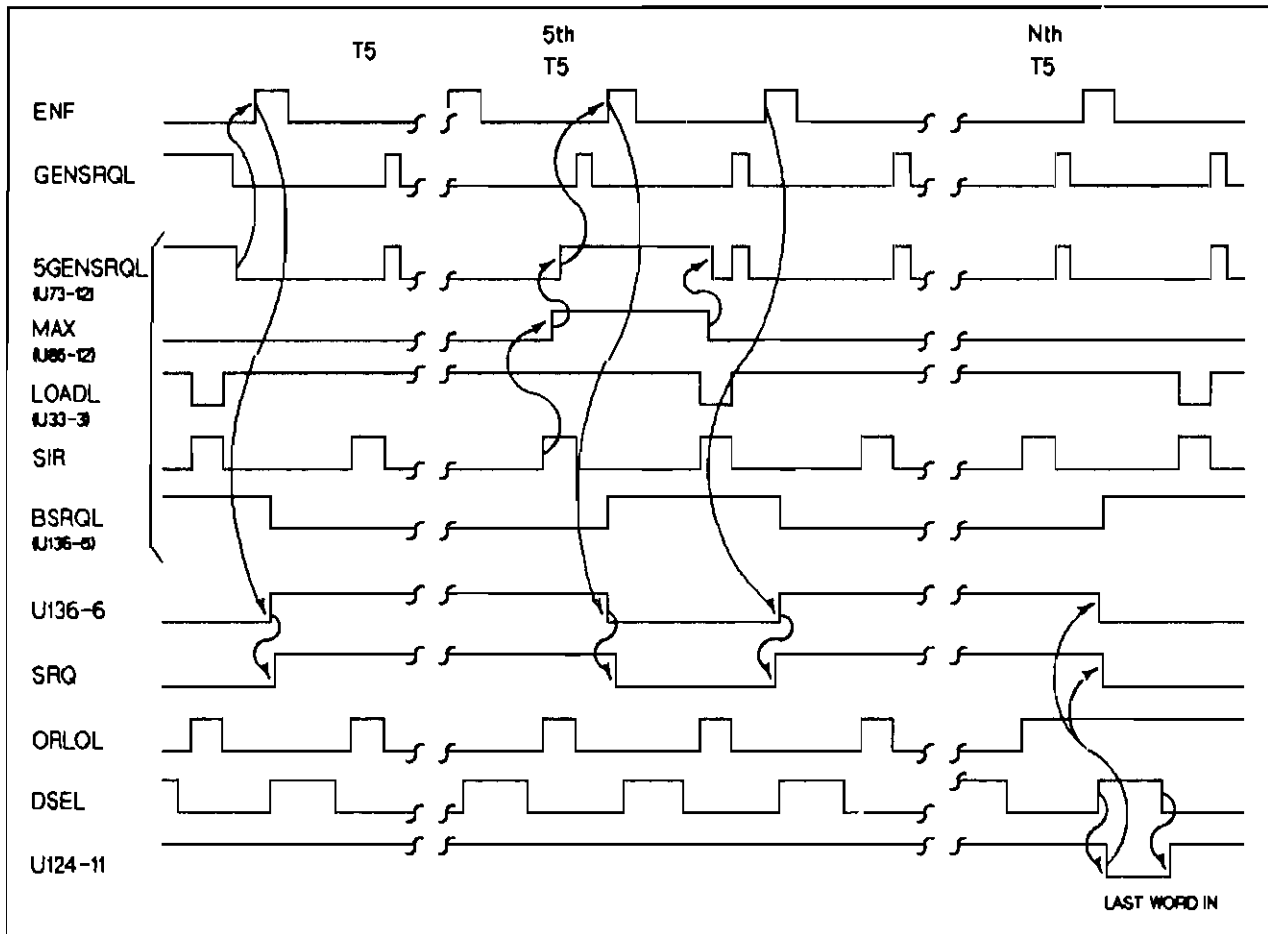


Figure 3-17. Service Request Logic (Input Transfer Assume Control=1)

U124-11 [2B-6] is used to "reset" the SRQ Logic when the FIFOs are empty (ORLOL remains high) and the last word is being read by the CPU. SRQ is pulled low before T4, which is when the CPU would examine SRQ. Thus no further machine cycles are requested.

Jumper W1 directs the signal GENSERQL to or around a wired-OR gate [3A-4] (U62-4,5,6; U73-12,13). Once the signal has passed through the jumper it is

known as 5GENSRQL. With the jumper in the "B" position, the wired-OR gate does not control 5GENSRQL. Because the DI is usually the highest priority IO interface, it can prevent other peripherals from gaining access to the computer for a relatively long time (microseconds). Some peripherals will time-out and go offline if they cannot gain access to the computer in a fixed time.

With jumper W1 in the "A" position, GENSRL will pass through the wired-OR gate. That gate is controlled by the counter at U85 [3A-4]. The counter counts the SIR (Service Interrupt Request) that occurs every T5 time period. After five T5's, the counter and wired-OR gate will change 5GENSRQL to high, if it was active. As Figure 3-17 illustrates, 5GENSRQL will remain high for one sequence of machine periods (T5 to next T5), long enough for a lower priority device to transfer one word.

See the Installation section "Setting the SRQ Control Jumper" in Chapter 2 for information about moving the jumper.

3.26 FLAG BUFFER FLIP-FLOP

The Flag Buffer Flip-Flop (U126-9)[2C-7] is normally set. It can be reset by SETFL if the Flag Flip-Flop is not already set, by POPIO, or by STF. The timing for these is shown in Figure 3-18. The Flag Buffer Flip-Flop is set by a CLF instruction or by IAK [2C,D-8] if the IRQ Flip-Flop (U126-13) [2C-7] is set. However, if SETFLG is true (equals 1) when CLF is executed, then the flip-flop will be reset after executing the CLF instruction. For most cases MR will disable SETFLG.

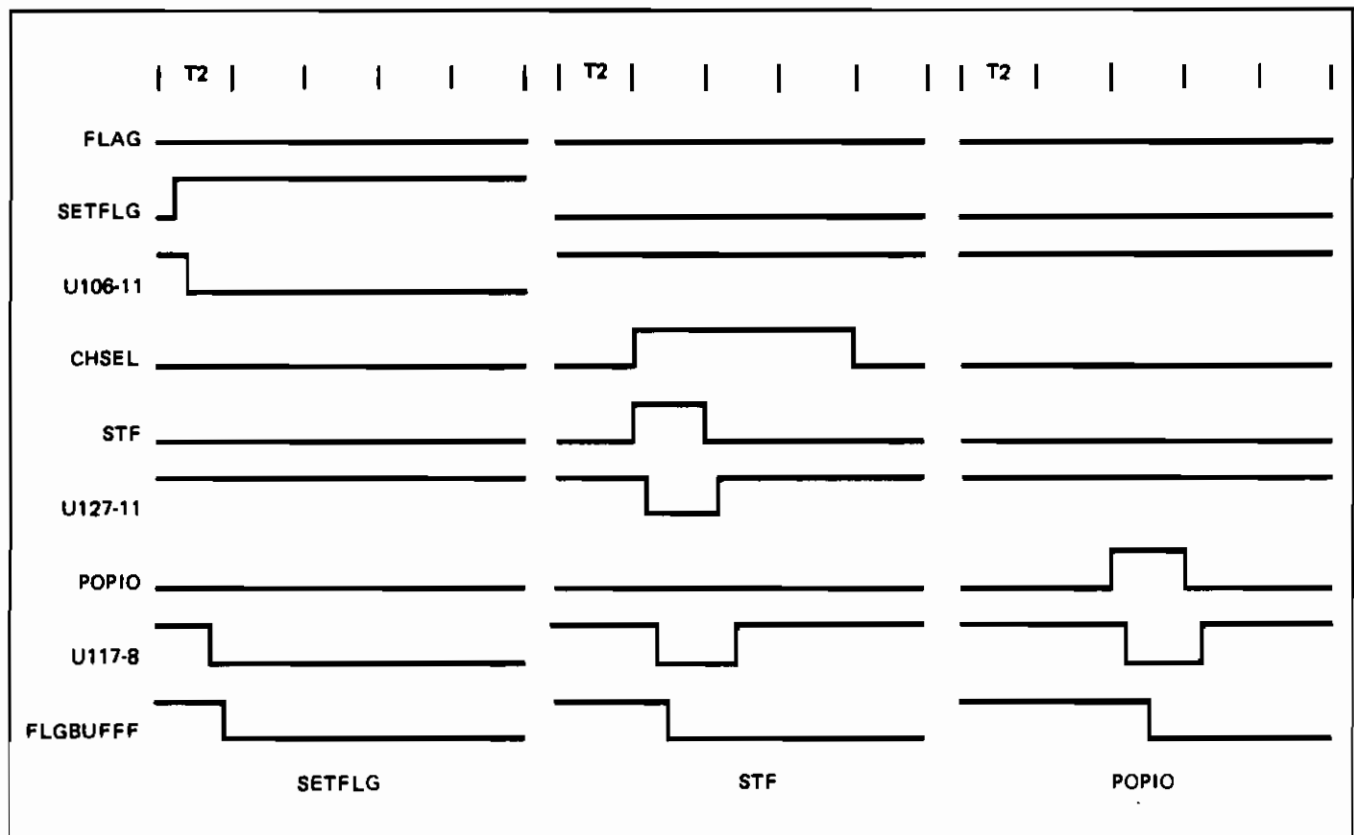


Figure 3-18. Flag Buffer Flip-Flop

3.27 FLAG LOGIC

The Flag Logic [2C,D-7] is made up of three logical blocks: the Flag Flip-Flop, the Priority Line Logic, and the Skip Flag Logic.

The Flag Flip-Flop (U126-13) is normally reset. It is set by ENF if the Flag Buffer Flip-Flop has been reset. The Flag Flip-Flop is reset by a CLF [2D-8].

When the Flag Flip-Flop is set, CONTROL (U116-10) [2C-7] is high (data mode), and IEN is high (interrupts are enabled) then U117-6 [2C-6] goes high. If PRH [2C-6] is high then a high value at U117-6 causes PRL to go low (U107-7) [2C-7], preventing lower priority devices from generating interrupts (see Figure 3-19).

The Skip Flag Logic consists of an AOI gate (U107-9) [2B-7] with SFS, FLAG and CHSEL as one set of inputs and SFC, FLAGL and CHSEL as the other. SKF is generated accordingly (see Figure 3-20).



Figure 3-19. Flag Flip-Flop

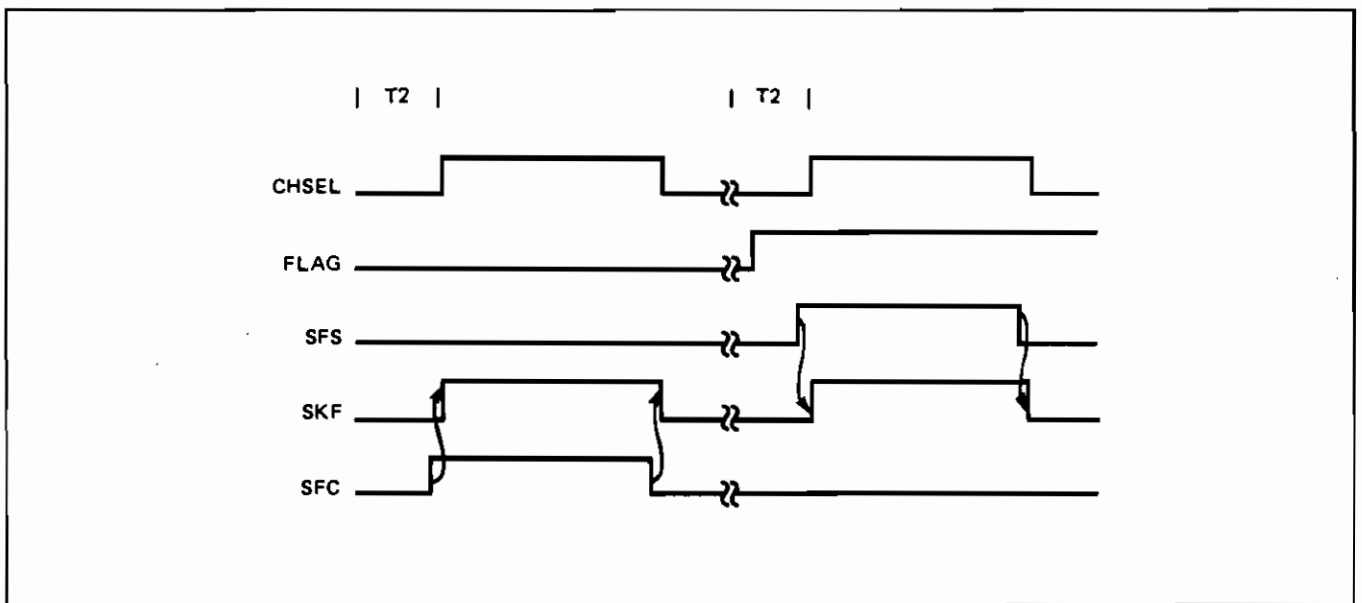


Figure 3-20. Skip Flag Logic

3.28 INTERRUPT REQUEST LOGIC

The IRQFF [2B-7] is normally reset. Three conditions must be met to set the flip-flop. U117-6 must be high (FLAG=CONTROL=IEN=1), the Flag Buffer Flip-Flop must be reset and PRH [2C-8] must be high. If these conditions are met, the IRQFF will be set by SIR [2B-8]. IRQFF goes high causing the CPU backplane signals IRQ (Interrupt Request) and FLGL (Flag Signal, Lower Select Code) to go high (U97).

The IRQFF is reset at the beginning of each machine cycle by ENF. Figure 3-21 shows the timing involved in generating an IRQ. During the first machine cycle shown, the Flag Buffer Flip-Flop is reset. At the beginning of the next machine cycle the Flag Flip-Flop is set, U117-6 [2C-7] goes high and PRL goes low [2C-7]. When SIR arrives at T5 the IRQFF is set and IRQ and FLGL are asserted. When the interrupt is acknowledged by IAK the Flag Buffer Flip-Flop is set. The IRQ Flip-Flop is reset at the beginning of the next machine cycle. The Flag and Control Flip-Flops (U126-13) [2C-7] and (U126-4) [2D-7], must be reset by software.

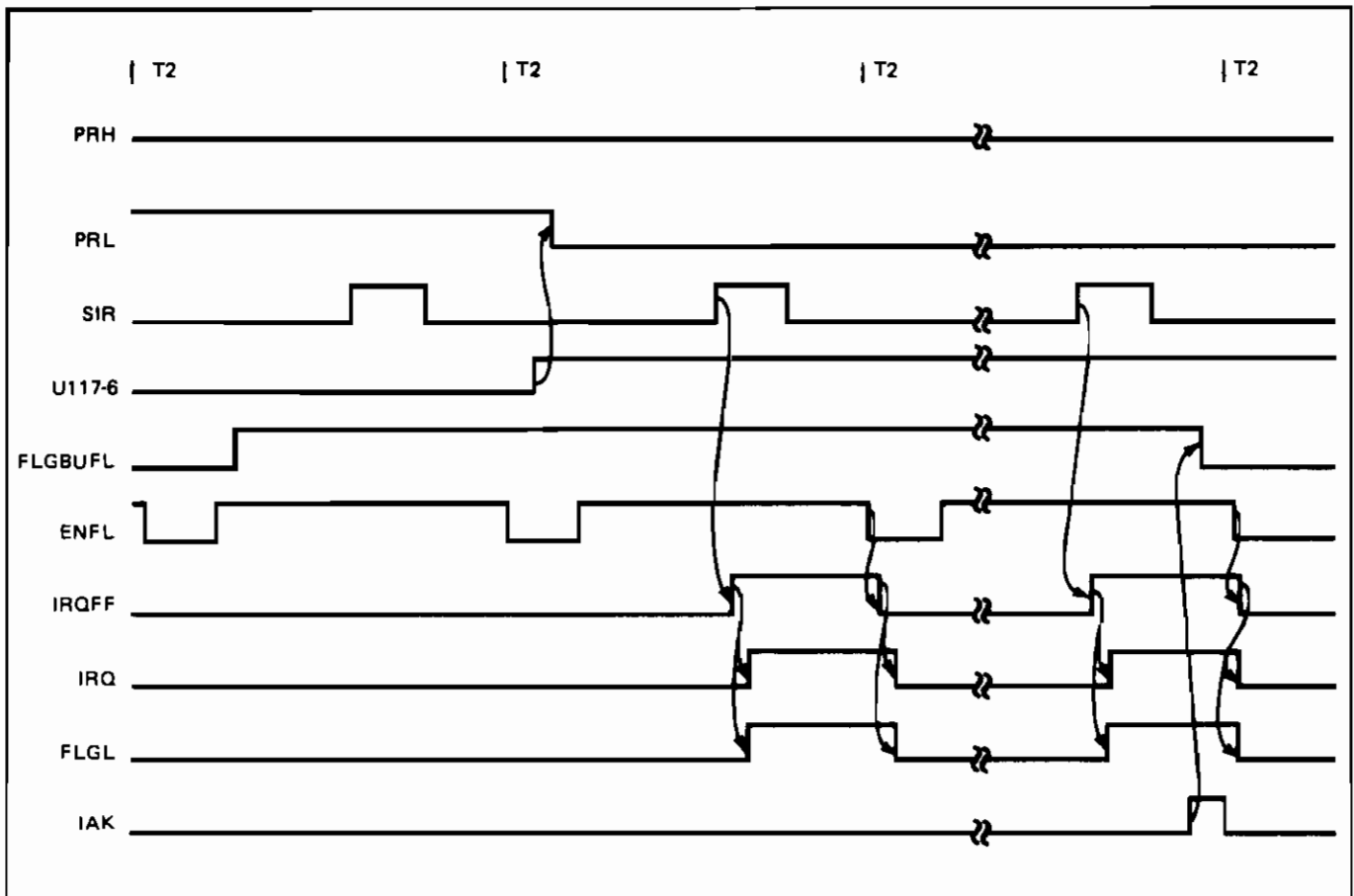


Figure 3-21. Interrupt Request Logic

3.29 INTERFACE CLEAR 100 MICROSECOND TIMER

A Dual Retriggerable Monostable Multivibrator is used for the IFT Timer (U91) [1C-7]. It is triggered when the IFCEN bit of the Control Word Register is set (U91-2) [1D-7], provided the DI is SYSCTL (U91-3) [1D-7]. If SYSCTL is low (card is not controller), the clear overrides the output (U91-13) keeping it low. The external resistor and capacitor are set to guarantee a minimum pulse width of 100 microseconds. IFCOUT is tied directly to the IFCL bus line.

3.30 INTERFACE CLEAR FLIP-FLOP

The IFC Flip-Flop (U123-13) [1B-5] is set whenever an IFC is received by or generated by the DI (since the transceiver for IFCL always has its receiver enabled). The flip-flop is reset by Master Reset.

3.31 PARALLEL POLL CONDUCT LOGIC

The Parallel Poll Conduct Logic [1C-4] timing is shown on Figure 3-22. When PPE and CIC are set in the Control Register, PPC (U73-6) [1C-5] is pulled high. The delay circuit provides the 2 microsecond delay before the DI can look for a parallel poll response. After this delay, as soon as a response is detected by the Command Decode Logic [1A-3,4] and PPR (U23) [1B-4] to (U33-8) [1C-4] is high, PPRLL [1D-4] goes low initiating the FIFO load sequence.

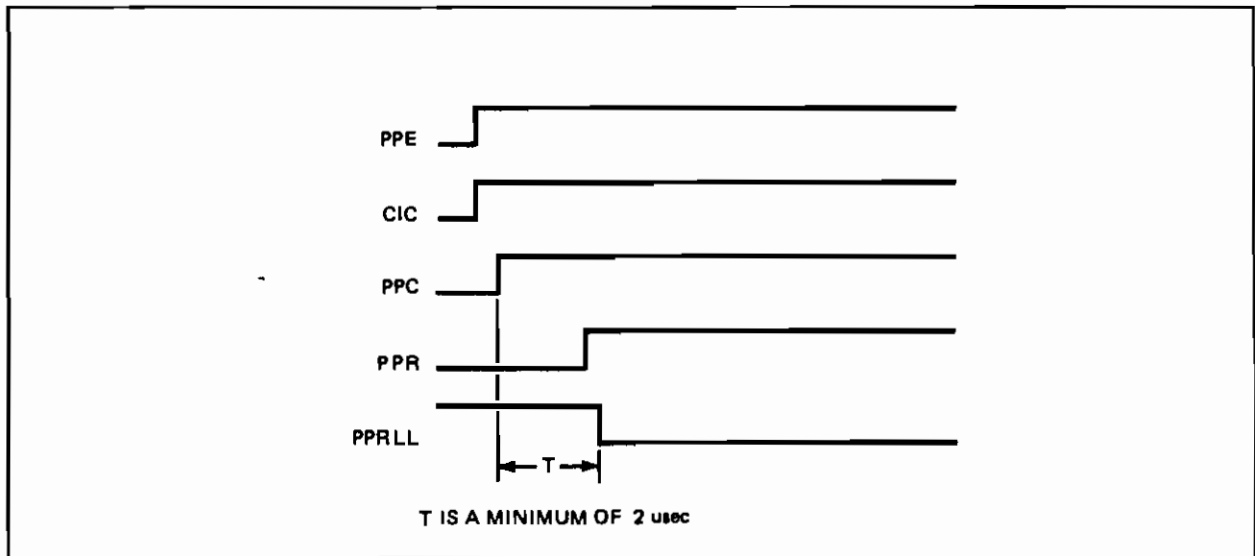


Figure 3-22. Parallel Poll Conduct Logic

3.32 BUS ADDRESS SWITCH

The Bus Address Switches are 8 rocker-switches on DIP (U13) [1B-3]. The first five switches set the DI's bus address with switch one as the least significant bit. The eighth switch (U13-8) [1D-7] sets the SYSCTL bit. An open switch corresponds to a one, a closed switch to a zero.

3.33 BUS ADDRESS COMPARATOR

A five-bit Comparator (U12) [1A-2] compares the bus Address Switch setting with the five least significant bits on the Bus Transceivers' data lines. When the inputs are equal, the comparator output, ADD, is high.

3.34 COMMAND DECODE LOGIC

The Command Decode Logic [1A-3,4] consists of a PROM (U23), an addressable latch (U22), a few gates, and a flip-flop (U72). The PROM detects parallel poll responses directly (U23-10) and detects line-feeds with the assistance of a NOR gate (U42-1). TALK, UNTALK, LISTEN, and UNLISTEN commands are decoded when the ADD input (U23-5) indicates the command is addressed to the DI. The TALK, etc., values are latched in U22.

U22-10 is a one when a LISTEN command is received and is zero when an UNLISTEN is received. The NOR gate U32-6 asserts LISTEN [1A-4] when LISTEN is asserted by the command decoder or the listen bit in the Control Word Register is set. U22-11 and U32-3 perform an analogous function for TALK and UNTALK. In this case the Control Word Register talk bit value is latched in U72-4 [2A-3].

The latch is cleared by CRSL [1A-5] or Interface Clear. It is enabled during the receive handshake cycle when an external command (EXTCMD=1) is being loaded into the FIFOs.

3.35 SYSTEM CONTROLLER

Switch eight of the DIP rocker switch (U13) [1D-7] determines the System, Controller function.

When the switch is open, the SYSCTL function is enabled (SYSCTL=1), allowing the DI to assert IFC and REN on the bus per the state of the associated bits (bits 14 and 13 respectively).

When the switch is closed (SYSCTL=0) the DI is not functioning as System Controller. In this mode the DI receives the IFC and/or REN from the bus, causing the DI's flag to set if either of the associated Control Word Register bits are set (bits 14 and 13 respectively).

4.1 INTRODUCTION

This section provides safety precautions, preventive maintenance instructions, troubleshooting, and diagnostic information.

4.2 SAFETY PRECAUTIONS

To avoid injury and to prevent damage to the equipment, service personnel should observe the following safety precautions:

- * Observe all WARNING and CAUTION and other hazard labels affixed to the equipment being checked.
- * Use extreme caution when working on equipment with the covers removed, since hazardous line voltage is present within the mainframe.
- * Remove watches, rings, and other such jewelry before working on equipment.
- * Do not attempt to install or remove PCA's or interconnecting cables without first removing power from all devices.

4.3 PREVENTIVE MAINTENANCE

Preventive maintenance should be performed at scheduled intervals to minimize performance degradation. Preventive maintenance consists of inspecting, cleaning, and verifying performance of the PCA. Inspect the interface cable and connectors for cracks, burns, or wear. Ensure that the PCA is properly seated.

4.4 TROUBLESHOOTING

Troubleshooting consists of performing the diagnostic test. The PCA is not field repairable, when a PCA is found to be defective it should be replaced with an exchange assembly and the defective PCA returned to Hewlett-Packard for repair. A parts location diagram, reference parts list, 59310-60008 pin connections and schematic diagrams are provided in this section as an aid in isolating malfunctions.

4.5 DIAGNOSTIC TEST

The HP 12821A Disc Interface Diagnostic, part number 12821-16001 is included in the HP 24396A-F Diagnostic Library and in the HP 1000 Computer System Diagnostic Library (24998-14002). To execute the complete diagnostic, two disc interface PCA's and two interface cables are required. Step-by-step instructions for running the diagnostic are contained in the HP 12821A Diagnostic Reference Manual, part number 12821-90002.

4.6 REPLACEMENT PROCEDURE

If the PCA must be removed from the computer, refer to the removal instructions in the appropriate computer installation and service manual.

Replacement of the PCA is accomplished by reversing the removal procedures. Be sure to configure the DIP switches as described in paragraph 2-5.

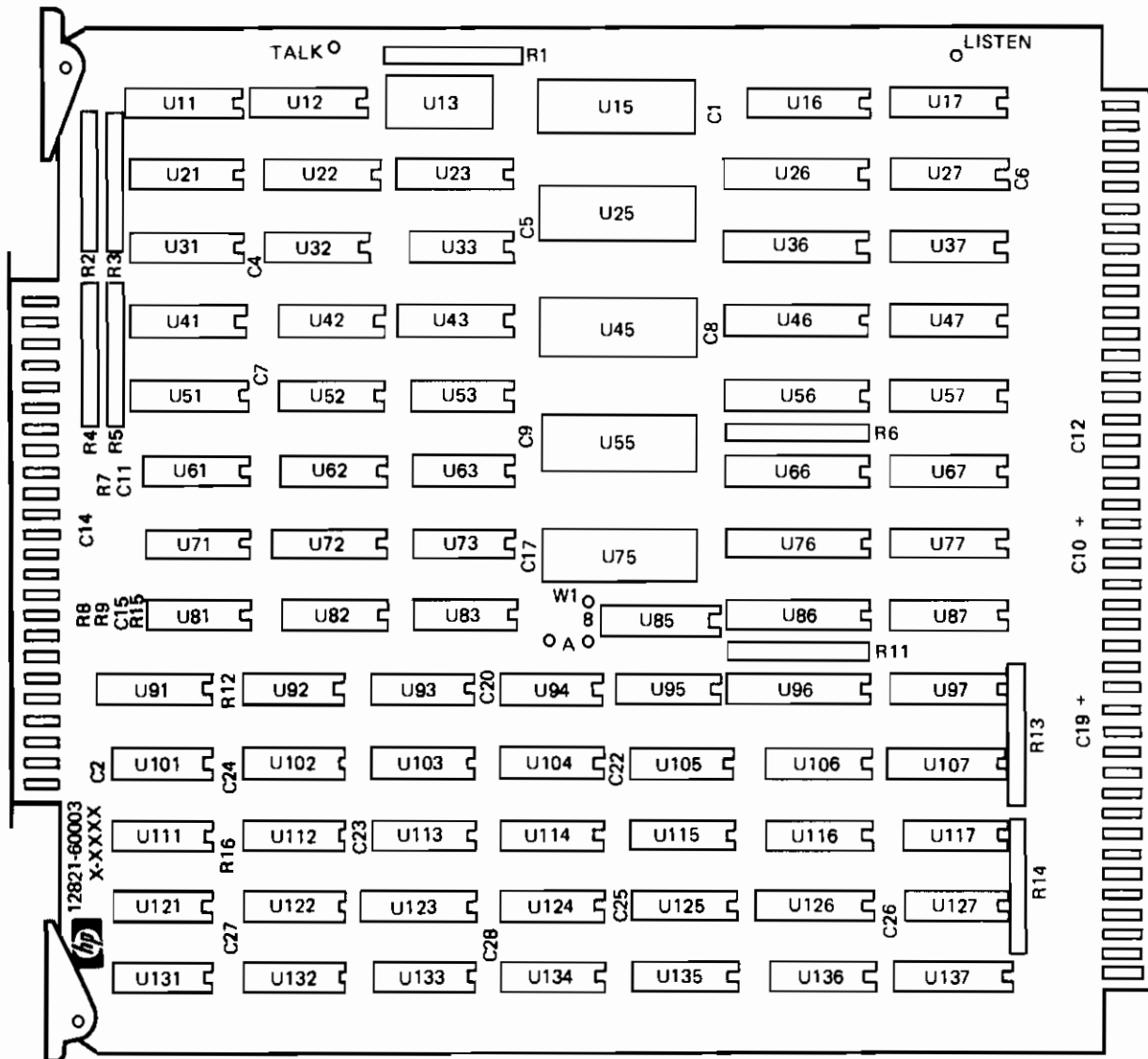


Figure 4-1. 12821-60003 Parts Location Diagram

Table 4-1. Replaceable Parts for Card Assembly 12821-60003

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12821-60003	3	1	ASSY-DISC INTFCE	28480	12821-60003
C1	0160-4832	4	22	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0180-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C10	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C11	0160-4808	4	2	CAPACITOR-FXD 470PF +-5% 100VDC CER	26480	0160-4808
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C13	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C14	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C15	0160-4810	8	1	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
C16				NOT ASSIGNED		
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	1500106X9020B2
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4830	2	1	CAPACITOR-FXD 2200PF +-10% 100VDC CER	28480	0160-4830
C25	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
R1	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R2	1810-0298	8	2	NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
R3	1810-0270	6	2	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
R4	1810-0298	8		NETWORK-RES 10-SIP240.0 OHM X 9	01121	210A241
R5	1810-0270	6		NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
R6	1810-0726	7	1	NETWORK-RES 10-SIP MULTI VALUE	28480	1810-0726
R7	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
R8	0698-3152	8	2	RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
R9	0698-3152	8		RESISTOR 3.48K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3481-F
R11	1810-0276	2	3	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R12	0698-3452	1	1	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
R13	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R14	1810-0276	2		NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R15	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
U1-				NOT ASSIGNED		
U10				NOT ASSIGNED		
U11	1820-0468	5	1	IC DDDR TTL BCD-TO-DEC 4-TO-10-LINE	01295	SN7445N
U12	1820-0706	4	1	IC COMPTT TTL MAGTD 5-BIT	07263	9324PC
U13	3101-1983	9	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
U14				NOT ASSIGNED		
U15	1816-0934	1	5	IC TTL 64-BIT MEM 3-S	07263	9403PC
U16	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U17	1820-1080	9	11	IC DRVR TTL LINE DRVR DUAL 6-IMP	01295	SN75121N SELECTED
U18-				NOT ASSIGNED		
U20				NOT ASSIGNED		
U21	1820-2161	9	3	IC MISC TTL	27014	DS8835N
U22	1820-1729	3	1	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U23	12821-80002	4	1	BURNIN 1816-0710	28480	12821-80002
U24				NOT ASSIGNED		
U25	1816-0934	1		IC TTL 64-BIT MEM 3-S	07263	9403PC
U26	1820-1730	6	4	IC FF TTL LS D-TYPE POS-EDGE TRIG COM	01295	SN74LS273N
U27	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-IMP	01295	SN75121N SELECTED
U28-				NOT ASSIGNED		
U30				NOT ASSIGNED		

Table 4-1. Replaceable Parts for Card Assembly 12821-60003 (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U31	1820-2161	9		IC MISC TTL	27014	DS8835N
U32	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U33	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U34				NOT ASSIGNED		
U35				NOT ASSIGNED		
U36	1820-1794	2	2	IC BFR TTL LS NON-INV OCTL	27014	DM81LS95N
U37	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U38-				NOT ASSIGNED		
U40				IC MISC TTL	27014	DS8835N
U41	1820-2161	9		IC MISC TTL	27014	DS8835N
U42	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U43	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TD-1-LINE QUAD	01295	SN74LS157N
U44				NOT ASSIGNED		
U45	1816-0934	1		IC TTL 64-BIT MEM 3-S	07263	9403PC
U46	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U47	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U48-				NOT ASSIGNED		
U50				NOT ASSIGNED		
U51	1820-1875	0	1	IC MISC TTL QUAD	18324	8T38N
U52	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U53	1820-1201	6	4	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U54				NOT ASSIGNED		
U55	1816-0934	1		IC TTL 64-BIT MEM 3-S	07263	9403PC
U56	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U57	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U58-				NOT ASSIGNED		
U60				NOT ASSIGNED		
U61	1820-1197	9	7	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U62	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U63	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U64				NOT ASSIGNED		
U65				NOT ASSIGNED		
U66	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U67	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U68-				NOT ASSIGNED		
U70				NOT ASSIGNED		
U71	1820-0471	0	1	IC INV TTL HEX 1-INP	01295	SN7406N
U72	1820-1440	5	3	IC LCH TTL LS QUAD	01295	SN74LS279N
U73	1820-1199	1	4	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U74				NOT ASSIGNED		
U75	1816-0934	1		IC TTL 64-BIT MEM 3-S	07263	9403PC
U76	1820-1794	2		IC BFR TTL LS NON-INV OCTL	27014	DM81LS95N
U77	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U78-				NOT ASSIGNED		
U80				NOT ASSIGNED		
U81	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U82	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U83	1820-1202	7	4	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U84				NOT ASSIGNED		
U85	1820-1278	7	1	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U86	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U87	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U88-				NOT ASSIGNED		
U90				NOT ASSIGNED		
U91	1820-1423	4	1	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
U92	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U93	1820-1285	6	2	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
U94	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U95	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U96	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U97	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U98-				NOT ASSIGNED		
U100				NOT ASSIGNED		
U101	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U102	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U103	1820-1285	8		IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
U104	1820-1201	8		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U105	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N

Table 4-1. Replaceable Parts for Card Assembly 12821-60003 (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U106	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U107	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U108- U110				NOT ASSIGNED		
U111	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U112	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U113	1820-1210	7	2	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U114	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U115	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U116	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U117	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
U118- U120				NOT ASSIGNED		
U121	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U122	1820-1201	8		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U123	1820-1440	5		IC LCH TTL LS QUAD	01295	SN74LS279N
U124	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U125	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U126	1820-1440	5		IC LCH TTL LS QUAD	01295	SN74LS279N
U127	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U128- U130				NOT ASSIGNED		
U131	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U132	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U133	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
U134	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U135	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U136	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U137	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
	1251-1556	7	3	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
	5040-6001	4	1	EXTRACTOR-PC	28480	S040-6001
	1258-0124	7	1	PIN-PROGRAMING DUMPER .30 CONTACT	91506	8136-475G1
	5040-6065	0	1	EXTRACTOR-RED	28480	S040-6065
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	12821-80003	5	1	PC BOARD	28480	12821-80003

Table 4-2. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address	Zip Code
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS TX	75222
03888	K D I PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85008
07263	FAIRCHILD SEMINONDUCTOR DIV	MOUNTAIN VIEW CA	94042
14433	ITT SEMICONDUCTOR, INTL TELE&TELEGRAPH CORP	W. PALM BEACH FL	33402
18324	SIGNETICS CORP	SUNNYVALE CA	94042
19701	MEPCO/ELECTRA CORP	MINERAL WELLS TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
32293	INTERSIL INC	CUPERTINO CA	95014
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE SC	06226
91506	AUGAT INC	ATTLEBORO MA	02703

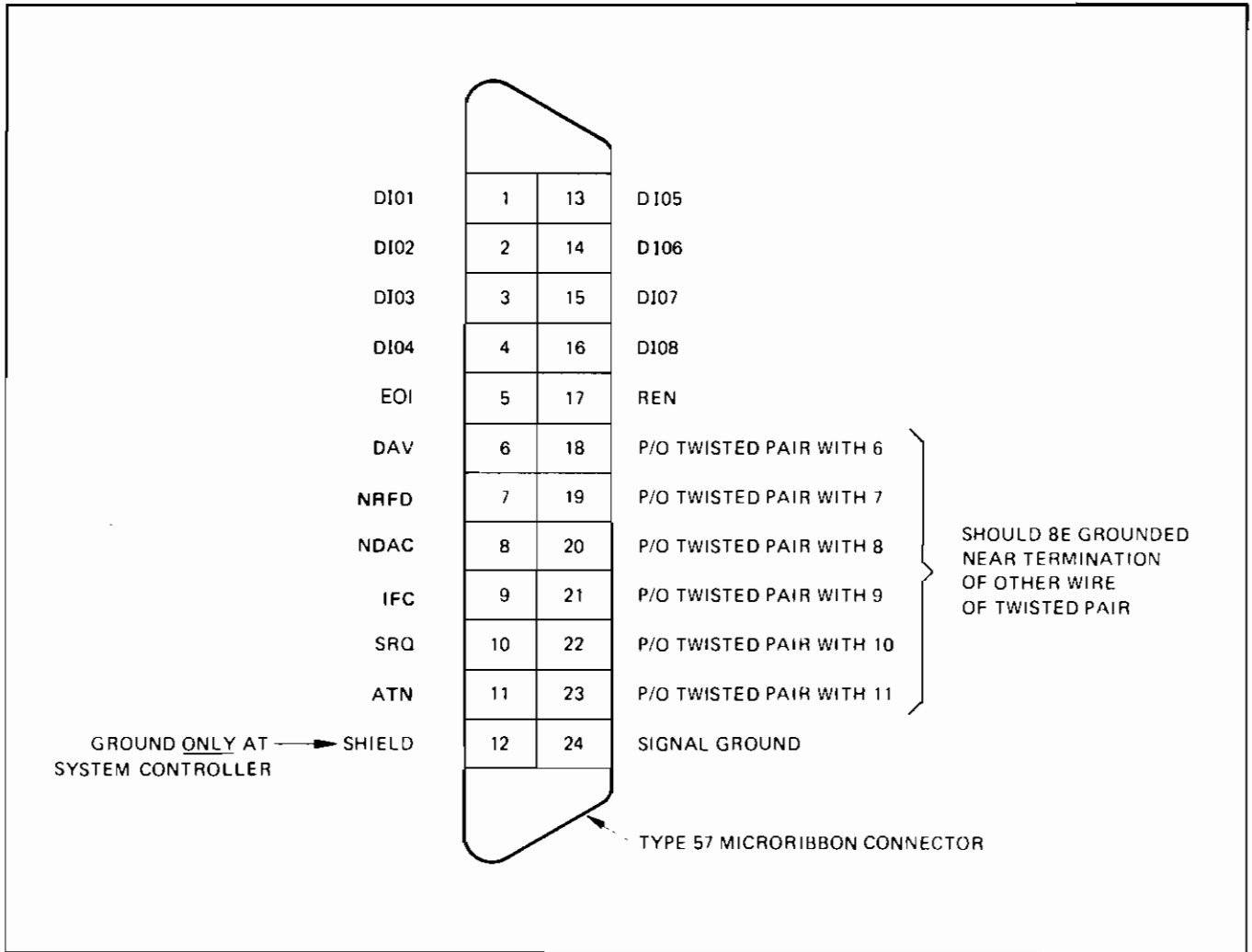


Figure 4-2. Pin Connections of the Bus Cable 59310-60008

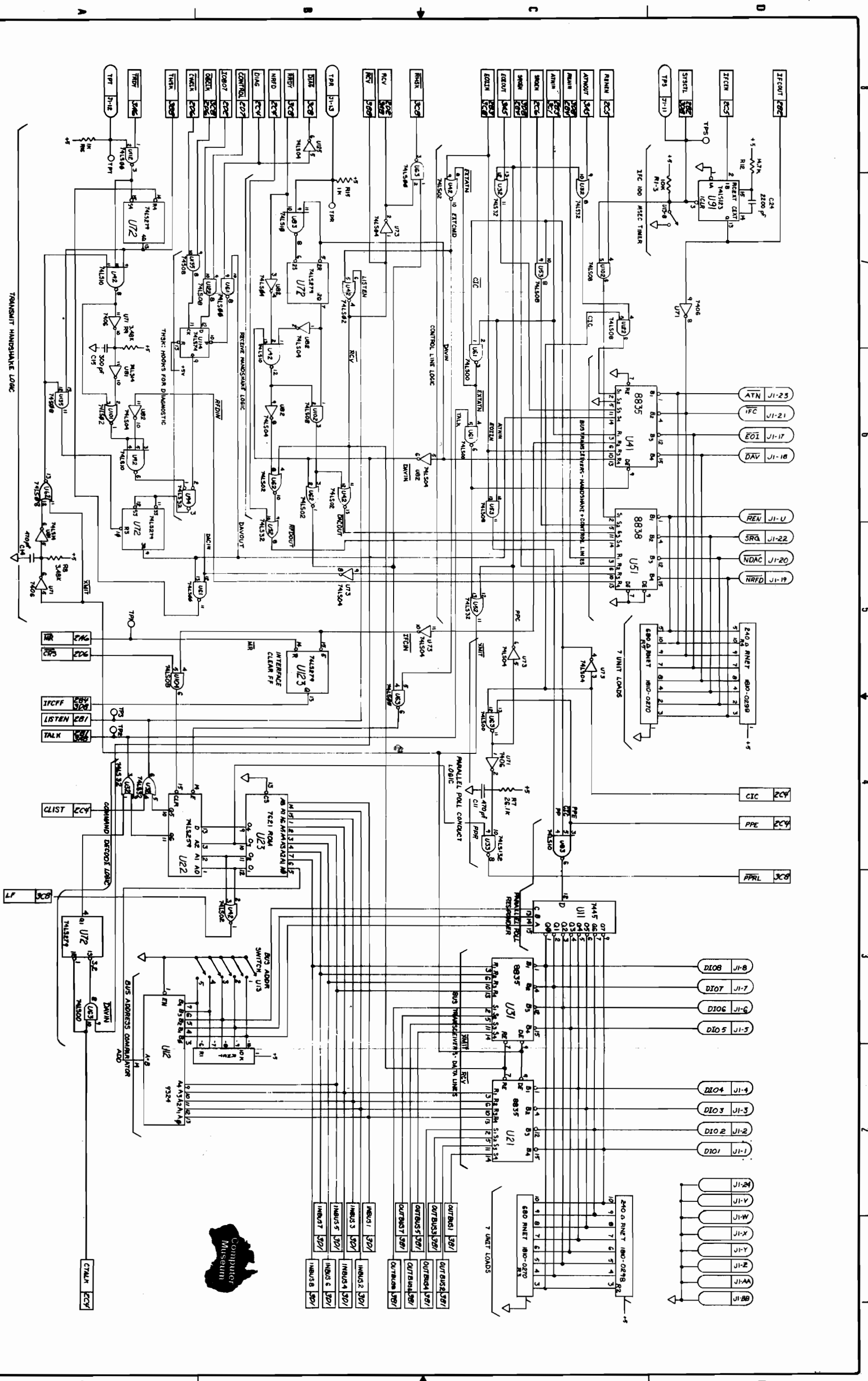


Figure 4-3. Schematic Diagram sheet 1 of 3 4-9/4-10

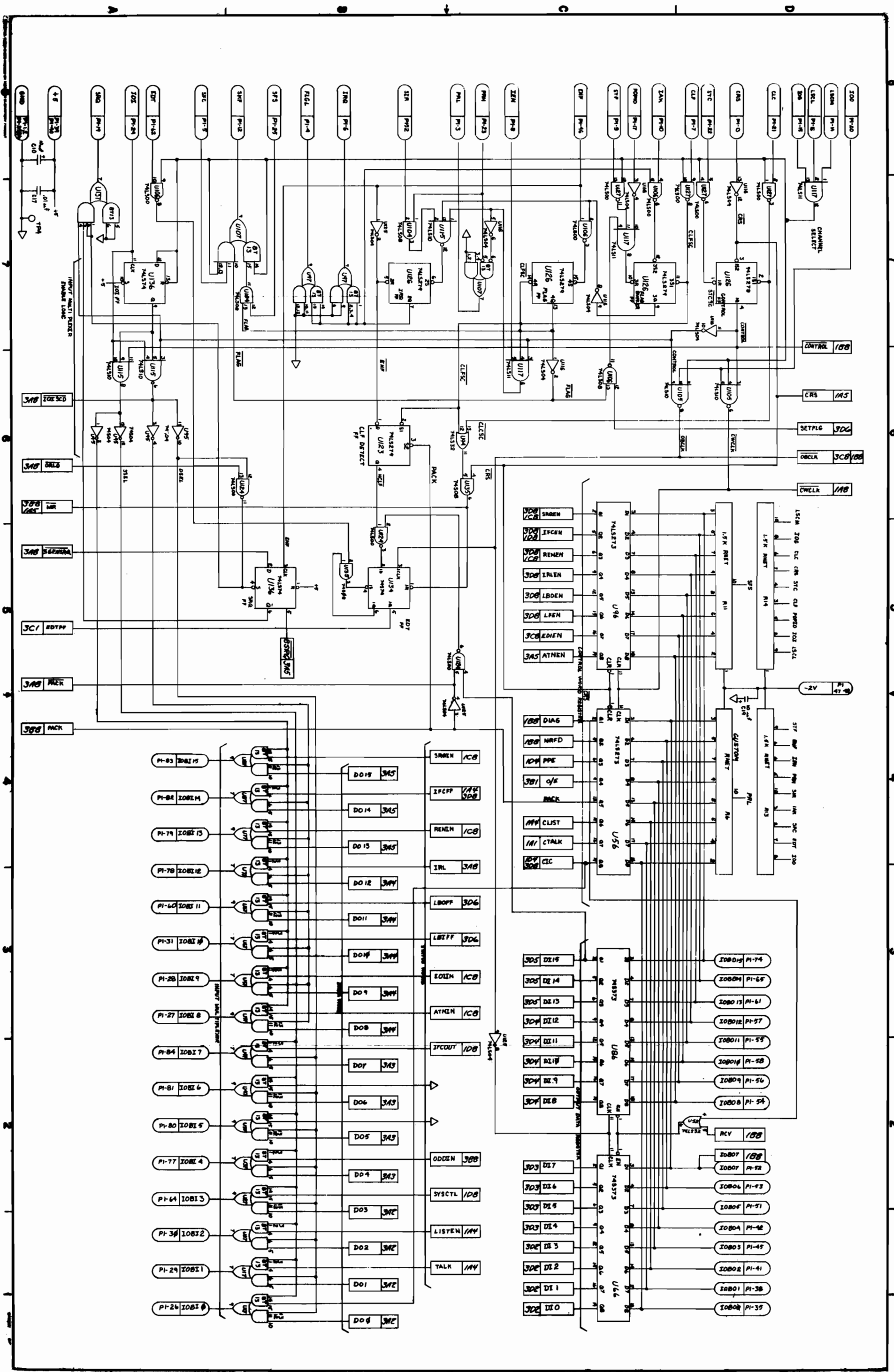


Figure 4-3. Schematic Diagram
sheet 2 of 3
4-11/4-12

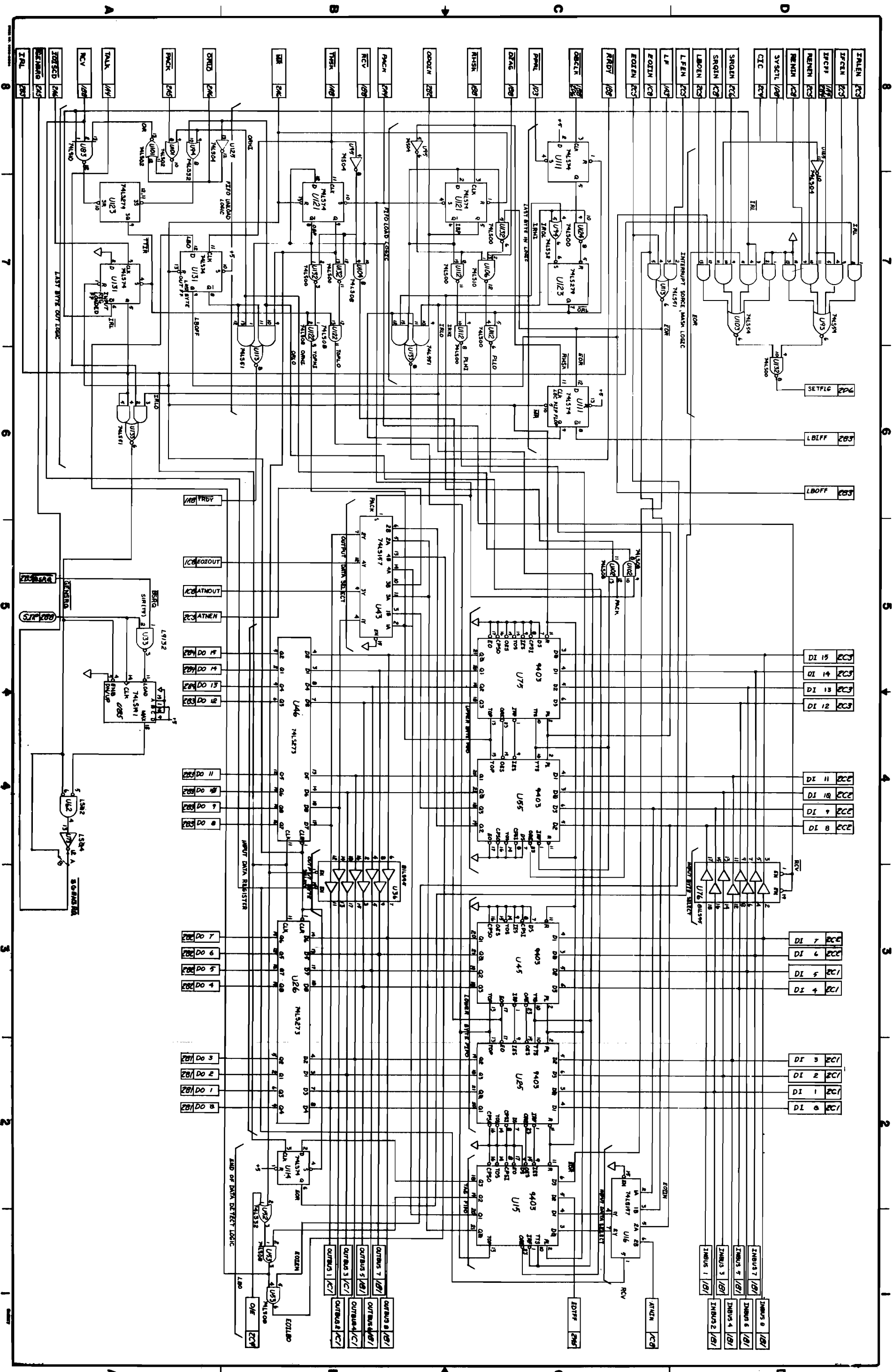


Figure 4-3. Schematic Diagram
 Sheet 3 of 3
 4-13/4-14



5.1 INTRODUCTION

This chapter provides a brief description of differences between Disc Interfaces (DI) with different date codes.

5.2 CONVENTIONS

Signal names are mnemonic identifiers usually chosen to be as close to the signal usage as possible. These signal identifiers may have a bar over them on the schematics to indicate the signal is active low. In text the same signal will contain an "L" at the end of the signal name to indicate the active low condition.

In this chapter we may refer to the disc interface's schematic and component location diagrams in Chapter 4. The schematic diagram is printed on three fold-out pages, so during our discussion we have indicated sheet numbers and coordinates within brackets []. The coordinates will be those of an area of the schematic which contains the logic circuit described in the text. A reference to a particular component in those coordinates will usually be printed in parenthesis ().

Example: [2D-7] (U117-2) refers you to sheet 2 at coordinates D-7 and component U117's pin number 2.

No coordinate-system is used on the component location diagram.

5.3 LISTING

12821-60001, all date codes

These DI cards all lacked the counter U85, Jumper W1, and related circuitry. The output of U133-6 [3A-6] is wired directly to U136-2 [2B-5]. U133-6's output was called GENSRQL. The output from U136-5 [2B-5] was not used. These DI cards cannot be set to cut off their own SRQ after five T5-periods.

12821-60003, date code A-2323

This version and all succeeding versions of the DI card, unless noted otherwise below, have the counter U85, Jumper W1, and related circuitry. These DI cards are capable of cutting off their own SRQ after five T5-periods. See Chapter 3 under the heading "Service Request Logic" for more information.

12821-60003, date code A-2424

The custom resistor pack at R6 was replaced by HP part number 1810-0726. The internal resistors in 1810-0726 have the following values: R1 to R8 are 1500 (1.5k) ohms while R9 is 285 ohms. In the old part, HP part number 1810-0276, all of internal resistors had a value of 1500 (1.5k) ohms. A jumper wire connecting pin 10 of R6 to pin 7 of U107 was also added.

12821-60003, date code B-2424

The jumper wire on 'A-2424 was deleted because an equivalent internal connection was added to the printed circuit assembly.

Summary of Changes

GLOSSARY	BSRQL, 5GENSRQL, and FIFO have been added.
1 - INTRODUCTION	Part number changes were made on page 1-2. Sections were renumbered for easier access.
2 - INSTALLATION	New Section 2.5.1 "Setting the SRQ Control Jumper" was added. A "Note" was also added to item 7 of Section 2.6.
3 - PRINCIPLES OF OPERATION	Cross references between items in this chapter and the Schematic Diagrams located in Chapter 4 are now shown in brackets [] as explained on page 3-1, Section 3.2 "Signal Names and Locations".
4 - MAINTENANCE	A new Parts Location Diagram, new Replaceable Parts List, as well as new Schematic Diagrams have been provided in this section.
5 - BACKDATING INFORMATION	This is a new chapter which provides a brief description of differences between Disc Interfaces with different date codes.

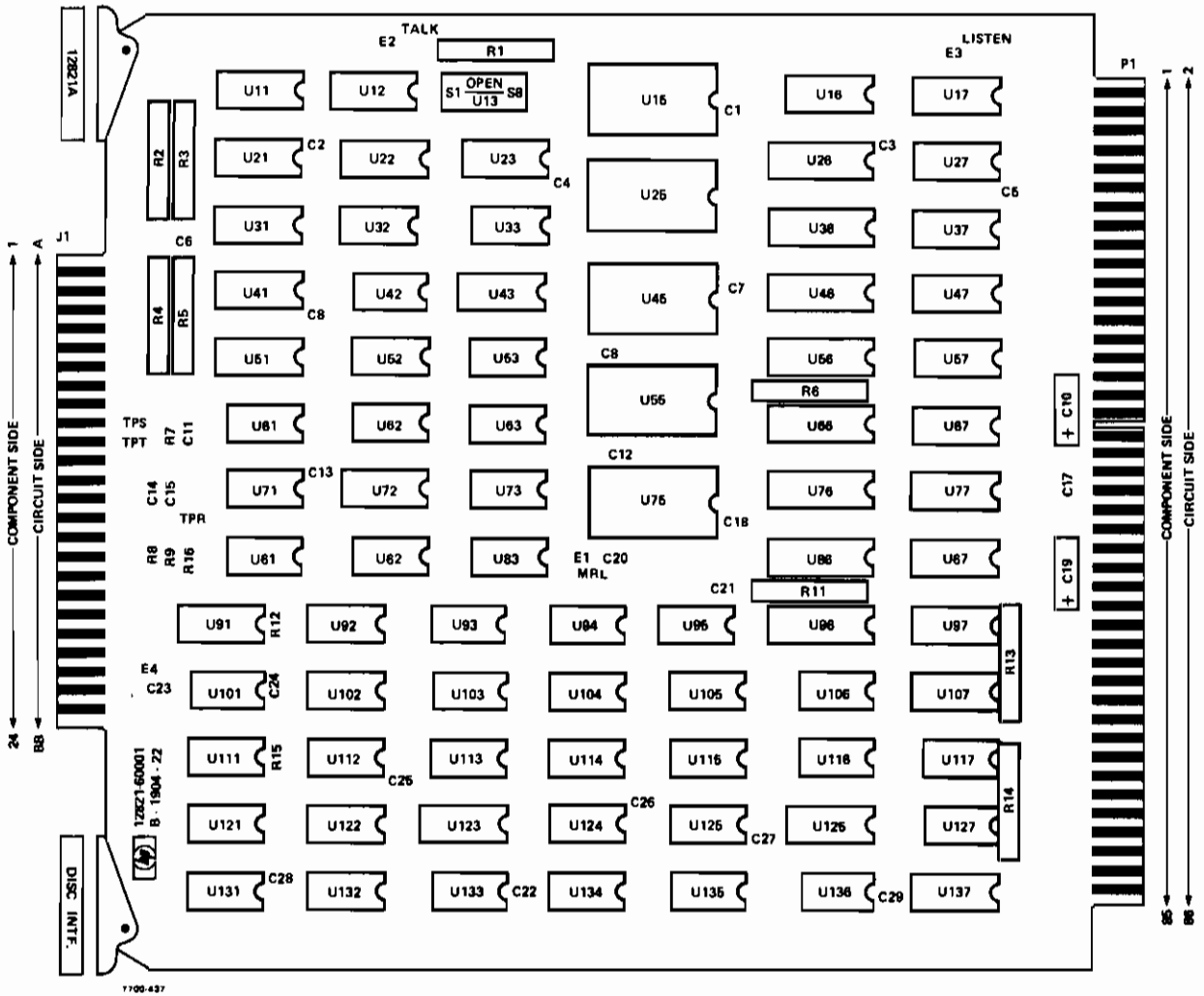


Figure 5-1. 12821-60001 Parts Location Diagram

Table 5-1. Reference Parts List for Card Assembly 12821-60001

REF DESIG	PART NUMBER	DESCRIPTION
	59310-60002	Disc Interface Cable Assy
	12821-60001	Disc Interface PCA
C15	0160-2207	Capacitor, 300pf 5%
C11,14	0160-3353	Capacitor, 470pf 5%
C1-9,12, 13,17,18, 20-23,25- 29	0160-3379	Capacitor, 0.01mf 20%
C24	0160-4299	Capacitor, 2200pf 2%
C10,19	0180-0374	Capacitor, 10mf
R8,9	0698-3152	Resistor, 3.48kohms 1% 0.125W
R7	0698-3159	Resistor, 26.1kohms 1% 0.125W
R12	0698-3542	Resistor, 147kohms 1% 0.125W
R15,16	0757-0280	Resistor, 1.0kohms 1% 0.125W
R3,5	1810-0270	Resistor, Network 9X680 ohms
R6,11,13, 14	1810-0276	Resistor, Network 9X1.5kohms
R1	1810-0280	Resistor, Network 9X10kohms
R2,4	1910-0298	Resistor, Network 9x240ohms
U15,25,45, 55,75	1816-0934	IC, 9403PC FIFO Buffer Memory (TTL)
U11	1820-0468	IC, SN7445N BCD to Decoder/Driver
U71	1820-0471	IC, SN74S06N Hex Inv. Bufr/Dvr OC
U95	1820-0683	IC, SN74S04N Hex Inv.
U134	1820-0693	IC, SN74S74N Dual D-Type FF
U12	1820-0706	IC, 9324PC 5-Bit Comparator
U17,27,37 47,57,67, 77,87,97, 107,137	1820-1080	IC, 8T13B Dual Line Driver
U111,114, 121,131,136	1820-1112	IC, SN74LS74N Dual D-Type FF
U42,62,101	1820-1144	IC, SN74LS02N Quad 2-Input Pos. NOR
U61,63, 106,112,124 127,132	1820-1197	IC, SN74LS00N Quad 2-Input Pos. NAND
U73,82, 116,125	1820-1199	IC, SN74LS04N Dual D-Type FF
U53,102, 104,122	1820-1201	IC, SN74LS08N Quad 2-Input Pos. AND
U83,92, 105,115	1820-1202	IC, SN74LS10N Triple 3-Input Pos. NAND
U117	1820-1203	IC, SN74LS11N Triple 3-Input Pos. AND
U32,52,94	1820-1208	IC, SN74LS32N Quad 2-Input OR

Table 5-1. Reference Parts List for Card Assembly 12821-60001 (continued)

REF DESIG	PART NUMBER	DESCRIPTION
U113,133	1820-1210	IC, SN74LS51N Dual AND-OR-INVERT
U93,103	1820-1285	IC, SN74LS54N 4-Wide AND-OR-INVERT
U135	1820-1367	IC, SN74S08N Quad 2-Input Pos. AND
U81	1820-1416	IC, SN74S14N Hex Schmitt-Trig-Inv.
U91	1820-1423	IC, SN74LS123N Dual Retriggerable Monostable MV
U33	1820-1425	IC, SN74LS132N Quad 2-Input Pos. NAND Schmitt Triggers
U72,123, 126	1820-1440	IC, SN74LS279N Quad "not S-not R" Latches
U16,43	1820-1470	IC, SN74LS157N Quad 2 to 1 MUX
U66,86	1820-1676	IC, S74S373N Octal D-Type Latch
U22	1820-1729	IC, SN74LS259N 8-Bit Addressable Latch
U26,44, 56,96	1820-1730	IC, SN74LS273N Octal D-Type FF. AND
U36,76	1829-1794	IC, 81LS95 Non-Inverting Buffer
U51	1820-1875	IC, DS8838N Quad O.C. Bus Transceiver
U21,31,41	1820-2161	IC, DS8835N Quad Tri-State Bus Transceiver
U23	12821-80002	IC, 4 X 512 ROM
U13,S1-S8	3101-1983	Switch, DIP, 8-Rocker

