HEWLETT PACKARD

HP 12821A
Disc Interface

installation and service manual

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

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MANUAL UPDATE

MANUAL IDENTIFICATION

Title: HP 12821A Disc Interface
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This Packet also Includes:

Computer Museum

THIS UPDATE GOES WITH: First Edition January 1980

THE PURPOSE OF THIS MANUAL UPDATE
is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the product.

THIS UPDATE CONSISTS OF
this cover sheet, a printing history page, all replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the text. New pages to be added do not contain change bars.

TO UPDATE YOUR MANUAL
identify the latest Update (if any) already contained in your manual by referring to the Printing History Page (page ii). Incorporate only the Updates from this packet not already included in your manual. Following the instructions on the back of this page, replace existing pages with the Update pages and insert new pages as indicated. If any page is changed in two or more Updates, such as the Printing History Page which is furnished new for each Update, only the latest page will be included in the Update package. Destroy all replaced pages. If "write-in" instructions are included they are listed on the back of this page.

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TECHNICAL MANUAL UPDATE
(12821-90006)

Note that "*" indicates a changed page.

UPDATE	DESCRIPTION
1	A. Replace the following pages with the pages supplied.

i*/ii*
iii*/iv*
v*/vi*
vii*/viii*
ix*/x*
xi*
1-1*/1-2*
1-3*/1-4*
2-1*/2-2*
2-3*/2-4*

SAFETY CONSIDERATIONS

GENERAL - This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING **WARNING**

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

PREFACE

This manual provides installation and service instructions for the HP 12821A, Disc Interface Card (DI). The 12821A is a single, logic circuit card used as the HP 1000 M/E/F Series hardware interface for the H-Series and CS80-Series disc drives operating under the control of either the RTE-IVB (92068A) or RTE-6/VM (92084A) Operating System Driver DVA 32 or DVM/DVN 33 respectively.

Other publications which should be available for reference when using this manual for the following purposes are:

General
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1) Disc Loader ROM Installation and Service Manual, HP Part No. 12992-90001

2) DVR/DVA 32 Reference Manual, HP Part No. 92068-90012 for H-Series disc drives

3) DVM/DVN 33 Reference Manual, HP Part No. 92084-90025 for CS80 Series disc drives

Diagnostics
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1) 12821-90002, Diagnostic Reference Manual

2) 91711B, Diagnostics And Verification Package, which includes the following:

   * Diagnostics And Verification Reference Manual, HP Part No. 91711-90006 for System Processor, I/O Cards and Peripherals

   * Integrated Controller Disc Utilities Reference Manual, HP Part No. 5955-4355 for H-Series disc drives

   * CS80 External Exerciser Reference Manual, HP Part No. 5955-3462 for CS80-Series disc drives

Table of Contents

List of Illustrations

List of Tables

GLOSSARY

This is a basic list of mnemonics and acronyms which will be helpful in using this manual. With your addition of an appropriate prefix or suffix (such as EN, IN, OUT, etc. to indicate enable, input, output) this basic list can be leveraged to cover those situations likely to arise in the use of this manual:

MNEMONIC	DESCRIPTION
ADD	Address Detected
ATNL	Attention, Low True
ATNEN	Attention Enable
ATNIN	Attention In
CHSEL	Channel Select
CIC	Controller-In-Charge
CLCSCL	Clear Control Select Code, Low True
CLFSCL	Clear Flag Select Code, Low True
CONTROL	Control
CONTROLL	Control, Low True
CRSL	Control Reset, Low True
CWCLKL	Control Word Clock, Low True
CS80-Series	HP Model 7908x, 7911x, 7912x or 7935x disc drive using HP-IB controller
DACIN	Data Accepted In
DACOUTL	Data Accepted Out, Low True
DAVINL	Data Valid In, Low True
DAVL	Data Valid, Low True
DAVOUTL	Data Valid Out, Low True
DIAG	Diagnostic
DSEL	Data Word Selected
EDT	End Data Transmission
ENFL	Enable Flag, Low True
EOIIN	End Or Indentify IN
EOIL	End Or Identify, Low True
EOILBO	End Or Identify Last Byte Out
EORL	End Of Record, Low True
EDT	End Data Transfer
FLAGL	Flag, Low True
GENSRQL	Generate SRQ, Low True
H-Series	HP Model 7906H, 7920H, 7925H or 9895A disc drive using HP-IB controller

IBP	Input Byte Pointer
ICD	Another name for H-Series disc drives
IESL	Serial Input Enable, Low True
IFCEN	Interface Clear Enable
IFCIN	Interface Clear Input
IFCL	Interface Clear, Low True
IFCOUT	Interface Clear Output
IOI	I/O Input
IOISCDL	I/O Input of Data
IOO	I/O Output
IRHI	Input Register full-upper byte, Low True
IRL	Input Register Loaded
IRLEN	Input Register Loaded Enable
IRLO	Input Register full-lower byte, Low True
L	Listen
LBIFF	Last Byte In Flip-Flop
LBOFF	Last Byte Out Flip-Flop
LF	Line Feed
MR	Master Reset
NCLFL	No Clear Flag, Low True
NDACL	Not Data Accepted, Low True
NRFDL	Not Ready For Data, Low True
O/E	Odd-Even
OBCLKL	Output Byte Clock, Low True
OBP	Output Byte Pointer
ODDIN	Odd IN
OR	Output Ready
OREL	Output Register Empty, Low True
ORHI	Output Register full-upper byte FIFO
ORLL	Output Register Loaded, Low True
ORLO	Output Register Full-Lower Byte and Tag FIFOs
PACK	Enable Packing
PLHI	Parallel Load-upper byte
PLLO	Parallel Load-lower byte
PP	Parallel Poll
PPC	Parallel Poll Conduct
PPE	Parallel Poll Enable
PPRL	Parallel Poll Response, Low True
PPRLL	Parallel Poll Response Load, Low True
RCV	Receive
RENL	Remote Enable, Low True
RFDIN	Ready For Data In
RFDOUTL	Ready For Data Out, Low True
RHSKL	Receive Handshake, Low True
RRDYL	Receive Ready, Low True

SETFLG	Set Flag
SRQL	Service Request, Low True
SSEL	Status Select
SYSCTL	System Controller
T	Talk
THSKL	Transmit Handshake, Low True
TOPHI	Transfer Out Parallel-Upper Byte FIFO
TOPLO	Transfer Out Parallel-Lower Byte and Tag FIFO
TRDYL	Transmit Ready, Low True
TTIRL	Transfer To Input Register, Low True
TTSL	Transfer To Stack, Low True
XMITL	Transmit, Low True

INTRODUCTION — CHAPTER 1

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1.1 Description

The HP 12821A is HP's implementation of IEEE Standard 488-1978 conforming to the Higher Speed Operations Guidelines of paragraph 5.2.3 to provide high speed, bidirectional interchange of digital data between the computer and its disc drive.

Both the H-Series (7906H, 7920H, 7925H, 9895A) and the CS80-Series (7908x, 7911x, 7912x, 7935x) disc drives are supported on the 12821A. This compatibility extends to the integrated Cartridge Tape Unit found in certain models of the CS80-Series disc drives (7908x, 7911x and 7912x]. While both the H-Series and CS80-Series disc drives are supported under RTE-6/VM, only the H-Series discs are supported under RTE-IVB. See Figure 1-1 for representative Multi-Disc configuration.

1.2 Multi-Disc Configurations

Each 12821A will support either two H-Series or four CS80-Series disc drives (maximum). However, when both series disc drives are interfaced to the same computer, each series must be configured on a separate interface, each with its own driver.

1.2.1 Interconnection Disc Cabling

The disc drive is supplied with a standard 4 meter cable used to connect the DI. Table 1-1 lists the HP supported interconnection cables used to connect additional disc drives (either series):

Table 1-1. Disc Cables

LENGTH	PART NUMBER
1 meter	10833A
2 meter	10833B

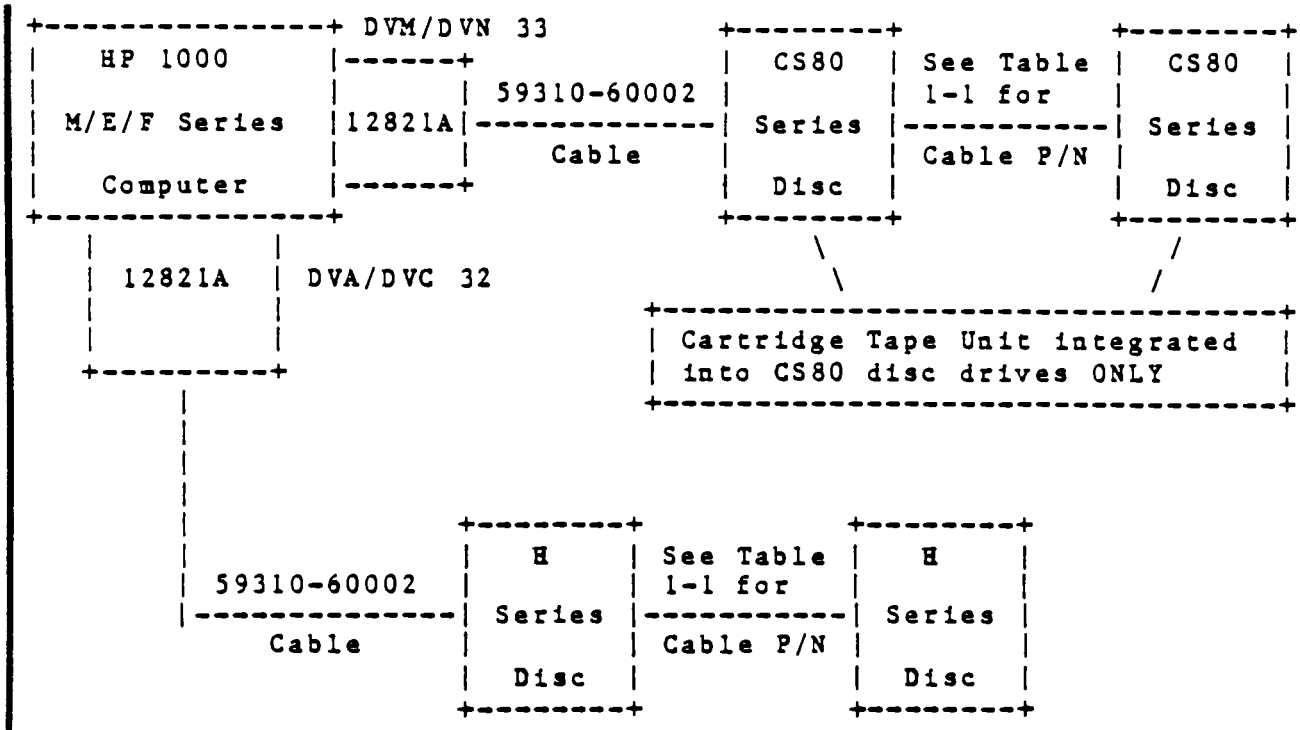

Figure 1-1 Multi-Disc Configuration

1.3 Product Contents

The 12821A Disc Interface product consists of:

1) Disc Interface Card, HP Part No. 12821-60001.
2) HP-IB Cable Assembly, HP Part No. 59310-60002.
3) Disc Interface Installation And Service Manual, HP Part No. 12821-90006.
4) 12992 Loader ROM Installation Manual, HP Part No. 12992-90001.
5) 12992H, Disc Loader ROM (for H-Series disc drive only).

-OR-

6) For CS80-Series, Option 001 is ordered (deletes item 5) and 12992J, Disc Loader ROM is ordered as a line item.

1.4 Related Items

The following items are not included in 12821A component shipments but are included in HP 1000 Computer System shipments. When purchasing a component product or system or adding to or upgrading a previously purchased system, these items will be needed (as indicated) for typical system operation:

1) Software Driver DVA/DVC 32, HP Part No. 92067-16553 for H-Series disc drive. Included with the RTE-IVB (92068A) or the RTE-6/VM (92084) Operating System.

2) Software Driver DVM/DVN 33, HP Part No. 92084-16650, for CS80 Series disc drive. Included in the RTE-6/VM (92084A) Operating System.

3) HP-IB bus cables (see Table 1-1) for multi-disc installation.

4) 12992J, Disc Loader ROM for CS80-Series disc drives (see item 6, Related Items above).

5) 24998-14002, HP 1000 Computer System Diagnostic Library, supplied with shipments of HP 1000 Systems.

6) 91711B, Diagnostics And Verification Package, supplied with current shipments of HP1000 Systems.

1.5 Identification

1.5.1 Product

Five digits and a letter suffix (12821A in this case) are used to define and identify HP products used with HP computers. The five digits identify the product while the letter indicates the revision level of the product.

1.5.2 Circuit Card

The interface circuit card assembly is further identified by a part number marked on the card. In addition to this a letter and a date code consisting of four digits are placed below the part number.

The letter identifies the etched circuit on the card. The four-digit series code identifies the electrical characteristics of the loaded circuit card:

12821-60001
  A-1926

If this series code does not exactly agree with the series code on the title page of this manual, there are differences between your circuit card and the one described in this manual. These differences are covered either in manual supplements (accompanying this manual) or the supplements are available through the nearest HP Sales and Service Office (listed in the back of this manual).

1.6 Power and Environmental Requirements

The 12821A operating temperature range is 0 to 55 degrees Celsius. Power requirements are:

SUPPLY VOLTAGE	MAX. CURRENT REQUIRED
+30	NONE
+12	NONE
+5	3.34A
-2	0.10A
-12	NONE

1.7 Operation

The 12821A architecture has been optimized for DMA transfer. However, this does not inhibit the ease of interrupt-driven transfers of small data buffers. The DI operates under control of either RTE-IVB (92068A) or RTE-6/VM (92084) operating system drivers making efficient data transfers approaching a full megabyte per second without user intervention (user transparency). To achieve this high transfer rate, the DI is preloaded with seven unit resistive loads. Because drivers are device specific routines, the following drivers will be used with the indicated Series disc:

*DVA/DVC 32 for H-Series disc drives
*DVM/DVN 33 for CS80-Series disc drives

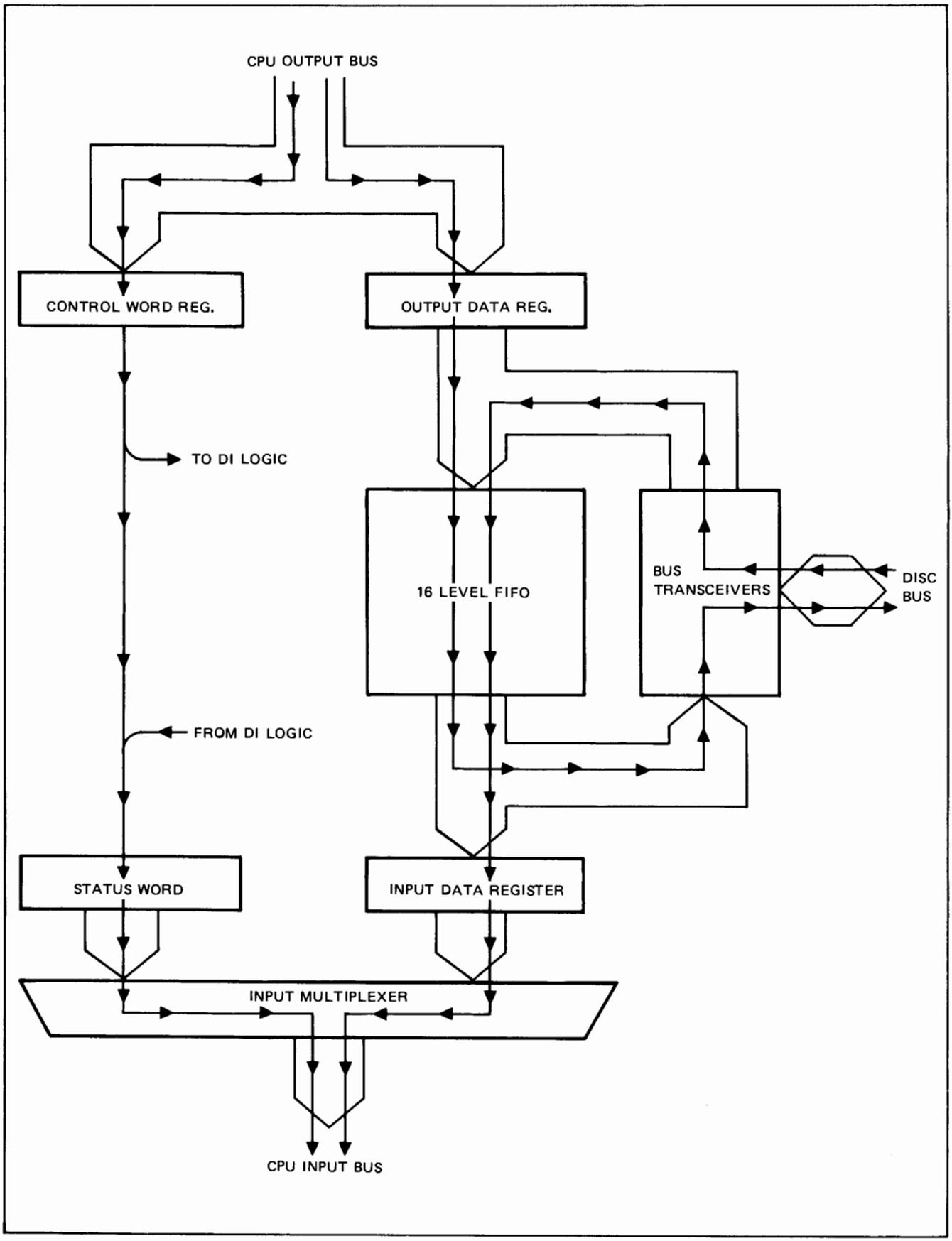

Figure 1-2. Disc Interface Data Paths Block Diagram

1-9. FUNCTIONAL DESCRIPTION

The HP 12821A Disc Interface PCA architecture has been optimized for DMA transfer; however, interrupt-driven transfers of small data buffers are easily performed. The PCA operates under control of a software driver (DVA 32) supplied with the operating system, thus the transfer method is transparent to the user. The PCA is capable of transferring data up to a full one megabyte rate. To achieve this transfer rate the PCA is preloaded with seven unit resistive loads.

The Disc Interface (DI) in the Data Mode is bi-directional, data may be transfered from the CPU or memory to a disc or from a disc to the CPU or memory. The DI is defined to be a talker when transferring data from the computer to the disc and to be a listener when transferring data from the disc to the computer. In addition to the Data Mode the CPU can place the DI in the Configure Mode as a talker or the Status Mode as a listener.

Figure 1-2 is a functional block diagram showing the data paths within the DI. Information from the computer I/O bus can be seen to have two possible destinations the Control Word Register (Configure Mode) or the Output Data Register (Data Mode). The Control Word sets up the DI logic and alerts the disc that data is to be transmitted. When the disc acknowledges the request and is ready to receive, the data is processed through the FIFO and the tranceivers to the disc. To obtain data from the disc the DI must first be set up as a talker to inform the disc that data is going to be requested. When the disc acknowledges the commands the DI is then made a listener and the data transfer takes place through the Transceivers, FIFO, Input Data Register, and Input Multiplexer to the computer.

The key to the high transfer rate of the DI is the 16 word FIFO buffer. The FIFO can be loaded from the Output Data Register when the DI is a talker or from the transceivers when a listener. Data from the computer, being 16 bits wide, is loaded directly into the FIFO, while byte data from the disc can be packed two bytes per word.

Similarly, data out of the FIFO can be sent to the computer from the Input Data Register when DI is a listener, or to the disc from the transceivers when DI is a talker. FIFO words can be unpacked to form two 8-bit bytes. The routing of data into and out of the FIFO is done by Tri-state logic. If packing is used the upper byte of each FIFO word is the first to be sent or received. If no packing is specified, the lower byte FIFO is always selected.

Data for the computer is selected by the Input Multiplexer. The input mode will determine whether the Input Data Register or the Status Word will be read by the computer.

1-10. OUTPUT MODES

The formats for the Data Mode and the Configure Mode are shown in the following paragraphs. Data output to the DI will be received by Output Data Register or the Control Word Register depending on the previously selected mode. The Control Word Register (Configure Mode) is selected by clearing the Control Flip-Flop.

1-11. Data Mode (Control Flip-Flop set)

Data can be output to the DI in two formats, packed or unpacked. In general, the unpacked format will be used when outputting less than 17 bytes of commands and/or data in a software controlled transfer. The packed format is most often used when outputting more than 17 bytes of data in a DMA transfer.

The unpacked data output format is shown in Figure 1-3.

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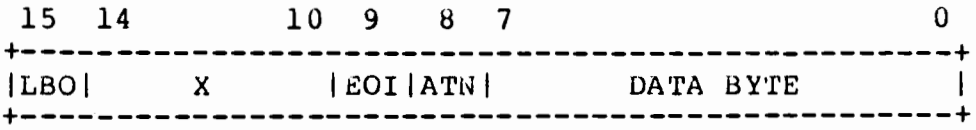


Figure 1-3. Unpacked Data Format

Bits 0-7 contain the data byte, while bits 8 and 9 contain the values of the disc ATN and EOI lines to be associated with this data. Note that this format allows disc commands (ATN=1) and data (ATN=0) to be mixed in any order within the FIFO.

Bits 10-14 are ignored by the DI in the unpacked format. Bit 15 signals to the DI that this is the last byte of the current output string. (See description of LBO.)

The packed data output format is shown in Figure 1-4.

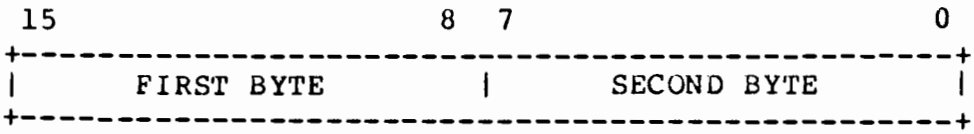


Figure 1-4. Packed Data Format

Here two 8-bit bytes are contained within the word. The values of ATN and EOI associated with each byte are determined by two bits of the Control Word Register (see paragraph 1-12).

1-12. Configure Mode (Control Flip-Flop Clear)

The data format of the Control Word Register is shown in Figure 1-5.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRQ	IFC	REN	IRL	LBO	LF	EOI	ATN	$DIAG$	$NRFD$	PPE	O/E	P	L	T	CIC

Figure 1-5. Control Word Format

Note that each bit has a specific function, and that no multibit encoding is used. The functions of each Control Word Register bit are as follows:

CIC (Controller In Charge, Bit 0) - tells the DI that it is currently controlling the disc.

T (Talk, Bit 1) - indicates that the DI a talker to the disc

L (Listen, Bit 2) - indicates that the DI a listener (from disc)

Pack (Enable Packing, Bit 3) - indicates that the packed data format is to be used for input or output.

O/E (Odd-even, Bit 4) - If set, indicates that for the current Packed Output operation an odd number of bytes is to be output to the disc (i.e., the second byte of the last word will not be sent). For the definition of "last word" see the description of LBO control bit.

PPE (Parallel Poll Enable, Bit 5) - sets ATN and EOI on the bus, indicating that a Parallel Poll is being conducted. T and L must also be set for a parllel poll. After 2 microseconds, the DI looks for a response. When the response occurs it is automatically loaded into the FIFO.

NRFD (Not Ready for Data, Bit 6) - sets the corresponding line on the bus, indicating that the DI is not ready to receive data. This function is required when the DI has been receiving data from a disc and now wishes to untalk the device. NRFD will prevent the disc from placing any further data on the bus while the DI is being reconfigured to talk and the untalk command is being loaded into the FIFO.

DIAG (Diagnostic, bit 7) This bit is used by the diagnostic program. When set, this bit enables the diagnostic program to circle data from the FIFOs thru the transceivers back into the FIFOs.

ATN (Attention, Bit 8) - in the Packed output mode, specifies the value of the bus Attention line. The CIC bit in the control register must also be set.

EOI (End or Identify, Bit 9) - in the Packed output mode, specifies that the last byte sent will be tagged with EOI (see following description of LBO).

When the DI is inputting, EOI specifies that reception of a byte tagged with EOI will set the EOR (End of Record) Flip-Flop. EOR will generate NRFD, indicating to the disc that the DI is no longer ready to receive data. A tag indicating that this is the last word of the current input transfer is placed in the FIFO with the data. When this word has been read by the CPU the DI flag will be set. Any byte signaling EOR will automatically be loaded into the lower byte of the FIFO. Thus if an odd number of bytes are received, the EOR byte will be put in both halves of the FIFO and appear twice in memory. This mechanism is necessary to insure that an odd-numbered byte tagged with EOI will be sent to the CPU. The possible ambiguity of a double last byte in memory can be resolved by reading the O/E bit in the DI Status word.

LF (Line Feed, Bit 10) - enables the line feed detector to set EOR if a line feed is received by the DI. (The results of EOR are the same as described above).

LBO (Last Byte Output, Bit 11) - causes the DI flag to be set when the last byte of the current output transfer has been accepted by the disc.

The last word of an output transfer is signalled to the DI in either of two ways. If a DMA transfer is occurring, the DCPC will automatically signal when the last word is output. This tag will be placed in the FIFO along with the data word.

If the data is being output via software (in the unpacked mode), bit 15 of the data word will indicate to the DI that this word is the last of the current transfer. If the data is output in the packed format the last word is indicated by outputing the word with an OTA DI instruction rather than outputing with an OTA DI,C instruction.

If the output data format is packed, the last byte of the transfer will be the byte of the last word specified by the O/E bit of the Control Word Register (Bit 4). If the output data format is unpacked, the lower byte is automatically assumed to be the last byte.

IRL (Input Register Loaded, Bit 12) - will cause the DI flag to be set when the Input Data Register is loaded. If packing is disabled, reception of one data byte from the disc will load the register; if packing is enabled, 2 bytes must be received. The IRL interrupt is useful for notifying the software that a Parallel Poll response has been received.

REN (Remote Enable, Bit 13) - determines the state of the disc REN line. The system controller switch must be set on the DI for this signal to be output to the disc.

IFC (Interface Clear, Bit 14) - the positive going transition of this bit will generate a 100 microsecond IFC signal to the disc. The System Controller switch must be set on the DI for this signal to be generated.

SRQ (Service Request, Bit 15) - allows any SRQ received by the DI to set the DI flag. The DI must be Controller-In-Charge.

The Control Flip-Flop is cleared by the CPU backplane signal CRS, which occurs at power-up, or when the "PRESET" button is pressed and also when a CLC 0 instruction is executed.

1-13. INPUT MODES

Data input from the DI will come from either the Input Data Register or the Status Word, depending upon the previously selected mode. The Status Mode is selected by clearing the DI Control Flip-Flop; input will then be the Status Word. (Reading status will not change the mode of the DI.)

Similarly, when the DI Control Flip-Flop is set, the Data Mode is selected and data will be input from the Input Data Register.

1-14. Data Mode (Control Flip-Flop set)

Data is input from the DI in two formats, packed or unpacked.

The unpacked data input format is shown in Figure 1-6.

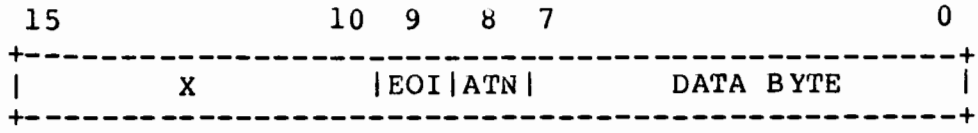


Figure 1-6. Unpacked Data Input Format

Bits 0-7 contain the data byte, while bits 8 and 9 contain the values of the disc ATN and EOI line associated with the data. If the DI is conducting a Parallel Poll, the poll response will be in the data positions and both bits 8 and 9 will be set, indicating the poll function. Bits 10-15 are undefined in the unpacked format, and should be masked by software.

The packed data input format is shown in Figure 1-7.

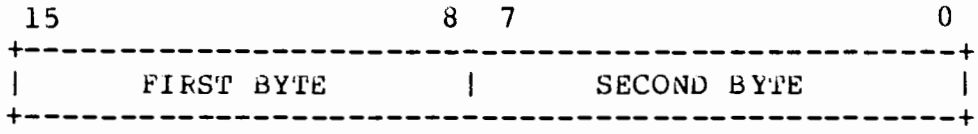


Figure 1-7. Packed Data Input Format

Here two 8-bit bytes are contained within the word. As described in "EOI" paragraph 1-12, an odd numbered byte signalling End of Record will appear in both bytes of the data word.

1-15. Status Mode (Control Flip-Flop clear)

The data format of the Status Word is shown in Figure 1-8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRQ	IFC_I	REN	IRL	LBO	LB_I	EO_I	ATN	IFC_O	X	X	O/E	SYS CTL	L	T	CIC

Figure 1-8 Status Word Format

The definition of each Status Bit is as follows:

CIC- (Controller-In-Charge bit 0) Indicates that the DI is currently controlling the disc.

T (Talk, Bit 1) - indicates that the DI is currently a talker to the disc.

L (Listen, Bit 2) - indicates that the DI is currently a listener to the disc.

SYSCTL (System Controller, Bit 3) - indicates the position of the System Controller Switch on the DI.

ODDIN (Bit 4) - if set, indicates that an odd number of bytes were received in the last (packed) input transfer. (In the unpacked mode, this bit is always set.)

IFCO (Interface Clear Output, Bit 7) - indicates that the 100 microsecond IFC one-shot is still fired.

ATN (Attention, Bit 8) - indicates the instantaneous state of the disc ATN line. This may or may not be the same as the values of ATN stored in the FIFO for each data byte.

EOI (End Identify, Bit 9) - same as above for the disc EOI line.

LBI (Last Byte Input, Bit 10) - indicates that the EOR Flip-Flop has been set.

LBO (Last Byte Output, Bit 11) - indicates that the LBO Flip-Flop has been set.

IRL (Input Register Loaded, Bit 12) - indicates that a byte (unpacked) or 2 bytes (packed) are valid in the Input Data Register.

REN (Remote Enable, Bit 13) - indicates the state of the disc REN line.

IFCI (Interface Clear Input, Bit 14) - indicates that the IFC Flip-Flop has been set due to IFC asserted on the bus.

SRQ (Service Request, Bit 15) - indicates the state of the disc SRQ line.

1-16. MASTER RESET

1-17. Master Reset Functions

The Master Reset signal is used to reset and/or initialize all data paths and Flip-Flops on the DI. MR will affect the following logic elements of the DI:

(1) Clear the DI Control Flip-Flop
(2) Clear the DI Flag Flip-Flop
(3) Reset the DI FIFO
(4) Clear the Input Data Register
(5) Reset the LBO (Last Byte Output) Flip-Flop
(6) Reset the LBI (Last Byte Input) Flip-Flop
(7) Reset the IRL (Input Register Loaded) Flip-Flop
(8) Set the input byte pointer to upper byte (if packed)

(9) Set the output byte pointer to upper byte (if packed)
(10) Reset the IFCI (Interface Clear) Flip-Flop

The MR signal is also generated by the CPU backplane signal CRS.

1-18. Rules Concerning MR

Two rules must be followed for generating MR prior to a data transfer:

a. MR must be generated before the DI is made a Talker or a Listener. This will prevent "garbage" left in the FIFO from some previous transfer from either being transmitted to the bus or read into the DI Input Data Register.

b. MR must also be generated after Packing is enabled but before the first data word is transferred.

This is necessary because in the unpacked mode, the input and output byte pointers are held in the "lower byte" position and cannot be changed. When Packing is enabled, MR must then be sent to position these pointers at the "upper byte" position, to be ready for the first byte of data.

Thus, to make the DI a Talker in Packed output format, the proper sequence is:

(1) MR (Rule 1)
(2) Control Register = Talk,Packing
(3) MR (Rule 2)
(4) Output Data to DI

Computer Museum

INSTALLATION — CHAPTER 2

2.1 General

This section provides installation information needed to interface the 12821A, Disc Interface (DI) to an HP compatible disc. The H-Series (7906H, 7920H, 7925H and 9895A) and the CS80-Series (7908x, 7911x, 7912x and 7935x) disc drives are compatible with the DI. This interface is supported only when installed on an HP 1000 M/E/F Series CPU configured under either the RTE-IVB (92068A) or the RTE-6/VM (92084A) operating system. The user choice of operating system is supplied with an HP 1000 System or may be ordered separately under one of several options. Consult your local HP Sales and Service Office (listing in back of this manual) to determine which is most advantageous to you. Included in this section are installation requirements, DIP switch settings, cabling instructions and recommended packaging and shipping procedures for product reshipment.

2.2 Unpacking and Inspection

Inspect the product shipping container before opening. If there is external evidence of damage, request that the carrier's agent be present when the container is first opened. Carefully inspect each item for damage. If there is physical damage, immediately notify your local Hewlett Packard Sales and Service Office (listing included in the back of this manual) and the common carrier. If the product fails to meet HP's published specifications or the diagnostics cannot be successfully run (see Installation Checkout, next section and Chapter 4), notify your local Hewlett Packard Sales and Service Office.

Retain the shipping container and packing material for the carrier's and HP inspection. The HP Sales and Service Office will arrange for the repair or replacement of your shipment, without waiting for your claim against the carrier to be resolved.

2.3 Checkout

To verify operation of this product, perform the diagnostics included in the 24998-14002 Diagnostic Library, included in your HP 1000 Model 60 or 65 System.

2.4 Storage and Reshipment

If your local HP Sales and Service Office instructs you to return the shipment for repair, attach a tag identifying the owner and (if possible) the HP Sales Order Number. Indicate on the tag the service to be performed or the problem encountered with this shipment. If the original, factory packaging material is available and in reusable condition, it may be useful. Whether packaged for reshipment by your Traffic Department, or a third party, good grade commercial material should be used. Carefully follow the local HP Sales and Service Office's instructions for expeditious repair or replacement of your defective product.

2.5 System Controller DIP Switch

Before installation of the DI in the CPU backplane, the System Controller function must be enabled. The eight position DIP Switch located at position U13 (see Figure 4-1) on the PCA has switch eight (U13-S8) assigned to the system controller function. Set S8 to the OPEN (OPEN = 1) position to enable the system controller function. Switches 1 through 7 are used by the diagnostic only. Setting S1-S7 to be closed position will provide an address of 0 when requested by the diagnostic.

WARNING

Hazardous voltages are present inside the computer mainframe! Before installing the DI or the loader ROM, set the POWER switch to OFF. Failure to observe this warning can result in serious injury.

2.6 Installation

Install the DI as follows:

1) Set the computer ~POWER switch to OFF.

2) Remove the I/O card cage cover.

3) If you are installing the DI in an HP 1000 system, insert the DI into the I/O slot (select code) reserved for it (refer to Table 1 of your HP 1000 Primary System Configuration Data Data Manual) otherwise install it in any convenient I/O slot.

4) Install the HP 12992H Disc Loader ROM for H-Series disc drive operation using the instructions contained in the 12992 Loader ROM's Installation Manual, HP Part No. 12992-90001.

-OR-

5) If CS80-Series disc drives are to be used, Option 001 was ordered to delete the H-Series Loader ROM and the 12992J, CS-80 Series Loader ROM was ordered as a separate line item. Install it using the instructions contained in the 12992J Loader ROM Installation Manual, HP Part No. 12992-90001.

NOTE

If the DI was purchased as part of an original HP 1000 System, order the DI and the loader ROM will have been installed. Refer to the decal on the inside of the cabinet front door to determine the DI and loader ROM location.

6) Turn OFF all disc drives before connecting cables to the DI or the disc drive.

7) Perform the disc installation and checkout procedures described in your Disc Installation and Service Manual before connecting the 59310-60002 cable from the DI to the first disc drive.

CAUTION

ALL disc drives must be OFF before connecting cables

2.7 Interconnecting Cables

a) If you are installing an HP 1000 Model 60 or 65 System, attach the 59310-60002 cable (3.69 meters) from the DI to the first disc drive and interconnection cables to any additional disc drives (see Figure 1-1 and Table 1-1). Then perform the primary system tests described in your "Getting Started" manual.

b. If you are installing an HP 1000 Series M/E/F computer, run the 24998 diagnostics (refer to the Disc Interface Diagnostic Manual, 12821-90002). Then connect the 59310-60002 cable from the DI to the first disc drive, and the interconnecting cable to any additional disc drive.

2.8 System or Subsystem Checkout

Refer to the HP 1000 Model 60/65 Installation And Service Manual, HP Part Number 5955- 4359 for system checkout procedures or to the diagnostic manual 12821-90002 for DI checkout procedures. If a disc or system level problem is indicated, use the 91711B, Diagnostics And Verification Package to isolate.

NOTE

In order to prevent degraded operation, ALL disc drives cabled to the disc interface (DI) must be powered ON whenever your computer or system is operating.

3-1. INTRODUCTION

This section provides a brief description of the logical operation of the Disc Interface. This theory is presented to aid in confirming that a problem exists on the DI rather than another component of the subsystem. The DI is a multilayer PCA and should be returned to a Hewlett-Packard service center for repair, warranty may be voided if repaired by unqualified personnel. Assembly and schematic diagrams to be used in conjunction with this discussion are located in section IV.

3-2. SIGNAL NAMES AND LOCATIONS

Signal names are mnemonic identifiers usually chosen to be as close to the signal usage as possible. These signal identifiers may have a bar over them on the schematics to indicate the signal is active low. In text the same signal will contain an "L" at the end of the signal name to indicate the active low condititon. This section references the the disc interface logic diagram D-12821-60001-51 through 53. During the discussion, sheet number and coordinates are indicated by brackets. The coordinates will be that of an area of the schematic which contains the logic circuit described in the text.

3-3. CHANNEL SELECT LOGIC

The CHSEL (Channel Select U117-4) signal [52A-1] is the logical AND of IOG (I/O Group Instruction), LSCM (Lower Select Code, Most Significant Digit), and LSCL (Lower Select Code, Least Significant Digit). It is used to enable the Control, Flag Buffer, Flag, and Input Multiplexer Enable logic blocks when an I/O instruction is being executed and is directed to the DI's select code.

3-4. CONTROL LOGIC

3-5. Control Flip-Flop and Logic

The Control Flip-Flop Output signal CONTROLL [52B-1] (U126-4, low true) determines whether the DI is in Data Mode or in Configure/Status Mode. Data Mode is selected by executing an STC DI instruction. The CHSEL signal (U117-4) enables the STC signal [52B-2] (U127-5) to the Control Flip-Flop. STC is inverted through the NAND gate (U127) and resets the Control Flip-Flop

(U126-1) so that CONTROLL is low. CONTROLL is inverted and is input to the NAND gate which generates OBCLKL [52C-2](U105-8) in addition to being input to the Flag and input Mux Enable logic. OBCLKL is derived from IOO when CONTROLL is zero and CHSEL is one, i.e., when an I/O output instruction to the DI is executed and the card is in data mode. OBCLKL is used to clock the Output Data Register.

Similarly a CLC DI instruction selects Configure/Status mode by settng the Control Flip-Flop (CONTROLL = 1). CONTROLL enables the NAND gate which generates CWCLKL [52C-1]. CWCLKL is derived from IOO when CONTROLL and CHSEL are one, i.e. when an I/O output instruction to the DI is executed and the card is in configure mode. CWCLKL is used to clock the Control Word Register [52E-2].

3-6. Control Word Register

The Control Word Register is made up of two Octal D-type flip-flops (U96, U56, 74LS273) with a common clock. The inputs are the IOBO (Input/Output Bus Output) lines from the CPU. Data is latched on the rising edge of CWCLKL. The Control Word Register is cleared by the CRSL (Control Reset, low true) [52C-1] signal and not by MR.

3-7. Bus Transceivers and Control Line Logic

The bus transceivers used are National 8835 inverting quad tri-state party line transceivers (U41, U31, U21) and National 8838 inverting quad unified bus transceiver (U51) with open collector drivers [51C,D-2 and 51G-3].

The 8838 is used for the NDACL, NRFDL, SRQL and RENL control lines. The open collector drivers allow wired-OR connection of the lines. The drivers are always enabled so that any signal seen on the S inputs are sent to the bus and any signal seen on the bus is received at the R outputs.

In general, a signal to be sent to the disc will be called XXXOUT, and one received from the disc will be called XXXIN where XXX is the mnemonic of the appropriate control line (ATN, REN, NDAC etc.)

An 8835 is used for the other bus transceiver on the control lines. Its receivers are always enabled. Its drivers, however, are enabled only when the DI is controller-in-charge and the DI is a talker. The driver enable signal is generated by some of the combinational logic referred to as the Control Line Logic (U61-3, U61-6) [51C-3].

The driver enable signal is ORed with the PPC (Parallel Poll Conduct) signal to generage XMITL (U52-11) [51D-3]. XMITL is used to enable the drivers on the Data Line Bus Transceivers (U31,21) and also tells the transmit handshake logic that a data transfer is about to begin.

U102-6 [51B-2] allows RENL to go low if the DI is System Controller and the RENEN bit in the Control Register is set. Similarly, U53-8 [51B-3] allows SRQL to go low if the DI is not controller-in-charge and the SRQEN bit in the Control Register is set. The gates U122-6 [51B-2] and U32-11 [51A-3] are used to assert ATNL (DI must be Controllerin-Charge) or EOIL respectively, if ATNOUT or EOIOUT are asserted, or if a parallel poll is being conducted (PPC is high) by the DI.

The bus transceivers on the data lines (U31,21) have the FIFO and Output Byte Select logic outputs (OUTBUS1-8) [51H-3,4] as their driver inputs. The drivers are enabled whenever XMITL is low. Their receiver outputs (INBUS1-8) are input to the FIFOs [53D,H-3] and Input Byte Select logic. The receivers are enabled whenever RCVL is low.

The bus lines are loaded by seven equivalent HP-IB loads. The loading is done by the 240 (R2,R4) and 680 ohm (R3,R5) biasing resistors [51E-1 and H-3]. In their high state the lines are at 3.7V with no external devices connected to the DI.

Computer Museum

3-8. OUTPUT DATA REGISTER

The Output Data Register is made up of two octal latches (U86, U66) [52G-2] with common clock and enable. While OBCLKL is low the latch outputs follow the IOBO lines. Data is latched when OBCLKL returns high. Typically the latch outputs are enabled. The outputs will be high impedence if RCV is a one indicating that the DI is receiving data from the disc or if the DIAG bit of the Control Register [52E-2] is set (see paragraph 3-20). The latch outputs are input to the FIFOs and the Input Byte Select logic [53F-2].

3-9. INPUT BYTE SELECT LOGIC

The Input Byte Select logic [53F-2] is used to enable the INBUS to the Upper Byte FIFO when the DI is receiving data from the disc. National's 81LS95 Tristate Octal Buffer (U76) is used with RCVL as the enable.

3-10. INPUT DATA SELECT

The Input Data Selector [51H-3] is a 74LS157 Quad 2 to 1 Data Selector (U16). Its outputs are always enabled and are input to the Tag FIFO. RCV is used as the select. When the DI is receiving data from the disc (RCV = 1), the ATN (ATNIN) and EOI (EOIIN) values associated with the current byte on the bus are selected. When the DI is transmitting data over the bus (RCV=0) bits DI8 and DI9 are selected. Note that these bits correspond to ATN and EOI when in unpacked data format.

3-11. THE FIFO`s

3-12. Introduction

The Fairchild 9403 First In First Out Buffer Memory is used as the basic building block for the DI FIFO Buffers [53F-3]. A general description of the 9403 will be given first, then a more detailed description of how the DI utilizes this part. For a more complete description of the 9403 consult the Fairchild Macrologic Bipolar Microprocessor Data Book.

3-13. The 9403 IC

The 9403 is organized as 16 words by four bits (Figure 3-1). It is capable of being expanded to any number of bits and may be loaded and unloaded asynchronously and parallel. The outputs are tristate.

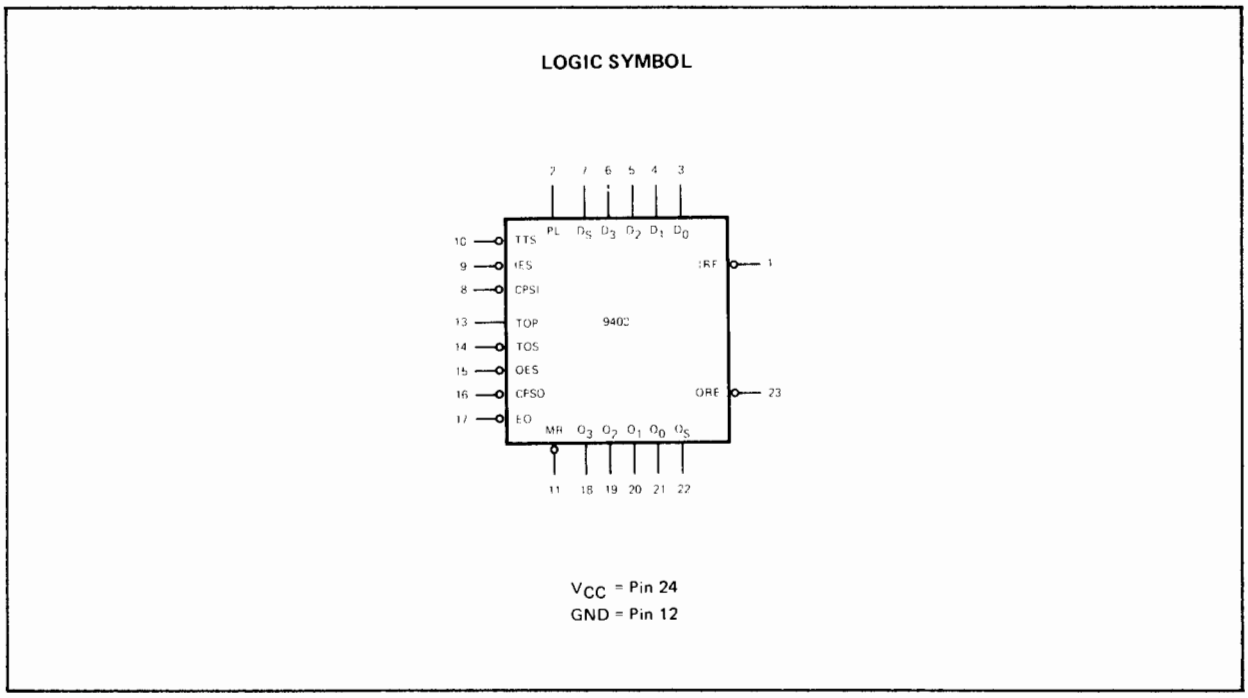


Figure 3-1. The 9403 FIFO IC

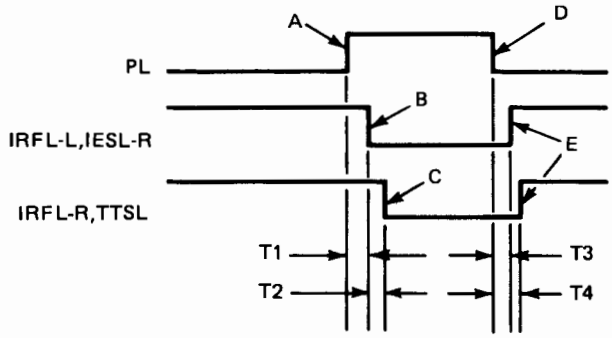
A high on PL (Parallel Load Input) parallel loads the D inputs into the input register internal to the FIFO, and IRFL (Input Register Full Output, low true) goes low indicating the register is full. (Note: IESL (Serial Input Enable) must be low to enable parallel inputs). The input register feeds the FIFO stacks and if the top location of the stack is empty then when TTSL (Transfer to Stack input, low true) goes low the data falls through to the stack automatically - pausing only when necessary to wait for the next location to empty. The input register is reinitialized when PL returns low. When the FIFO's input data register contents have been transferred to the stack IRFL returns high, assuming horizontal expansion to more than 4 bits in width, automatic FIFO action is achieved by connecting the IRFL output of the rightmost tip of a logical block to the TTSL input of all the FIFOs of that block.

After data has entered the 9403 and fallen through to the last stack location it is transferred into the FIFOs output data register if TOP (Transfer Out Parallel Input) is high. After this transfer OREL (Output Register Empty Output, low true) goes high indicating there is valid data in the FIFO's output data register. If EOL (Output Enable, low true) is low the output data register contents are seen at the FIFO outputs.

TOP is used to "clock" out such words. When TOP goes low the data is latched in the output data register. OREL goes low to indicate that the data has been extracted. However, the data remains in the output data register until TOP returns high, allowing the next word to be transferred into the register.

3-14. The DI FIFO Buffers

The FIFO buffers are logically divided into two blocks; the Upper Byte FIFO, and the Lower Byte and Tag FIFOs. The Upper Byte FIFO consists of two 9403's organized as 16 words by 8 bits. The Lower Byte and Tag FIFO's are made up of 3 9403's organized as 16 words by 12 bits. Since the structure of each block is similar the Upper Byte FIFO will be described and then the differences in the Lower Byte and Tag FIFO will be pointed out. The 9403's which make up the Upper Byte FIFO have a common PL signal (PLHI) and TTSL signal. The IRFL output of the rightmost FIFO provides the TTSL signal and is ultimately used to derive IRHI. The IRFL output of the left-most FIFO provides the rightmost FIFO IESL input. The inputs are always enabled on the leftmost FIFO. Thus for loading the upper byte the sequence of events is as shown in Figure 3-2.



A A HIGH ON THE PL INPUT LOADS THE LEFTMOST 9403 OF THE UPPER BYTE FIFO.

B IRFL OF THE LEFTMOST 9403 GOES LOW ENABLING THE INPUTS OF THE FIFO TO ITS RIGHT.

C IRFL OF THE RIGHT 9403 GOES LOW INDICATING ITS INPUT REGISTER IS FULL. THE UPPER BYTE IS COMPLETELY LOADED. TTSL IS PULLED LOW ON BOTH 9403'S ENABLING THE TRANSFER OF THE INPUT DATA REGISTER CONTENTS TO THE FIFO STACKS.

D PL RETURNS LOW. THE INPUT REGISTER IS REINITIALIZED.

E THE INPUT DATA REGISTER CONTENTS HAVE BEEN TRANSFERRED TO THE FIFO STACKS AND THE IRFL SIGNALS MAY RETURN HIGH.

T1, T2, T3 AND T4 ARE INTERNAL FIFO DELAYS.

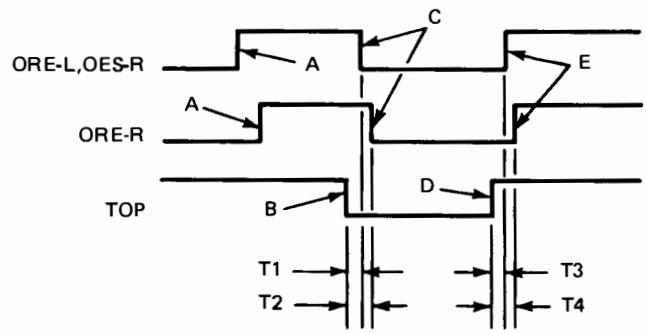
Figure 3-2. Upper Byte FIFO Loading

The FIFOs also have a common TOP signal. The outputs of the leftmost FIFO are always enabled and its OREL output signal provides the output enable to the rightmost FIFO. The rightmost FIFO's OREL signal is used in deriving ORHI. The sequence of events for unloading the upper byte are as shown in Figure 3-3.

The Lower Byte and Tag FIFO's 9403's are chained together and loaded in the same manner as in the Upper Byte FIFO. The PL signal is PLLO and the IRFL output of the rightmost FIFO is IRLO.

Unloading the Lower Byte and Tag FIFOs differs from the Upper Byte only in when the FIFO outputs are enabled. The Lower Byte FIFO's outputs are high impedence when the DI is not receiving data (RCV=0) and the Output Byte Pointer points to the Upper Byte (OBP=1). When the DI is transmitting over the bus the Output Byte Select logic enables the Upper Byte to the OUTBUS lines when OBP is high. When OBP points to the lower byte the Lower Byte outputs are enabled to the OUTBUS lines and the Output Byte Select logic outputs are high impedance.

The Tag FIFO outputs are always enabled. All five 9403's have a common reset line, MRL.



A A BYTE HAS BEEN LOADED INTO THE UPPER BYTE FIFO'S OUTPUT DATA REGISTER.

B TOP GOES LOW LATCHING THE DATA

C OREL GOES LOW INDICATING THAT THE DATA HAS BEEN EXTRACTED. RECALL THAT VALID DATA REMAINS AT THE FIFO OUTPUTS UNTIL TOP RETURNS HIGH.

D TOP RETURNS HIGH, ALLOWING A NEW BYTE TO BE LOADED INTO THE FIFO'S OUTPUT DATA REGISTER.

E A NEW DATA BYTE IS LOADED INTO THE FIFO'S OUTPUT DATA REGISTER.

T1, T2, T3 AND T4 ARE INTERNAL FIFO DELAYS.

Figure 3-3. Upper Byte FIFO Unloading

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3-15. OUTPUT BYTE SELECT LOGIC

The Output Byte Select Logic (U36) [53F-4] is used to enable the Upper Byte FIFO's outputs to the OUTBUS lines when the DI is transmitting data to the disc in packed data format. As discussed above, the 81LS95's outputs are enabled when RCV is low and OBP is high. Otherwise the outputs are high impedance.

3-16. OUTPUT DATA SELECT

A 74LS157 (U43) [53D-4] was used with the PACK bit of the Control Word Register as the select and its outputs always enabled. The outputs provide the ATNOUT and EOIOUT signals sent to the bus transceivers and the values of bits 8 and 9 of the Input Data Register or Output Byte, depending on what type of transfer is taking place. Figure 3-4 summarizes the function of the Input and Output Data Selectors.

3-17. INPUT DATA REGISTER

The Input Data Register [53F5] consists of two 74LS273 Octal D Flip-Flops with a positive-edge-triggered clock and direct clear input. The clear signal is Master Reset and the clock is Input Register Loaded. Inputs come from the FIFOs and Output Data Select Logic (EOI and ATN during unpacked input transfers). The register outputs are input to the Input Data Multiplexer [52G-5].

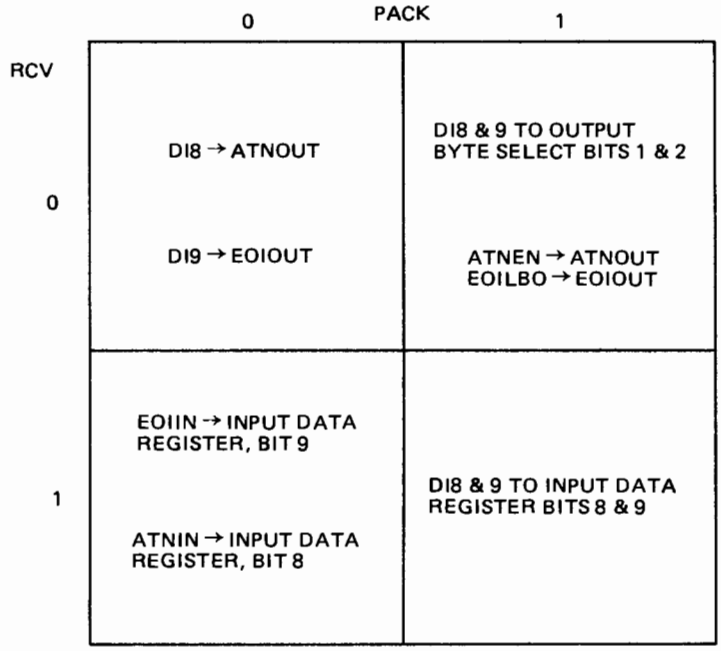

Figure 3-4. Function of Input Output Data Selectors

(A) IBI TRANSMITTING DATA OVER THE HP-IB IN UNPACKED DATA FORMAT. DI8 AND DI9 CORRESPOND TO THE ATN AND EOI VALUES ASSOCIATED WITH THE DATA BYTE DI7-0 AND ARE OUTPUT TO THE HANDSHAKE AND CONTROL LINE BUS TRANSCEIVERS AS THE DATA BYTE IS OUTPUT TO THE DATA TRANSCEIVERS.

(B) IBI TRANSMITTING DATA OVER THE HP-IB IN PACKED DATA FORMAT. THE UPPER BYTE (DI8-15) IS OUTPUT TO THE BUS INTACT. ATNOUT IS DETERMINED BY THE CONTROL WORD REGISTER, EOIOUT BY THE CONTROL WORD REGISTER AND THE END-OF-DATA DETECT LOGIC.

(C) IBI RECEIVING DATA FROM THE HP-IB IN UNPACKED DATA FORMAT. THE EOI AND ATN VALUES ASSOCIATED WITH EACH BYTE ARE LOADED INTO BITS 9 AND 8 OF THE INPUT DATA REGISTER AS THE DATA IS LOADED INTO BITS 0-7.

(D) IBI RECEIVING DATA FROM THE HP-IB IN PACKED DATA FORMAT. THE UPPER BYTE IS LOADED INTO THE INPUT DATA REGISTER INTACT.

3-18. END OF DATA DETECT LOGIC (L1)

The End of Data Detect Logic [53H-5] examines the EORL and EDTFF tags from the Tag FIFO looking for the last byte in an input or output transfer, respectively. The EORL Tag is input to a D-type flip-flop (U114). The flip-flop is clocked by IRL as the data word the EORL Tag corresponds to it is clocked into the Input Data Register. The flip-flop output EORFF (End of Record Flip-Flop, low true) is input to the Interrupt Source, Mask Logic [53B-2]. This flip-flop is preset by Master Reset.

The EDTFF tag is input to an AND gate (U53-2) which is enabled (U52-3) when the Output Byte Pointer points to the lower byte (OBPL=1; unpacked format or packed format-even no. of bytes) or the O/E bit of the Control Register is set (packed format-odd no. of bytes). When EDTFF goes high LBO is generated (U53-3). If the EOIEN bit of the Control Word Register [52E-2] is set EOILBO also goes high (U53-6).

3-19. TRANSMIT HANDSHAKE LOGIC (L1)

The Transmit Handshake Logic [51B-5] controls the handshake for output transfer. It generates DAVOUTL and monitors the NRFDL and NDACL lines. It also generates THSKL, which is used as a clock by the FIFO Unload and [53B-4] Last Byte Out Logic [53B-5] blocks.

Figure 3-5 shows the timing and signal transitions within the Transmit Handshake Logic. The RC delay circuits provide the 1.0 microsecond delay before transfer of the first byte and the 350ns. delay prior to each subsequent byte as required by the IEEE 488-1978 Standard. When the last byte has been transferred TRDYL remains high, freezing the bus with DAVOUTL held high.

3-20. HOOKS FOR THE DIAGNOSTIC (L1)

Included in the Transmit Handshake Logic [51B-5] and the Output Data Register [52G-2] is logic [51B-5] used by the diagnostic program to enable the DI to "talk to itself". This logic is enabled by setting bit 7 (DIAG) in the Control Word Register.

The test sequence loads the FIFO with known data, cycles that data through the FIFO out to the bus transceivers and back into the FIFOs, and then reads the data back into the CPU to check its validity. The Receive Handshake, Transmit Handshake, FIFO Load and Unload logic is checked in addition to the FIFOs and the Bus Transceivers.

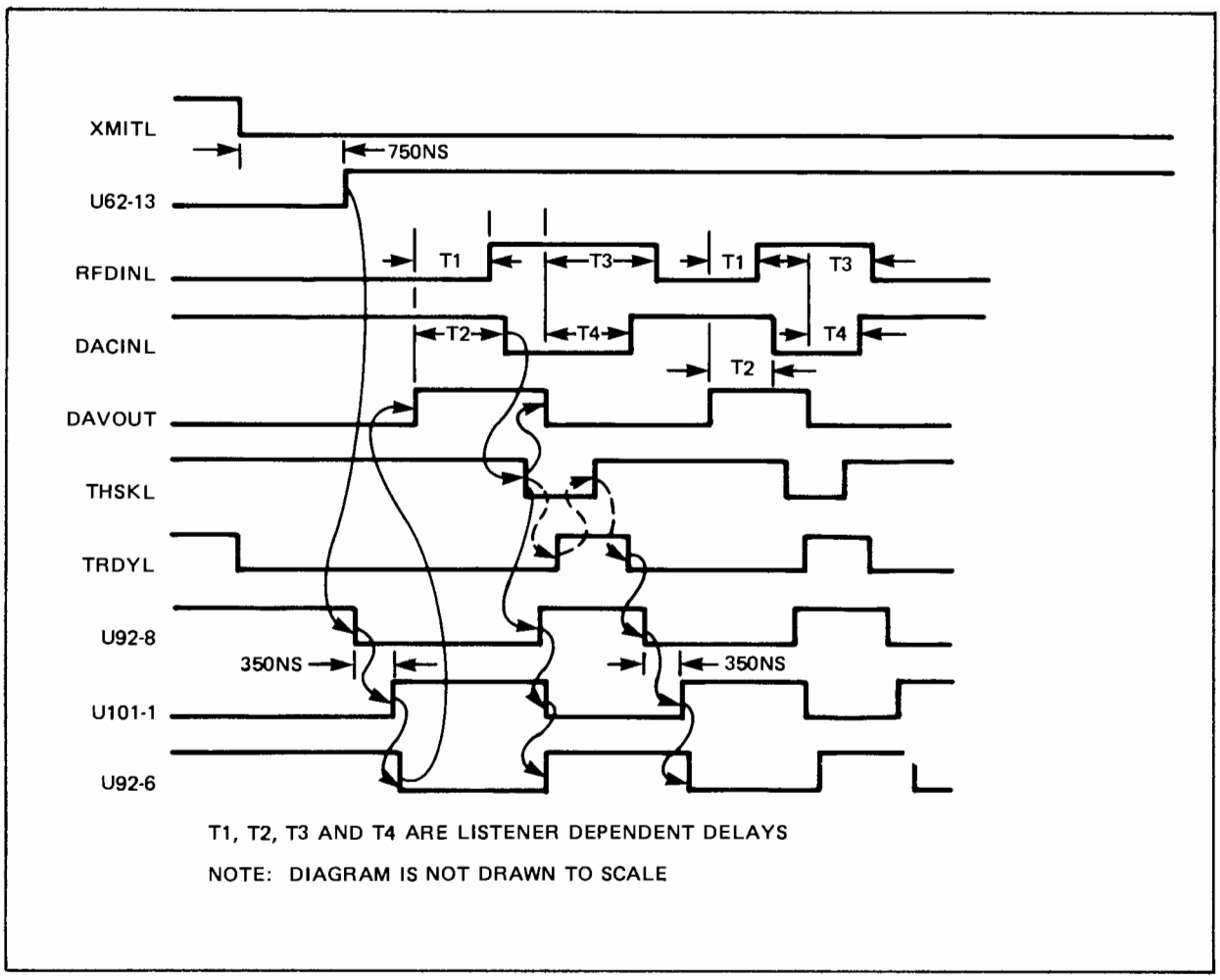

Figure 3-5. Transmit Handshake Logic Timing

The diagnostic first fills the FIFO with data, then the card is configured with the DIAG,T,L and CIC bits set. The card is now enabled to both receive and transmit data. The transceivers have their drivers enabled to their receivers so the OUTBUS and INBUS lines are tied together and DAVOUT is tied to DAVIN, RFDOUT to RFDIN, and DACOUT to DACIN. There is valid data on the OUTBUS/INBUS lines.

When the card is configured with control word 207 (octal) the flip-flop U114-9 is set, disabling U94-3 (Figure 3-6). The card is placed in data mode and an OTA DI,C or OTB DI,C instruction is executed for each byte rotated. Recall that an OT* instruction results in the signal OBCLKL.

On the rising edge of OBCLKL U114-9 is reset and U94-3 goes low causing DAVOUT (and DAVIN) to be asserted. The FIFO load sequence begins. When the byte is loaded DACOUT (and DACIN), and RFDOUT (and RFDIN) are asserted. When DACINL goes low U7209 is set and DAVOUT (and DAVIN) goes low. A new byte is now transferred to the FIFOs outputs. RFDOUT (RFDIN) and DACOUT (DACIN) return low but futher transfers are inhibited until the next OT* DI,C instruction is executed (Figure 3-6).

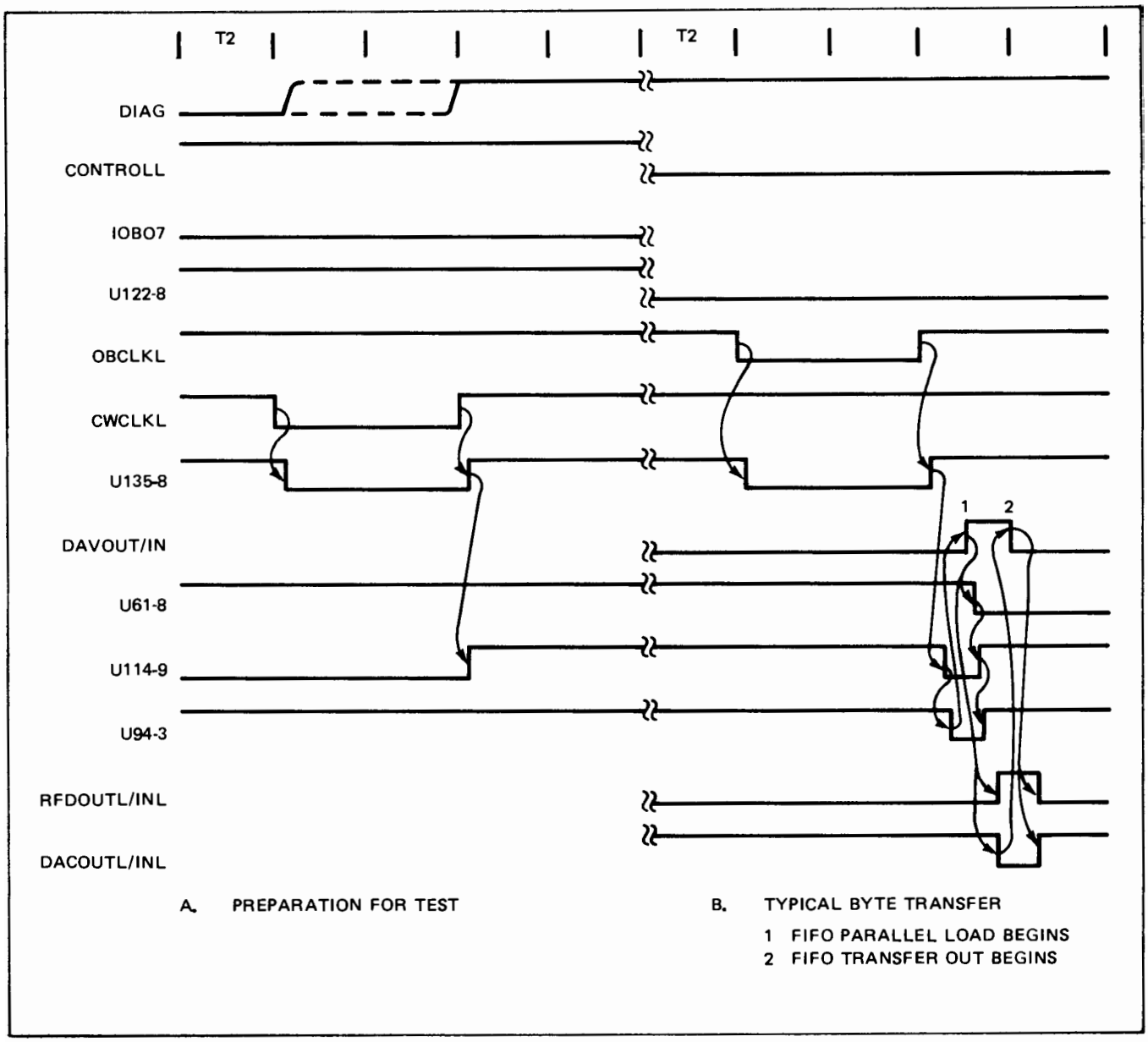

Figure 3-6. Diagnostic Timing Logic

Note that a DIAG bit value of one disables the Output Data Register (U52-6)[52G-2], causing its outputs to be high impedence. For all other transfers or tests the DIAG bit is clear and U114-9 [51B-5] is always a zero, enabling U94-3. Thus it is as if U92-6 was tied directly to U72-11 and 12.

3-21. RECEIVE HANDSHAKE LOGIC

The Receive Handshake Logic [51C-4], controls the bus handshake for input transfers. It monitors the DAVIN line and generates RFDOUTL and DACOUTL accordingly. RHSKL is also generated and serves as a clock input to the FIFO Load Logic and Last Byte In Logic [53B-3].

Figure 3-7 shows the timing in the RHSK Logic. In a typical input transfer where the DI is CIC RCVL goes low when the DI is made a listener.

When the last byte in a transfer is received RRDYL remains high freezing the RHSK Logic with RFDOUTL high. Note that RFDOUTL may also be asserted by setting the NRFD bit of the Control Register to one (U52-10). DACOUTL will remain low until DAVL returns high at which time DACOUTL goes high.

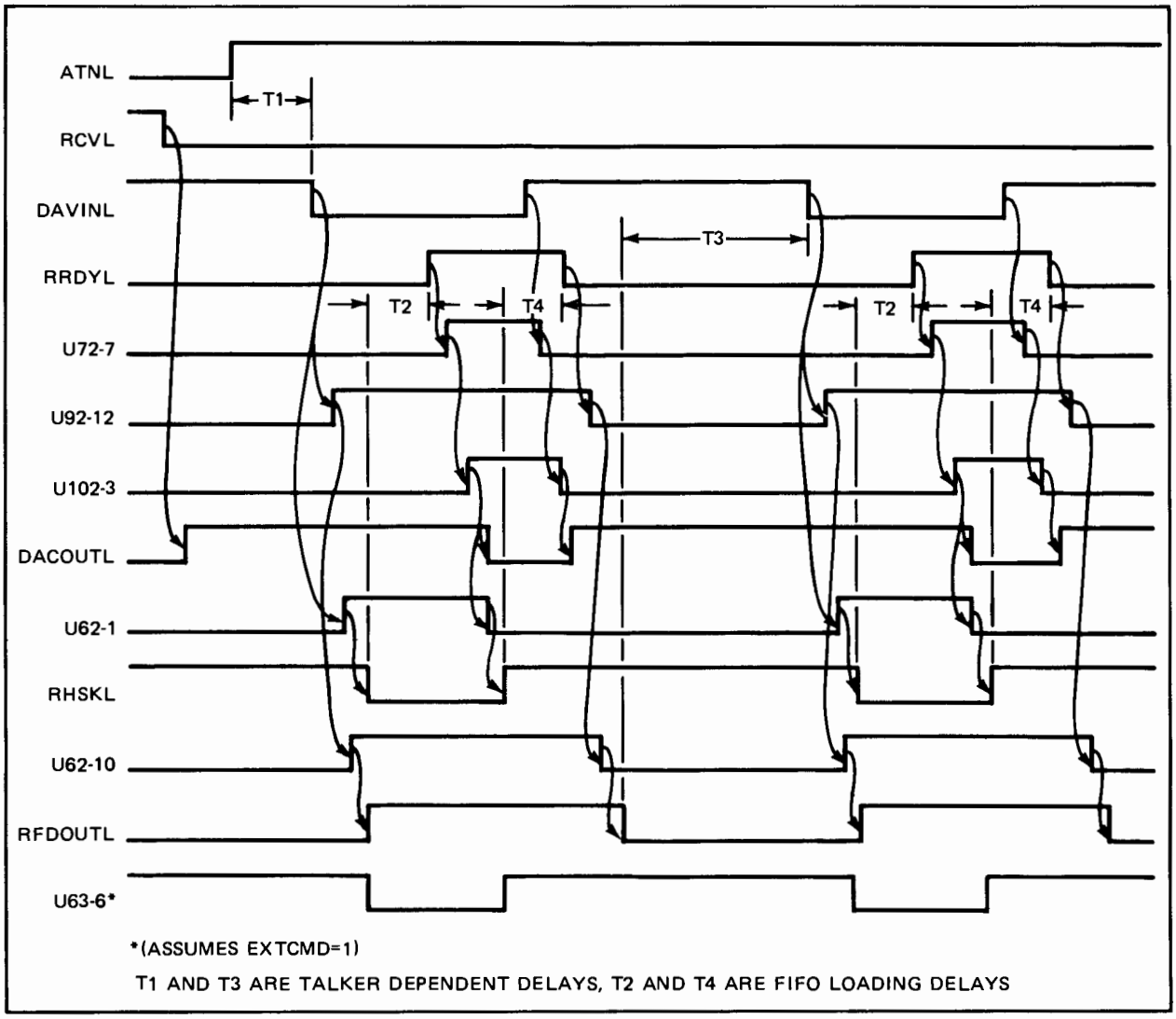

Figure 3-7. Receive Handshake Logic Timing

3-22. THE LAST BYTE IN LOGIC

The Last Byte In Logic [53B-3] performs three distinct functions. During an output transfer the LBI Logic generates ORLL (Output Register Loaded, low true). Recall that ORLL is used by the FIFO Load Logic to generate the FIFO loading signals PLHI and PLLO. The timing for this is shown in Figure 3-8.

Figure 3-8 shows the timing for loading a parallel poll response. In this case the loading sequence is initiated by PPRLL [51F-1 and 53A-3]. Because PPRLL remains low the ORLL signal is generated repeatedly, until the FIFO fills. This features is admittedly poor but not disastorous since after the PP response is read by the CPU the FIFOs will be cleared and thus the multiple loading is ignored.

Lastly, the DI Logic detects the last byte in an input transfer. If the LFEN and/or the EOIEN bits of the Control Register are one then EORL (End of Record, low true) will be generated when a LF or EOI is received by the DI, respectively (U113-6). The Last Byte In Flip-Flop is then reset on the rising edge of RHSKL to assert LBIFF high.

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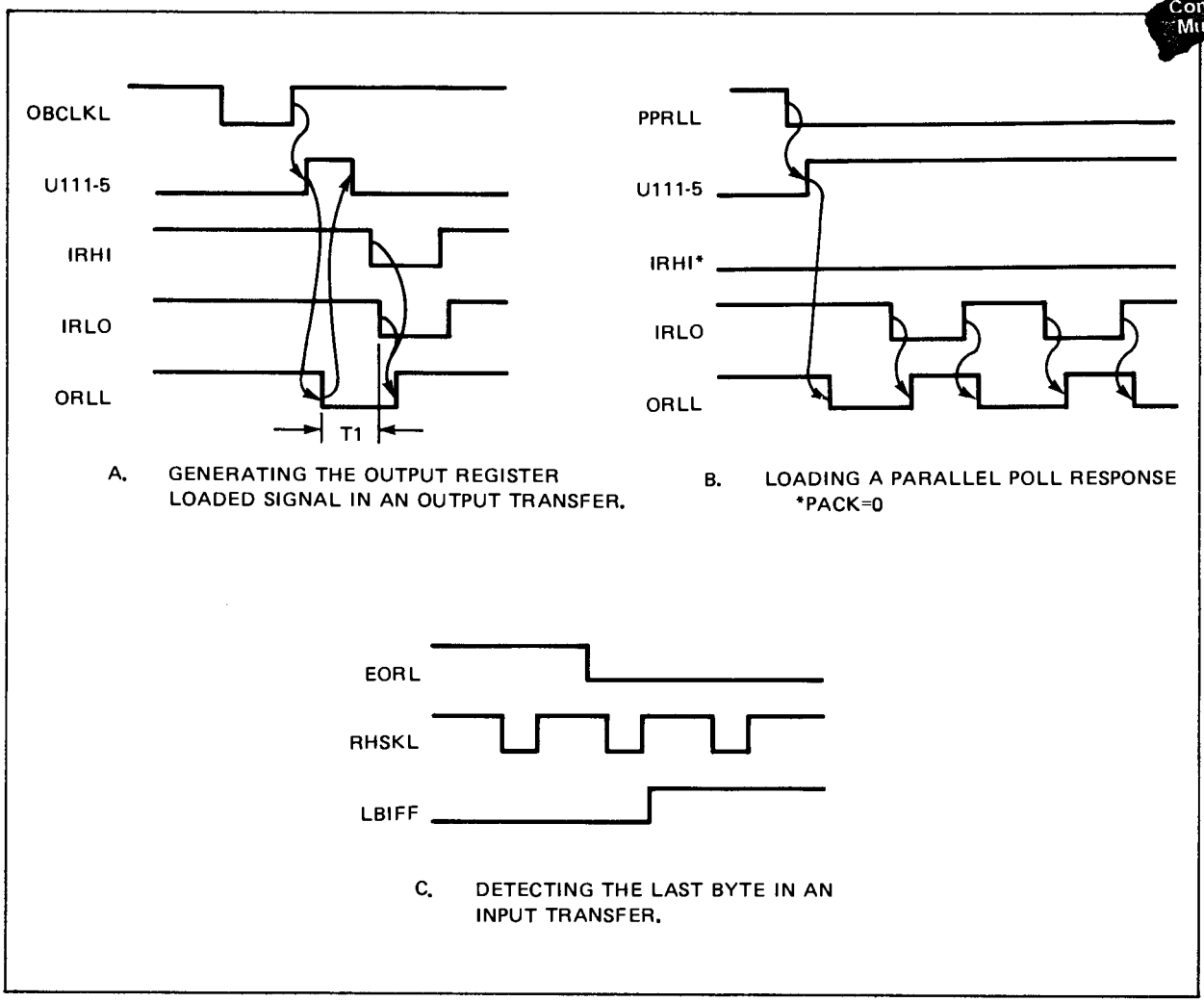

Figure 3-8. Last Byte In Logic

3-23. FIFO LOAD LOGIC

The FIFO Load Logic [53B-3] generates the FIFO loading signals for all input and output transfers, and for loading parallel poll responses.

The timing for an input transfer is given in Figure 3-9. Packed data format and an odd number of bytes have been assumed. RHSKL causes the Input Byte Pointer to switch to select either PLHI or PLLO. A master reset is executed before a transfer in packed format to set the IBP to the upper byte (U121-1).

For a transfer in unpacked data format PACK is low and the IBP is held pointing to the lower byte (U121-4). Thus PLHI remains low and PLLO is generated for each byte received.

Also shown in Figure 3-9 is the loading of an odd numbered last byte. When the last byte is received EORL goes low forcing U132-6 to a one. Thus U105-12 is enabled and both PLHI and PLLO are generated. The odd numbered last byte is loaded into both the upper and lower byte FIFOs. On the rising edge of RHSKL the LBI Flip-Flop is set. LBIFFL disables the RRDYL line (U133-8) preventing further input transfers. The IBP pointer is set to the lower byte in anticipation of another byte. Thus ODDIN (U121-5), the complement of IBP, is high, indicating an odd number of bytes was input.

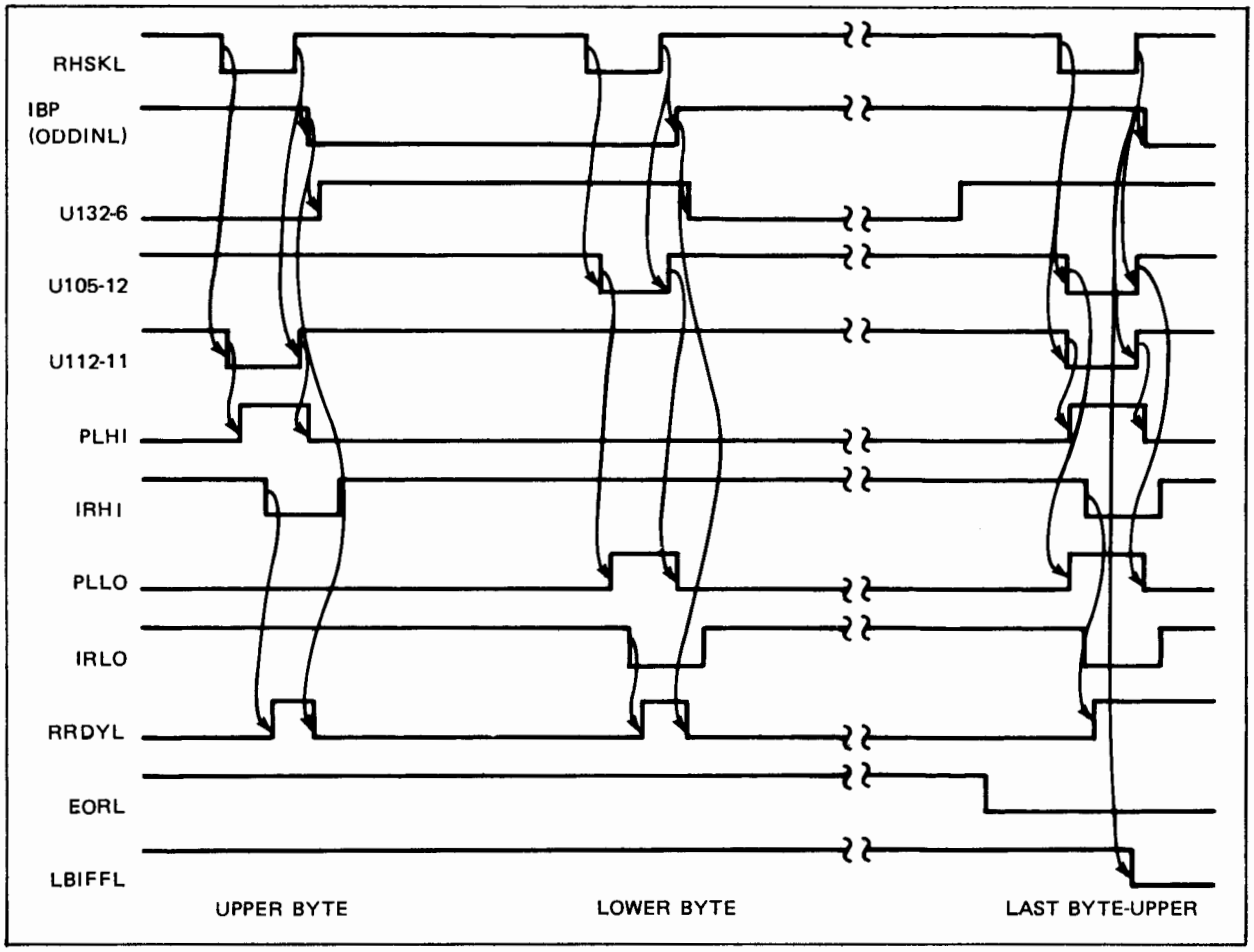

Figure 3-9. FIFO Load Logic (Packed Data Format Input from Bus)

If the last byte is an even numbered byte it is loaded into the lower byte FIFO and LBIFFL disables the RRDYL line as above. The IBP is set to the upper byte and ODDIN is low indicating that an even number of bytes were transferred.

When the FIFOs are being loaded with the Output Data Register contents or with a parallel poll response only gates U112-6 and U112-8 of the FIFO Load Logic are used (Figure 3-10). Because RHSKL is high the gate outputs U105-12 and U112-11 are also high enabling the above gates to generate PLHI and PLLO each time ORLL is generated. If unpacked data format is used IRHI remains low (U102-11) and the Upper Byte FIFO is ignored.

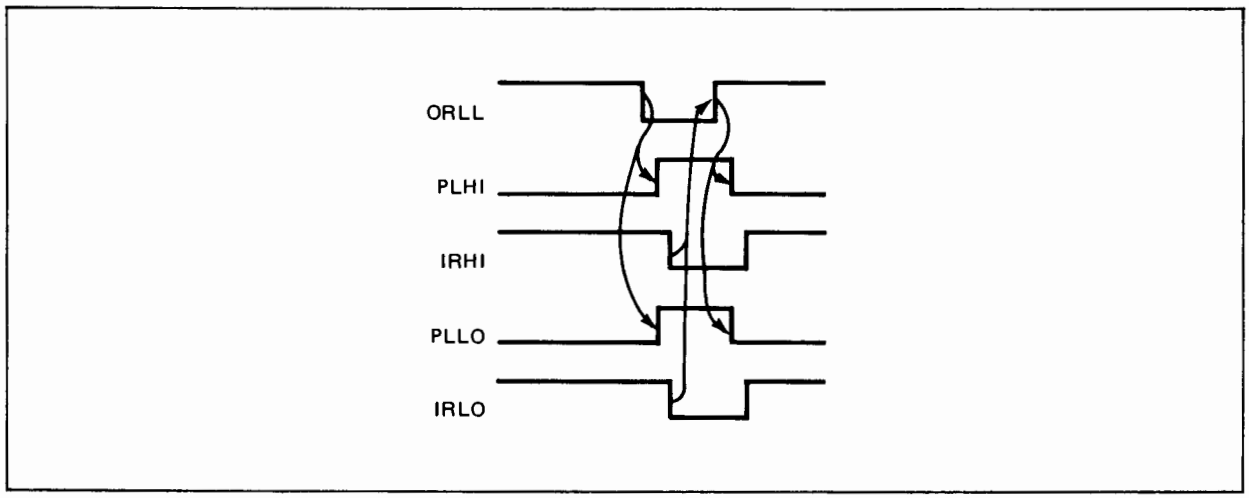

Figure 3-10. FIFO Load Logic (Load Output Data Register into FIFO's)

3-24. FIFO UNLOAD LOGIC

The FIFO Unload Logic [53B-4] controls the FIFO unloading signals TOPHI and TOPLO. Data is output to the disc or loaded into the Input Data Register [53F-5].

Figure 3-11 shows the timing for an output transfer in packed format. The Output Byte Pointer causes the logic to alternate between generating TOPHI and TOPLO from THSKL. A master reset before the transfer in packed format guarantees the OBP points to the upper byte first (U121-13).

If unpacked data format is used PACK is low causing the OBP to point to the lower byte continuously (U121-10). Thus TOPHI remains high and ORHI remains low (U102-8) throughout the transfer. TOPLO is generated with each THSKL to load the Lower Byte FIFO.

Also shown in Figure 3-11 is the unloading of the last byte. If the last byte is the lower byte (OPB=0) or the last byte is the upper byte and the O/E bit in the Control Word Register is equal to one then the Last Byte Out Flip Flop is set on the rising edge of THSKL. LBOFFL inhibits further transfers by holding TRDYL high (U113-11,12).

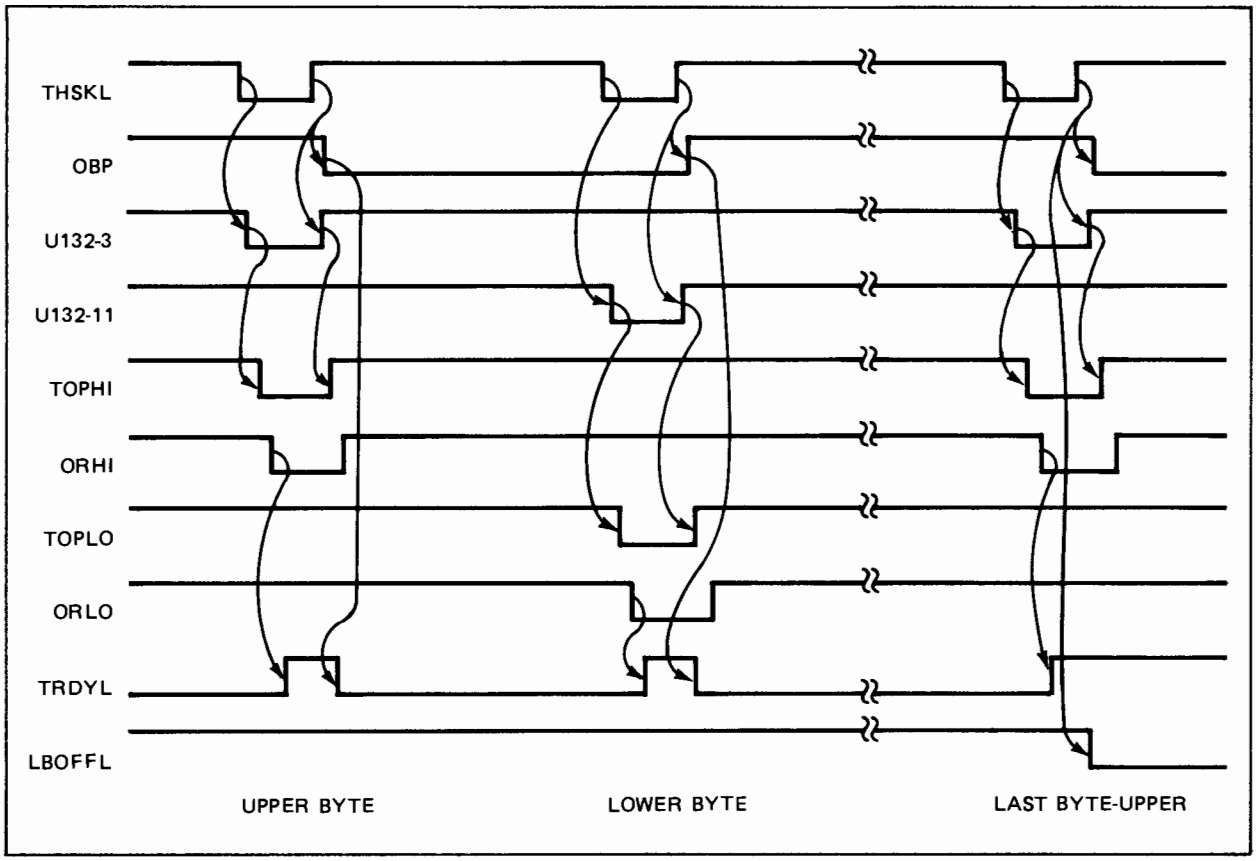

Figure 3-11. FIFO Unload Logic (Packed Data Format Output to Bus)

Figure 3-12 shows how the FIFO unloading signals are generated when the FIFOs are being unloaded into the Input Data Register. THSKL is high causing the outputs U132-3 and U132-11 to be high, enabling U122-11 and U122-3 respectively. The LBO Logic generates TTIRL (Transfer To Input Register, low true) each time a word is to be input. TOPHI and TOPLO are generated simultaneously from TTIRL. None of the other FIFO Unload Logic is used.

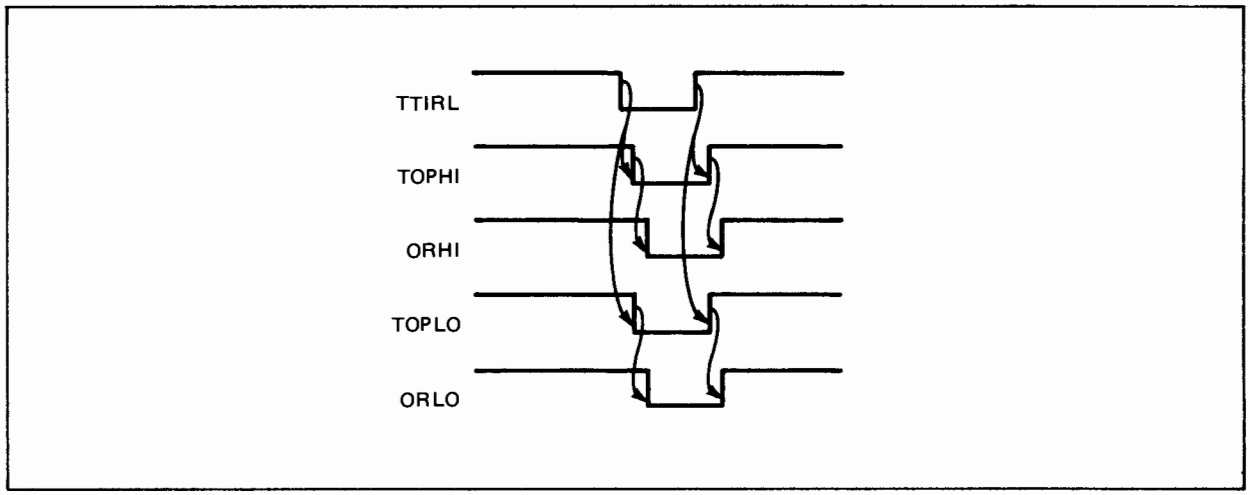

Figure 3-12. FIFO Unload Logic (Packed Data Format, FIFOs to Input Data Register)

3-25. LAST BYTE OUT LOGIC

The LBO Logic [53B-5] consists of three parts; the LBO Flip-Flop (U131-9), the Generate Service Request Logic (U133-6)[53C-5], and the Input Register Load logic.

Figure 3-13 shows the timing for the Input Register Load and GENSRQ Logic [53A-5 and 52D-5]. Transfer of the first word into the Input Data Register is initiated by Output Ready (U83-13) as soon as both ORHI and ORLO are high (U83-13). Transfer of each succeeding word is initiated by IRLL (U83-1), providing that the word is available at the FIFO outputs.

If unpacked data format is used then Output Ready is equivalent to ORLO (U101-10). The LBO and IRL Flip-Flops are reset by the master reset signal. The IRL logic is enabled only when RCV is a one (U83-2), i.e., when the DI is inputting data from the disc.

After the last word is loaded into the Input Data Register OR remains low; disablng further TTIRL signals. After the last word is read into the CPU IRL remains low and GENSRQL remains high.

The GENSRQ logic is also used during output transfers. GENSRQL is generated when the DI is a talker and IRLO is high. Recall that as long as IRLO is high there is room for another word.

The LBO Flip-Flop is straightforward. The flip-flop is clocked on the rising edge of THSKL. Its input is the Last Byte Out Signal generated by the End Of Data Detect Logic [52D-4]. When LBO is high the flip-flop is set and LBOFF is high. LBOFF remains high until reset by a Master Reset signal.

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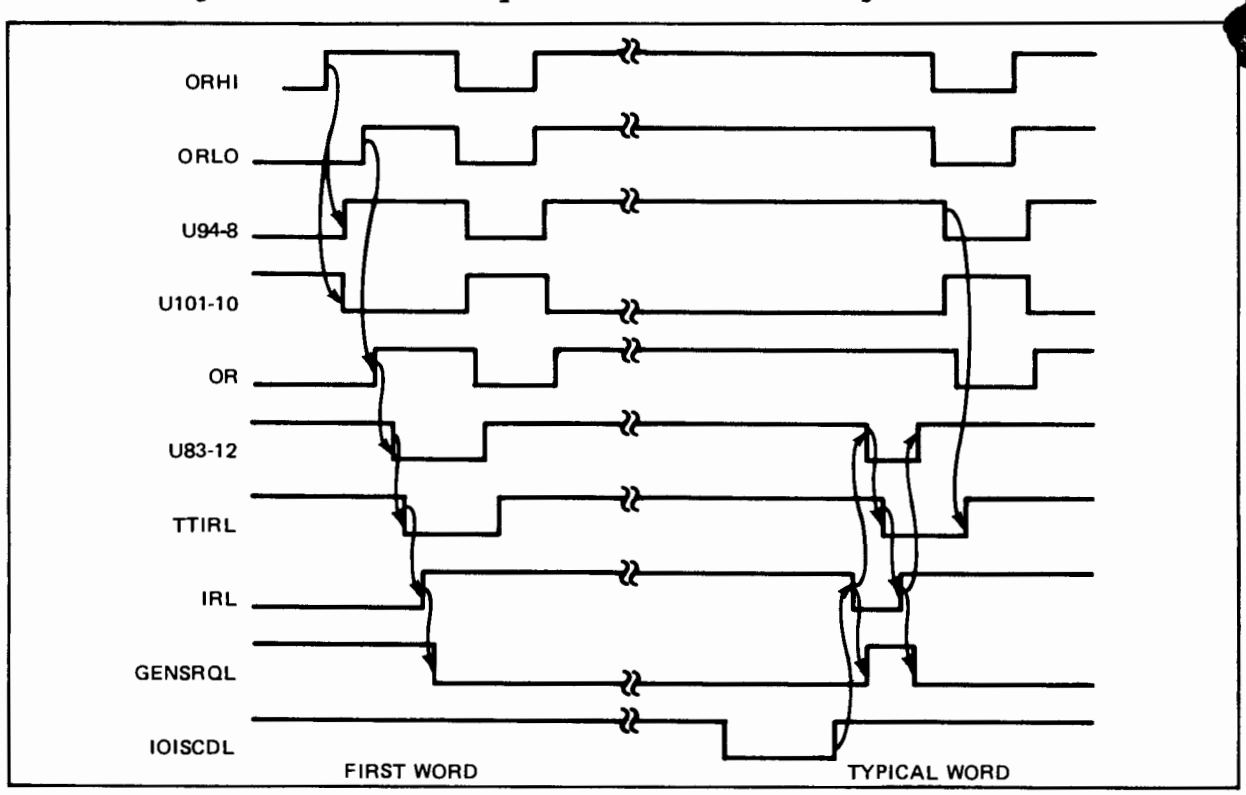

Figure 3-13. Last Byte Out Logic

3-26. INTERRUPT SOURCE, MASK LOGIC

Table 3-1 summarizes the function of the Interrupt Source, Mask Logic [53B-2]. The first column lists the signal which is to result in a "set flag" or an interrupt request. Column two lists the bits in the DI Control Register which must be set and other conditions which must be met so that the signal in column one can generate SETFLG. The third column is a brief discussion of the use of each interrupt. The SETFLG signal causes the DI Flag Flip-Flop to be set. Software can check for this condition or, if interrupts are enabled, the DI will assert IRQ and FLGL. For most cases an MR is required to disable the SETFLG signal.

Table 3-1. Interrupt Source, Mask Logic

SIGNAL	CONDITIONS	DESCRIPTION
IRL	IRLEN	Typically used for a software controlled input transfer. Interrupt request generated when data, command, or parallel poll response is in input data register.
IFCFF	IFCEN, SYSCTL	The IFC flipflop is set whenever an interface clear is issued to the bus. An IFC can only be generated by the system controller, thus if the IBI is SYSCTL then IFCFF is ignored.
RENIN	RENEN, SYSCTL	Used to detect a remote enable signal on the bus. REN can only be generated by the system controller, thus if the IBI is SYSCTL then RENIN is ignored.
EORFF	IRL	Typically used for a software controlled input transfer to detect the last byte. The EOR flipflop is set when the byte/word tagged with EOR or a LF is loaded into the input data register.
SRQIN	SRQEN, CIC	Used to detect a service request on the bus. The IBI must be controller in charge to acknowledge a SRQ. Note that the IBI can generate an SRQ only if it is not CIC.
LBOFF	LBOEN	Typically used in a software controlled output transfer to detect the end of transfer. The LBO flipflop is set when the last byte is output to the bus.

3-27. INPUT MULTIPLEXER

The DI's Input Multiplexer [52G-5] is made up of 16 Signetics 8T13 Dual Line Drivers. Each line driver has a data bit from the Input Data Register [53F-5] as one input and a status bit as the other. The Input Mux Enable Logic [52B-5] provides the select signals which enable these inputs to the CPU Input Bus.

3-28. INPUT MULTIPLEXER ENABLE LOGIC

The Timing for the Input Mux Enable Logic [52B-5] is shown in Figure 3-14. When the Control Flip-Flop is set IOI is used to generate the Data Select signal. The status word is selected when the Control Flip-Flop is cleared.

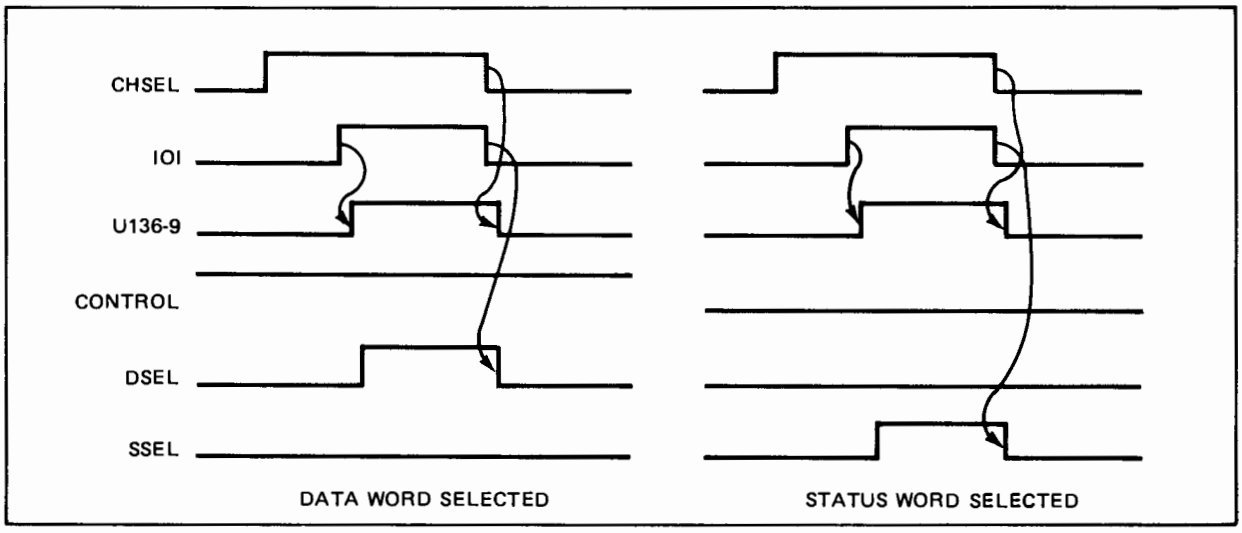

Figure 3-14. Input Multiplexer Enable Logic

3-29 CLEAR FLAG DETECT FLIP-FLOP

The Clear Flag Detect Logic [52C-4] is used to detect the last word of a software controlled output transfer in packed format. The flip-flop is reset at the beginning of each machine cycle. If a CLF is executed during that cycle the flip-flop is set (see Figure 3-15), if not, NCLFL remains low. If unpacked data format is used the flip-flop output remains high (U123-3).

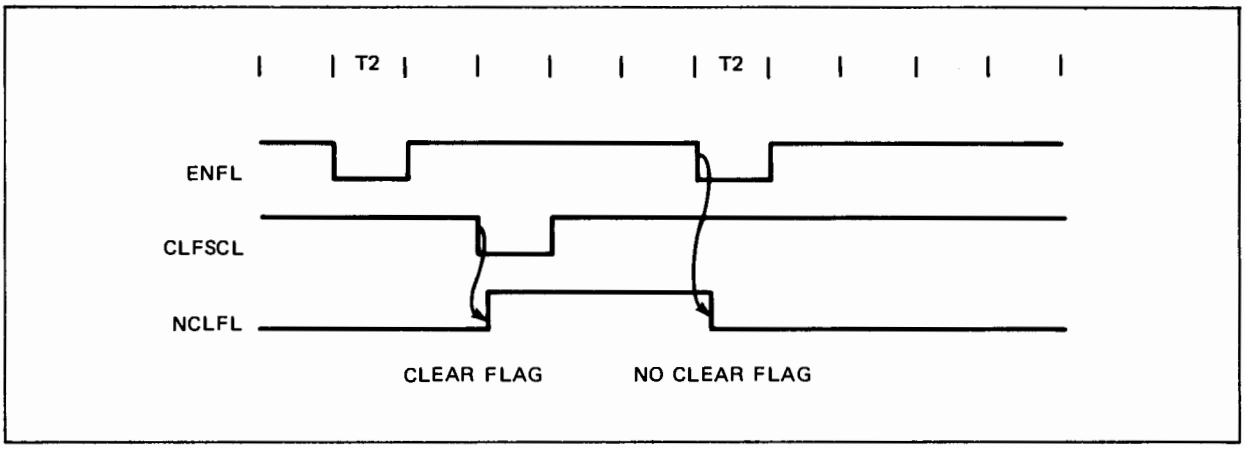

Figure 3-15. Clear Flag Detect Flip-Flop (Assume Pack=1)

3-30. END OF DATA TRANSFER FLIP-FLOP

The EDT Flip-Flop [52D-4] can be set three different ways, illustrated in Figure 3-16. In a software controlled transfer in unpacked format U124-6 goes low when bit 15 of the Output Data Register is a one. U124-3 goes high and the flip-flop is set on the rising edge of OBCLKL. In a software controlled transfer in packed format the last word is output without a CLF. NCLFL remains low and U124-3 is high. Again the flip-flop is set on the rising edge of OBCLKL. In a DMA transfer the flip-flop is set when the DCPC asserts EDT (U106-8)[52B-5].

The AND gate U135-3 guarantees that once set the EDT Flip-Flop will remain set until a Master Reset is generated. This prevents the flip-flop from being reset on the rising edge of OBCLKL during a DMA transfer.

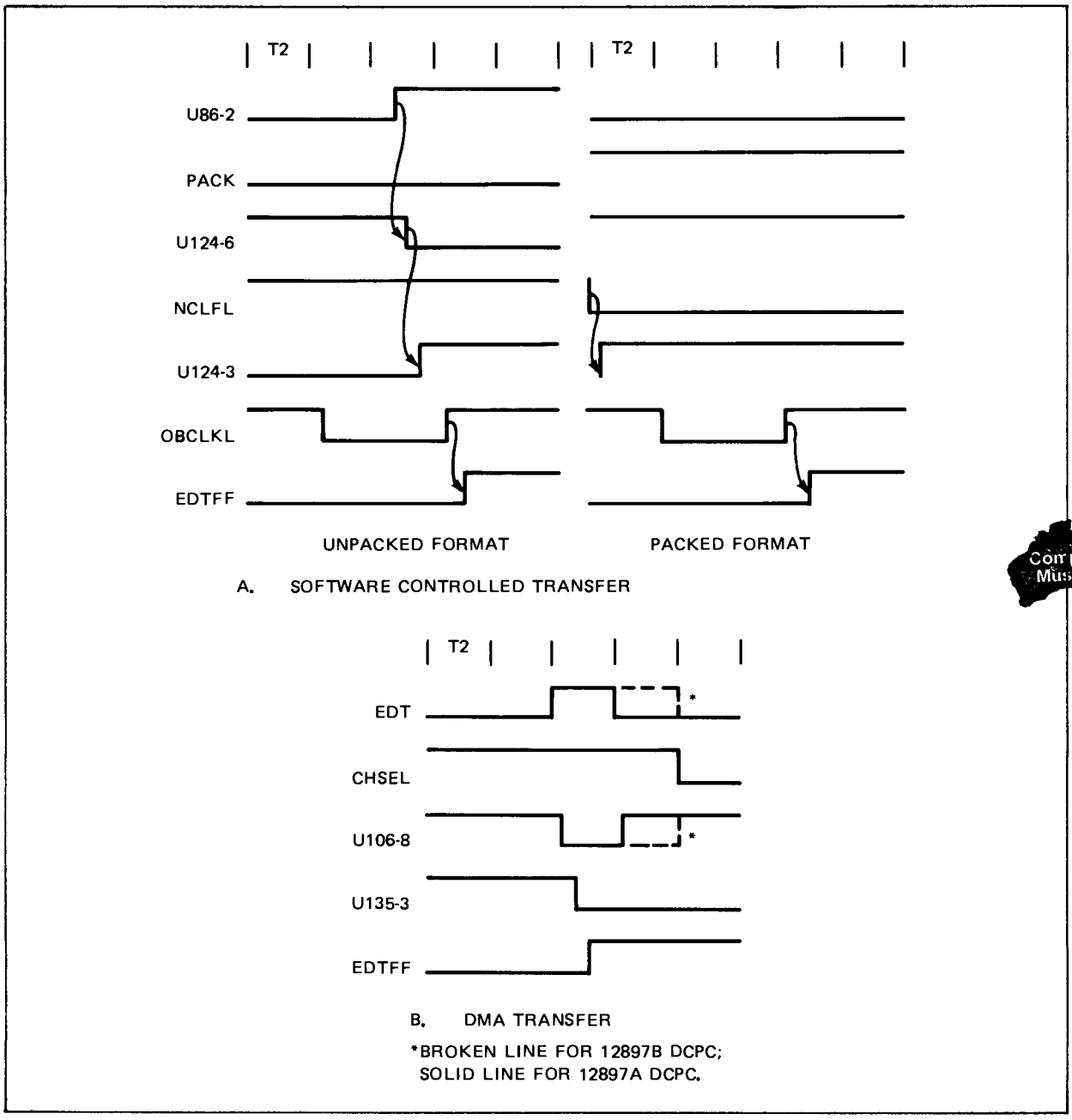

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Figure 3-16. End Data Transfer Flip-Flop

3-31. SERVICE REQUEST LOGIC

The SRQ Logic includes the SRQ Flip-Flop (U136-6)[52D-4], the AOI gate used to generate SRQ (U137-7)[52B-5], and U124-11 (Figure 3-17). The flip-flop is clocked at the beginning of each T2 time period. If GENSRQL is low the flip-flop output goes high. SRQ is then asserted if CONTROl is high (data mode) and U124-11 is high.

U124-11 is used to "reset" the SRQ Logic when the FIFOs are empty (ORLOL remains high) and the last word is being read by the CPU. SRQ is pulled low before T4, which is when the CPU would examine SRQ. Thus no further machine cycles are requested.

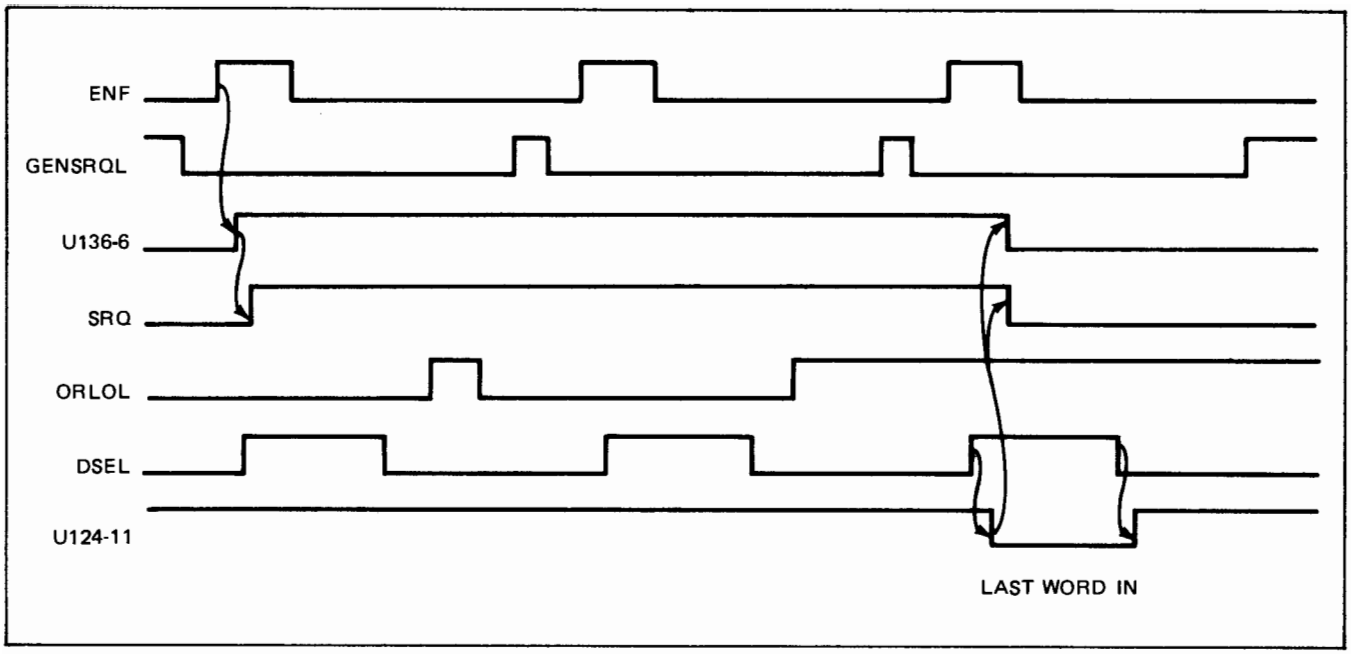

Figure 3-17. Service Request Logic (Input Transfer Assume Control=1)

3-32 FLAG BUFFER FLIP-FLOP

The Flag Buffer Flip-Flop [52B-2] is normally set. It can be reset by SETFLG if the Flag Flip-Flop is not already set, by POPIO, or by STF. The timing for these is shown in Figure 3-18.

The flip-flop is set by a CLF instruction or by IAK if the IRQ Flip-Flop is set. However if SETFLG is true (equals 1) when CLF is executed then the flip-flop will be reset after executing the CLF instruction. For most cases MR will disable SETFLG.

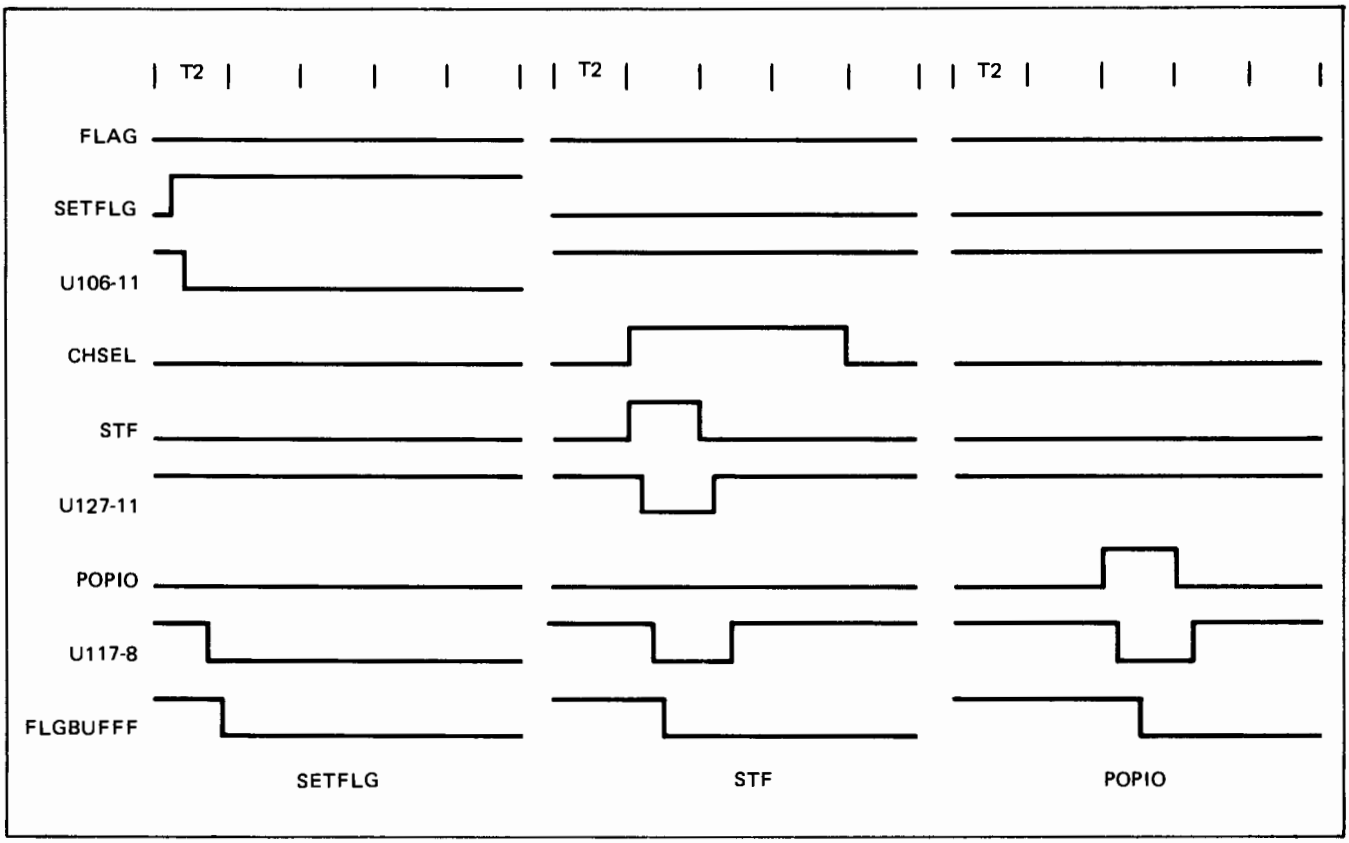

Figure 3-18. Flag Buffer Flip-Flop

3-33. FLAG LOGIC

The Flag Logic [52B-4] is made up of three logical blocks; the Flag Flip-Flop, the Priority Line Logic, and the Skip Flag Logic.

The Flag Flip-Flop is normally reset. It is set by ENF if the Flag Buffer Flip-Flop has been reset. The Flag Flip-Flop is reset by a CLF.

When the Flag Flip-Flop is set, CONTROL is high (data mode), and IEN is high (interrupts are enabled) then U117-6 goes high. If PRH is high then a high value at U117-6 causes PRL to go low (U107-7)[52B-3], preventing lower priority devices from generating interrupts (see Figure 3-19).

The Skip Flag Logic consists of an AOI gate (U107-9)[52B-4] with SFS, FLAG and CHSEL as one set of inputs and SFC, FLAGL and CHSEL as the other. SKF is generated accordingly (see Figure 3-20).

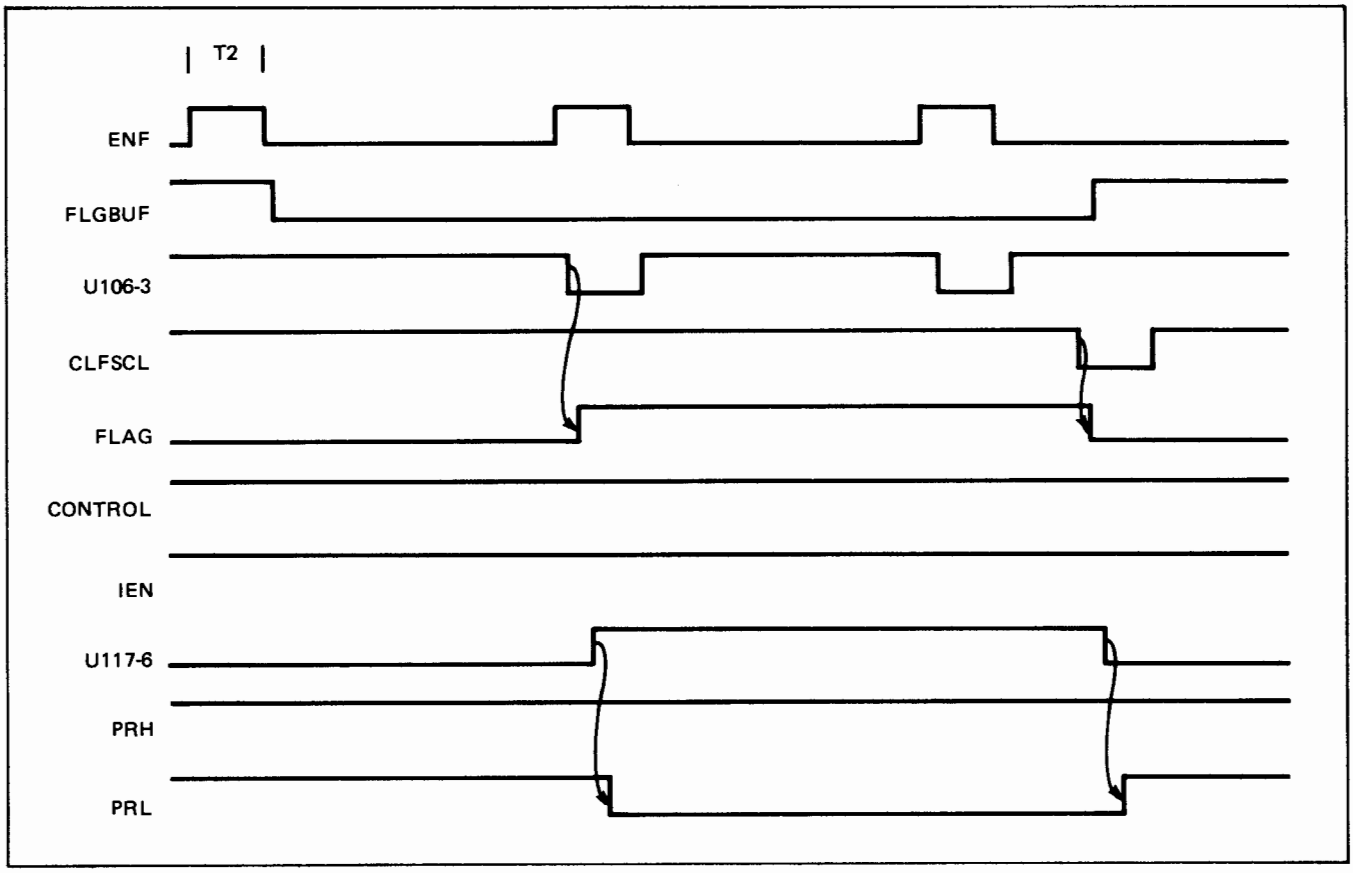

Figure 3-19. Flag Flip-Flop

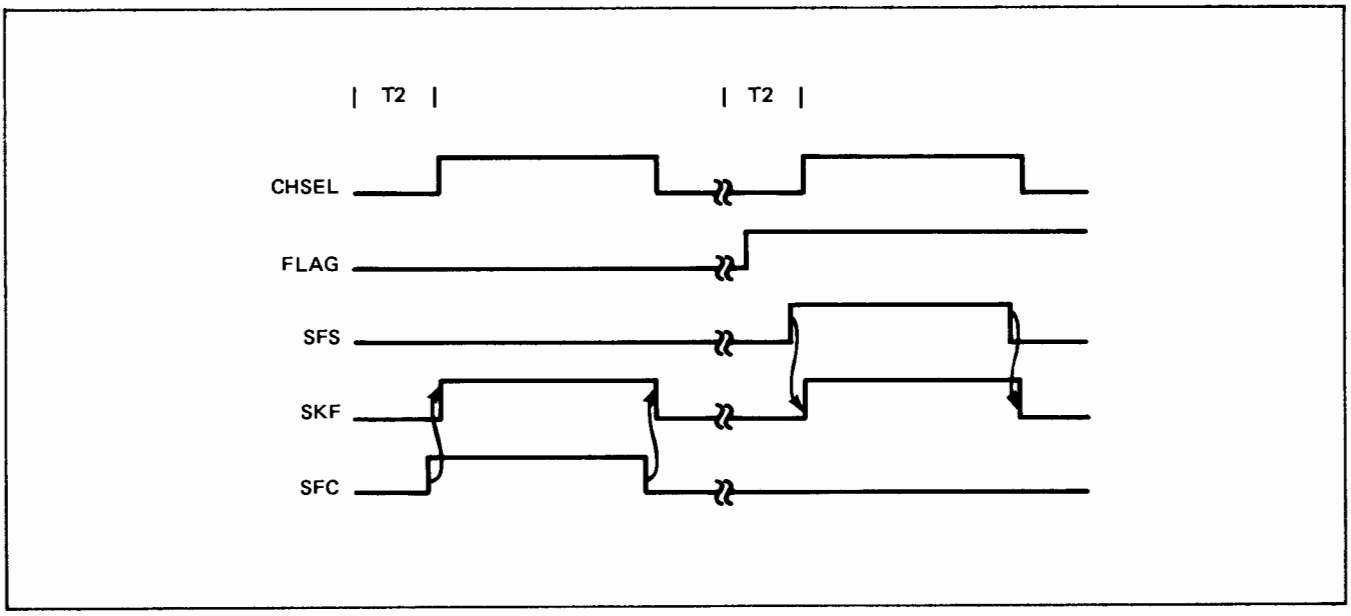

Figure 3-20. Skip Flag Logic

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3-34. INTERRUPT REQUEST LOGIC

The IRQFF [52B-3] is normally reset. Three conditions must be met to set the flip-flop. U117-6 must be high (FLAG=CONTROL= IEN=1), the Flag Buffer Flip-Flop must be reset and PRH [52A-3] must be high. If these conditions are met the IRQFF will be set by SIR. IRQFF goes high causing the CPU backplane signals IRQ (Interrupt Request) and FLGL (Flag Signal, Lower Select Code) to go high (U97).

The IRQFF is reset at the beginning of each macine cycle by ENF. Figure 3-21 shows the timing involved in generating an IRQ. During the first machine cycle shown the Flag Buffer Flip-Flop is reset. At the beginning of the next machine cycle the Flag Flip-Flop is set, U117-6 goes high, and PRL goes low. When SIR arrives at T5 the IRQFF is set and IRQ and FLGL are asserted. When the interrupt is acknowledged by IAK the Flag Buffer Flip-Flop is set. The IRQ Flip-Flop is reset at the beginning of the next machine cycle. The Flag and Control Flip-Flops must be reset by software.

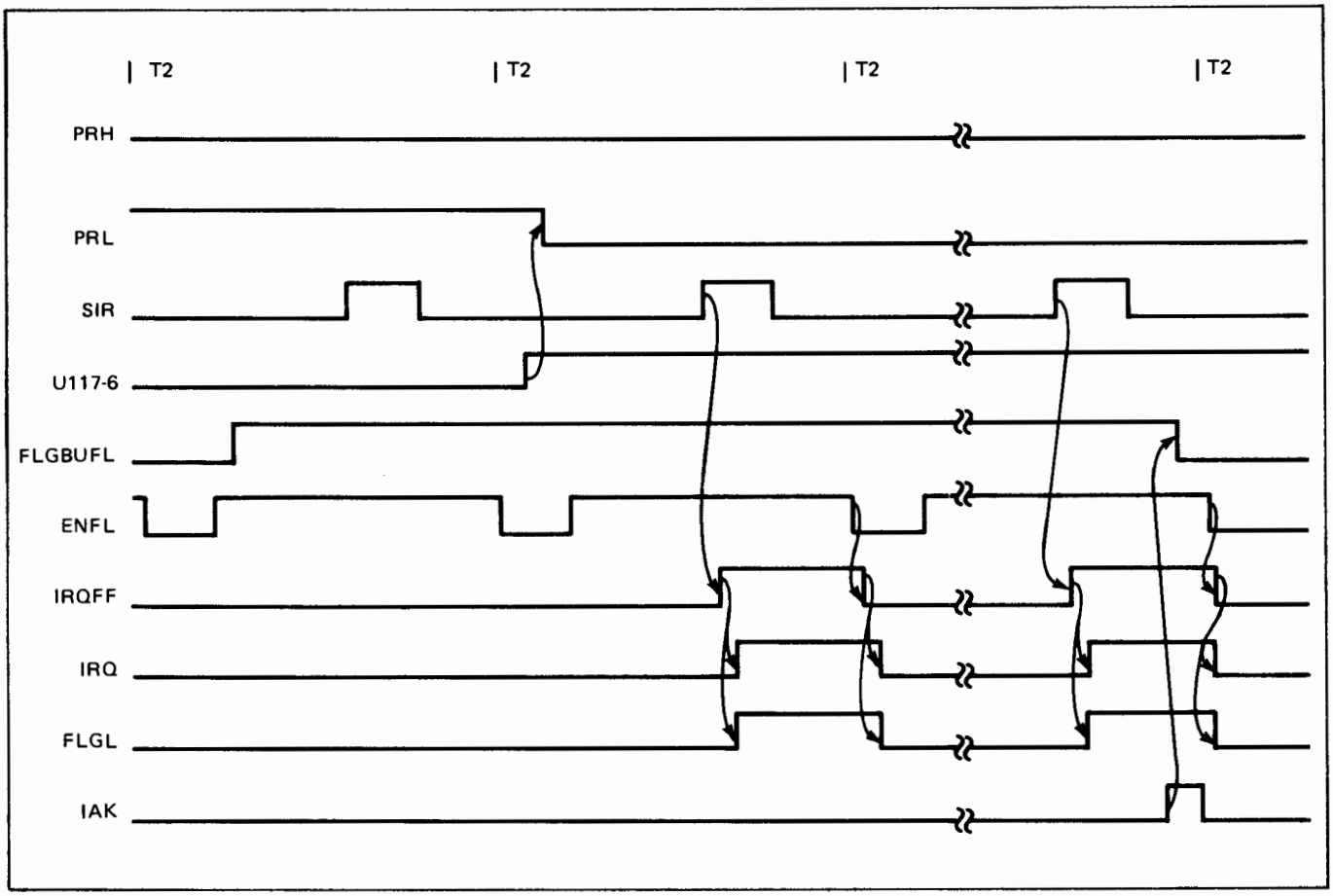


Figure 3-21. Interupt Request Logic

3-35. INTERFACE CLEAR 100 MICROSECOND TIMER

A Dual Retriggerable Monostable Multivibrator (74LS123,U91) is used for the IFC Timer [51A-1]. It is triggered when the IFCEN bit of the Control Word Register is set (U91-2), provided the DI is SYSCTL (U91-3). If SYSCTL is low the clear overrides the output keeping it low. The external resistor and capacitor are set to guarantee a minimum pulse width of 100 microsecnds. IFCOUT is tied directly to the IFCL bus line.

3-36. INTERFACE CLEAR FLIP-FLOP

The IFC flip-flop (U123-13) [51E-4] is set whenever an IFC is received by or generated by the DI (since the transceiver for IFCL always has its receiver enabled). The flip-flop is reset by Master Reset.

3-37. PARALLEL POLL CONDUCT LOGIC

The Parallel Poll Conduct Logic [51E-3] timing is shown on Figure 3-22. When PPE and CIC are set in the Control Register PPC is pulled high. The delay circuit provides the 2 microsec delay before the DI can look for a parallel poll response. After this delay, as soon as a response is detected by the Command Decode Logic and PPR is high, PPRLL goes low initiating the FIFO load sequence.

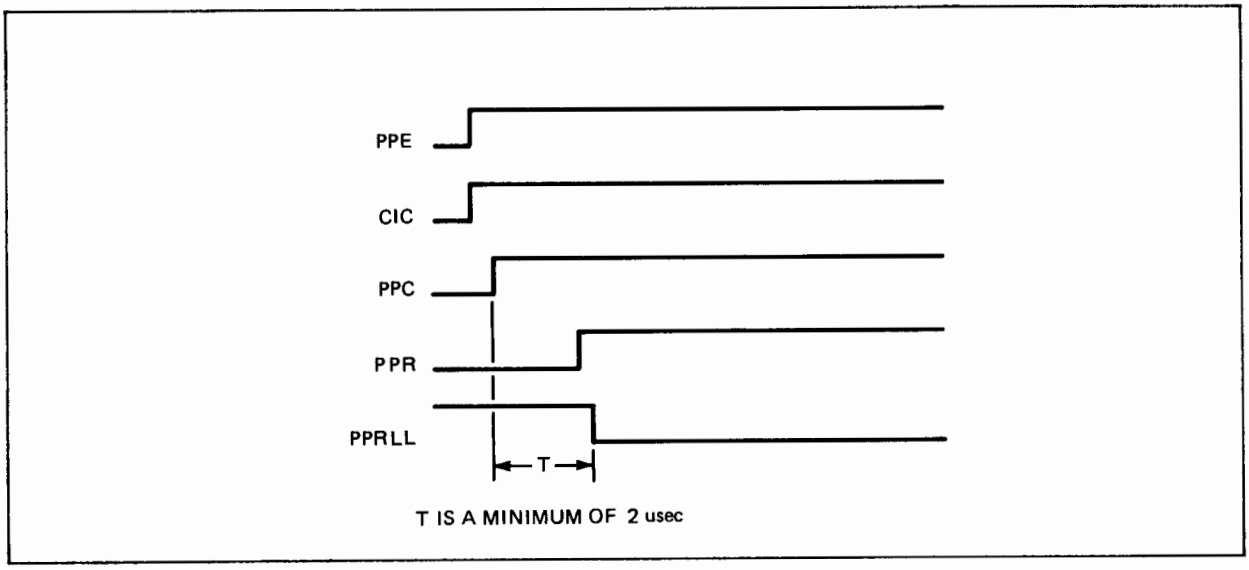


Figure 3-22. Parallel Poll Conduct Logic

3-38. BUS ADDRESS SWITCH

The Bus Address Switch [51F-4] is an 8 rocker switch DIP (U13). The first five switches set the DI's bus address with switch one as the least significant bit. The eighth switch sets the SYSCTL bit. An open siwtch corresponds to a one, a closed switch to a zero.

3-39. BUS ADDRESS COMPARATOR

A Signetics 9324, Five Bit Comparator [51G-5] compares the bus Address Switch setting with the five least significant bits of the bus Data lines. When the inputs are equal the comparator output, ADD, is high.

3-40. COMMAND DECODE LOGIC

The Command Decode Logic [51E-5] consists of a Harris 7621 PROM (U23), a 74LS259 Addressable Latch (U22), and a few miscellaneous gates and a flip-flop. The PROM detects parallel poll responses directly (U23-10) and detects line-feeds with the assistance of a nor gate (U42-1). Talk, untalk, listen, and unlisten commands are decoded when the ADD input (U23-5) indicates the command is addressed to the DI. The talk, etc., values are latched in U22.

U22-10 is a one when a listen command is received and is zero when an unlisten is received. The nor gate U32-6 asserts LISTEN when listen is asserted by the command decoder or the listen bit in the Control Word Register is set. U22-11 and U32-3 perform an analogous function for talk and untalk. In this case the Control Word Register talk bit value is latched in U72-4.

The latch is cleared by CRSL or Interface Clear. It is enabled during the receive handshake cycle when an external command (EXTCMD=1) is being loaded into the FIFOs.

3-41. SYSTEM CONTROLLER

Switch eight of the DIP rocker switch (U13)[51B-2] determines the System, Controller function.

When the switch is open the SYSCTL function is enabled (SYSCTL=1), allowing the DI to assert IFC and REN on the bus per the state of the associated bits (bits 14 and 13 respectively).

when the switch is closed (SYSCTL=0) the DI is not functioning as System Controller. In this mode the DI receives the IFC and/or REN from the bus, causing the DI's flag to set if either of the associated Control Word Register bits are set (bits 14 and 13 respectively).

MAINTENANCE	SECTION IV

4-1. INTRODUCTION

This section provides safety precautions, preventive maintenance instructions, trobleshooting, and diagnostic information.

4-2. SAFETY PRECAUTIONS

To avoid injury and to prevent damage to the equipment, service personnel should observe the following safety precautions:

* Observe all WARNING and CAUTION and other hazard labels affixed to the equipment being checked.

* Use extreme caution when working on equipment with the covers removed, since hazardous line voltage is present within the mainframe.

* Remove watches, rings, or other such jewelry before working on equipment.

* Do not attempt to install or remove PCA's or interconnecting cables without first removing power from all devices.

4-3. PREVENTIVE MAINTENANCE

Preventive maintenance should be performed at scheduled intervals to minimize performance degradation. Preventive maintenance consists of inspecting, cleaning, and verifying performance of the PCA. Inspect the interface cable and connectors for cracks, burns, or wear. Ensure that the PCA is properly seated.

4-4. TROUBLESHOOTING

Troubleshooting consists of performing the diagnostic test. The PCA is not field repairable, when a PCA is found to be defective it should be replaced with an exchange assembly and the defective PCA returned to Hewlett-Packard for repair. A parts location diagram, reference parts list, 59310-60002 pin connections and schematic diagrams are provided in this section as an aid in isolating malfunctions.

4-5. DIAGNOSTIC TEST

The HP 12821A Disc Interface Diagnostic, part no. 12821-16001 is included in the HP 24396A-F Diagnostic Library and in the HP 1000 Computer System Diagnostic Library (24998-14002). To execute the complete diagnostic two disc interface PCA's and two interface cables are required. Step-by-step instructions for running the diagnostic are contained in the HP 12821A Diagnostic Reference Manual, part no. 12821-90002.

4-6. REPLACEMENT PROCEDURE

If the PCA must be removed from the computer, refer to the removal instructions in the appropriate computer installation and service manmual.

Replacement of the PCA is accomplished by reversing the removal procedure. Be sure to configure the DIP switches as described in paragraph 2-4.

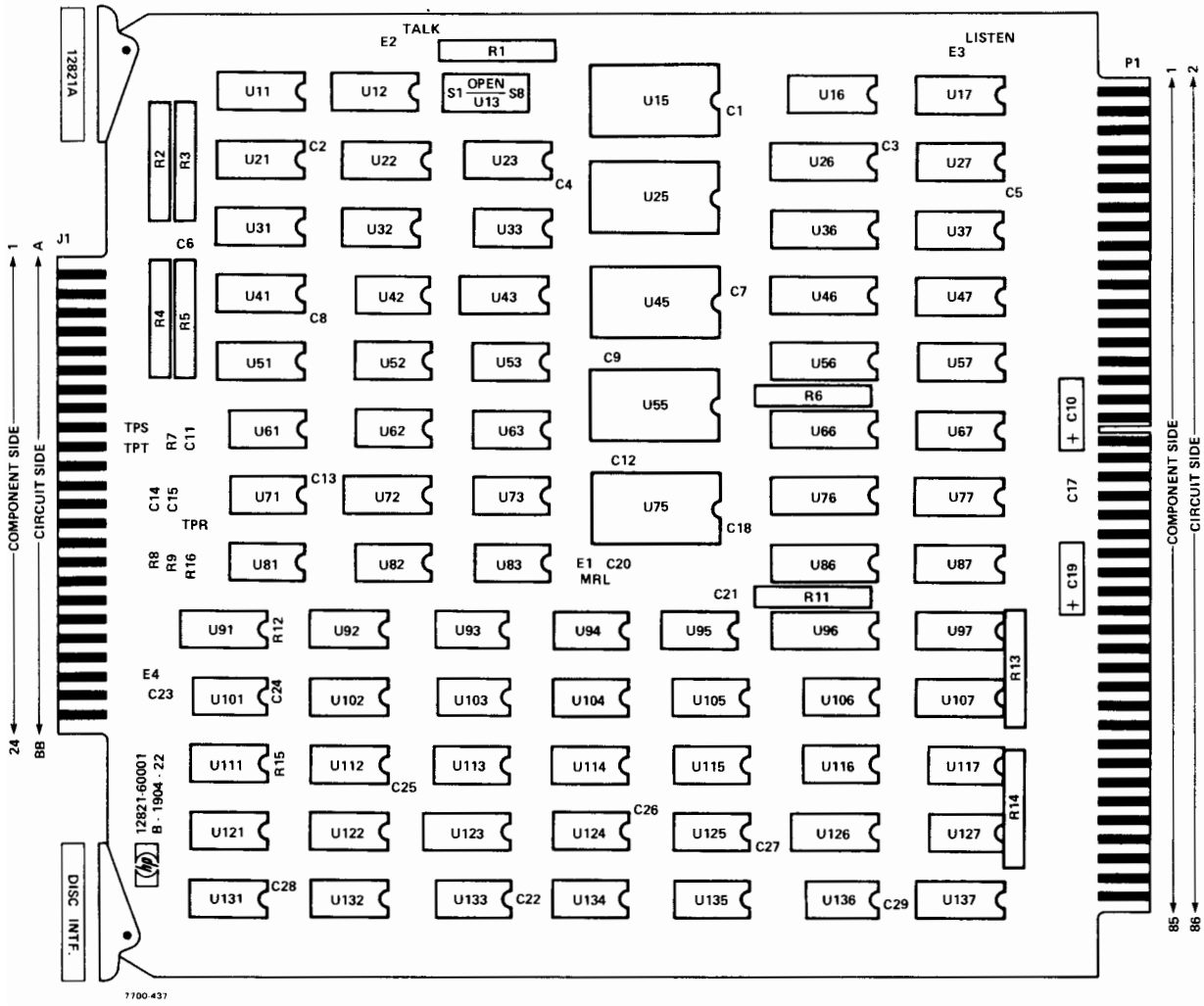


Figure 4-1. 12821-60001 Parts Location Diagram

Table 4-1. Reference Parts List (Continued)

REF DESIG	PART NO.	DESCRIPTION
	59310-60002	Disc Interface Cable Assy
	12821-60001	Disc Interface PCA
C15	0160-2207	Capacitor, 300pf 5%
C11,14	0160-3353	Capacitor, 470pf 5%
C1-9,12, 13,17,18, 20-23,25-29	0160-3379	Capacitor, 0.01mf 20%
C24	0160-4299	Capacitor, 2200pf 2%
C10,19	0180-0374	Capacitor, 10mf
R8,9	0698-3152	Resistor, 3.48kohms 1% 0.125W
R7	0698-3159	Resistor, 26.1kohms 1% 0.125W
R12	0698-3542	Resistor, 147kohms 1% 0.125W
R15,16	0757-0280	Resistor, 1.0kohms 1% 0.125W
R3,5	1810-0270	Resistor, Network 9X680ohms
R6,11,13, 14	1810-0276	Resistor, Network 9X1.5kohms
R1	1810-0280	Resistor, Network 9X10kohms
R2,4	1910-0298	Resistor, Network 9X240ohms
U15,25,45, 55,75	1816-0934	IC, 9403PC FIFO Buffer Memory (TTL)
U11	1820-0468	IC, SN7445N BCD to Decoder/Driver
U71	1820-0471	IC, SN74S06N Hex Inv. Bufr/Dvr OC
U95	1820-0683	IC, SN74S04N Hex Inv.
U134	1820-0693	IC, SN74S74N Dual D-Type FF
U12	1820-0706	IC, 9324PC 5-Bit Comparator
U17,27,37, 47,57,67, 77,87,97, 107,137	1820-1080	IC, 8T13B Dual Line Driver
U111,114, 121,131,136	1820-1112	IC, SN74LS74N Dual D-Type FF
U42,62,101	1820-1144	IC, SN74LS02N Quad 2-Input Pos. NOR
U61,63, 106,112,124		
127,132	1820-1197	IC, SN74LS00N Quad 2-Input Pos. NAND
U73,82, 116,125	1820-1199	IC, SN74LS04N Dual D-Type FF
U53,102, 104,122	1820-1201	IC, SN74LS08N Quad 2-Input Pos. AND
U83,92, 105,115	1820-1202	IC, SN74LS10N Triple 3-Input Pos. NAND
U117	1820-1203	IC, SN74LS11N Triple 3-Input Pos. AND
U32,52,94	1820-1208	IC, SN74LS32N Quad 2-Input OR

Table 4-1. Reference Parts List (Continued)

REF DESIG	PART NO.	DESCRIPTION
U113,133	1820-1210	IC, SN74LS51N Dual AND-OR-INVERT
U93,103	1820-1285	IC, SN74LS54N 4-Wide AND-OR-INVERT
U135	1820-1367	IC, SN74S08N Quad 2-Input Pos. AND
U81	1820-1416	IC, SN74S14N Hex Schmitt-Trig-Inv.
U91	1820-1423	IC, SN74LS123N Dual Retriggerable Monostable MV
U133	1820-1425	IC, SN74LS132N Quad 2-Input Pos.NAND Schmitt Triggers
U72,123,126	1820-1440	IC, SN74LS279N Quad "not S-not R" Latches
U16,43	1820-1470	IC, SN74LS157N Quad 2 to 1 MUX
U66,86	1820-1676	IC, SN74S373N Octal D-Type Latch
U22	1820 1729	IC, SN74LS259N 8-Bit Addressable Latch
U26,44,56,96	1820-1730	IC, SN74LS273N Octal D-Type FF
U36,76	1820-1794	IC, 81LS95 Non-Inverting Buffer
U51	1820-1875	IC, DS8838N Quad O.C. Bus Transceiver
U21,31,41	1820-2161	IC, DS8835N Quad Tri-state Bus Transceiver
U23	12821-80002	IC, 4 X 512 ROM
U13S1-S8	3101-1983	Switch, DIP, 8-Rocker

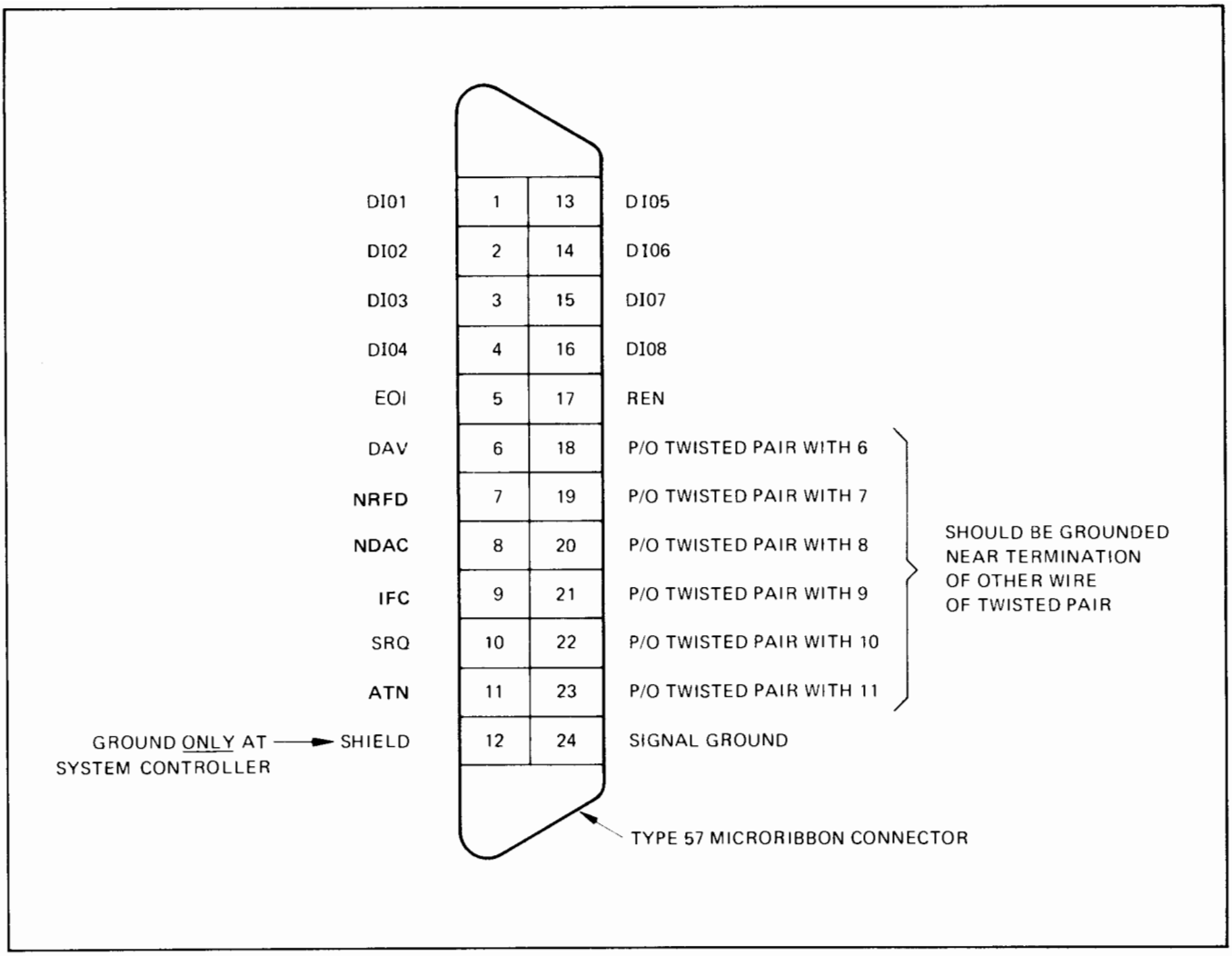
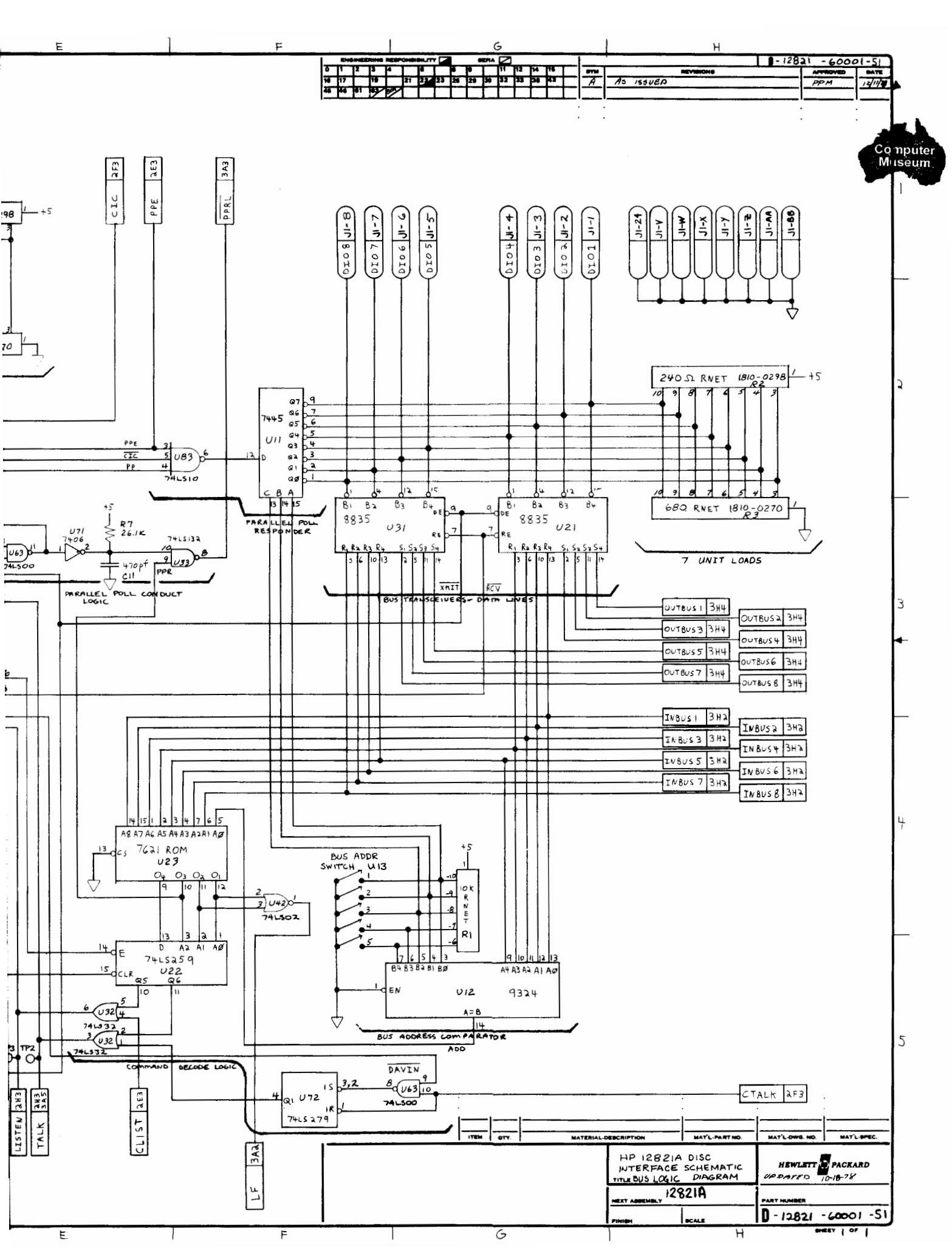
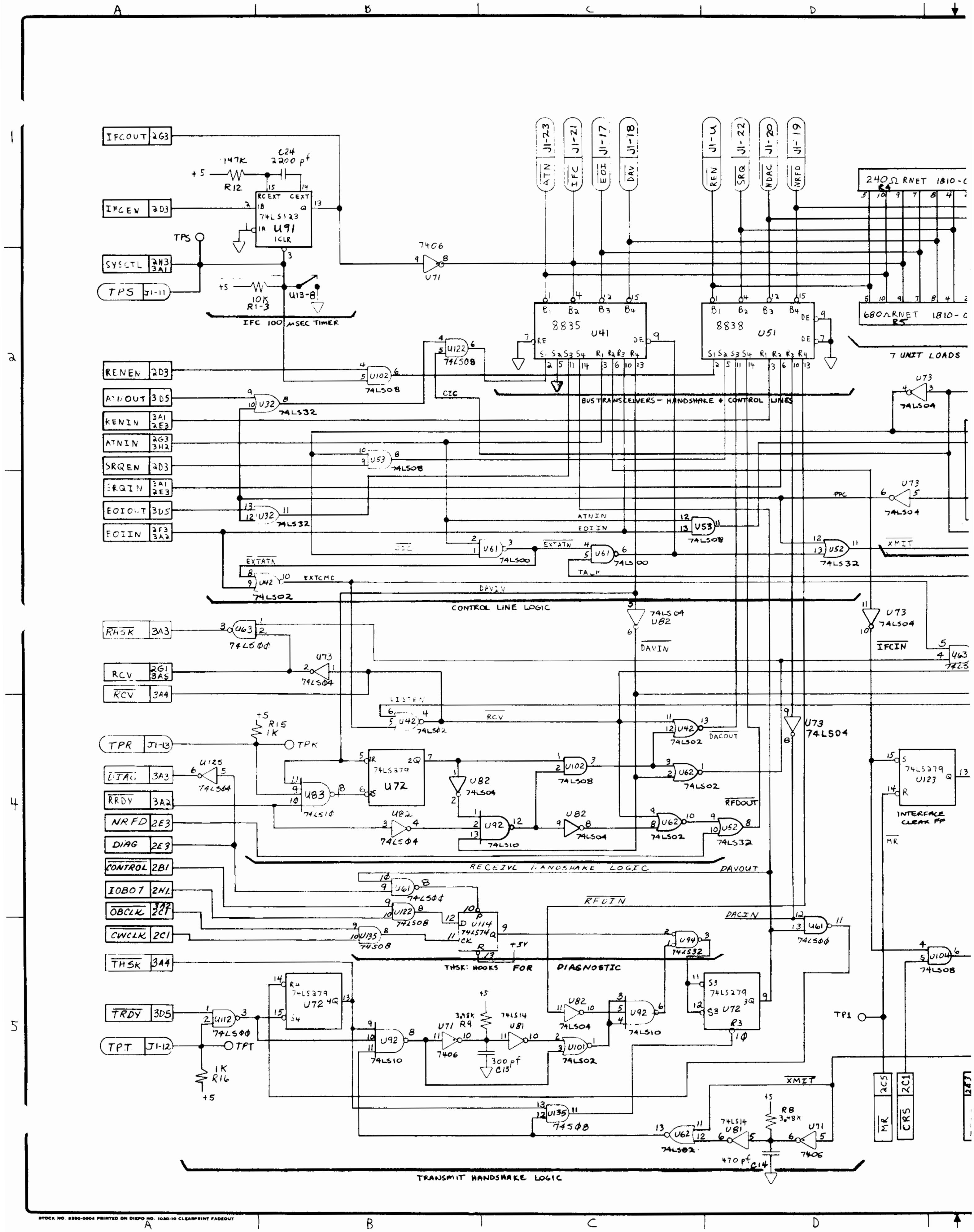


Figure 4-2. Pin Connections of the Bus Cable 59310-60002


D-12821-60001-51
REVISIONS
A5 ISSUED
APPROVED PPM
DATE 12/11/78
Computer Museum
CIC 2F3
PPE 2E3
PPRL 3A3
DIO 8 J1-8
DIO 7 J1-7
DIO 6 J1-6
DIO 5 J1-5
DIO 4 J1-4
DIO 3 J1-3
DIO 2 J1-2
DIO 1 J1-1
J1-24
J1-V
J1-W
J1-X
J1-Y
J1-Z
J1-AA
J1-BB
240Ω RNET 1810-0298 R2
680 RNET 1810-0270 R3
7 UNIT LOADS
7445 U11
PARALLEL POLL RESPONDER
8835 U31
8835 U21
BUS TRANSCEIVERS - DATA LINES
XMIT
RCV
U83 74LS10
U71 7406
R7 26.1K
470pf C11
PARALLEL POLL CONDUCT LOGIC
74LS132 U33
PPR
OUTBUS 1 3H4
OUTBUS 2 3H4
OUTBUS 3 3H4
OUTBUS 4 3H4
OUTBUS 5 3H4
OUTBUS 6 3H4
OUTBUS 7 3H4
OUTBUS 8 3H4
INBUS 1 3H2
INBUS 2 3H2
INBUS 3 3H2
INBUS 4 3H2
INBUS 5 3H2
INBUS 6 3H2
INBUS 7 3H2
INBUS 8 3H2
7621 ROM U23
BUS ADDR SWITCH U13
10K RNET R1
U42 74LS02
74LS259 U22
9324 U12
A=B
BUS ADDRESS COMPARATOR
ADD
U32 74LS32
COMMAND DECODE LOGIC
DAVIN
U72 74LS279
U63 74LS00
CTALK 2F3
LISTEN 2H3
TALK 2H3 3A5
CLIST 2E3
LF 3A2
TP2
ITEM QTY. MATERIAL-DESCRIPTION MAT'L-PART NO. MAT'L-DWG. NO. MAT'L-SPEC.
HP 12821A DISC INTERFACE SCHEMATIC
TITLE BUS LOGIC DIAGRAM
HEWLETT PACKARD
UPDATED 10-18-78
NEXT ASSEMBLY 12821A
PART NUMBER D-12821-60001-51
FINISH SCALE
SHEET 1 OF 1



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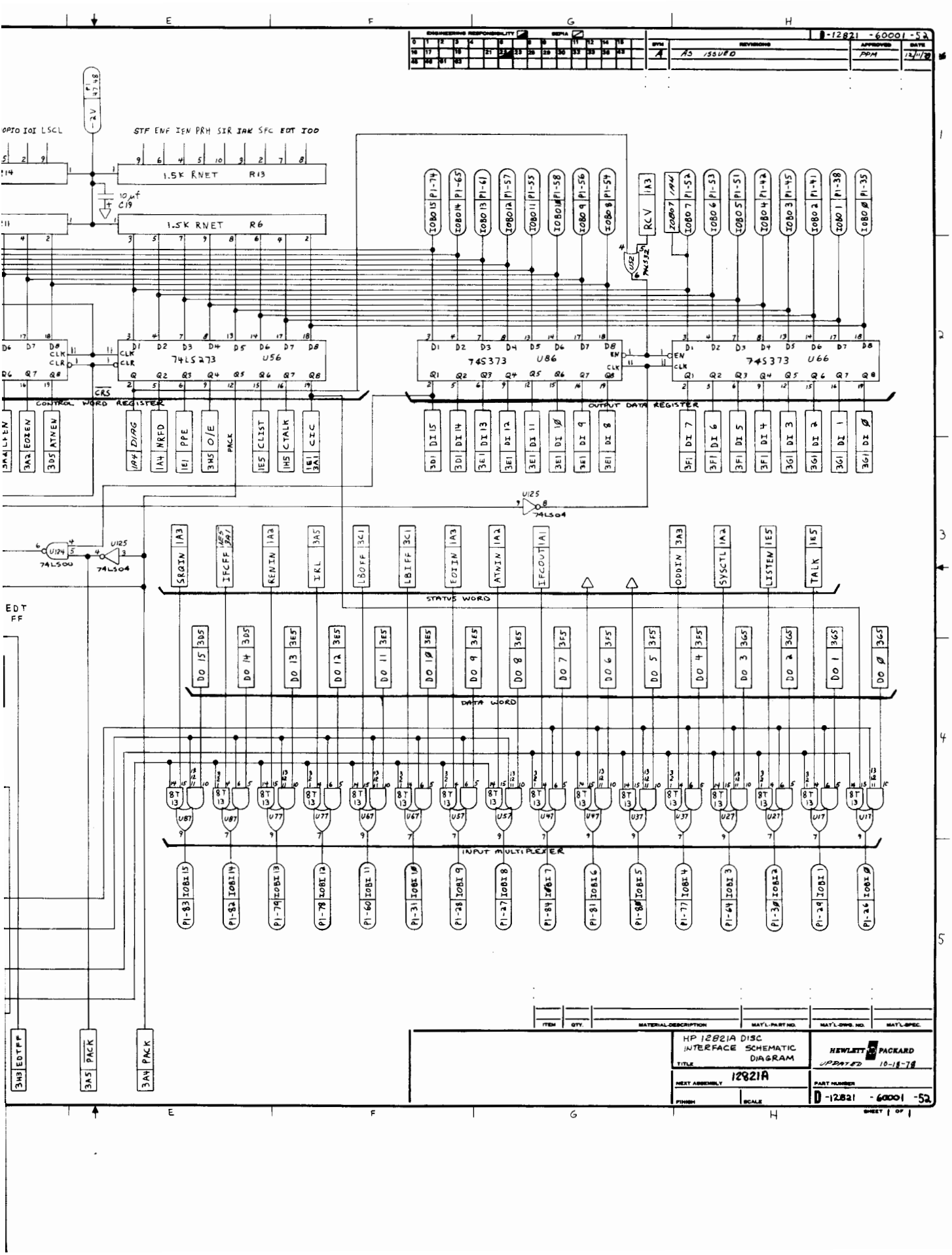
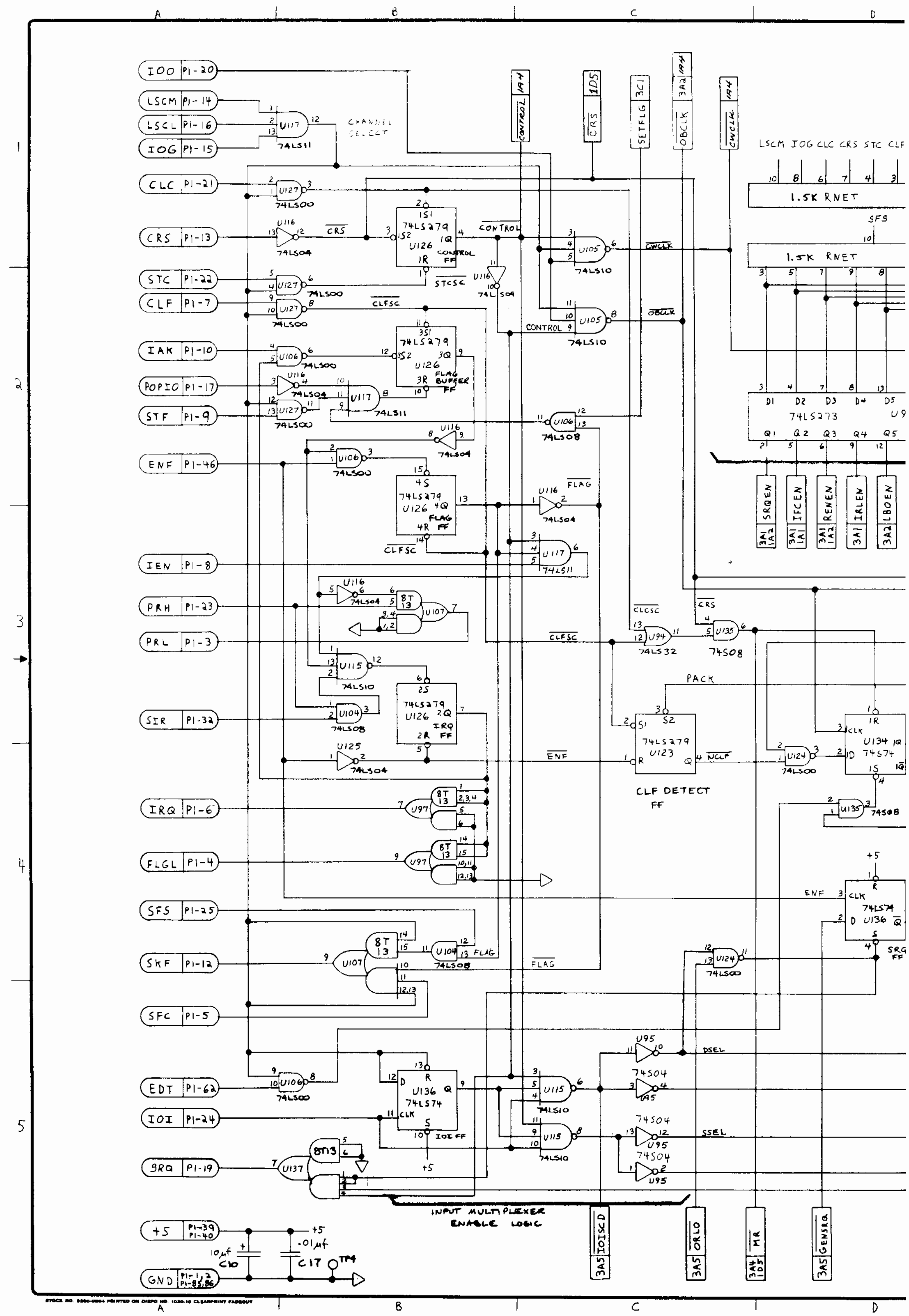
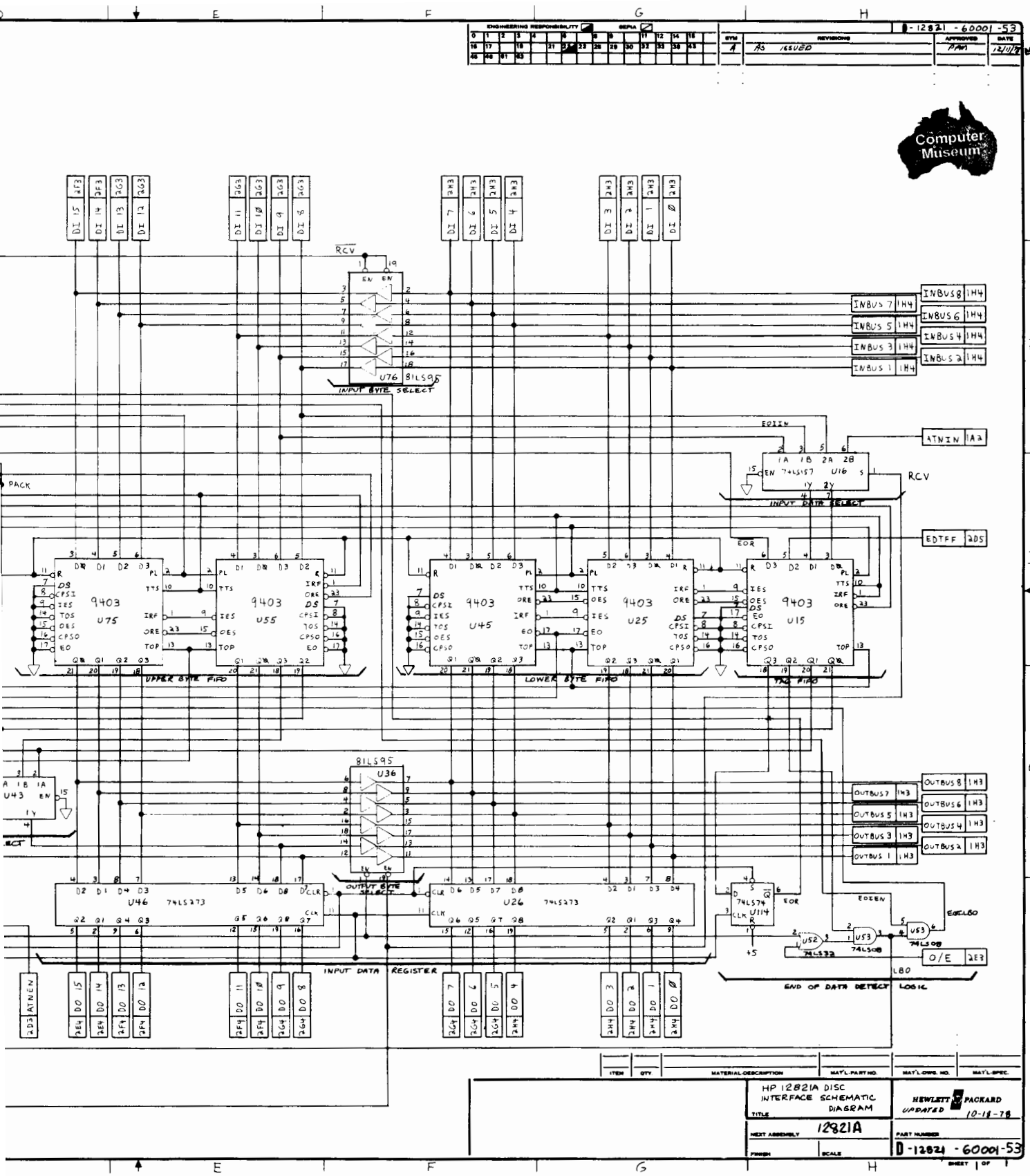
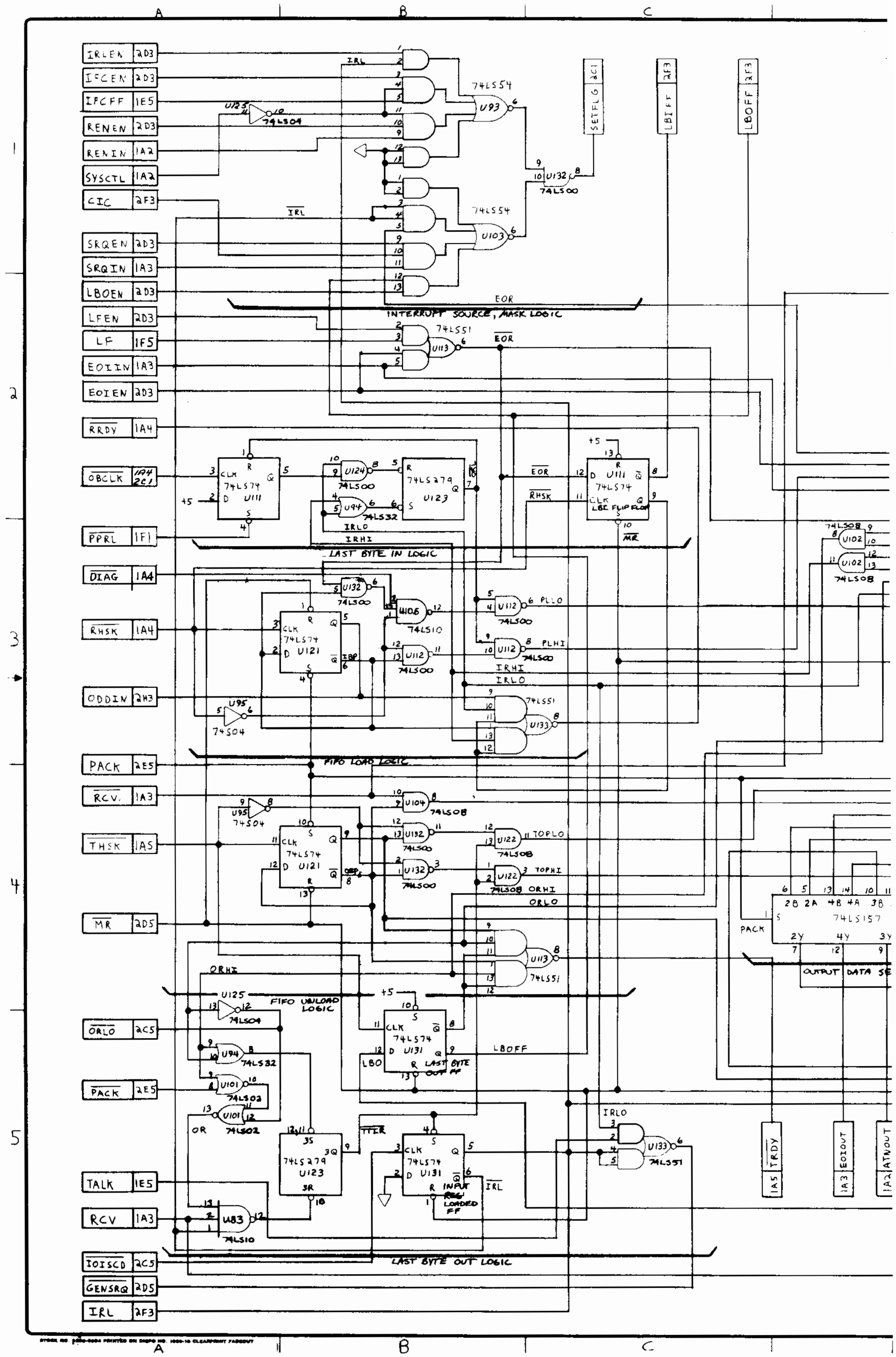

D-12821 -60001 -52
REVISIONS
A AS ISSUED
APPROVED PPM
DATE 13/11/78
1.5K RNET R13
1.5K RNET R6
10 µf C19
-2V
74LS273 U56
74S373 U86
74S373 U66
CONTROL WORD REGISTER
OUTPUT DATA REGISTER
74LS00
74LS04
STATUS WORD
DATA WORD
INPUT MULTIPLEXER
SRQIN
IFCFF
RENIN
IRL
LBOFF
LBIFF
EOIN
ATNIN
IFCOUT
ODDIN
SYSCTL
LISTEN
TALK
DIAG
NRFD
PPE
O/E
CLIST
CTALK
CIC
DI 15
DI 14
DI 13
DI 12
DI 11
DI 10
DI 9
DI 8
DI 7
DI 6
DI 5
DI 4
DI 3
DI 2
DI 1
DI 0
DO 15
DO 14
DO 13
DO 12
DO 11
DO 10
DO 9
DO 8
DO 7
DO 6
DO 5
DO 4
DO 3
DO 2
DO 1
DO 0
RCV
EDTPF
PACK
HP 12821A DISC INTERFACE SCHEMATIC DIAGRAM
HEWLETT PACKARD
UPDATED 10-18-78
12821A
D-12821 -60001 -52
SHEET 1 OF 1



IOO P1-20
LSCM P1-14
LSCL P1-16
IOG P1-15
CLC P1-21
CRS P1-13
STC P1-22
CLF P1-7
IAK P1-10
POPIO P1-17
STF P1-9
ENF P1-46
IEN P1-8
PRH P1-23
PRL P1-3
SIR P1-32
IRQ P1-6
FLGL P1-4
SFS P1-25
SKF P1-12
SFC P1-5
EDT P1-62
IOI P1-24
SRQ P1-19
+5 P1-39 P1-40
GND P1-1,2 P1-85,86
CHANNEL SELECT
74LS279 U126 CONTROL FF
FLAG BUFFER FF
FLAG FF
IRQ FF
74LS279 U123
CLF DETECT FF
PACK
1.5K RNET
SFS
LSCM IOG CLC CRS STC CLF
74LS273
U134 74S74
74LS74 D U136
SRG FF
U136 74LS74 IOI FF
INPUT MULTIPLEXER ENABLE LOGIC
DSEL
SSEL
CONTROL
CRS
STCSC
CLFSC
CWCLK
OBCLK
FLAG
ENF
NCLF
CLCSC
SETFLG 3C1
CRS 1D5
CONTROL 1A4
OBCLK 3A2 1A4
CWCLK 1A4
SRQEN 3A1 1A2
IFCEN 3A1 1A1
RENEN 3A1 1A2
IRLEN 3A1
LBOEN 3A2
IOISCD 3A5
ORLO 3A5
MR 3A4 1D5
GENSRQ 3A5
10µf C10
.01µf C17
TP4


D-12821-60001-53
REVISIONS
AS ISSUED
INBUS 8 1H4
INBUS 7 1H4
INBUS 6 1H4
INBUS 5 1H4
INBUS 4 1H4
INBUS 3 1H4
INBUS 2 1H4
INBUS 1 1H4
DI 15 2F3
DI 14 2F3
DI 13 2G3
DI 12 2G3
DI 11 2G3
DI 10 2G3
DI 9 2G3
DI 8 2G3
DI 7 2H3
DI 6 2H3
DI 5 2H3
DI 4 2H3
DI 3 2H3
DI 2 2H3
DI 1 2H3
DI 0 2H3
RCV
U76 81LS95
INPUT BYTE SELECT
EOIIN
ATNIN 1A2
1A 1B 2A 2B
U16 74LS157
INPUT DATA SELECT
EDTFF 2D5
EOR
9403
U75
U55
U45
U25
U15
UPPER BYTE FIFO
LOWER BYTE FIFO
TAG FIFO
U36 81LS95
OUTPUT BYTE SELECT
OUTBUS 8 1H3
OUTBUS 7 1H3
OUTBUS 6 1H3
OUTBUS 5 1H3
OUTBUS 4 1H3
OUTBUS 3 1H3
OUTBUS 2 1H3
OUTBUS 1 1H3
U46 74LS273
U26 74LS273
U114 74LS74
EOIEN
EOCLBO
U52 74LS32
U53 74LS08
O/E 2E3
LBO
INPUT DATA REGISTER
END OF DATA DETECT LOGIC
DO 15 2E4
DO 14 2E4
DO 13 2F4
DO 12 2F4
DO 11 2F4
DO 10 2F4
DO 9 2G4
DO 8 2G4
DO 7 2G4
DO 6 2G4
DO 5 2G4
DO 4 2H4
DO 3 2H4
DO 2 2H4
DO 1 2H4
DO 0 2H4
2D3 ATNEN
HP 12821A DISC INTERFACE SCHEMATIC DIAGRAM
HEWLETT PACKARD
UPDATED 10-18-78
12821A
D-12821-60001-53
SHEET 1 OF 1


IRLEN 2D3
IFCEN 2D3
IFCFF 1E5
RENEN 2D3
RENIN 1A2
SYSCTL 1A2
CIC 2F3
SRQEN 2D3
SRQIN 1A3
LBOEN 2D3
LFEN 2D3
LF 1F5
EOIIN 1A3
EOIEN 2D3
RRDY 1A4
OBCLK 1A4 2C1
PPRL 1F1
DIAG 1A4
RHSK 1A4
ODDIN 2H3
PACK 2E5
RCV. 1A3
THSK 1A5
MR 2D5
ORLO 2C5
PACK 2E5
TALK 1E5
RCV 1A3
IOISCD 2C5
GENSRQ 2D5
IRL 2F3
SETFLG 2C1
LBIFF 2F3
LBOFF 2F3
74LS54
U93
U103
U132
74LS00
74LS04
INTERRUPT SOURCE, MASK LOGIC
EOR
74LS51
U113
74LS74
U111
74LS279
U123
LBI FLIP FLOP
LAST BYTE IN LOGIC
IRLO
IRHI
U121
74LS10
PLLO
PLHI
U133
74S04
FIFO LOAD LOGIC
74LS08
TOPLO
TOPHI
ORHI
ORLO
FIFO UNLOAD LOGIC
U131
LAST BYTE OUT FF
LBOFF
74LS32
74LS02
INPUT LOADED FF
LAST BYTE OUT LOGIC
74LS157
OUTPUT DATA SE
1A5 TRDY
1A3 EOIOUT
1A2 ATNOUT
A
B
C
1
2
3
4
5