HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

12607

DIRECT MEMORY ACCESS

(2114B COMPUTER ACCESSORY KIT)

Note

This manual should be retained with the Installation and Maintenance Manual (part no. 02114-90399) for the HP 2114B Computer.

12607-90002

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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DIRECT MEMORY ACCESS COMPUTER ACCESSORY KIT (FOR THE 2114B COMPUTER)

model 12607A

UPDATING SUPPLEMENT 26 JAN 1970

MANUAL IDENTIFICATION

Manual Serial Prefixed: N/A

Manual Printed: Nov. 1969

Manual Part Number: 12607-90002

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

INSTRUMENT CHANGES

Prefix-Serial	Changes

ASSEMBLY CHANGES

Ref Des	Description	HP Part No.	Rev	Changes

Changes 1 through 10 dated 26 January, 1970.

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CHANGE	DESCRIPTION
1	Manual title page. Change: 12607 To: 12607A
2	Page 4-3. The equation for $\overline{SWCR}$ should read: $\overline{SWCR} = CRFF + \overline{T7}$
3	Page 4-3. The reset equation for the UIA FF should read: Reset = $\overline{PH5} \cdot ENF$
4	Page 4-5. The direct set and reset equations for the XMR1 FF should read: Direct Set = IOB1 · LMAR Direct Reset = $\overline{IOB1} \cdot$ LMAR
5	Page 4-9/4-10, figure 4-1. Replace the DMA schematic diagram with the attached schematic diagram.
6	Page MS-4, paragraph MS-20. Change lines 4 and 5 of the paragraph to read as follows: test points: TP1, TP2, TP3, and GND. To run the rate test, TP1 should be connected to TP2, and TP3 should be connected to GND.
7	Page MS-4, paragraph MS-25. Change step "b" to read as follows: b. Remove the DMA board (slot A16) and short TP1 to TP2, and TP3 to GND.
8	Page 4-8, table 4-3. Add the following: MC76; 1820-0111; INTEGRATED CIRCUIT:TTL; 07263; U6B930159X. MC77; 1820-0132; INTEGRATED CIRCUIT:TTL; 07263; U6A901659X.
9	Page 5-2, table 5-1. Add the following: 1820-0111; INTEGRATED CIRCUIT:TTL; 07263; U6B930159X; 1.
10	Page 5-2, table 5-1. Change the TQ column for part no. 1820-0132 from 2 to 3.

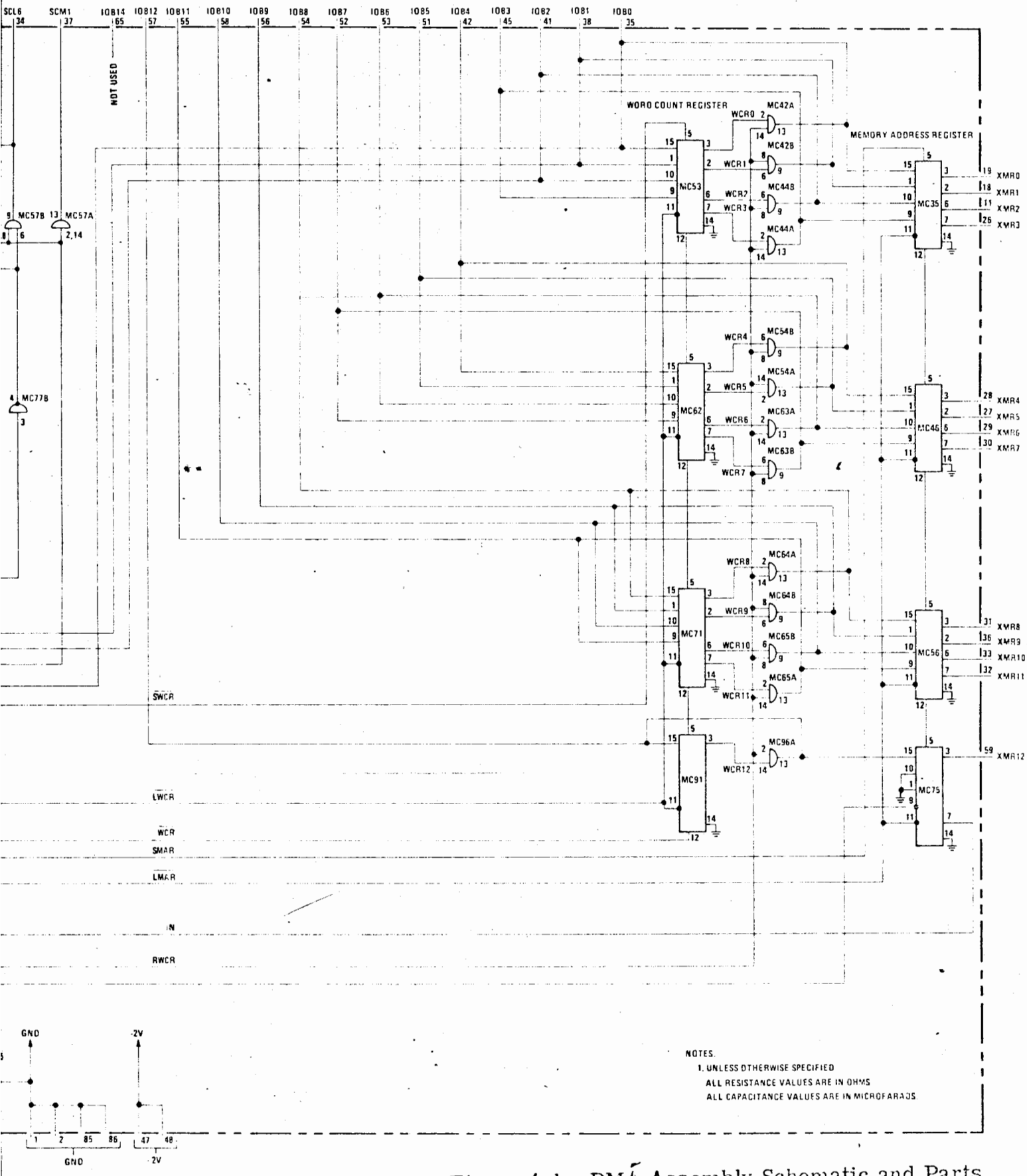
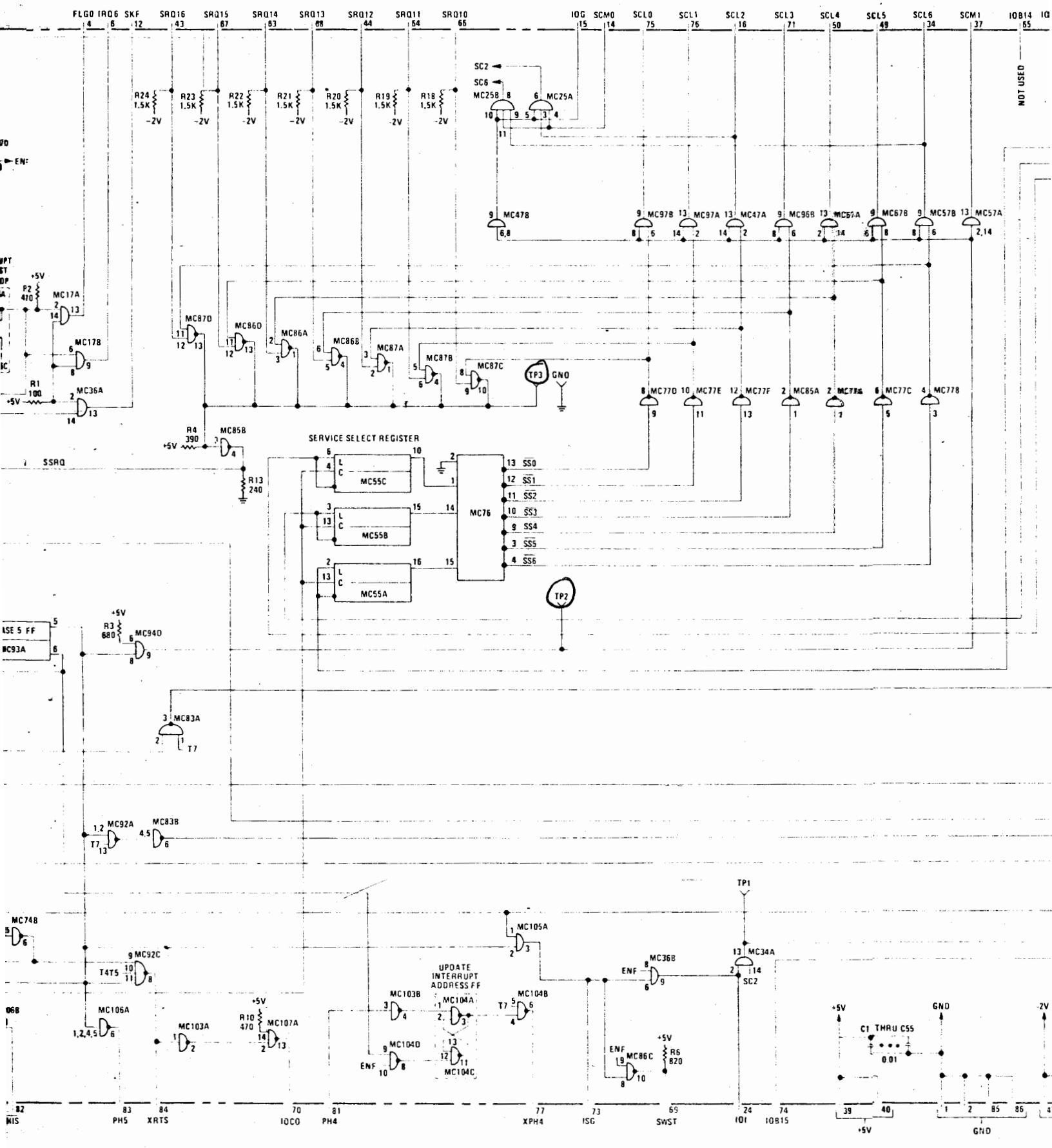
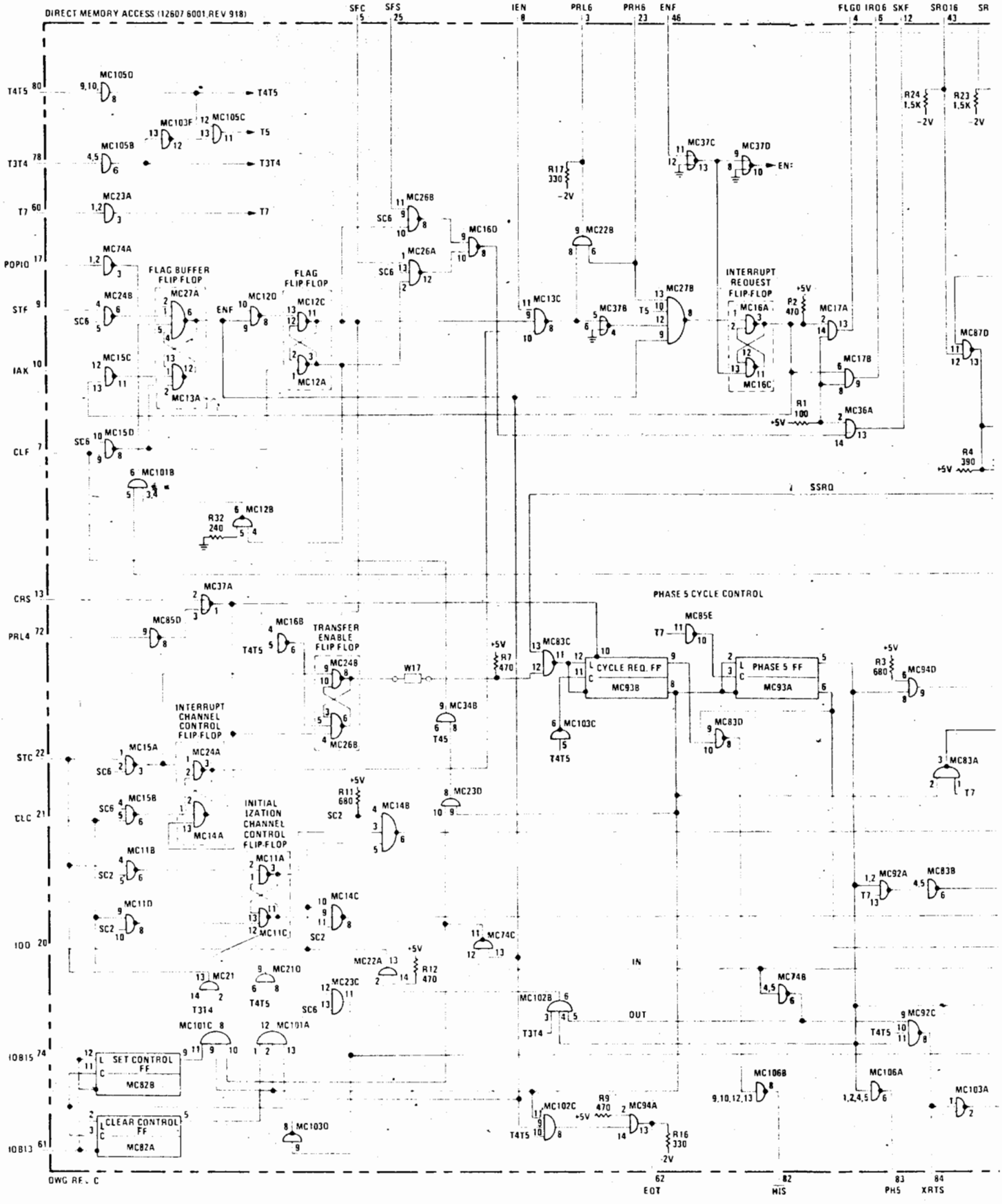


Figure 4-1. DMA Assembly Schematic and Parts Location Diagrams


FLG0 IRQ6 SKF SRQ16 SRQ15 SRQ14 SRQ13 SRQ12 SRQ11 SRQ10
IOG SCM0 SCL0 SCL1 SCL2 SCL3 SCL4 SCL5 SCL6 SCM1 IOB14
NOT USED
SC2
SC6
MC25B
MC25A
R24 1.5K -2V
R23 1.5K -2V
R22 1.5K -2V
R21 1.5K -2V
R20 1.5K -2V
R19 1.5K -2V
R18 1.5K -2V
MC47B
MC97B MC97A MC47A MC96B MC67A MC67B MC57B MC57A
+5V
P2 470
MC17A
MC87D
MC86D
MC86A
MC86B
MC87A
MC87B
MC87C
MC178
R1 100
MC36A
TP3
GND
MC77D MC77E MC77F MC85A MC77C MC77B
R4 390
MC85B
SERVICE SELECT REGISTER
SSRQ
R13 240
MC55C
MC55B
MC55A
MC76
SS0 SS1 SS2 SS3 SS4 SS5 SS6
TP2
R3 680
MC94D
MC83A
T7
MC92A
MC83B
MC74B
MC92C
T4T5
MC106A
MC103A
R10 470
MC107A
MC105A
UPDATE INTERRUPT ADDRESS FF
MC103B
MC104A
MC104B
MC104D
MC104C
ENF
MC36B
MC34A
SC2
TP1
ENF
MC86C
R6 820
+5V
C1 THRU C55
0.01
GND
MIS
PH5
XRTS
IOCO
PH4
XPH4
ISG
SWST
IOI
IOB15
+5V
GND


DIRECT MEMORY ACCESS (12607 6001 REV 918)
SFC
SFS
IEN
PRL6
PRH6
ENF
FLG0
IRQ6
SKF
SR016
SR
T4T5
T3T4
T7
POPIO
STF
IAK
CLF
CRS
PRL4
STC
CLC
IOO
IOB15
IOB13
MC105D
MC105C
MC105B
MC103F
MC23A
MC74A
MC24B
MC15C
MC15D
MC10IB
MC12B
R32 240
FLAG BUFFER FLIP FLOP
MC27A
MC13A
MC12D
FLAG FLIP FLOP
MC12C
MC12A
MC26B
MC26A
MC16D
MC13C
R17 330 -2V
MC37C
MC37D
EN
MC22B
MC37B
MC27B
INTERRUPT REQUEST FLIP-FLOP
MC16A
MC16C
P2 470
MC17A
MC17B
MC87D
R1 100
MC36A
R24 1.5K -2V
R23 1.5K -2V
R4 390
SSRQ
PHASE 5 CYCLE CONTROL
MC85E
MC83C
CYCLE REQ. FF
MC93B
PHASE 5 FF
MC93A
R3 680
MC94D
MC83D
MC103C
MC34B
MC16B
TRANSFER ENABLE FLIP-FLOP
MC26B
W17
R7 470
INTERRUPT CHANNEL CONTROL FLIP-FLOP
MC15A
MC24A
MC14A
MC15B
INITIAL IZATION CHANNEL CONTROL FLIP-FLOP
MC11A
MC11C
MC11B
MC11D
R11 680
MC14B
MC23D
MC14C
MC74C
MC22A
R12 470
MC21
MC21D
MC23C
MC101C
MC101A
MC102B
MC74B
MC92C
MC92A
MC83B
MC83A
MC102C
R9 470
MC94A
R16 330 -2V
MC106B
MC106A
MC103A
MC103D
SET CONTROL FF
MC82B
CLEAR CONTROL FF
MC82A
IN
OUT
DWG REV C
EOT
MIS
PHS
XRTS

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the optional Hewlett-Packard 12607A Direct Memory Access (DMA) Accessory Kit.

1-3. GENERAL DESCRIPTION.

1-4. The DMA option is used with the HP 2114B general purpose computer. The DMA option consists of a single plug-in card, which plugs into a prewired slot in the computer. DMA is single-channelled and is program-assignable to addresses 10 through 16. The HP 12607A DMA Accessory Kit includes the following items:

a. 12607-6001 Single-Channel DMA Card.

b. 12607-90002 DMA Operating and Service Manual and Diagnostic Supplement.

c. HP 20524A (or later) DMA Binary Diagnostic Tape.

d. HP 20525A (or later) DMA Binary Rate and Transfer Diagnostic Tape.

1-5. DMA enables the computer to transfer data directly between memory and external devices at a maximum rate of 500,000 16-bit words per second in block lengths of 1 to 8192 words. Word transfer time is 2.0 microseconds for each 16-bit word. No character packing hardware is provided on the card; when using byte (eight bit) oriented devices, character packing and unpacking may be accomplished with software, before or after data transfer.

1-6. To be placed in operation, the DMA system must first be initialized for a specific operating mode by instructions and control words in the main program. Data interchange then occurs automatically when a service request signal is received from an I/O channel programmed to DMA. The DMA option then takes control of the central processor and I/O system, suspends the running program at the end of the current phase, and during the following machine cycle, generates a special phase 5 memory cycle to read or write a word directly into or out of a predetermined memory location. At the end of the phase 5 memory cycle (one complete machine cycle), control is returned to the central processor and I/O system, and the main program is automatically resumed at the point where it was suspended, without loss of continuity. A new phase 5 cycle is initiated each time the I/O device signals DMA that it is ready to input or output another word. When all data in a predetermined block length have been transferred, DMA initiates a normal interrupt to a service subroutine.

1-7. IDENTIFICATION.

1-8. Printed-circuit card revisions are identified by a letter and a date code stamped on the card. The letter code identifies the version of the etched trace pattern on the unloaded card. The date code refers to the electrical characteristics of the loaded card. If the date code stamped on the printed circuit card does not agree with the date code shown on the schematic diagram in section IV of this manual for the DMA card, there are differences between your card and the card described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section contains installation and programming information for the DMA option, including program word formats and a typical DMA program.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the card is unpacked. Inspect the card for damage (cracks, broken parts, etc.). If the card is damaged or fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged card without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. No special installation procedures are required to install the DMA option. However, make certain that power is off at the computer before plugging the DMA card into connector XA16 in the computer mainframe. After the DMA card has been installed, perform diagnostic test procedures contained in the diagnostic supplement to this manual to ensure proper operation of the DMA card.

2-7. PROGRAM WORD FORMATS.

2-8. The DMA option is programmed using HP assembler language. The instruction, control, and data word formats used in the operation of DMA are shown in figure 2-1 and are defined below.

a. Input/output instruction words: I/O group instructions addressed to select code 2 or 6 that permit the central processor to control the following DMA functions through the I/O select codes specified:

(1) Select code 2 permits initialization channel control flip-flop on DMA card to be addressed by CLC and STC instructions.

(2) Select code 2 preceded by a CLC instruction permits DMA memory address register to be addressed by an OTA instruction.

(3) Select code 2 preceded by a STC instruction permits DMA word count register to be addressed by OTA and LIA instructions.

(4) Select code 6 permits DMA switching functions to be addressed by OTA, CLC, STC, CLF, STF, SFC, and SFS instructions.

b. DMA program control words: Program constants that can be programmed to DMA to specify the following information:

(1) The I/O channel select code address of the device to be serviced by DMA (bits 0 through 2 select devices 10 through 16).

(2) Clear (turn off) control on device after last word in data block has been transferred (bit 13 = 1).

(3) Do not clear control on device after data transfer (bit 13 = 0).

(4) Set (turn on) control on device after each word in data block has been transferred (bit 15 = 1).

(5) Do not set control on device after each transfer (bit 15 = 0).

c. DMA address words: Program constants that can be programmed to DMA to specify the following information:

(1) Starting memory address for first word of input/output data block (bits 0 through 14).

(2) Memory input from device I/O channel (bit 15 = 1).

(3) Memory output to device I/O channel (bit 15 = 0).

d. DMA block length words: Program constants that can be programmed to DMA to specify the number of words in the data block. Word count is a number expressed as the two's complement of the positive binary equivalent of the number.

e. Data input/output words: Format used to transfer data directly between the device I/O channel and memory.

2-9. TYPICAL DMA PROGRAM.

2-10. An example of a typical program that uses the DMA option is listed in table 2-1. In this program, a memory input operation is carried out where a block of 50_{10} words is read from a tape reader (I/O channel select code address 10_8) into computer memory locations 200_8 through 261_8.

INPUT/OUTPUT INSTRUCTION WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IO GROUP					INSTRUCTION				SELECT CODE 2 OR 6					

DMA PROGRAM CONTROL WORD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	STC	NOT	CLC	NOT USED										DEVICE SELECT CODE		
0	$\overline{\text{STC}}$	USED	$\overline{\text{CLC}}$													

DMA ADDRESS WORD

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	IN	NOT		WORD ADDRESS												
0	OUT	USED														

DMA BLOCK LENGTH WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED			WORD COUNT												

DATA INPUT/OUTPUT WORD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16-BITS															

2048-4

Figure 2-1. DMA Instruction and Control Word Formats

Note

The program in table 2-1 assumes that the interrupt system is enabled (STF0 instruction) and that DMA will initiate an interrupt to a service subroutine when all words in the assigned data block have been transferred.

Table 2-1. Typical DMA Program

LABEL	OP CODE	OPERAND	REMARKS
			INITIALIZE DMA FOR INPUT
ASGN	LDA	CW1	Fetches control word 1 (CW1) from memory and loads it in A-register.
	OTA	6	Outputs CW1 to DMA.
MAR	CLC	2	Prepares DMA memory address register to receive and store control word 2 (CW2).
	LDA	CW2	Fetches CW2 from memory and loads in in A-register.
	OTA	2	Outputs CW2 to DMA.
WCR	STC	2	Prepares DMA word count register to receive and store control word 3 (CW3).
	LDA	CW3	Fetches CW3 from memory and loads it in A-register.
	OTA	2	Outputs CW3 to DMA.
			START DEVICE AND DMA
STRT	STC	10B,C	Initiate tape reader data transfer.
	STC	6B,C	Activate DMA.
			DMA DATA TRANSFER
	. . .	. . .	Continue program while data transfer takes place.
			DMA CONTROL WORDS
CW1	OCT	120010	Assignment for DMA; specifies I/O channel select code address (10_8), STC after each word is transferred, and CLC after final word is transferred.
CW2	OCT	100200	Memory address register control for DMA; specifies memory input operation and starting memory address (200_8).
CW3	DEC	-50	Word count register control for DMA; specifies the two's complement of the number of words in the block to be transferred.

SECTION III
THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief functional description and a detailed circuit description for the DMA option.

Note

For a description of abbreviations (mnemonics) used in this section, refer to table 4-1.

3-3. FUNCTIONAL DESCRIPTION.

3-4. The DMA option adds a fifth phase to the four-phase capability of the basic computer. Phase 5 is a special memory cycle that requires one machine timing cycle (T0 through T7). Once initiated by service request signals received from I/O channels programmed to DMA, phase 5 operation is automatic and independent of program control. Each phase 5 cycle permits one input or output word to be exchanged between an external device (tape reader, disc memory, magnetic tape unit, etc.) and computer memory.

3-5. When a service request is received by DMA, the main program is suspended for one machine cycle to achieve data transfer (one 16-bit word per cycle), rather than achieving data transfer by interrupting to a service subroutine. While the program is suspended, the computer is in phase 5 and data is transferred to or from the external device. At the end of the phase 5 cycle, the main program (now delayed by one machine cycle) continues from the point that it was suspended since the counting registers in the central processor are not stepped during a phase 5 cycle. A DMA interrupt occurs only after the word count function signals that all words in a data block have been transferred.

3-6. Figure 3-1 is a functional block diagram showing the relationship between the HP 2114B logic circuitry and the DMA logic. Table 3-1 lists the step-by-step sequence for DMA operation. When referencing figure 3-1 and table 3-1, assume that the typical DMA program in table 2-1 is being run. Since this program is for a memory input operation, table 3-1 does not cover the sequence for a memory output operation. However, the two operations are the same except for the signals generated to transfer data between the IOB lines and memory. These signals are shown for both operations in figure 3-1.

3-7. DETAILED CIRCUIT DESCRIPTION.

3-8. The following paragraphs contain a detailed circuit description for the DMA option. The description covers initialization, generation of a phase 5 signal, data input and output operations, DMA register stepping and device turn-off, and DMA completion interrupt. See the schematic diagram for DMA (figure 4-1) whenever referring to this circuit description.

3-9. INITIALIZATION

3-10. When the DMA option is initialized, the first control word is output to the DMA card on the IOB lines with an OTA 6 instruction in the main program. At T3T4, bits 0, 1, and 2 are clocked into service select register FF's MC55A, MC55B, and MC55C. The bits are encoded by MC76 to provide the least significant octal digits of the select code of the external device involved in the data transfer. This information will remain on the service select (SS) lines until the data transfer is complete and a succeeding data transfer is initiated. Bit 13 of the first control word sets the clear control FF if the bit is true and a true bit 15 sets the set control FF. These flip-flops are clocked at T3T4 when the SC6 signal and the IOO signal are both true.

3-11. The second step in initializing DMA is to output a CLC 2 instruction which resets the initialization channel control FF. The second control word may then be loaded into the A-register and output to DMA over the IOB lines by a OTA 2 instruction. Bits 0 through 12 of control word 2 specify the starting address of the block of data to be transferred, and bit 15 specifies whether the data transfer is an input or an output operation (bit 15 = logic 1 = input operation). At T3T4 the IOO signal is true, making all inputs to MC14C true, and a false $\overline{\text{LMAR}}$ signal is generated. The false $\overline{\text{LMAR}}$ signal allows the starting address on the IOB lines to be clocked into the memory address register, and the address appears on lines XMR0 through XMR12. At the same time, bit 15 is clocked into the memory address register and pin 7 of MC75 goes true for a data input operation or false for an output operation.

3-12. Next, an STC 2 instruction is output to DMA which sets the initialization control FF. Control word 3 is then loaded into the A-register and output to DMA on the IOB lines, again by an OTA 2 instruction. Bits 0 through 12 of control word 3 specify the 2's complement of the number of words in the data block to be transferred. At T3T4, all inputs to MC14B are true and a false $\overline{\text{LWCR}}$ signal is generated. The false $\overline{\text{LWCR}}$ signal clocks bits 0 through 12 of control word 3 into the word count register. The word count register output lines (WCR0 through WCR12) now reflect the 2's complement of the number of words in the data block.

3-13. An IOI signal (resulting from an LIA, LIB, MIA, or MIB instruction) will cause the WCR bits to be read onto

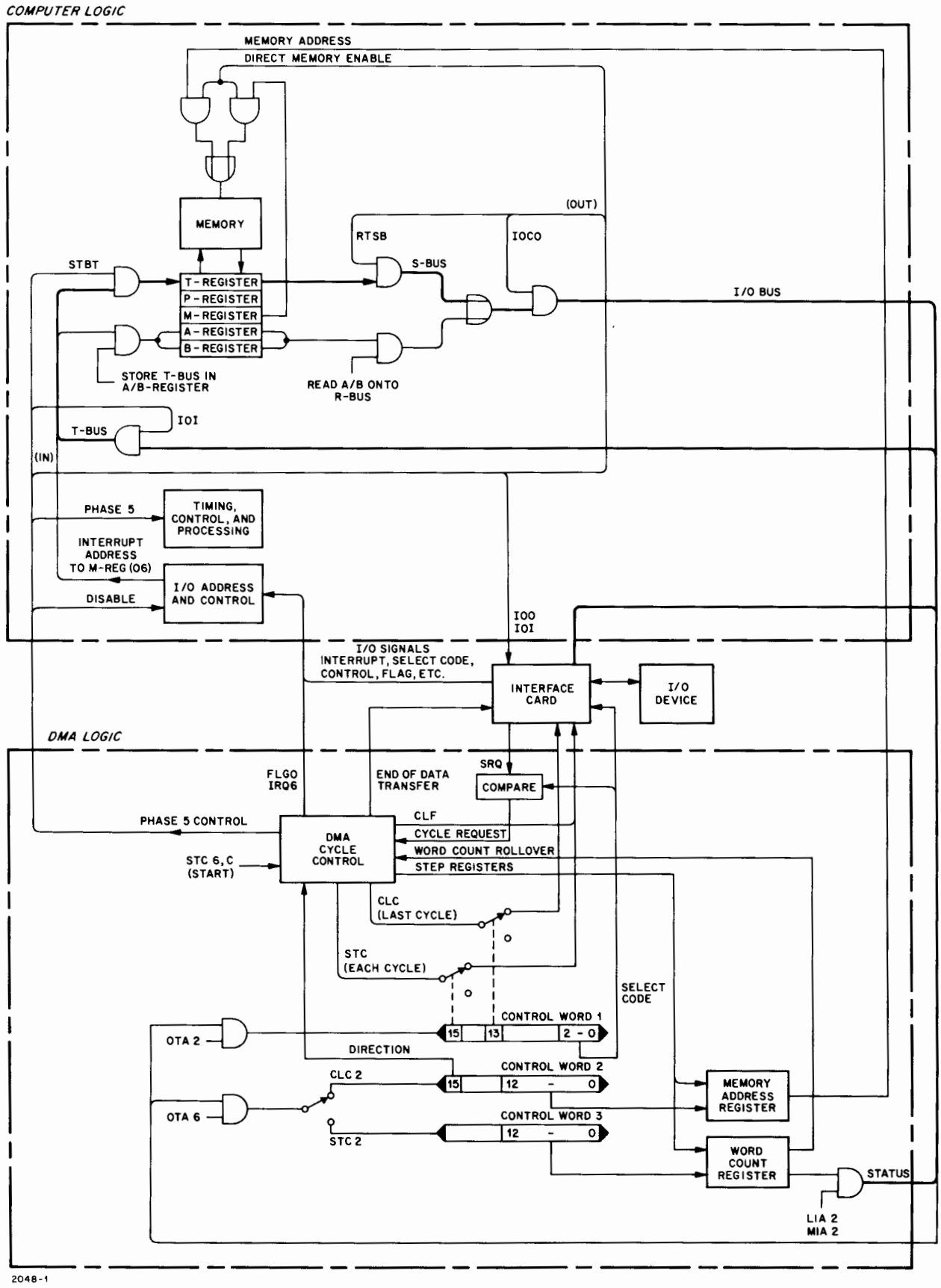


Figure 3-1. DMA Functional Block Diagram

Table 3-1. Basic Sequence for DMA Data Transfer

INITIALIZE DMA FOR AN INPUT OPERATION
a. Control word 1 (CW1) is transferred to the DMA card from the A-register on the IOB lines by an OTA 6 instruction. b. Bits 0 thru 3, 13, and 15 of CW1 are stored on the DMA card. Bits 0 thru 3 specify the select code of the device involved in the data transfer. Bit 13 (if true) specifies CLC of the device after the final word is transferred. Bit 15 (if true) specifies STC of the device after each word is transferred. c. A CLC 2 instruction prepares DMA to receive control word 2 (CW2), and OTA 2 transfers CW2 to the DMA card. d. Bits 0 thru 12 and 15 of CW2 are stored on the DMA card. Bits 0 thru 12 specify the starting address in memory of the data transfer and are stored in the memory address register. Bit 15 specifies whether the transfer is a memory input or an output operation (bit 15 = logic 1 = memory input operation). e. A STC 2 instruction prepares DMA to receive control word 3 (CW3), and OTA 2 transfers CW3 to the DMA card. f. Bits 0 thru 12 of CW3 are stored in the word count register of the DMA card and specify the 2's complement of the number of words (octal) in the block length of data to be transferred. g. I/O signals turn on DMA (STC 6,C) and the I/O device (STC 10,C).
DMA DATA TRANSFER
a. Device sets interface flag when ready to transfer data, generating an SRQ signal. b. On the DMA card, an SRQ signal is compared with the stored select code of the device and, if the select code of the device that originated the SRQ signal is the same as the select code that is stored on the DMA card, a cycle request signal is originated. c. The cycle request signal causes a PH5 signal to be generated at the end of the current cycle, which: (1) Puts the computer into the phase 5 mode, disabling all other phases and the instruction register. An ISG signal inhibits the reading of memory into the T-register. (2) Disables normal I/O operation by inhibiting select code logic. (3) Reads the interface card data onto the I/O bus lines using DMA generated select code and IOI signals. (4) Gates the data from the IOB lines onto the T-bus with an IOI signal. (5) Stores the T-bus bits in the T-register using a DMA STBT signal. (6) Enables the memory address register to select the desired memory location for input. d. The computer now continues into a memory cycle. Since memory reading is inhibited, the T-register retains the input word through the read portion of the memory cycle, and the word is written into memory on the write portion of the cycle. e. At the end of the phase 5 cycle, a CLF signal and a STC signal (if selected) are issued to the interface card, releasing the device to obtain the next input word.
DATA TRANSFER COMPLETION
a. At the end of each phase 5 cycle, the memory address register and the word count register are advanced by one count. This allows the memory address register to address the next higher memory location and advances the word count register one count closer to zero from the initial negative value. b. When the word count register reaches zero, word count rollover occurs and the phase 5 cycle control is disabled. c. If the interrupt system is on, an interrupt to location 06 will occur through the interrupt system. d. Anytime during or after data transfer, the status of the word count register may be checked by LIA 2 or MIA 2 instruction, which loads the word count register into the A-register. e. A SFS 6 instruction may be used to test for transfer completion since the DMA flag is set at word count rollover. f. If selected during initialization, a CLC signal is issued to the interface card to turn off the device.

the IOB lines if the respective instruction is addressed to code 2. This allows the status of the data transfer to be checked as desired. Also, if SFC or SFS instructions are addressed to SC6 in the main program and the flag is clear or set as required by the respective instruction, a true SKF signal will result at pin 12 of the DMA card.

3-14. The last step in the initialization process consists of setting control and clearing flag FF's on the DMA card and the device interface card to or from which data is to be transferred. This is done by STC,C instructions in the program to the select code of the device and to select code 6 (the DMA select code). On the DMA card, the STC instruction sets the interrupt channel control FF and the transfer enable FF. The CLF instruction resets the flag buffer FF and flag FF. Data transfer can now begin.

3-15. GENERATION OF A PHASE 5 SIGNAL.

3-16. When the device is ready to transfer a word, an SRQ signal is generated on the appropriate SRQ line. The SRQ signal and the corresponding service select register bit are combined in a nand-gate. The resulting output is inverted by MC85B to provide the SSRQ signal. The true set output of the transfer enable FF and the SSRQ signal are combined in MC83C. The resulting false output of MC83C resets the cycle request FF at T4T5. At T7 of the same cycle, the phase 5 FF is set, generating the PH5 signal.

3-17. When the PH5 signal is generated, central processor operation is suspended for one machine cycle. To accomplish data transfer, DMA must generate control signals that would normally be generated within the central processor unit. During the phase 5 cycle, the following control signals are generated by DMA:

a. A $\overline{\text{PH5}}$ signal at pin 83 is generated by inverting the PH5 signal in MC106A. During phase 5, this signal inhibits the enable phase gate on the computer timing generator card and prevents the computer from going into phase 1, 2, 3, or 4 until phase 5 is complete.

b. An ISG signal is generated for a memory input operation by combining the PH5 and IN signals in MC105A. A true ISG signal inhibits the memory strobe time (MST) signal from being generated on the computer timing generator card.

c. IOI and $\overline{\text{SWST}}$ are generated to implement memory input operations.

d. IOCO and $\overline{\text{XRTS}}$ signals are generated to implement memory output operations.

e. An $\overline{\text{XPH4}}$ signal is generated by the update interrupt address FF during T7 which causes a phase 4 signal to be generated at the timing generator card during T7 to store M-register bits 0 through 5.

f. The $\overline{\text{PH5}}$ and CRFF signals cause MC83D to output a true signal during phase 5. This, in turn, generates an HIS signal to the I/O control card which prevents interrupt requests from other devices from being serviced during phase 5.

3-18. DATA INPUT OPERATION.

3-19. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal. This allows DMA to address the device on the appropriate select code lines (10 through 16). At the device interface card, SCL and SCM signals from DMA are combined with an IOG signal and the resulting output is combined with an IOI signal to gate data from the interface card onto the IOB lines.

3-20. On the DMA card, the PH5 and IN signals are combined in MC105A. The output of MC105A combines with the ENF signal to generate $\overline{\text{SWST}}$ and IOI signals. (See figure 3-2.) The IOI signal gates the IOB bits onto the T-bus in the central processor. The $\overline{\text{SWST}}$ signal is decoded by the instruction decoder in the computer. The STBT signal, which results from the $\overline{\text{SWST}}$ signal being decoded, clocks the T-bus bits into the T-register. The T-register output is then routed directly into computer memory and the data transfer for the first word is complete. This process is repeated for each word to be transferred into memory.

3-21. DATA OUTPUT OPERATION.

3-22. When the phase 5 FF is set, the service select register bits are gated onto the select code lines along with the SCM1 signal, allowing DMA to address I/O select codes 10 through 16. At the device interface card, SCL, SCM, IOG, and IOO signals from DMA are used to gate data from the IOB lines into the interface card registers. To transfer data out of computer memory and onto the IOB lines, DMA generates $\overline{\text{XRTS}}$ and IOCO control signals. (See figure 3-3.) The $\overline{\text{XRTS}}$ signal and the RTS signal from the computer instruction decoder card combine to generate the RTSB signal. The RTSB signal gates the T-register bits onto the S-bus. The S-bus bits are inverted and are gated onto the IOB lines by the IOCO signal. The IOB bits are then transferred into the interface card and the device, as mentioned previously, and a single word transfer is complete. This process is repeated until all words in the data block have been transferred.

3-23. DMA REGISTER STEPPING AND DEVICE TURN-OFF.

3-24. At T7 of phase 5, the output of MC83B goes true, and the memory address register is advanced one count by the true SMAR signal. This updates the memory address register to the memory location involved in the next word transfer. At the end of the same T7, the output of MC83A goes true and the true $\overline{\text{SWCR}}$ signal advances the word count register one count.

3-25. The above process is repeated for each phase 5 cycle until all words in the data block have been transferred. Since the word count register is initially loaded with

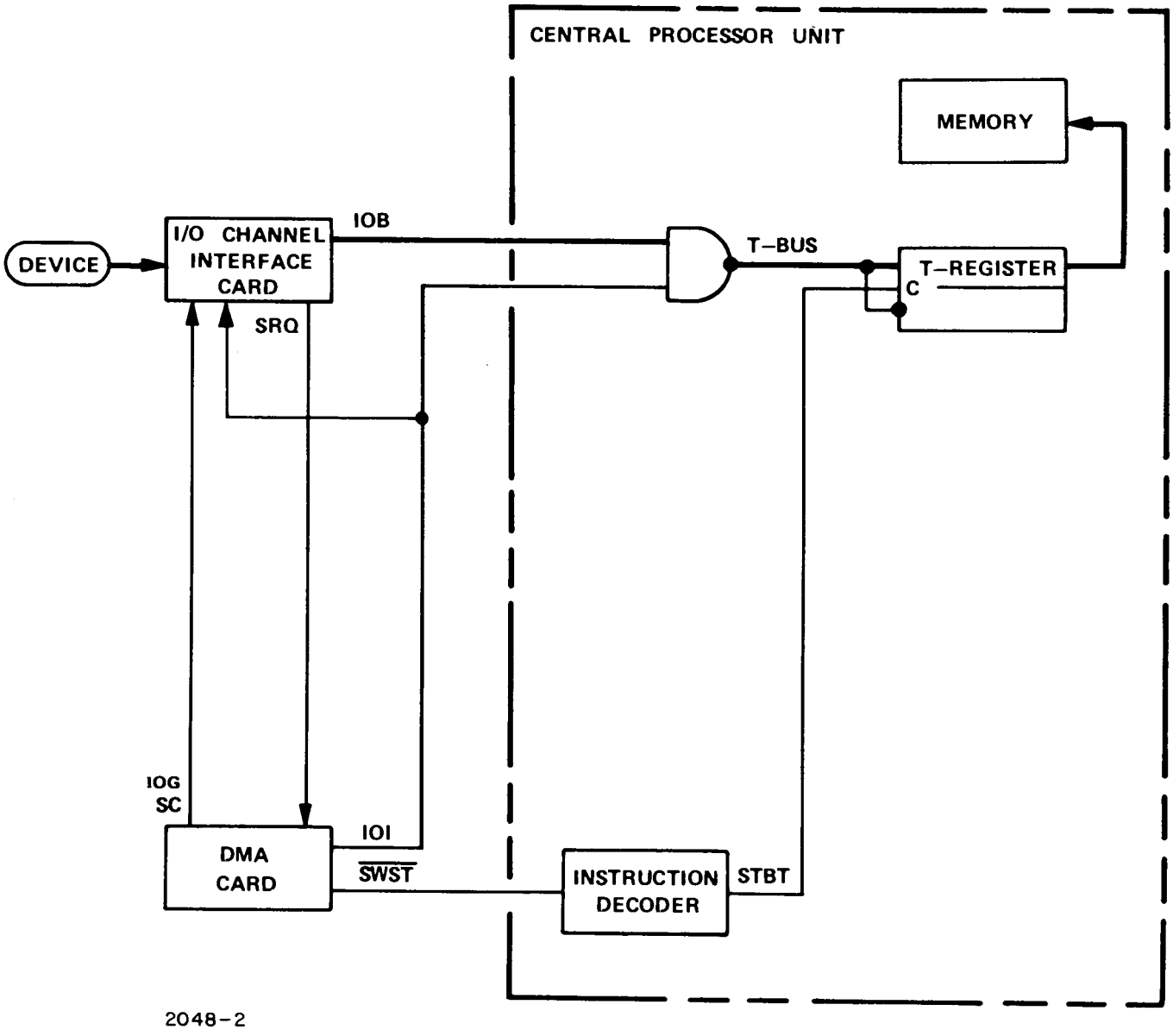


Figure 3-2. Transferring Data from an External Device to Memory

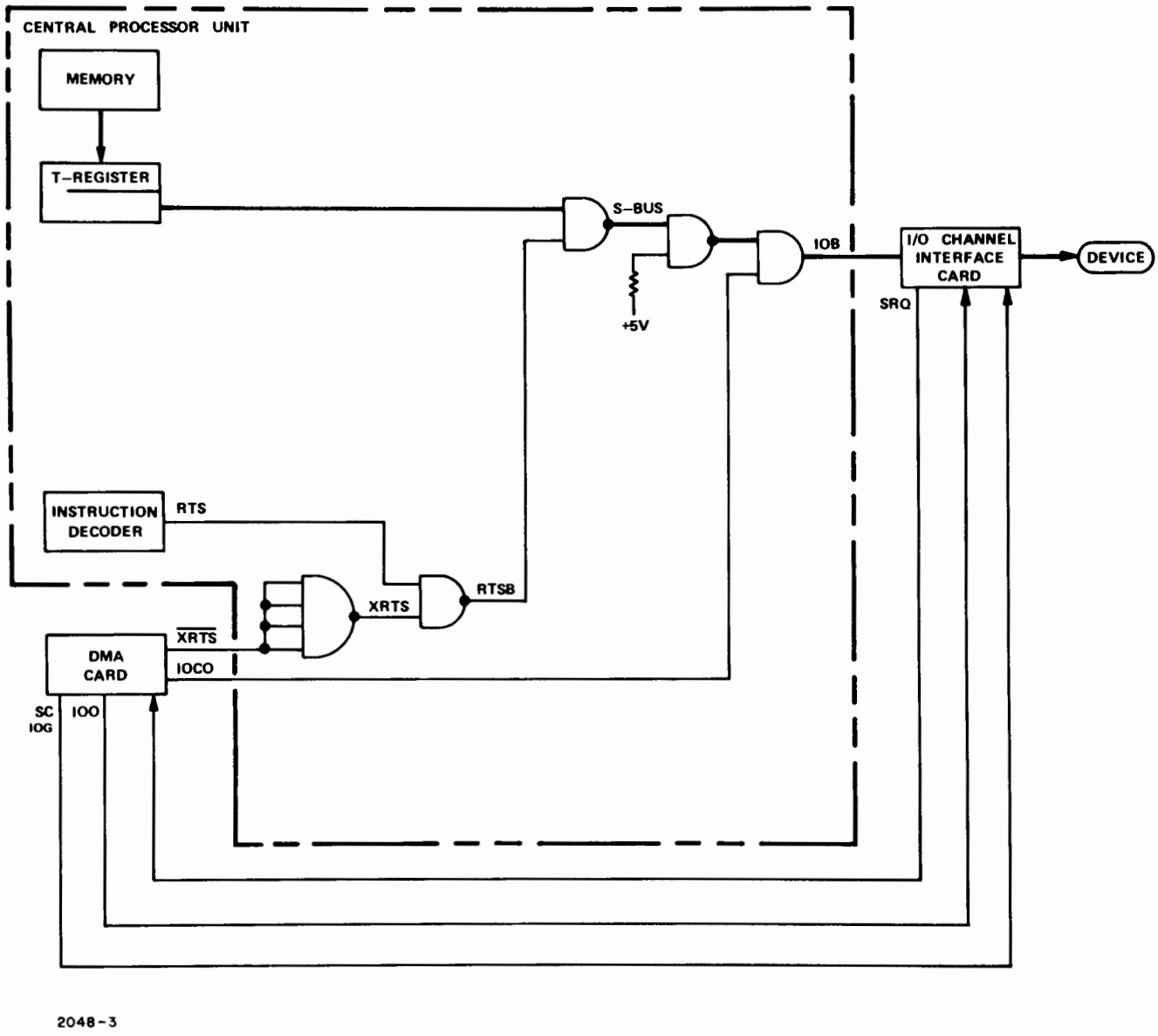


Figure 3-3. Transferring Data from Memory to an External Device

the two's complement of the number of words in the data block, the word count register will contain all zero's when all words have been transferred. The final $\overline{SWCR}$ signal sets all WCR bits to zero and causes pin 12 of MC91 (the carry output) to go false. The false $\overline{WCR}$ signal makes the output of MC101B false, setting the flag buffer FF. At T2, the ENF signal and the true FBFF signal set the flag FF.

3-26. Setting the STC and CLC FF's during initialization causes a STC signal to be generated after each word transfer and a CLC signal to be generated after the final word transfer. The STC FF output is applied to MC101C along with the reset output of the cycle request FF and the output of MC74C. The MC74C output will be true until the last word transfer when the flag buffer FF is set. The cycle request FF is reset by every SRQ signal. Therefore, a STC signal will be generated at pin 22 of the DMA card for every word transfer except the last when the flag buffer FF is set. Also, the true output of MC74C causes a CLF signal to be generated at pin 7 every T4T5 to clear the device flag after every word transfer, except the last. The CLC FF output is applied to MC101A along with the reset output of the cycle request FF and the set output of the flag buffer FF. The false flag buffer FF output signal inhibits MC101A until after the final word transfer. The flag buffer FF signal then goes true and a CLC signal is generated at pin 21 of the DMA card to turn off the external device. This inhibits any SRQ signals from being generated by the device until DMA is reinitialized.

3-27. DMA COMPLETION INTERRUPT.

3-28. The true FBFF and FLFF signals enable the generation of flag and interrupt signals at the end of the final word transfer. The true FLFF signal along with true ICCFF and IEN signals make MC13C output a false signal to MC37B. True signals from MC37B, FBFF, and PRH6 make MC27B output a false signal at T5 to set the interrupt request FF and generate FLG0 and IRQ6 signals. The FBFF signal also enables the generation of an EDT signal at the DMA card which is used by some of the I/O devices to signal the end of data transfer.

3-29. At the I/O control card, the FLG0 and IRQ6 signals try to generate an interrupt, but the interrupt system is disabled for at least one phase to allow a main program instruction to be executed following a phase 5 operation. At the end of this cycle, DMA interrupts, causing the generation of a phase 4 cycle and forcing the DMA trap cell location into the M-register. The next fetched instruction will be the call instruction for the DMA completion subroutine. In the DMA completion subroutine, DMA is turned off and must be reinitialized before being placed in operation again.

SECTION IV

MAINTENANCE

4-1. INTRODUCTION.

4-2. This section contains information on the diagnostics and troubleshooting for the DMA option.

4-3. DIAGNOSTICS.

4-4. Complete diagnostic procedures and listings are contained in the manual supplement attached to this manual. The manual supplement contains a DMA general diagnostic and a DMA rate and transfer diagnostic.

4-5. TROUBLESHOOTING.

4-6. Troubleshooting the DMA option is accomplished by performing the diagnostic tests contained in the manual supplement attached to this manual and analyzing the error halts that occur as the test is being run. To further isolate trouble, refer to the list of signals and equations in table 4-1 and the DMA schematic and parts location diagrams in figure 4-1. Table 4-2 contains a list of connector pin functions for the DMA card and a listing of reference numbers for each signal. The reference numbers correspond to consecutive reference numbers on the HP 2114B Computer backplane wiring list which appears in Volume Two of the Operation and Maintenance Manual for the computer. Table 4-3 contains a complete parts list for the DMA card with parts listed in alphanumeric order of reference designations. Refer to Volumes Two and Three of the HP 2114B Operation and Maintenance Manual for additional information on backplane wiring, signal data, etc., not included in this manual.

Table 4-1. DMA Signals and Equations

MNEMONIC	SIGNAL NAME	EQUATION
CLC	Clear Control	CLC = CLC FF
CLC FF	Clear Control FF	Data = IOB13 Clock = (SC6 · IOO)
CR FF	Cycle Request FF	Data = $\overline{SSRQ}$ + $\overline{TEFF}$ Clock = $\overline{T4T5}$
EDT	End of Data Transfer	EDT = FBFF · T4T5 · $\overline{CRFF}$
FB FF	Flag Buffer FF	Set = POPIO + (STF · SC6) + WCR Reset = (IAK · IRQFF) + (CLF · SC6)
FL FF	Flag FF	Set = FBFF · ENF Reset = CLF · SC6
FLG0	Flag 0	FLG0 = IRQFF
$\overline{HIS}$	"Not" Hold Interrupt System	$\overline{HIS}$ = $\overline{PH5}$ · CRFF
ICC FF	Interrupt Channel Control FF	Set = STC6 · SC6 Reset = (CLC · SC6) + (CRS + $\overline{PRL4}$)
IOCO	Input/Output Control Out	IOCO = OUT · T4T5 · PH5
IN	DMA Input	IN = IOB15 · LMAR
INI FF	Initialization Channel Control FF	Set = STC · SC2 Reset = CLC · SC2
IRQ FF	Interrupt Request FF	Set = PRH6 · T5 · IEN · FLGFF · ICCFF · FBFF Reset = ENF
IRQ6	Interrupt Request 6	IRQ6 = IRQFF
ISG	Interrupt Strobe Generator	ISG = PH5 · IN
$\overline{LMAR}$	"Not" Load Memory Address Register	$\overline{LMAR}$ = $\overline{SC2}$ + $\overline{IOO}$ + INIFF
$\overline{LWCR}$	"Not" Load Word Count Register	$\overline{LWCR}$ = $\overline{SC2}$ + $\overline{IOO}$ + $\overline{INIFF}$
OUT	DMA Output	OUT = $\overline{IN}$
PH5	Phase 5	PH5 = PH5 FF
PH5 FF	Phase 5 FF	Data = $\overline{CRFF}$ Clock = $\overline{T7}$
PRL6	Priority Low 6	PRL6 = PRH6 · ($\overline{IEN}$ + $\overline{FLGFF}$ + $\overline{ICCFF}$)
RWCR	Read Word Count Register	RWCR = (IOI · SC2)
SC2	Select Code 2	SC2 = IOG · SCM0 · SCL2
SC6	Select Code 6	SC6 = IOG · SCM0 · SCL6

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
SCL0	Select Code Least Significant Octal 0	SCL0 = PH5 · SS0
SCL1	Select Code Least Significant Octal 1	SCL1 = PH5 · SS1
SCL2	Select Code Least Significant Octal 2	SCL2 = PH5 · SS2
SCL3	Select Code Least Significant Octal 3	SCL3 = PH5 · SS3
SCL4	Select Code Least Significant Octal 4	SCL4 = PH5 · SS4
SCL5	Select Code Least Significant Octal 5	SCL5 = PH5 · SS5
SCL6	Select Code Least Significant Octal 6	SCL6 = PH5 · SS6
SCM1	Select Code Most Significant Octal 1	SCM1 = PH5
SKF	Skip on Flag Signal	SKF = (SFS · SC6 · FLGFF) + (SFC · SC6 · $\overline{\text{FLGFF}}$)
SMAR	Step Memory Address Register	SMAR = PH5 · T7
SSRQ	Selected Service Request	SSRQ = (SS0 · SRQ10) + (SS1 · SRQ11) + (SS2 · SRQ12) + (SS3 · SRQ13) + (SS4 · SRQ14) + (SS5 · SRQ15) + (SS6 · SRQ16)
STC	Set Control	STC = STC FF
STC FF	Set Control FF	Data = IOB15 Clock = (SC6 · IOO) + (SC6 · OUT · T3T4 · PH5)
$\overline{\text{SWCR}}$	"Not" Step Word Count Register	$\overline{\text{SWCR}}$ = $\overline{\text{CRFF}}$ + $\overline{\text{T7}}$
$\overline{\text{SWST}}$	Switch Store in T-Register	$\overline{\text{SWST}}$ = $\overline{\text{ENF}}$ + $\overline{\text{PH5}}$ + $\overline{\text{IN}}$
TE FF	Transfer Enable FF	Set = STC · SC6 Reset = (FLGFF · T4T5) + CRS + $\overline{\text{PRL4}}$
UIA FF	Update Interrupt Address FF	Set = PH4 Reset = PH5 · ENF
$\overline{\text{WCR}}$	"Not" Word Count Rollover	$\overline{\text{WCR}}$ = WCR0 thru WCR12 · $\overline{\text{SWCR}}$
WCR0	Word Count Register Bit 0	WCR0 = WCR0 FF

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
WCR0 FF	Word Count Register Bit 0 FF	Clock = $\overline{SWCR}$ Direct Set = IOBO · LWCR Direct Reset = $\overline{IOBO}$ · LWCR
WCR1	Word Count Register Bit 1	WCR1 = WCR1 FF
WCR1 FF	Word Count Register Bit 1 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ Direct Set = IOB1 · LWCR Direct Reset = $\overline{IOB1}$ · LWCR
WCR2	Word Count Register Bit 2	WCR2 = WCR2 FF
WCR2 FF	Word Count Register Bit 2 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ · $\overline{WCR1}$ Direct Set = IOB2 · LWCR Direct Reset = $\overline{IOB2}$ · LWCR
WCR3	Word Count Register Bit 3	WCR3 = WCR3 FF
WCR3 FF	Word Count Register Bit 3 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR2}$ Direct Set = IOB3 · LWCR Direct Reset = IOB3 · LWCR
WCR4	Word Count Register Bit 4	WCR4 = WCR4 FF
WCR4 FF	Word Count Register Bit 4 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR3}$ Direct Set = IOB4 · LWCR Direct Reset = $\overline{IOB4}$ · LWCR
WCR5	Word Count Register Bit 5	WCR5 = WCR5 FF
WCR5 FF	Word Count Register Bit 5 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR4}$ Direct Set = IOB5 · LWCR Direct Reset = $\overline{IOB5}$ · LWCR
WCR6	Word Count Register Bit 6	WCR6 = WCR6 FF
WCR6 FF	Word Count Register Bit 6 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR5}$ Direct Set = IOB6 · LWCR Direct Reset = $\overline{IOB6}$ · LWCR
WCR7	Word Count Register Bit 7	WCR7 = WCR7 FF
WCR7 FF	Word Count Register Bit 7 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR6}$ Direct Set = IOB7 · LWCR Direct Reset = $\overline{IOB7}$ · LWCR
WCR8	Word Count Register 8	WCR8 = WCR8 FF
WCR8 FF	Word Count Register Bit 8 FF	Clock = $\overline{SWCR}$ · $\overline{WCR0}$ thru $\overline{WCR7}$ Direct Set = IOB8 · LWCR Direct Reset = $\overline{IOB8}$ · LWCR

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
WCR9	Word Count Register Bit 9	WCR9 = WCR9 FF
WCR9 FF	Word Count Register Bit 9 FF	Clock = $\overline{SWCR} \cdot \overline{WCR0}$ thru $\overline{WCR8}$ Direct Set = IOB9 · LWCR Direct Reset = $\overline{IOB9}$ · LWCR
WCR10	Word Count Register 10	WCR10 = WCR10 FF
WCR10 FF	Word Count Register Bit 10 FF	Clock = $\overline{SWCR} \cdot \overline{WCR0}$ thru $\overline{WCR9}$ Direct Set = IOB10 · LWCR Direct Reset = $\overline{IOB10}$ · LWCR
WCR11	Word Count Register Bit 11	WCR11 = WCR11 FF
WCR11 FF	Word Count Register Bit 11 FF	Clock = $\overline{SWCR} \cdot \overline{WCR0}$ thru $\overline{WCR10}$ Direct Set = IOB11 · LWCR Direct Reset = $\overline{IOB11}$ · LWCR
WCR12	Word Count Register Bit 12	WCR12 = WCR12 FF
WCR12 FF	Word Count Register Bit 12 FF	Clock = $\overline{SWCR} \cdot \overline{WCR0}$ thru $\overline{WCR11}$ Direct Set = IOB12 · LWCR Direct Reset = $\overline{IOB12}$ · LWCR
XMR0	External M-Register Bit 0	XMR0 = XMR0 FF
XMR0 FF	External M-Register Bit 0 FF	Clock = SMAR Direct Set = IOB0 · LMAR Direct Reset = $\overline{IOB0}$ · LMAR
XMR1	External M-Register Bit 1	XMR1 = XMR1 FF
XMR1 FF	External M-Register Bit 1 FF	Clock = SMAR · $\overline{XMR0}$ Direct Set = IOB · LMAR Direct Reset = $\overline{IOB}$ · LMAR
XMR2	External M-Register Bit 2	XMR2 = XMR2 FF
XMR2 FF	External M-Register Bit 2 FF	Clock = SMAR · $\overline{XMR0}$ · $\overline{XMR1}$ Direct Set = IOB2 · LMAR Direct Reset = $\overline{IOB2}$ · LMAR
XMR3	External M-Register Bit 3	XMR3 = XMR3 FF
XMR3 FF	External M-Register Bit 3 FF	Clock = SMAR · $\overline{XMR0}$ thru $\overline{XMR2}$ Direct Set = IOB3 · LMAR Direct Reset = $\overline{IOB3}$ · LMAR
XMR4	External M-Register Bit 4	XMR4 = XMR4 FF

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
XMR4 FF	External M-Register Bit 4 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR3}}$ Direct Set = IOB4 · LMAR Direct Reset = $\overline{\text{IOB4}}$ · LMAR
XMR5	External M-Register Bit 5	XMR5 = XMR5 FF
XMR5 FF	External M-Register Bit 5 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR4}}$ Direct Set = IOB5 · LMAR Direct Reset = $\overline{\text{IOB5}}$ · LMAR
XMR6	External M-Register Bit 6	XMR6 = XMR6 FF
XMR6 FF	External M-Register Bit 6 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR5}}$ Direct Set = IOB6 · LMAR Direct Reset = $\overline{\text{IOB6}}$ · LMAR
XMR7	External M-Register Bit 7	XMR7 = XMR7 FF
XMR7 FF	External M-Register Bit 7 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR6}}$ Direct Set = IOB7 · LMAR Direct Reset = $\overline{\text{IOB7}}$ · LMAR
XMR8	External M-Register Bit 8	XMR8 = XMR8 FF
XMR8 FF	External M-Register Bit 8 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR7}}$ Direct Set = IOB8 · LMAR Direct Reset = $\overline{\text{IOB8}}$ · LMAR
XMR9	External M-Register Bit 9	XMR9 = XMR9 FF
XMR9 FF	External M-Register Bit 9 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR8}}$ Direct Set = IOB9 · LMAR Direct Reset = $\overline{\text{IOB9}}$ · LMAR
XMR10	External M-Register Bit 10	XMR10 = XMR10 FF
XMR10 FF	External M-Register Bit 10 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR9}}$ Direct Set = IOB10 · LMAR Direct Reset = $\overline{\text{IOB10}}$ · LMAR
XMR11	External M-Register Bit 11	XMR11 = XMR11 FF
XMR11 FF	External M-Register Bit 11 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR10}}$ Direct Set = IOB11 · LMAR Direct Reset = $\overline{\text{IOB11}}$ · LMAR
XMR12	External M-Register Bit 12	XMR12 = XMR12 FF
XMR12 FF	External M-Register Bit 12 FF	Clock = SMAR · $\overline{\text{XMR0}}$ thru $\overline{\text{XMR11}}$ Direct Set = IOB12 · LMAR Direct Reset = $\overline{\text{IOB12}}$ · LMAR

Table 4-1. DMA Signals and Equations (Continued)

MNEMONIC	SIGNAL NAME	EQUATION
XPH4	External Phase 4	XPH4 = $\overline{T7} + \overline{UIA\ FF}$
$\overline{XRTS}$	"Not" External Read T to S-Bus	$\overline{XRTS}$ = $\overline{OUT} + \overline{T4T5} + \overline{PH5}$

Table 4-2. Connector Pin Index

PIN	FUNCTION	REF
1	Ground	337
2	Ground	337
3	PRL6	334
4	FLG0	323
5	SFC	010
6	IRQ6	240
7	CLF	013
8	IEN	233
9	STF	006
10	IAK	232
11	XMR2	514
12	SKF	252
13	CRS	234
14	SCM0	228
15	IOG	038
16	SCL2	222
17	POPIO	078
18	XMR1	513
19	XMR0	512
20	IOO	020
21	CLC	014
22	STC	011
23	PRH6	258
24	IOI	019
25	SFS	012
26	XMR3	515
27	XMR5	517
28	XMR4	516
29	XMR6	518
30	XMR7	519
31	XMR8	520
32	XMR11	523
33	XMR10	522
34	SCL6	226
35	IOB0	106
36	XMR9	521
37	SCM1	227
38	IOB1	107
39	+5 volts	335
40	+5 volts	335
41	IOB2	108
42	IOB4	132
43	SRQ16	331

PIN	FUNCTION	REF
44	SRQ12	327
45	IOB3	109
46	ENF	067
47	-2 volts	336
48	-2 volts	336
49	SCL5	225
50	SCL4	224
51	IOB5	133
52	IOB7	135
53	IOB6	134
54	IOB8	156
55	IOB11	159
56	IOB9	157
57	IOB12	178
58	IOB10	158
59	XMR12	524
60	T7	093
61	IOB13	179
62	EDT	526
63	SRQ14	329
64	SRQ11	326
65	IOB14	180
66	SRQ10	325
67	SRQ15	330
68	SRQ13	328
69	$\overline{SWST}$	083
70	IOCO	027
71	SCL3	223
72	PRL4	255
73	ISG	315
74	IOB15	181
75	SCL0	220
76	$\overline{SCL1}$	221
77	$\overline{XPH4}$	310
78	T3T4	097
79	Not used	—
80	T4T5	098
81	PH4	076
82	$\overline{HIS}$	312
83	$\overline{PH5}$	313
84	XRTS	525
85	Ground	338
86	Ground	338

Table 4-3. DMA Card Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR. CODE NO.	MFR. PART NO.
C1 thru C55	0160-2055	C: FXD CER 0.01 UF +80-20% 100 VDCW	91418	TA
MC11,12,15,16,24,74,83,104	1820-0054	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7400N
MC13,14,26, 92	1820-0068	INTEGRATED CIRCUIT: TTL	56289	USN7410A
MC17,21,22,34,36,42,44,47,54, 57,63 thru 67,94, 96,97,107	1820-0956	INTEGRATED CIRCUIT: CTL	07263	SL3459
MC23,105	1820-0141	INTEGRATED CIRCUIT	28480	1820-0141
MC25,101,102	1820-0372	INTEGRATED CIRCUIT: TTL	01295	SN74H11N
MC27	1820-0069	INTEGRATED CIRCUIT: TTL	56289	USN7420A
MC35,46,53,56,62,71,75,91	1820-0233	INTEGRATED CIRCUIT: TTL	01295	SN10625
MC37	1820-0328	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7402N
MC55	1820-0301	INTEGRATED CIRCUIT: QUAD BISTABLE LATCH	01285	SN7475N
MC82,93	1820-0077	INTEGRATED CIRCUIT: "D" EDGE TRANSFER FLIP-FLOP	01295	SN7474N
MC85,103	1820-0132	INTEGRATED CIRCUIT: TTL	07263	U6A901659X
MC86,87	1820-0327	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7401N
MC106	1820-0071	INTEGRATED CIRCUIT: 4-INPUT DR NAND	01295	SN7440N
R1	0683-1015	R: FXD COMP 100 OHM 5% 1/4W	01121	CB 1015
R2,7,9,10,12	0683-4715	R: FXD COMP 470 OHM 5% 1/4W	01121	CB 4715
R3,11	0683-6815	R: FXD COMP 680 OHM 5% 1/4W	01121	CB 6815
R4	0683-3915	R: FXD COMP 390 OHM 5% 1/4W	01121	CB 3915
R5,16,17	0683-3315	R: FXD COMP 330 OHM 5% 1/4W	01121	CB 3315
R6	0683-8215	R: FXD COMP 820 OHM 5% 1/4W	01121	CB 8215
R13,32	0683-2415	R: FXD COMP 240 OHM 5% 1/4W	01121	CB 2415
R18 thru R24	0683-1525	R: FXD COMP 1500 OHM 5% 1/4W	01121	CB 1525
W1	8159-0005	JUMPER WIRE	28480	8159-0005

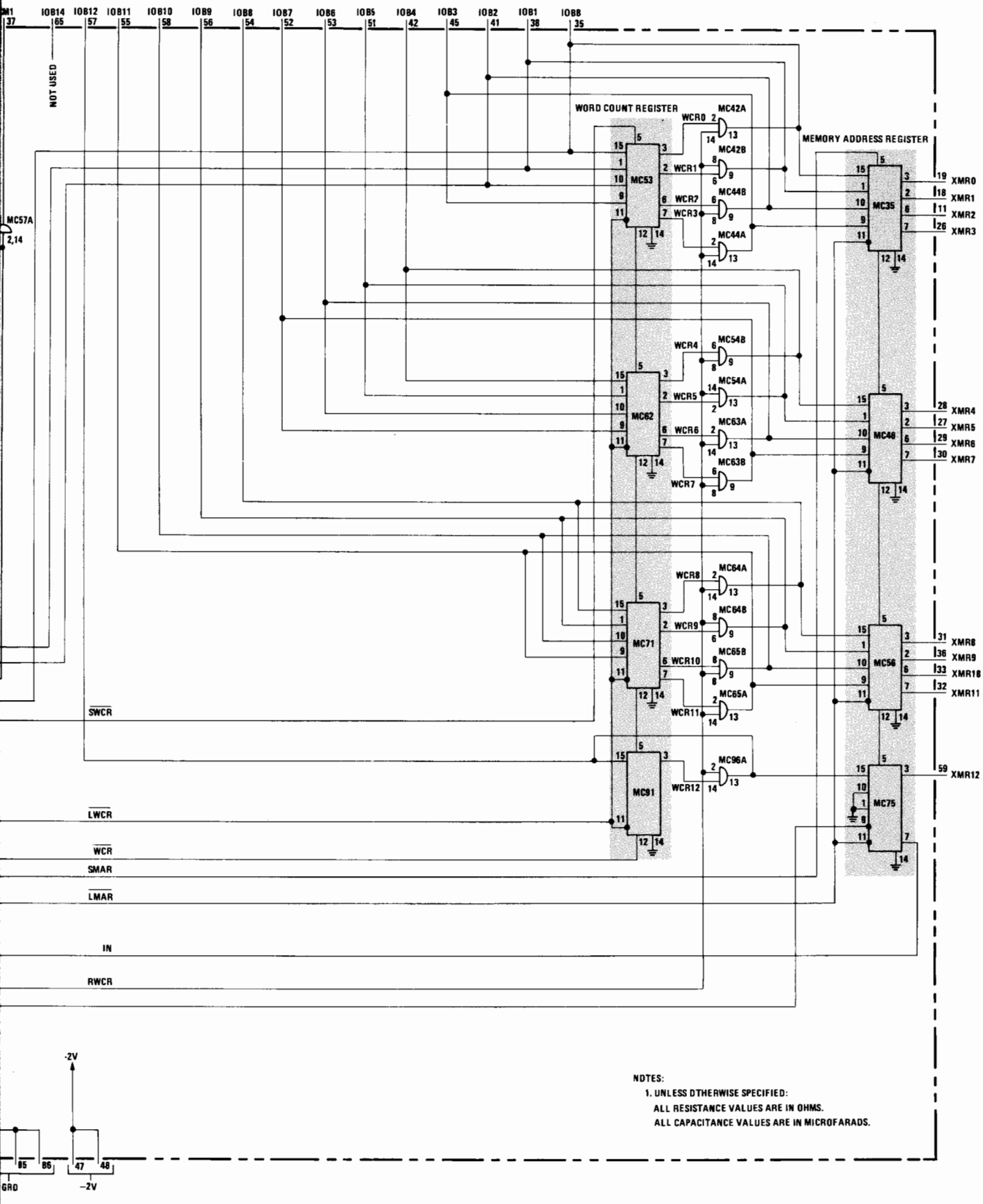
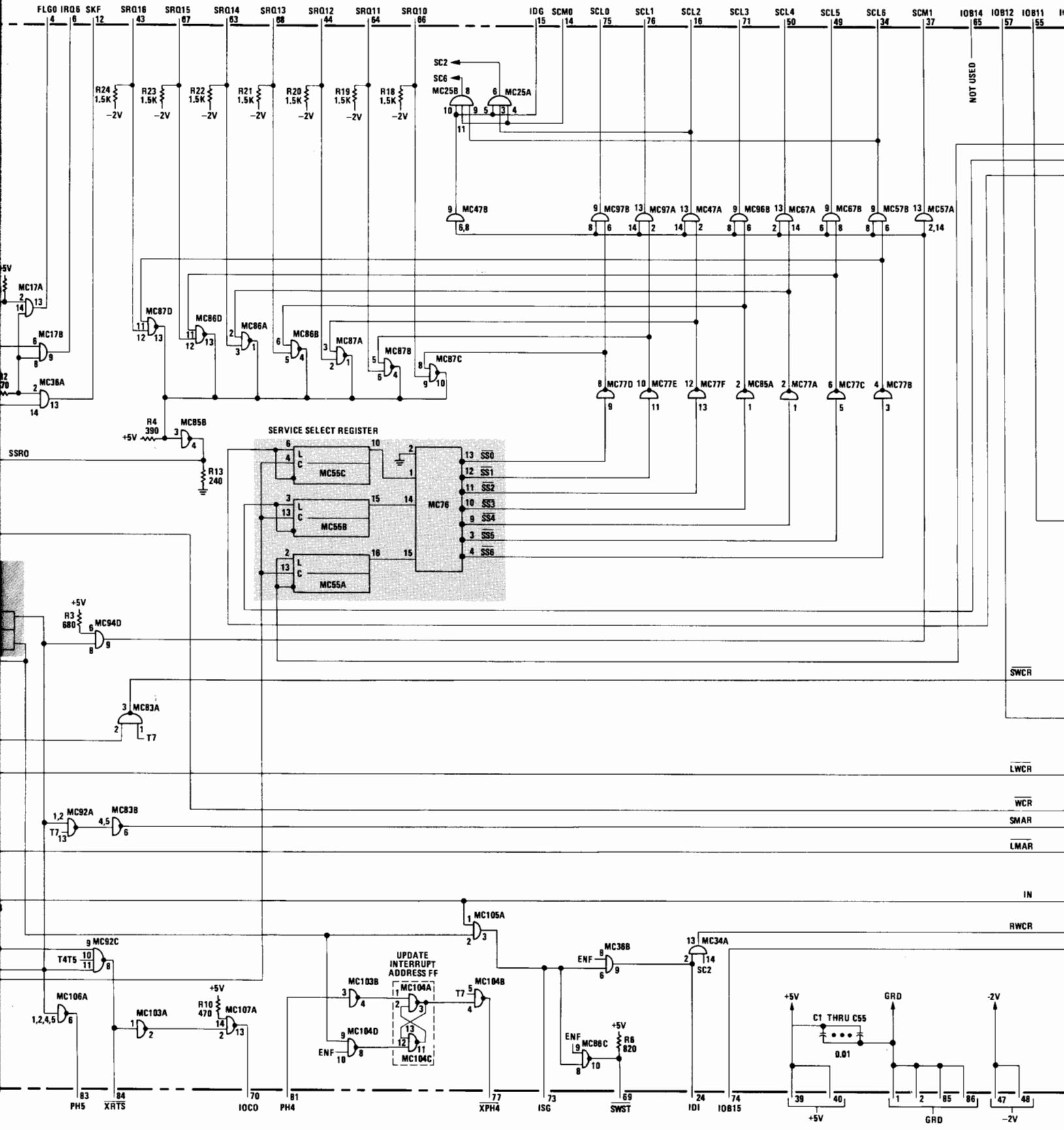
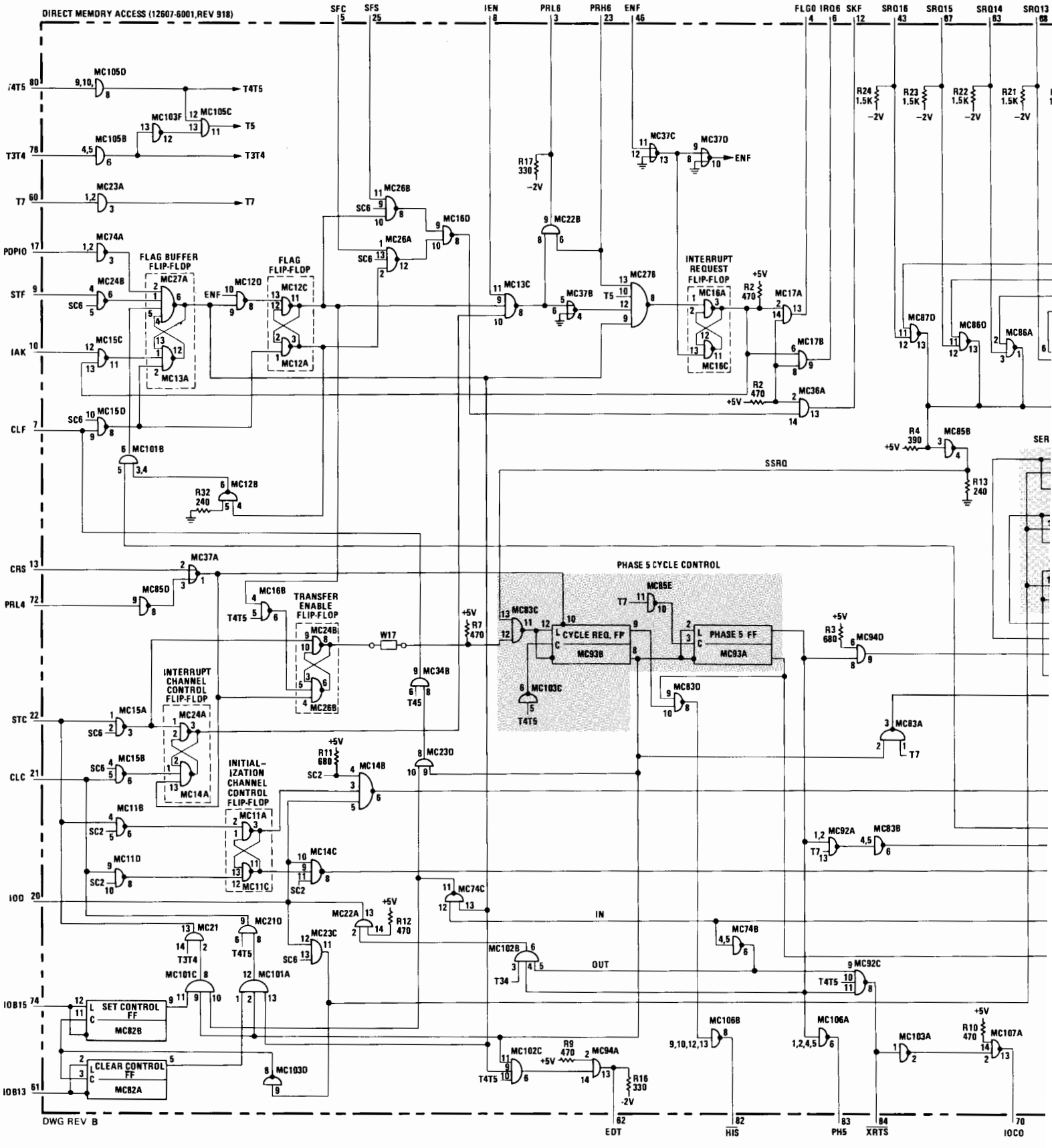
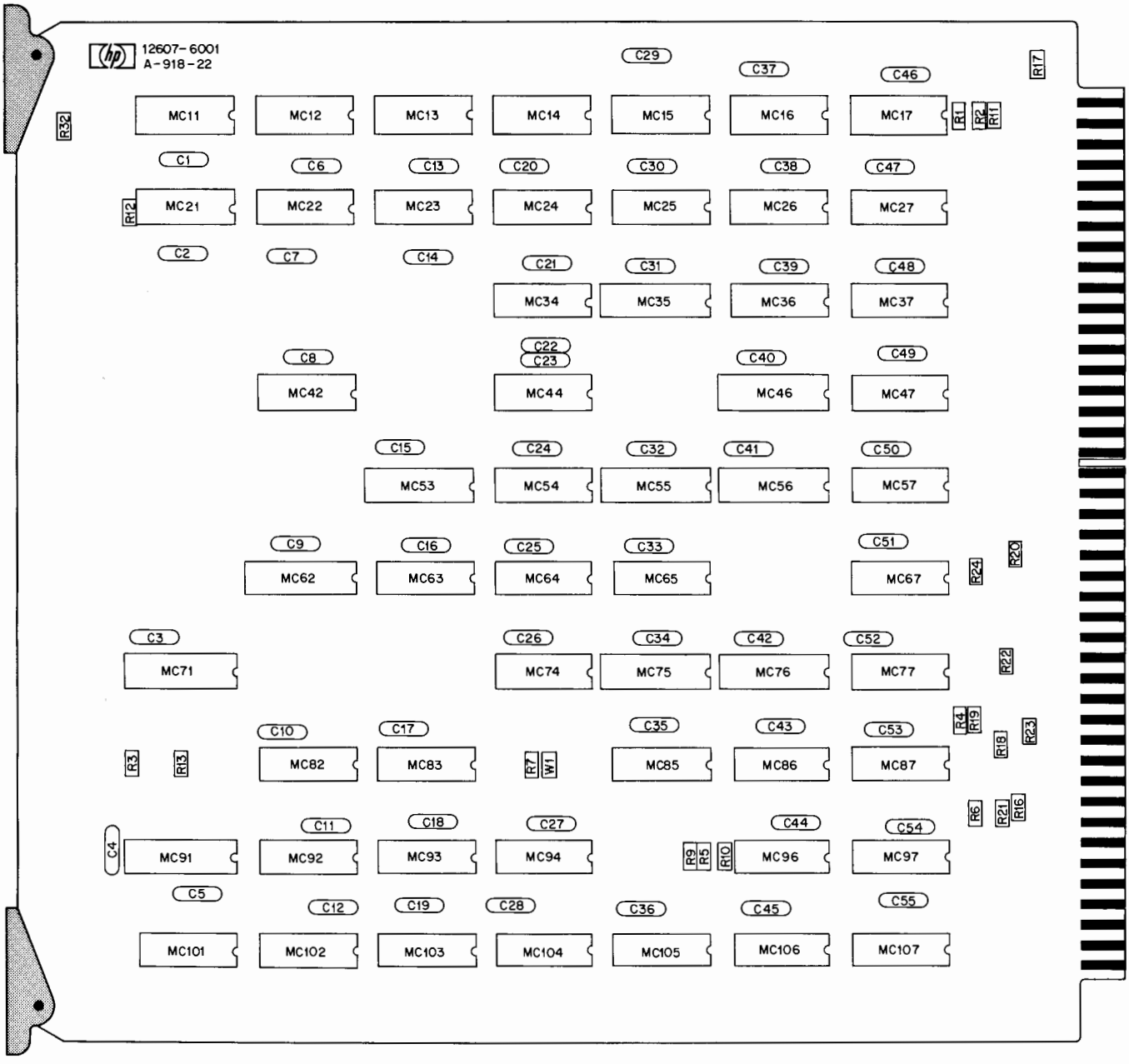


Figure 4-1. DMA Assembly Schematic and Parts Location Diagrams

See Updated Schematic 4-9/4-10


FLG0 IRQ6 SKF SRQ16 SRQ15 SRQ14 SRQ13 SRQ12 SRQ11 SRQ10 IDG SCM0 SCL0 SCL1 SCL2 SCL3 SCL4 SCL5 SCL6 SCM1 IOB14 IOB12 IOB11
NOT USED
SC2
SC6
MC25B
MC25A
R24 1.5K −2V
R23 1.5K −2V
R22 1.5K −2V
R21 1.5K −2V
R20 1.5K −2V
R19 1.5K −2V
R18 1.5K −2V
MC47B
MC97B MC97A MC47A MC96B MC67A MC67B MC57B MC57A
MC17A
MC17B
MC36A
MC87D
MC86D
MC86A
MC86B
MC87A
MC87B
MC87C
MC77D MC77E MC77F MC85A MC77A MC77C MC77B
R4 390
MC85B
SSR0
R13 240
SERVICE SELECT REGISTER
MC55C
MC55B
MC55A
MC76
SS0 SS1 SS2 SS3 SS4 SS5 SS6
R3 680
MC94D
MC83A
T7
SWCR
LWCR
WCR
SMAR
LMAR
IN
RWCR
MC92A
MC83B
MC92C
T4T5
MC106A
MC103A
R10 470
MC107A
MC105A
UPDATE INTERRUPT ADDRESS FF
MC103B
MC104A
MC104B
MC104D
MC104C
MC36B
ENF
MC34A
SC2
MC86C
R6 820
C1 THRU C55
0.01
PH5 XRTS IOCO PH4 XPH4 ISG SWST IDI IOB15
+5V GRD -2V


DIRECT MEMORY ACCESS (12607-6001,REV 918)
SFC
SFS
IEN
PRL6
PRH6
ENF
FLG0
IRQ6
SKF
SRQ16
SRQ15
SRQ14
SRQ13
T4T5
T3T4
T7
PDPIO
STF
IAK
CLF
CRS
PRL4
STC
CLC
IOO
IOB15
IOB13
MC105D
MC105C
MC103F
MC105B
MC23A
MC74A
MC24B
MC15C
MC15D
MC101B
MC12B
MC37A
MC85D
MC16B
MC24B
MC26B
MC26A
MC16D
MC22B
MC37C
MC37D
MC13C
MC37B
MC27B
MC16A
MC16C
MC17A
MC17B
MC36A
MC87D
MC86D
MC86A
MC85B
MC15A
MC24A
MC15B
MC14A
MC11B
MC11A
MC11D
MC11C
MC14B
MC14C
MC23D
MC74C
MC22A
MC21
MC21D
MC23C
MC101C
MC101A
MC82B
MC82A
MC103D
MC102B
MC102C
MC94A
MC74B
MC92C
MC106B
MC106A
MC103A
MC107A
MC83C
MC103C
MC85E
MC93B
MC93A
MC94D
MC83D
MC83A
MC92A
MC83B
FLAG BUFFER FLIP-FLOP
FLAG FLIP-FLOP
INTERRUPT REQUEST FLIP-FLOP
TRANSFER ENABLE FLIP-FLOP
INTERRUPT CHANNEL CONTROL FLIP-FLOP
INITIAL-IZATION CHANNEL CONTROL FLIP-FLOP
SET CONTROL FF
CLEAR CONTROL FF
CYCLE REQ. FF
PHASE 5 FF
PHASE 5 CYCLE CONTROL
SSRQ
IN
OUT
W17
R2 470
R4 390
R7 470
R9 470
R10 470
R11 680
R12 470
R13 240
R21 1.5K
R22 1.5K
R23 1.5K
R24 1.5K
R3 680
R16 330
R17 330
R32 240
-2V
+5V
EDT
HIS
PH5
XRTS
IOCO
DWG REV B



SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the DMA option. Table 5-1 lists parts in alphanumeric order of the HP stock numbers and lists the following information on each part:

a. Description of the part. (Refer to table 5-2 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the DMA option.

5-3. A separate parts list is provided along with the parts location diagram for the DMA card in section IV of this manual. This parts list lists the parts in alphanumeric order of reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.

b. Hewlett-Packard stock number for each part.

c. Description of each part.

d. Circuit reference designation.

Table 5-1. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR	MFR PART NO.	TQ
0160-2055	C:FXD CER 0.01 UF +80-20% 100VDCW	91428	TA	55
0683-1015	R:FXD COMP 100 OHM 5% 1/4W	01121	CB 1015	1
0683-1525	R:FXD COMP 1500 OHM 5% 1/4W	01121	CB 1525	7
0683-2415	R:FXD COMP 240 OHM 5% 1/4W	01121	CB 2415	2
0683-3315	R:FXD COMP 330 OHM 5% 1/4W	01121	CB 3315	3
0683-3915	R:FXD COMP 390 OHM 5% 1/4W	01121	CB 3915	1
0683-4715	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715	5
0683-6815	R:FXD COMP 680 OHM 5% 1/4W	01121	CB 6815	2
0683-8215	R:FXD COMP 820 OHM 5% 1/4W	01121	CB 8215	1
1820-0054	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7400N	8
1820-0068	INTEGRATED CIRCUIT: TTL	56289	USN7410A	4
1820-0069	INTEGRATED CIRCUIT: TTL	56289	USN7420A	1
1820-0071	INTEGRATED CIRCUIT: 4-INPUT DR NAND	01295	SN7440N	1
1820-0077	INTEGRATED CIRCUIT: "D" EDGE TRIGGER F/F	01295	SN7474N	2
1820-0132	INTEGRATED CIRCUIT: TTL	07263	U6A901659X	2
1820-0141	INTEGRATED CIRCUIT	28480	1820-0141	2
1820-0233	INTEGRATED CIRCUIT: TTL	01295	SN10625	8
1820-0301	INTEGRATED CIRCUIT: QUAD BISTABLE LATCH	01295	SN7475N	1
1820-0327	INTEGRATED CIRCUIT: QUAD 2-INPUT NAND	01295	SN7401N	2
1820-0328	INTEGRATED CIRCUIT: QUAD 2-INPUT NOR	01295	SN7402N	1
1820-0372	INTEGRATED CIRCUIT: TTL	01295	SN74H11N	3
1820-0956	INTEGRATED CIRCUIT: CTL	07263	SL3459	18
8159-0005	JUMPER WIRE	28480	8159-0005	1
12607-6001	DIRECT MEMORY ACCESS KIT	28480	12607-6001	1

Table 5-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A = assembly	J = receptacle connector	TB = terminal board
B = motor	K = relay	TP = test point
BT = battery	L = inductor	U = integrated circuit
C = capacitor	M = meter	V = vacuum tube, neon bulb, photocell, etc.
CP = coupler	MC = microcircuit	
CR = diode	P = plug connector	VR = voltage regulator
DL = delay line	Q = transistor	W = cable, jumper
DS = device signaling (lamp)	R = resistor	X = socket
E = misc hardware	RT = thermistor	Y = crystal
F = fuse	S = switch	Z = tuned cavity, network
FL = filter	T = transformer	

ABBREVIATIONS

A = amperes	IMPG = impregnated	P/O = part of
AC = alternating current	IN. = inch, inches	POLY = polystyrene
AFC = automatic frequency control	INCD = incandescent	PORC = porcelain
ALUM = aluminum	INCL = include(s)	POS = position(s)
AL-ELECT = aluminum electrolytic	INS = insulation(ed)	POT = potentiometer
ASSY = assembly	INT = internal	PP = peak-to-peak
	I/O = input/output	PT = point
BFO = beat frequency oscillator		PWV = peak working voltage
BE CU = beryllium copper	K = kilo = 1000	
BH = binder head		R = resistor
BP = bandpass	LH = left hand	RECT = rectifier
BRS = brass	LIN = linear taper	RF = radio frequency
BWO = backward wave oscillator	LK WASH = lock washer	RH = round head or right hand
	LOG = logarithmic taper	RMO = rack mount only
C = capacitor	LPF = low pass filter	RMS = root-mean square
CCW = counterclockwise		RWV = reverse working voltage
CER = ceramic	M = milli = 10^{-3}	
CMO = cabinet mount only	MEG = mega = 10^{6}	S-B = slow-blow
COEF = coefficient	MET FLM = metal film	SCR = screw
COM = common	MET OX = metal oxide	SE = selenium
COMP = composition	MFR = manufacturer	SECT = section(s)
COMPL = complete	MHz = megahertz	SEMICON = semiconductor
CONN = connector	MINAT = miniature	SI = silicon
CP = cadmium plate	MOM = momentary	SIL = silver
CRT = cathode-ray tube	MTG = mounting	SL = slide
CTL = capacitor-transistor logic	MY = Mylar	SPDT = single-pole, double-throw
CW = clockwise		SPG = spring
	N = nano (10^{-9})	SPL = special
DC = direct current	N/C = normally closed	SPST = single-pole, single-throw
DEPC = deposited carbon	NE = neon	SR = split ring
DPDT = double-pole, double-throw	NI PL = nickel plate	SST = stainless steel
DPST = double-pole, single-throw	NO. = number	STL = steel
DR = drive	N/O = normally open	
	NPN = negative-positive-negative	TA = tantalum
ELECT = electrolytic		TD = time delay
ENCAP = encapsulated	NPO = negative positive zero (zero temperature coefficient)	TGL = toggle
EXT = external		THD = thread
	NRFR = not recommended for field replacement	TI = titanium
F = farads		TOL = tolerance
FH = flat head	NSR = not separately replaceable	TRIM = trimmer
FIL H = fillister head		TTL = transistor-transistor logic
FXD = fixed	OBD = order by description	TWT = traveling wave tube
	OD = outer diameter	
G = giga (10^{9})	OH = oval head	U (μ) = micro = 10^{-6}
GE = germanium	OX = oxide	
GL = glass		VAR = variable
GND/GRD = ground(ed)	P = peak	VDCW = direct current working volts
	PC = printed circuit	
H = henries	PF = picofarads = 10^{-12} farads	W/ = with
HDW = hardware	PH = Phillips head	W = watts
HEX = hexagonal	PH BRZ = phosphor bronze	WIV = working inverse voltage
HG = mercury	PHL = Phillips	WW = wirewound
HR = hour(s)	PIV = peak inverse voltage	W/O = without
HZ = hertz	PNP = positive-negative-positive	
ID = inner diameter		
IF = intermediate frequency		

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 (Name to Code) and H4-2 (Code to Name) and their latest supplements. The date of revision and the date of the supplements used appear at the bottom of each page. Alphabetical codes have been arbitrarily assigned to suppliers not appearing in the H4 Handbooks.

Code No.	Manufacturer	Address
00000	U. S. A. Common	Any supplier of U. S.
00136	McCoy Electronics	Mount Holly Springs, Pa.
00213	Sage Electronics Corp.	Rochester, N. Y.
00287	Cemco Inc.	Danielson, Conn.
00334	Humidial	Colton, Calif.
00348	Microtron Co., Inc.	Valley Stream, N. Y.
00373	Garlock Inc.	Cherry Hill, N. J.
00656	Aerovox Corp.	New Bedford, Mass.
00779	Amp. Inc.	Harrisburg, Pa.
00781	Aircraft Radio Corp.	Boonton, N. J.
00815	Northern Engineering Laboratories, Inc.	Burlington, Wis.
00853	Sangamo Electric Co., Pickens Div.	Pickens, S. C.
00866	Goe Engineering Co.	City of Industry, Cal.
00891	Carl E. Holmes Corp.	Los Angeles, Calif.
00929	Microlab Inc.	Livingston, N. J.
01002	General Electric Co., Capacitor Dept.	Hudson Falls, N. Y.
01009	Alden Products Co.	Brockton, Mass.
01121	Allen Bradley Co.	Milwaukee, Wis.
01255	Litton Industries, Inc.	Beverly Hills, Calif.
01281	TRW Semiconductors, Inc.	Lawndale, Calif.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
01349	The Alliance Mfg. Co.	Alliance, Ohio
01589	Pacific Relays, Inc.	Van Nuys, Calif.
01670	Gudebrod Bros. Silk Co.	New York, N. Y.
01930	Amerock Corp.	Rockford, Ill.
01961	Pulse Engineering Co.	Santa Clara, Calif.
02114	Ferroxcube Corp. of America	Saugerties, N. Y.
02116	Wheelock Signals, Inc.	Long Branch, N. J.
02286	Cole Rubber and Plastics Inc.	Sunnyvale, Calif.
02660	Amphenol-Borg Electronics Corp.	Broadview, Ill.
02735	Radio Corp. of America, Semiconductor and Materials Div.	Somerville, N. J.
02771	Vocaline Co. of America, Inc.	Old Saybrook, Conn.
02777	Hopkins Engineering Co.	San Fernando, Calif.
02875	Hudson Tool & Die Co.	Newark, N. J.
03508	G. E. Semiconductor Prod. Dept.	Syracuse, N. Y.
03705	Apex Machine & Tool Co.	Dayton, Ohio
03797	Eldema Corp.	Compton, Calif.
03818	Parker Seal Co.	Los Angeles, Calif.
03877	Transitron Electric Corp.	Wakefield, Mass.
03888	Pyrofilm Resistor Co., Inc.	Cedar Knolls, N. J.
03954	Singer Co., Diehl Div. Finderne Plant	Sumerville, N. J.
04009	Arrow, Hart and Hegeman Elect. Co.	Hartford, Conn.
04013	Taurus Corp.	Lambertville, N. J.
04062	Arco Electronic Inc.	Great Neck, N. Y.
04222	Hi-Q Division of Aerovox	Myrtle Beach, S. C.
04354	Precision Paper Tube Co.	Wheeling, Ill.
04404	Dymec Division of Hewlett-Packard Co.	Palo Alto, Calif.
04651	Sylvania Electric Products, Microwave Device Div.	Mountain View, Calif.
04673	Dakota Engr. Inc.	Culver City, Calif.
04713	Motorola, Inc., Semiconductor Prod. Div.	Phoenix, Arizona
04732	Filtron Co., Inc. Western Div.	Culver City, Calif.
04773	Automatic Electric Co.	Northlake, Ill.
04796	Sequoia Wire Co.	Redwood City, Calif.
04811	Precision Coil Spring Co.	El Monte, Calif.
04870	P. M. Motor Company	Westchester, Ill.
04919	Component Mfg. Service Co.	W. Bridgewater, Mass.
05006	Twentieth Century Plastics, Inc.	Los Angeles, Calif.
05245	Components Corp.	Chicago, Ill.
05277	Westinghouse Electric Corp. Semi-Conductor Dept.	Youngwood, Pa.
05347	Ultronix, Inc.	San Mateo, Calif.
05397	Union Carbide Corp., Elect. Div.	New York, N. Y.
05574	Viking Ind. Inc.	Canoga Park, Calif.
05593	Icore Electro-Plastics Inc.	Sunnyvale, Calif.
05616	Cosmo Plastic (c o Electrical Spec. Co.)	Cleveland, Ohio
05624	Barber Colman Co.	Rockford, Ill.
05728	Tiffen Optical Co.	Roslyn Heights, Long Island, N. Y.
05729	Metro-Tel Corp.	Westbury, N. Y.
05783	Stewart Engineering Co.	Santa Cruz, Calif.
05820	Wakefield Engineering Inc.	Wakefield, Mass.
06004	Bassick Co., Div. of Stewart Warner Corp.	Bridgeport, Conn.
06090	Raychem Corp.	Redwood City, Calif.
06175	Bausch and Lomb Optical Co.	Rochester, N. Y.
06402	E. T. A. Products Co. of America	Chicago, Ill.
06540	Amatom Electronic Hardware Co., Inc.	New Rochelle, N. Y.
06555	Beede Electrical Instrument Co., Inc.	Penacook, N. H.
06666	General Devices Co., Inc.	Indianapolis, Ind.
06751	Components Inc., Ariz. Div.	Phoenix, Ariz.
06812	Torrington Mfg. Co., West Div.	Van Nuys, Calif.
06980	Varian Assoc. Eimac Div.	San Carlos, Calif.
07088	Kelvin Electric Co.	Van Nuys, Calif.
07126	Digitran Co.	Pasadena, Calif.
07137	Transistor Electronics Corp.	Minneapolis, Minn.
07138	Westinghouse Electric Corp. Electronic Tube Div.	Elmira, N. Y.
07149	Fulmohm Corp.	New York, N. Y.
07233	Cinch-Graphik Co.	City of Industry, Calif.
07256	Silicon Transistor Corp.	Carle Place, N. Y.
07261	Avnet Corp.	Culver City, Calif.
07263	Fairchild Camera & Inst. Corp. Semiconductor Div.	Mountain View, Calif.
07322	Minnesota Rubber Co.	Minneapolis, Minn.
07387	Birtcher Corp., The	Monterey Park, Calif.
07397	Sylvania Elect. Prod. Inc., Mt. View Operations	Mountain View, Calif.
07700	Technical Wire Products Inc.	Cranford, N. J.
07829	Bodine Elect. Co.	Chicago, Ill.
07910	Continental Device Corp.	Hawthorne, Calif.
07933	Raytheon Mfg. Co., Semiconductor Div.	Mountain View, Calif.
07980	Hewlett-Packard Co., Boonton Radio Div.	Rockaway, N. J.
08145	U. S. Engineering Co.	Los Angeles, Calif.
08289	Blinn, Delbert Co.	Pomona, Calif.
08358	Burgess Battery Co.	Niagara Falls, Ontario, Canada
08524	Deutsch Fastener Corp.	Los Angeles, Calif.
08664	Bristol Co., The	Waterbury, Conn.
08717	Sloan Company	Sun Valley, Calif.
08718	ITT Cannon Electric Inc., Phoenix Div.	Phoenix, Arizona
08727	National Radio Lab. Inc.	Paramus, N. J.
08792	CBS Electronics Semiconductor Operations, Div of C. B. S. Inc.	Lowell, Mass.
08806	General Electric Co. Miniat. Lamp Dept.	Cleveland, Ohio
08984	Mel-Rain	Indianapolis, Ind.
09026	Babcock Relays Div.	Costa Mesa, Calif.
09134	Texas Capacitor Co.	Houston, Texas
09145	Tech. Ind. Inc. Atohm Elect.	Burbank, Calif.
09250	Electro Assemblies, Inc.	Chicago, Ill.
09353	C & K Components Inc.	Newton, Mass.
09569	Mallory Battery Co. of Canada, Ltd.	Toronto, Ontario, Canada
09922	Burndy Corp.	Norwalk, Conn.
10214	General Transistor Western Corp.	Los Angeles, Calif.
10411	Ti-Tal, Inc.	Berkeley, Calif.
10646	Carborundum Co.	Niagara Falls, N. Y.
11236	CTS of Berne, Inc.	Berne, Ind.
11237	Chicago Telephone of California, Inc.	So. Pasadena, Calif.
11242	Bay State Electronics Corp.	Waltham, Mass.
11312	Teledyne Inc., Microwave Div.	Palo Alto, Calif.
11314	National Seal	Downey, Calif.
11453	Precision Connector Corp.	Jamaica, N. Y.
11534	Duncan Electronics Inc.	Costa Mesa, Calif.
11711	General Instrument Corp., Semiconductor Div., Products Group	Newark, N. J.
11717	Imperial Electronic, Inc.	Buena Park, Calif.
11870	Melabs, Inc.	Palo Alto, Calif.
12040	National Semiconductor	Danbury, Conn.
12136	Philadelphia Handle Co.	Camden, N. J.
12361	Grove Mfg. Co., Inc.	Shady Grove, Pa.
12574	Guiton Ind. Inc. Data System Div.	Albuquerque, N. M.
12697	Clarostat Mfg. Co.	Dover, N. H.
12728	Elmar Filter Corp.	W. Haven, Conn.
12859	Nippon Electric Co., Ltd.	Tokyo, Japan
12881	Metex Electronics Corp.	Clark, N. J.
12930	Delta Semiconductor Inc.	Newport Beach, Calif.
12954	Dickson Electronics Corp.	Scottsdale, Arizona
13103	Thermalloy	Dallas, Texas
13396	Telefunken (GmbH)	Hanover, Germany
13835	Midland-Wright Div. of Pacific Industries, Inc.	Kansas City, Kansas
14099	Sem-Tech	Newbury Park, Calif.
14193	Calif. Resistor Corp.	Santa Monica, Calif.
14298	American Components, Inc.	Conshohocken, Pa.
14433	ITT Semiconductor, A Div. of Int. Telephone & Telegraph Corp.	West Palm Beach, Fla.
14493	Hewlett-Packard Company	Loveland, Colo.
14655	Cornell Dubilier Electric Corp.	Newark, N. J.
14674	Corning Glass Works	Corning, N. Y.
14752	Electro Cube Inc.	San Gabriel, Calif.
14960	Williams Mfg. Co.	San Jose, Calif.
15203	Webster Electronics Co.	New York, N. Y.
15287	Scionics Corp.	Northridge, Calif.
15291	Adjustable Bushing Co.	N. Hollywood, Calif.
15558	Micron Electronics	Garden City, Long Island, N. Y.
15566	Amprobe Inst. Corp.	Lynbrook, N. Y.
15631	Cabletronics	Costa Mesa, Calif.
15772	Twentieth Century Coil Spring Co.	Santa Clara, Calif.
15801	Fenwal Elect. Inc.	Framingham, Mass.
15818	Amelco Inc.	Mt. View, Calif.
16037	Spruce Pine Mica Co.	Spruce Pine, N. C.
16179	Omni-Spectra Inc.	Farmington, Mich.
16352	Computer Diode Corp.	Lodi, N. J.
16585	Boots Aircraft Nut Corp.	Pasadena, Calif.
16688	Ideal Prec. Meter Co., Inc. De Jur Meter Div.	Brooklyn, N. Y.
16758	Delco Radio Div. of G. M. Corp.	Kokoma, Ind.
17109	Thermonetics Inc.	Canoga Park, Calif.
17474	Tranex Company	Mountain View, Calif.
17554	Components Inc.	Biddeford, Ma.
17675	Hamlin Metal Products Corp.	Akron, Ohio
17745	Angstrohm Prec. Inc.	No. Hollywood, Calif.

Table 5-3. Code List of Manufacturers (Continued)

Code No.	Manufacturer	Address
17870	McGraw-Edison Co.	Manchester, N.H.
18042	Power Design Pacific Inc.	Palo Alto, Calif.
18083	Clevite Corp., Semiconductor Div.	Palo Alto, Calif.
18324	Signetics Corp.	Sunnyvale, Calif.
18476	Ty-Car Mfg. Co., Inc.	Holliston, Mass.
18486	TRW Elect. Comp. Div.	Des Plaines, Ill.
18583	Curtis Instrument, Inc.	Mt. Kisco, N.Y.
18612	Vishay Instruments Inc.	Malvern, Pa.
18873	E.I. DuPont and Co., Inc.	Wilmington, Del.
18911	Durant Mfg. Co.	Milwaukee, Wis.
19315	The Bendix Corp., Navigation & Control Div.	Teterboro, N.J.
19500	Thomas A. Edison Industries, Div. of McGraw-Edison Co.	West Orange, N.J.
19589	Concoa	Baldwin Park, Calif.
19644	LRC Electronics	Horseheads, N.Y.
19701	Electra Mfg. Co.	Independence, Kansas
20183	General Atronics Corp.	Philadelphia, Pa.
21226	Executone, Inc.	Long Island City, N.Y.
21335	Fafnir Bearing Co., The	New Britain, Conn.
21520	Fansteel Metallurgical Corp.	N. Chicago, Ill.
23042	Texscan Corp.	Indianapolis, Ind.
23783	British Radio Electronics Ltd.	Washington, D.C.
24455	G.E. Lamp Division	Nela Park, Cleveland, Ohio
24655	General Radio Co.	West Concord, Mass.
24681	Memcor Inc., Comp. Div.	Huntington, Ind.
24796	Parelco Inc.	San Juan Capistrano, Calif.
26365	Gries Reproducer Corp.	New Rochelle, N.Y.
26462	Grobet File Co. of America, Inc.	Carlstadt, N.J.
26851	Compac Hollister Co.	Hollister, Calif.
26992	Hamilton Watch Co.	Lancaster, Pa.
27251	Specialities Mfg. Co., Inc.	Stratford, Conn.
28480	Hewlett-Packard Co.	Palo Alto, Calif.
28520	Heyman Mfg. Co.	Kenilworth, N.J.
30817	Instrument Specialties Co., Inc.	Little Falls, N.J.
33173	G.E. Receiving Tube Dept.	Owensboro, Ky.
35434	Lectrohm Inc.	Chicago, Ill.
36196	Stanwyck Coil Products Ltd.	Hawkesbury, Ontario, Canada
36287	Cunningham, W.H. & Hill, Ltd.	Toronto Ontario, Canada
37942	P.R. Mallory & Co. Inc.	Indianapolis, Ind.
39543	Mechanical Industries Prod. Co.	Akron, Ohio
40920	Miniature Precision Bearings, Inc.	Keene, N.H.
42190	Muter Co.	Chicago, Ill.
43990	C.A. Norgren Co.	Englewood, Colo.
44655	Ohmite Mfg. Co.	Skokie, Ill.
46384	Penn Eng. & Mfg. Corp.	Doylestown, Pa.
47904	Polaroid Corp.	Cambridge, Mass.
48620	Precision Thermometer & Inst. Co.	Southampton, Pa.
49956	Microwave & Power Tube Div.	Waltham, Mass.
52090	Rowan Controller Co.	Westminster, Md.
52983	Sanborn Company	Waltham, Mass.
54294	Shallcross Mfg. Co.	Selma, N.C.
55026	Simpson Electric Co.	Chicago, Ill.
55933	Sonotone Corp.	Elmsford, N.Y.
55938	Raytheon Co. Commercial Apparatus & Systems Div.	So. Norwalk, Conn.
56137	Spaulding Fibre Co., Inc.	Tonawanda, N.Y.
56289	Sprague Electric Co.	North Adams, Mass.
59446	Telex Corp.	Tulsa, Okla.
59730	Thomas & Betts Co.	Elizabeth, N.J.
60741	Triplett Electrical Inst. Co.	Bluffton, Ohio
61775	Union Switch and Signal, Div. of Westinghouse Air Brake Co.	Pittsburgh, Pa.
62119	Universal Electric Co.	Owosso, Mich.
63743	Ward-Leonard Electric Co.	Mt. Vernon, N.Y.
64959	Western Electric Co., Inc.	New York, N.Y.
65092	Weston Inst. Inc. Weston-Newark	Newark, N.J.
66295	Wittek Mfg. Co.	Chicago, Ill.
66346	Minnesota Mining & Mfg. Co. Revere Mincom Div.	St. Paul, Minn.
70276	Allen Mfg. Co.	Hartford, Conn.
70309	Allied Control	New York, N.Y.
70318	Allmetal Screw Product Co., Inc.	Garden City, N.Y.
70417	Amplex, Div. of Chrysler Corp.	Detroit, Mich.
70485	Atlantic India Rubber Works, Inc.	Chicago, Ill.
70563	Amperite Co., Inc.	Union City, N.J.
70674	ADC Products Inc.	Minneapolis, Minn.
70903	Belden Mfg. Co.	Chicago, Ill.
70998	Bird Electronic Corp.	Cleveland, Ohio
71002	Birnbach Radio Co.	New York, N.Y.
71034	Blitey Electric Co., Inc.	Erie, Pa.
71041	Boston Gear Works Div. of Murray Co. of Texas	Quincy, Mass.
71218	Bud Radio, Inc.	Willoughby, Ohio
71279	Cambridge Thermionics Corp.	Cambridge, Mass.
71286	Camloc Fastener Corp.	Paramus, N.J.
71313	Cardwell Condenser Corp.	Lindenhurst L.I., N.Y.
71400	Bussmann Mfg. Div. of McGraw-Edison Co.	St. Louis, Mo.
71436	Chicago Condenser Corp.	Chicago, Ill.
71447	Calif. Spring Co., Inc.	Pico-Rivera, Calif.
71450	CTS Corp.	Elkhart, Ind.
71468	ITT Cannon Electric Inc.	Los Angeles, Calif.
71471	Cinema, Div. Aerovox Corp.	Burbank, Calif.
71482	C.P. Clare & Co.	Chicago, Ill.
71590	Centralab Div. of Globe Union Inc.	Milwaukee, Wis.
71616	Commercial Plastics Co.	Chicago, Ill.
71700	Cornish Wire Co., The	New York, N.Y.
71707	Coto Coil Co., Inc.	Providence, R.I.
71744	Chicago Miniature Lamp Works	Chicago, Ill.
71785	Cinch Mfg. Co., Howard B. Jones Div.	Chicago, Ill.
71984	Dow Corning Corp.	Midland, Mich.
72136	Electro Motive Mfg. Co., Inc.	Willimantic, Conn.
72619	Dialight Corp.	Brooklyn, N.Y.
72656	Indiana General Corp., Electronics Div.	Keasby, N.J.
72699	General Instrument Corp., Cap. Div.	Newark, N.J.
72765	Drake Mfg. Co.	Harwood Heights, Ill.
72825	Hugh H. Eby Inc.	Philadelphia, Pa.
72928	Gudeman Co.	Chicago, Ill.
72962	Elastic Stop Nut Corp.	Union, N.J.
72964	Robert M. Hadley Co.	Los Angeles, Calif.
72982	Erie Technological Products, Inc.	Erie, Pa.
73061	Hansen Mfg. Co., Inc.	Princeton, Ind.
73076	H.M. Harper Co.	Chicago, Ill.
73138	Helipot Div. of Beckman Inst., Inc.	Fullerton, Calif.
73293	Hughes Products Division of Hughes Aircraft Co.	Newport Beach, Calif.
73445	Amperex Elect Co.	Hicksville, L.I., N.Y.
73506	Bradley Semiconductor Corp.	New Haven, Conn.
73559	Carling Electric, Inc.	Hartford, Conn.
73586	Circle F Mfg. Co.	Trenton, N.J.
73682	George K. Garrett Co., Div. MSL Industries Inc.	Philadelphia, Pa.
73734	Federal Screw Products Inc.	Chicago, Ill.
73743	Fischer Special Mfg. Co.	Cincinnati, Ohio
73793	General Industries Co., The	Elyria, Ohio
73846	Goshen Stamping & Tool Co.	Goshen, Ind.
73899	JFD Electronics Corp.	Brooklyn, N.Y.
73905	Jennings Radio Mfg. Corp.	San Jose, Calif.
73957	Groov-Pin Corp.	Ridgefield, N.J.
74276	Signalite Inc.	Neptune, N.J.
74455	J.H. Winns, and Sons	Winchester, Mass.
74861	Industrial Condenser Corp.	Chicago, Ill.
74868	R.F. Products Division of Amphenol-Borg Electronics Corp.	Danbury, Conn.
74970	E.F. Johnson Co.	Waseca, Minn.
75042	International Resistance Co.	Philadelphia, Pa.
75263	Keystone Carbon Co., Inc.	St. Marys, Pa.
75378	CTS Knights Inc.	Sandwich, Ill.
75382	Kulka Electric Corporation	Mt. Vernon, N.Y.
75818	Lenz Electric Mfg. Co.	Chicago, Ill.
75915	Littlefuse, Inc.	Des Plaines, Ill.
76005	Lord Mfg. Co.	Erie, Pa.
76210	C.W. Marwedel	San Francisco, Calif.
76433	General Instrument Corp., Micamold Division	Newark, N.J.
76487	James Millen Mfg. Co., Inc.	Malden, Mass.
76493	J.W. Miller Co.	Los Angeles, Calif.
76530	Cinch-Monadnock, Div. of United Carr Fastener Corp.	San Leandro, Calif.
76545	Mueller Electric Co.	Cleveland, Ohio
76703	National Union	Newark, N.J.
76854	Oak Manufacturing Co.	Crystal Lake, Ill.
77068	The Bendix Corp., Electrodynamics Div.	N. Hollywood, Calif.
77075	Pacific Metals Co.	San Francisco, Calif.
77221	Phanostran Instrument and Electronic Co.	South Pasadena, Calif.
77252	Philadelphia Steel and Wire Corp.	Philadelphia, Pa.
77342	American Machine & Foundry Co. Potter & Brumfield Div.	Princeton, Ind.
77630	TRW Electronic Components Div.	Camden, N.J.
77638	General Instrument Corp., Rectifier Div.	Brooklyn, N.Y.
77764	Resistance Products Co.	Harrisburg, Pa.
77969	Rubbercraft Corp. of Calif.	Torrance, Calif.
78189	Shakeproof Division of Illinois Tool Works	Elgin, Ill.
78277	Sigma	So. Braintree, Mass.
78283	Signal Indicator Corp.	New York, N.Y.
78290	Struthers-Dunn Inc.	Pitman, N.J.
78424	Speciality Leather Prod. Co.	Newark, N.J.
78452	Thompson-Bremer & Co.	Chicago, Ill.
78471	Tilley Mfg. Co.	San Francisco, Calif.
78488	Stackpole Carbon Co.	St. Marys, Pa.
78493	Standard Thomson Corp.	Waltham, Mass.
78553	Tinnerman Products, Inc.	Cleveland, Ohio
78790	Transformer Engineers	San Gabriel, Calif.
78947	Ucinite Co.	Newtonville, Mass.
79136	Waldes Kohinoor Inc.	Long Island City, N.Y.
79142	Veeder Root, Inc.	Hartford, Conn.
79251	Wenco Mfg. Co.	Chicago, Ill.
79727	Continental-Wirt Electronics Corp.	Philadelphia, Pa.
79963	Zierick Mfg. Corp.	New Rochelle, N.Y.
80031	Mepco Division of Sessions Clock Co.	Morristown, N.J.
80120	Schnitzer Alloy Products Co.	Elizabeth, N.J.
80131	Electronic Industries Association. Any brand Tube meeting EIA Standards-Washington, DC.	
80207	Unimax Switch, Div. Maxon Electronics Corp.	Wallingford, Conn.
80223	United Transformer Corp.	New York, N.Y.
80248	Oxford Electric Corp.	Chicago, Ill.
80294	Bourns Inc.	Riverside, Calif.
80411	Acro Div. of Robertshaw Controls Co.	Columbus, Ohio

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DIAGNOSTIC PROGRAM

12607A DIRECT MEMORY ACCESS

(HP 2114B COMPUTER)

MS-1. INTRODUCTION

MS-2. The diagnostic programs for the 12607A Direct Memory Access Option of the HP 2114B Computer consist of two programs:

a. 2114B DMA General Diagnostic
b. 2114B DMA Rate and Transfer Diagnostic

MS-3. The first test confirms the DMA's ability to transfer data accurately from all memory locations, clear and set various peripheral device control bits and perform input/output functions related to Direct Memory Access.

MS-4. The second test establishes the accuracy of DMA data transfer and verifies the DMA function which holds the computer in the 'Execute' phase while data is input to memory (cycle stealing).

MS-5. 2114B DMA GENERAL DIAGNOSTIC

MS-6. HARDWARE CONFIGURATION

MS-7. This program is written for a 2114B computer (4K or 8K memory) with a buffered teleprinter (Model 12531B) and/or a micro-circuit register (MCR) with all other I/O cards removed. The diagnostic package will operate with an MCR or with a teleprinter. If a teleprinter is not used, certain tests are modified or omitted which lead to incomplete testing of the DMA option. The program itself will abort if one of two output devices is not included as part of the hardware setup.

MS-8. The ideal hardware configuration includes both a teleprinter to report errors and program status and MCR to aid in transferring data to and from the computer. In this mode, system input/output (SIO) is configured on the teleprinter channel and the diagnostics are run on the remaining channels. As each channel is checked, the MCR must be moved to a new channel until the teleprinter channel is the only one remaining to be tested. At this point the teleprinter must be configured with the SIO on a different channel (any channel may be used) in order to test the remaining channel.

MS-9. Without an MCR, each channel (10-16) must be configured with the SIO and checked using the teleprinter. Data transfers must be confirmed by using the paper tape punch/reader. (See MS-14. OPERATING PROCEDURES.)

MS-10. FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

MS-11. In order to tailor the diagnostic to his particular needs, the operator may specify several options for program execution by means of the switch register (as shown in table MS-1).

Table MS-1. Switch Register Characteristics

SWITCH REGISTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SWITCH	FUNCTION
0-5	Select code for the I/O channel containing the MCR (or the teleprinter if no MCR is available).
6	Set if no teleprinter is available. Clear if teleprinter is available.
7	Set if no MCR is available. Clear if MCR is available.
8-9	Spares
10	Set if error halts are to be omitted.
11	If set, each diagnostic test runs and halts (with the appropriate message on the teleprinter). This allows the operator to continue to the next test or repeat the current test by setting bit 14.
12	If set, bit 12 of the switch register turns on or off after each cycle through the complete diagnostic. This indicates that the program has not looped-up and that the tests are being executed.
13	If set, all type-out is suppressed. If cleared, type-out continues.
14	If set, the current test recycles instead of advancing to the next test within the diagnostic. If clear, the program automatically advances to the next test within the diagnostic.
15	If set, program recycles the entire diagnostic and omits the PRESET test. If clear, the program halts with the appropriate message on the teleprinter for the PRESET test and halts at the end of the diagnostic itself. If no MCR is available, setting bit 15 omits the memory address register test and the input/output data transfer tests.

MS-12. PROGRAM ORGANIZATION

MS-13. Figure MS-1 is a macro flow chart of the diagnostic subroutines and their execution. Each diagnostic subroutine will be described briefly.

SUBROUTINE	FUNCTION
T.BIO	Confirms the ability to set, clear and test the DMA flag and the DMA interrupt capability. This section includes the PRESET Test.
T.WC	Tests the ability of the DMA to set and read the word count register for all numbers.
T.WCR	Tests the word count increment function (rollover) by setting the word count to minus one and forcing a data transfer which should cause the DMA to interrupt.
T.AR	Tests the memory address register by making a DMA output transfer from every location in memory.
T.STC	Tests the DMA function which sets a device control bit when the STC (set control) decision flip-flop is set.
T.CLC	Tests the DMA function which clears a device control bit when the CLC (clear control) decision flip-flop is set.
T.DTO	Tests the DMA data output capability with all possible data patterns.
T.DTI	Tests the DMA data input capability with the same data patterns used in the T.DTO test.
T.DIO	Tests the DMA input/output block transfer capability via the teleprinter punch.

MS-14. OPERATING PROCEDURES

MS-15. The 2114B DMA General Diagnostic is run according to the following instructions:

a. If an MCR is to be used, insert MCR board no. 12566A-M1 or 12566A-M2 into the I/O channel assigned to the DMA (10-16). The MCRs should have the following jumpers:

W1 - B W3 - A W5 - IN W7 - IN
W2 - A W4 - B W6 - IN W8 - IN

b. If a 16-bit Duplex Register (12554A or 12554A-01) replaces the MCR Register, the Register should have the following jumpers:

W1 - IN W3 - IN W5 - A W7 - A
W2 - IN W4 - A W6 - B

c. If any of the four boards listed above are used, they must be interconnected on the 48-pin edge as follows:

A - 1	P - 13
B - 2	R - 14
C - 3	S - 15
D - 4	T - 16
E - 5	U - 17
F - 6	V - 18
H - 7	W - 19
J - 8	X - 20
K - 9	Y - 21
L - 10	Z - AA - 22 - 23
M - 11	BB - 24
N - 12	

Use the 24-pin edge connector 1251-0332 with pin 22 shorted to pin 23. All I/O channels preceding the MCR require either cards or a priority jumper.

d. After the hardware is ready, follow the steps listed below:

1. Load the DMA diagnostic program using the Basic Binary Loader.
2. Load Address 000100_8.
3. Set the switch register bits 0-5 to the select code of the I/O channel containing the MCR. If the MCR is not available, set bits 0-5 to the I/O channel select code of the teleprinter.
4. If the teleprinter is not available, set switch register bit 6.
5. If the MCR or Duplex Register is not available, set switch register bit 7.
6. Refer to table MS-1 and enter any other options desired by means of the switch register.
7. Press RUN.

e. If the teleprinter is being used, a mssage will be typed when the program has advanced to the PRESET test.

1. Press PRESET.
2. Press RUN.

f. If the MCR is the sole output device and the computer halts with 102011 in the T-Register:

1. Press PRESET.
2. Press RUN.

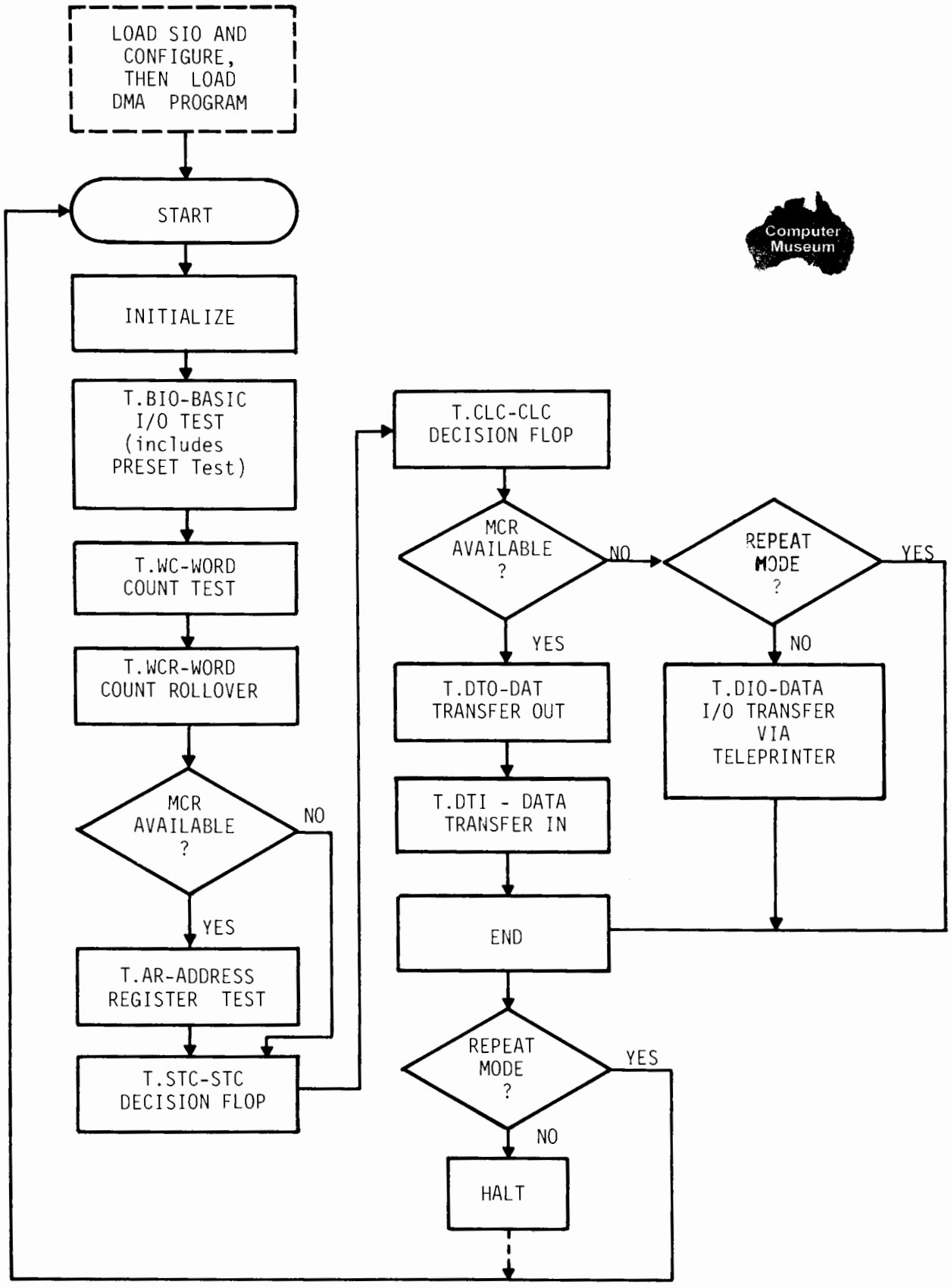

Figure MS-1. HP 2114B DMA General Diagnostic Flowchart

g. An appropriate message indicating the end of the diagnostic will be printed on the teleprinter if it is part of the hardware setup.

h. If an MCR is not used, the teleprinter will type a message, punch a tape and halt. The operator must load the tape reader with the tape punched by the teleprinter and push RUN. The program will read the tape and continue the test.

Note that the continuous feature (bit 15 of the switch register set) will omit this test.

i. If any error halts occur during this program, consult paragraph MS-16.

MS-16. ERROR ANALYSIS SECTION

MS-17. Whenever an error occurs during the execution of the diagnostic program, the computer halts with a coded message in the T-Register. If the teleprinter is included in the hardware configuration, appropriate messages prefixed with an error number (i.e., E12) are typed. Whenever the computer halts, the operator should consult table MS-2 for interpretation. All errors and program status messages are listed opposite the T-Register code and error number.

MS-18. 2114B DMA RATE AND TRANSFER DIAGNOSTIC

MS-19. HARDWARE CONFIGURATION

MS-20. The DMA Rate and Transfer Diagnostic Test requires a 2114B computer (4K or 8K memory) with certain hardware modifications. On the DMA card are four pins: T1, T2, T3, and T4. To run the rate test, T1 should be connected to T2, and T3 should be connected to T4.GND Neither a teleprinter nor a micro-circuit register is required to run the diagnostic.

MS-21. FUNCTIONAL AND OPERATIONAL CHARACTERISTICS

MS-22. The DMA Rate and Transfer Test verifies that the DMA steals every cycle and transfers data to all of memory. If any errors occur, the program will halt with a coded error message in the T-Register. Each time the program recycles completely, the extend register (which consists of one bit) will blink on or off (complement itself) to indicate that the program is not looping up. There are no options available for this program, and the test, once started, will continue to recycle until either an error condition or the operator halts the program.

MS-23. PROGRAM ORGANIZATION

MS-24. Figure MS-2 is a macro flow chart of the 2114B DMA Rate Test. The program consists primarily of one major test. The operator has no control over any particular section of the program.

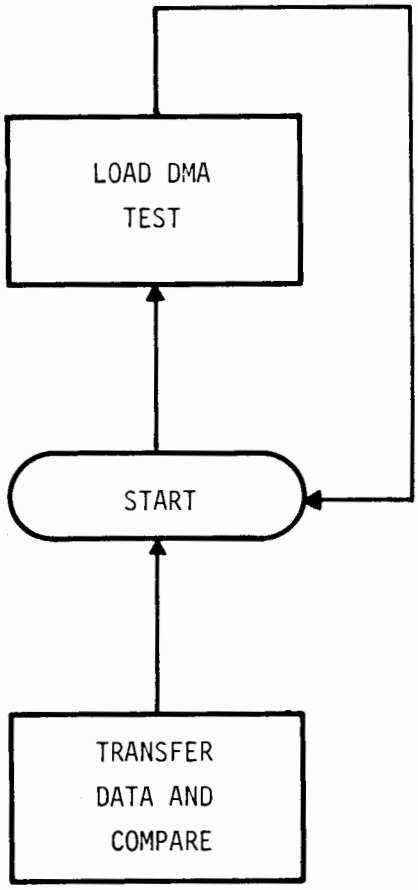

Figure MS-2. DMA Rate and Transfer Test Flowchart

MS-25. OPERATING INSTRUCTIONS

a. Turn computer power OFF.

b. Remove the DMA board (slot A16) and short pin T1 to T2, and pin T3 to T4.GND.

c. Reinsert the DMA board into slot A16, and turn on the computer power.

d. Load the DMA Rate Test using the Basic Binary Loader.

e. Load Address 000002_8.

f. Press PRESET.

g. Press RUN.

MS-26. The Rate Test should run continuously until an error is detected. After each successful cycle of the test, the E-Register will complement. If an error does occur, the appropriate message will be given in the T-Register. Table MS-3 explains the T-Register error messages.

Table MS-2. DMA General Diagnostic Test Errors and Messages

T-REGISTER	ERROR NO.	MESSAGE	COMMENTS
1060XX	(none)	(none)	Trap cell interrupt. P = memory address when interrupted, XX = the trap cell location.
102001	E1	(none)	The diagnostic must have a teleprinter and/or a MCR for a minimum hardware configuration (test aborted).
102002	E2	E2. CLF DID NOT CLEAR FLAG, OR SFS CAUSED SKIP WITH FLAG CLEAR.	Test the ability to clear the DMA flag and test the SFS instruction.
102003	E3	E3. SFC DID NOT SKIP WITH FLAG CLEAR.	Test the ability of the SFC instruction.
102004	E4	E4. STF DID NOT SET FLAG, OR SFC CAUSED SKIP WITH SET.	Test the ability to set the DMA flag and test the SFC instruction.
102005	E5	E5. SFS DID NOT SKIP WITH FLAG SET.	Test the ability of the SFS instruction.
102006	E6	E6. DID NOT INTERRUPT.	Test the DMA interrupt capability.
102007	E7	E7. THE RETURN ADDRESS (STORED IN A REG.) IS NOT CORRECT.	Test the return address that was placed in the DMA trap cell.
102010	E10	E10. CENTRAL INTERRUPT FUNCTION FAILED.	Test the central interrupt register for an indication that the DMA interrupted.
102011	E11	E11. PRESS PRESET. THEN PRESS RUN.	Checks that the PRESET switch will set the DMA flag. This is not an error.
102012	E12	E12. PRESET DID NOT SET THE DMA FLAG.	The test failed.
102013	(none)	END T.BIO	Select options and press RUN.
102020	E20	E20. WORD COUNT READBACK FROM DMA NOT THE SAME AS OUTPUT WORD. WORD COUNT IS XXXXX AND SHOULD BE XXXXX.	Tests the ability to set and read the word count register.
102021	(none)	(none)	Same message as 20 (with no teleprinter). Switch register contains the word which was output. Press RUN to display the word read back.
102022	(none)	(none)	Switch register contains the word read back from the DMA. Press RUN to continue test.
102023	(none)	END T.WC	Select options and press RUN.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

T-REGISTER	ERROR NO.	MESSAGE	COMMENTS
102025	E25	E25. DMA TRANSFER SHOULD BE FINISHED.	Checks the word count rollover by setting the word count to minus one and forcing a transfer. This should cause the DMA to interrupt before reaching this halt.
102026	E26	E26. DMA WORD COUNT ROLL-OVER IS XXXXXX AND SHOULD BE 000000.	Same test as E25. The DMA word count roll-over should be zero.
102027	E27	E27. DMA DID NOT INTERRUPT FROM THE CORRECT PLACE. INTERRUPT LOCATION IS XXXXX AND SHOULD BE XXXXX.	Same test as E25, E26. DMA is not interrupting from the correct location.
102030	(none)	(none)	Same message as E27 (with no teleprinter). Switch register contains the expected interrupt location. Press RUN to display the actual interrupt location.
102031	(none)	(none)	Switch register contains the actual interrupt location. Press RUN to continue test.
102032	(none)	END T.WCR	Select options and press RUN.
102035	E35	E35. DMA FLAG SHOULD BE SET.	Tests the memory address register by making a DMA output transfer from every available location in memory. The DMA flag is not set after the data transfer.
102036	E36	E36. WORD READ FROM MICRO-CIRCUIT REGISTER NOT CORRECT WORD IS XXXXXX AND SHOULD BE XXXXXX AND MEM. ADD IS XXXXXX.	Same test as E35 except that the data read is not the same as the data sent. This indicates that the data transfer may be bad or that the DMA is not transferring data from every memory location.
102037	(none)	(none)	Same message as E36 (with no teleprinter). Switch register contains the expected output word. Press RUN to display the word read from the MCR.
102040	(none)	(none)	Switch register contains the MCR. Press RUN to display the memory address.
102041	(none)	(none)	Switch register contains the memory address from which the transfer was executed. Press RUN to continue the test.
102042	(none)	END T.AR	Select options and press RUN.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

T-REGISTER	ERROR NO.	MESSAGE	COMMENTS
102043	E43	E43. DEVICE CONTROL BIT NOT SET BY DMA WHEN STC DECISION FLOP SET.	Tests the STC decision flip-flop. The DMA should set the device control bit when the STC decision flip-flop is set.
102044	E44	E44. DEVICE CONTROL BIT SET BY DMA WHEN STC DECISION FLOP CLEAR.	Tests the STC decision flip-flop. The DMA should not set the device control bit when the STC decision flip-flop is clear.
102045	(none)	END T.STC	Select options and press RUN.
102046	E46	E46. DEVICE CONTROL BIT NOT CLEARED BY DMA AT END OF BLOCK TRANSFER WHEN CLC DECISION FLOP SET.	Tests the CLC decision flip-flop. The DMA should clear the device control bit during the last transfer of a block when the CLC decision flip-flop is set.
102047	E47	E47. DEVICE CONTROL BIT CLEARED BY DMA WHEN CLC DECISION FLOP CLEAR.	Test the CLC decision flip-flop. The DMA should not clear the device control bit when the CLC decision flip-flop is clear. The DATA pattern (1Ø67ØXX) output may have caused the device control to be cleared on ring phase 5. The A14 assembly (shift logic card) must be 02114-6003 version B or later.
102050	(none)	END T.CLC	Select option and press RUN.
102051	E51	E51. DMA FLAG SHOULD BE SET.	Test all possible patterns in the DMA data output capability. The DMA flag is not set after data transfer.
102052	E52	E52. DATA PATTERN READ BACK FROM MCR NOT THE SAME AS THAT OUTPUT BY DMA. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E51 except that the data pattern transferred is in error.
102053	(none)	(none)	Same message as E52 (with no teleprinter). Switch register contains the word output by the DMA. Press RUN to display the word read back from the MCR.
102054	(none)	(none)	Switch register contains the word read back from the MCR. Press RUN to continue test.
102055	(none)	END T.DTO	Select options and press RUN.
102056	E56	E56. DMA FLAG SHOULD BE SET.	Tests all possible data patterns of the DMA input transfer capability. The DMA flag is not set after the data transfer.

Table MS-2. DMA General Diagnostic Test Errors and Messages (Continued)

T-REGISTER	ERROR NO.	MESSAGE	COMMENTS
102057	E57	E57. DATA PATTERN READ BACK FROM THE SAME AS THAT OUTPUT BY MCR. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E56 except that the data pattern transferred is in error.
102060	(none)	(none)	Same message as E57 (with no teleprinter). Switch register contains the word output from the MCR to the DMA. Press RUN to display the word input from the DMA.
102061	(none)	(none)	Switch register contains the word input from the DMA. Press RUN to continue tests.
102062	(none)	END T.DTI	Select options and press RUN.
102064	(none)	(none)	The DMA flag did not set after the transfer of data (this is a timed test).
102065	E65	E65. DATA PATTERN READ IN FROM READER IS NOT THE SAME AS THAT OUTPUT TO PUNCH. PATTERN IS XXXXXX AND SHOULD BE XXXXXX.	Same test as E64 except that the data pattern transferred is in error.
102066	(none)	END T.DIO	Select options and press RUN.
102077	E77	E77. DMA DIAGNOSTIC PROGRAMS HAVE BEEN EXECUTED. TELE-PRINTER USED FOR DATA TRANSFER.	Not an error message. Select options and press RUN to recycle the DMA diagnostic programs.

Table MS-3. DMA Rate and Transfer Diagnostic Test Errors and Messages

T-REGISTER	TEST DESCRIPTION
XXXXXX	If the program halts with any number in the T-Register other than the three listed below and any number other than 000044 in the M-Register, the DMA is not stealing every cycle.
1Ø2Ø7Ø	An incorrect data transfer has taken place. The switch register contains the correct data. Press RUN to display the incorrect data.
1Ø2Ø71	The incorrect data referenced by the above halt is now stored in the switch register. Press RUN to continue.
1Ø2Ø72	The DMA did not transfer the data when instructed, or it did transfer the data but did not interrupt as expected.