HEWLETT PACKARD

OPERATING AND SERVICE MANUAL

HP 12604B
DATA SOURCE INTERFACE KITS
(for 2100A/S, 21MX Computers)

Manual part no. 12604-90002
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Card Assemblies

12604-60001, Rev. 926, 932, 1020, 1418
12604-60010, Rev. 1331, 1418
12604-60011, Rev. 1418

NOTE

Retain this manual with the applicable computer system documentation.

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LIST OF EFFECTIVE PAGES

Changed pages are identified by a change number adjacent to the page number. Changed information is indicated by a vertical line in the outer margin of the page. Original pages do not include a change number and are indicated as change number 0 on this page. Insert latest changed pages and destroy superseded pages.

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SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

1-2. Interface Kit 12604B for the Hewlett-Packard computer systems provides the interface for transferring up to 32 data bits into an HP computer. Data levels from the data source can vary widely since capacitive coupling is used and the data source furnishes reference voltages to the interface card. The interface kit consists of the following:

a. Data Source Interface (DSI) Card, HP Part No. 12604-60001;

b. Connector Kit, 48-Pin, HP Part No. 5060-8339;

c. DSI Diagnostic Test Tape, HP Part No. 20337-60001;

d. BCS 8421 Driver D.40, HP Part No. 20008-60001. The BCS 8421/4221 DSI Driver D.40A, HP Part No. 20011-60001 is available on request as a replacement for the 8421 DSI Driver.

1-3. The interface card contains interrupt, control, and input logic. Section IV of this manual includes the diagnostic test procedure.

1-4. The DSI card does not have storage capability and therefore the data source must keep the data on the input lines until the information is transferred to the computer. When the data source is an HP instrument, the data is available to the DSI card until the card applies an Encode signal or removes a Hold signal to the data source.

1-5. Generally, the maximum reading rate is limited by the response time of the data source; i.e., the time required for the data source to respond to an Encode signal (or removal of a Hold signal), make a measurement, and issue a Record Command to the DSI card.

1-6. OPTIONS

1-7. OPTIONS 001 THROUGH 006

1-8. Options 001 through 006 of the 12604B Data Source Interface Kit provide data interfaces for several HP voltmeters and counters. For interface purposes, the HP counters are considered in two groups; those having BCD outputs routed through an Amphenol Blue Ribbon connector (HP Stock No. 1251-0087), and those having printed circuit (PC) board outputs. Each option is effected by replacing the 48-pin connector kit with an interconnecting cable. The cable furnished with each option is given in Table 1-1.

1-9. OPTION 020

1-10. Option 020 of the 12604B DSI Kit enables the 12604B DSI to be used with HP Real Time Executive (RTE) Systems. Option 020 adds RTE 12604B DSI Driver DVR40 (HP Part No. 29100-60041) to the DSI kit. Complete programming information for Option 020 is given in Appendix C.

1-11. OPTION 028

1-12. Option 028 of the 12604B DSI Kit decreases the data line settling delays from 1 ms and 0.1 ms to 900 μsec and 10 μsec. Option 028 is effected by replacing the standard DSI card with a DSI card having HP Part No. 12604-60010.

1-12A. OPTION 029

1-12B. Option 029 of the 12604B DSI Kit enables the HP 2100 series computer to be used with the HP 5300 series counters. Option 029 is effected by replacing the standard DSI card with a TTL Reference Card having HP Part No. 12604-60011.

1-13. DATA WORD FORMATS

1-14. When more than 16 data bits are provided by the data source, two 16-bit computer words must be used. The first word contains the least significant bits (0 through 15) and the second word contains the most significant bits (16 through 31). The word formats for the 2401C or 2402A Digital Voltmeter and the 3450A Multi-Function Meter are given in Figures 1-1 and 1-2.

Table 1-1. Cables Furnished with Standard Options

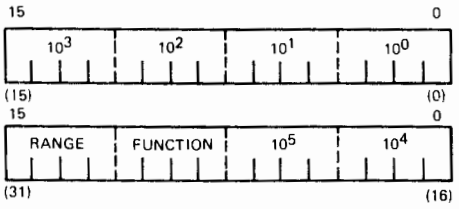
OPTION	FOR INSTRUMENT	INTERCONNECTING CABLE (HP PART NO.)
001	2401C/2402A Digital Voltmeter	12604-60002
002	HP Counters (up to 8 digit)(connector output)	02116-6153
003	HP Counters (up to 7 digit) (PC board output)	12604-60008
004	3440A Digital Voltmeter	12604-60004
005	3450A Multi-Function Meter	12604-60007
006	3460A/B Digital Voltmeter	02116-6114

1-15. IDENTIFICATION

1-16. The interface card is identified by a serial number, a stock number, and a revision code. The serial number is a 10-character number (e.g., 1009A00123) that identifies a specific interface card. The stock number, 12604-60001, is the same for all 12604B DSI Cards. The revision code (e.g., A-932-6) is a manufacturing identification primarily for the physical layout of the card. Cards having the same stock number but different revision codes are electrically identical except as noted on the schematic diagram. (See Figure 3-4.) If the revision code on your DSI card is not the same as either code on the title page of this manual, a supplement supplied with this manual will define the differences between your card and the DSI card described in this manual.

1-17. SPECIFICATIONS

1-18. The specifications for the 12604B DSI Card are given in Table 1-2.



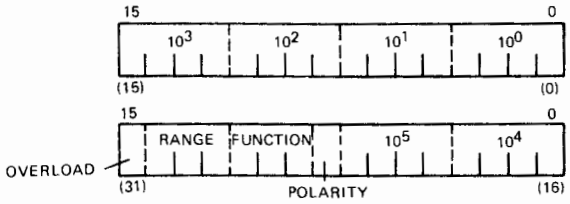
$10^0 - 10^5$: BCD numbers corresponding to the six digits of the voltmeter display.

Range: A BCD number (n) representing a decimal multiplier in the form 10^{-n}. (For the 2402A: a BCD 9 indicates an overload condition with the corresponding data invalid; a BCD 8 indicates calibration.)

Function: A BCD number indicating the function of the voltmeter, as follows:

NUMBER (BCD)	FUNCTION
0	Period (2401C only)
1	+ VDC
2	- VDC
3	Frequency
4	Ohms (2402A only)
4	KΩ (2401C only)
5	MΩ (2401C only)
9	Overload (2401C only)
11	VAC

Figure 1-1. Word Formats for Data Input from 2401C/2402A Voltmeter



$10^0 - 10^5$: BCD numbers corresponding to the six digits of the 3450A display.

Range: A BCD number (n) representing a decimal multiplier in the form 10^{-n}.

Polarity: "0" equals positive; "1" equals negative.

Overload: "0" equals no overload: "1" equals overload.

Function: A BCD number indicating the function of the 3450A, as follows:

NUMBER (BCD)	FUNCTION
0	DC volts
1	AC volts
2	Ohms
4	DC ratio
5	AC ratio
6	Ohms ratio

Figure 1-2. Word Formats for Data Input from 3450A Multi-Function Meter

Table 1-2. Specifications

DATA INPUT SIGNALS:

"1" state: At least 5V positive with respect to "0" state.

Separation; "1" to "0": 100V (max.).

Levels: Between +100V and -100V.

Line Settling Delays: 1 ms or 0.1 ms (jumper selected); 900 μsec (option 028).

CONTROL SIGNALS:

Outputs:

+Encode: Shift from -12V to ground through 10K ohms.

-Encode: Shift from +13.5V to ground through 9K ohms.

Pulsed Encode (jumper selected): Duration of 60 to 80 μsec.

+Hold: +17V through 1K ohm (10 mA max.).

-Hold: -11V through 2.2K ohm (10 mA max.).

Inputs:

Record Command: +4.5 to +24V (or -4.5 to -24V) pulse, 20 μs (minimum), AC-coupled.

External Low Set (not required for normal operation): +4.5V logic pulse to set for first 16 bits input.

References:

+Reference required: 0.5V negative with respect to "1"-state data (optimum). Refer to Figure 1-3 for +Reference source resistance.

-Reference: At least 4.5V negative with respect to +Reference. (Reference should fall within data levels.)

NOTE: -Reference is not used directly by the card. It may be used (in the cable) to set unused bits to zero.

Current Supplied by the Computer:

0.01A	(+12V)
0.024A	(-12V)
0.35A	(-2V)
1.1A	(+4.5V)
0.037A	(+28V*)

*If the interface is to be used in an HP 21MX Computer or an HP 12979A I/O Extender, the computer or extender must be modified to provide +28V dc at the backplane. Refer to the appropriate Installation and Service Manual (part no. 02108-90006 for 21MX or part no. 12979-90006 for 12979A) for modification details.

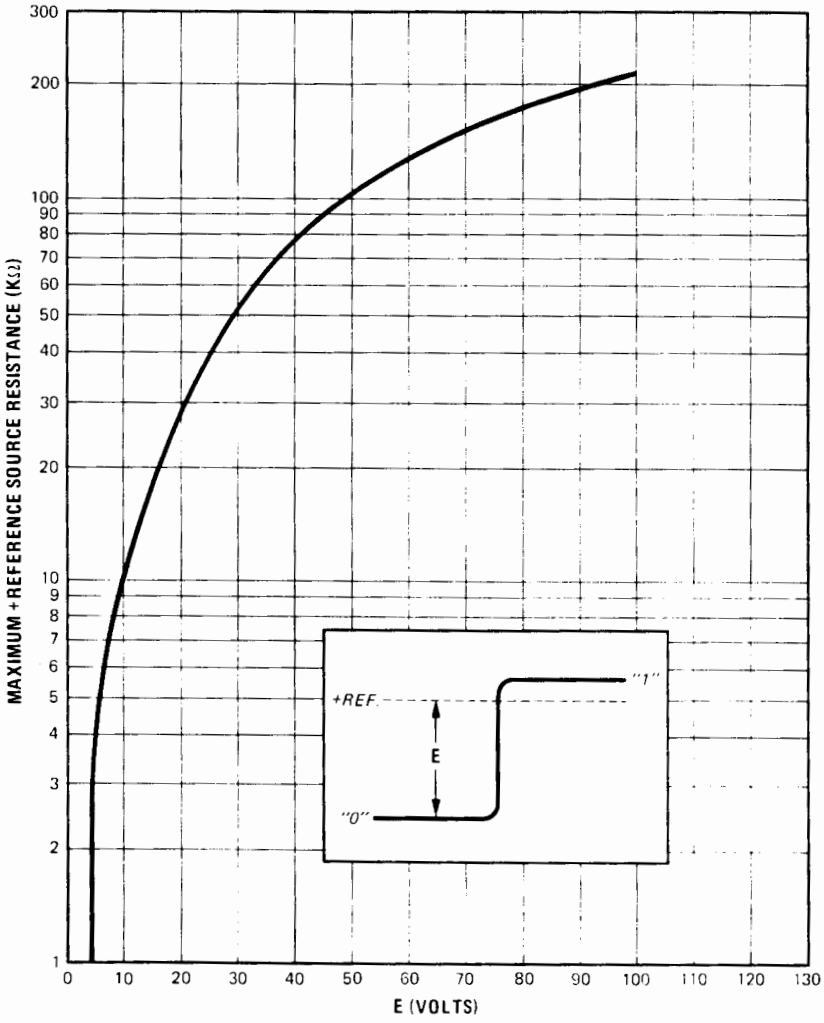


Figure 1-3. Maximum Source Resistance of Positive Reference Supply

SECTION II
INSTALLATION AND PROGRAMMING

2-1. INSTALLATION

2-2. UNPACKING AND INSPECTION

2-3. If the shipping container that holds the 12604B DSI Kit appears damaged, it should be unpacked with the carrier's agent present. Carefully inspect the interface kit for damage. If the kit is damaged, notify the carrier and the nearest Hewlett-Packard Field Office immediately. (Field Offices are listed at the back of this manual.) Retain the container and the packing materials for the carrier's inspection.

2-4. CABLE FABRICATION

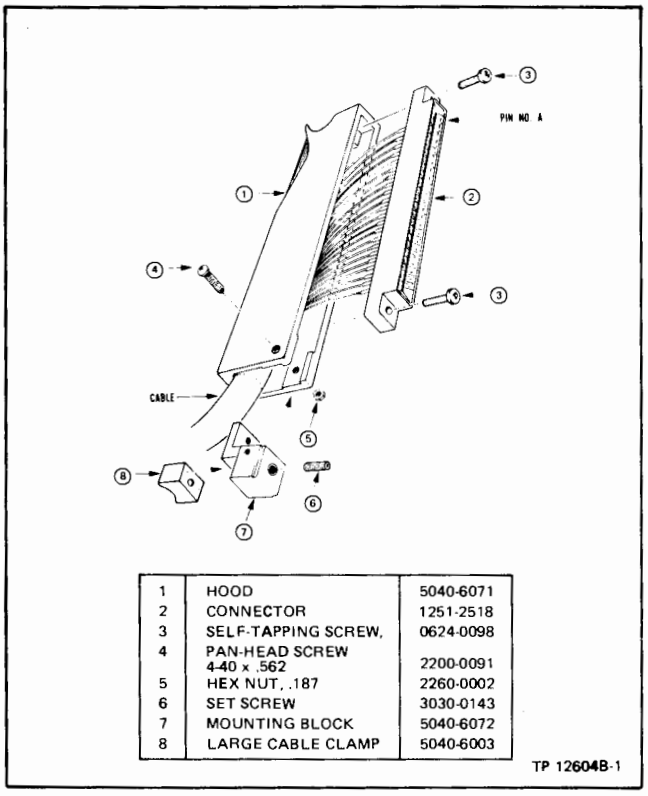
2-5. Since the 12604B DSI Kit is designed for use with various data sources, an interconnecting cable must be prepared for the particular data source being used; a 48-pin connector kit is furnished for this purpose. Figure 2-1 gives an exploded view and a parts list of the connector kit. As an aid in fabricating the interconnecting cable, Table 2-1 lists the signals to and from the DSI card and their pin assignments. The 48-pin connector slides onto one end of the interface card (see Figure 2-2). If the 12604B DSI Kit is purchased with one of the Options 001 through 006, the appropriate interconnecting cable replaces the 48-pin connector kit.

NOTE

Pins 1 and A of the 48-pin connector must be connected together in order for the DSI card to function. This connection is an interlock which prevents erroneous "data" readings from the card when the data source is disconnected. In the cables supplied as part of Options 001 through 006, the connection has been made in the 48-pin connector.

2-6. An open data input is interpreted by the DSI card as a logic "1". When using the BCS Driver D.40 (HP 20008-60001) with the Formatter to read BCD data, the BCD code 1111 is decoded as a blank. If the BCS Driver is not used and fewer than 32 data bits are connected, it may be necessary to tie the unused input pins to the -Reference. The unused inputs may also be eliminated by writing masking instructions into the subroutine program.

2-7. When it is necessary to input more than eight BCD digits (32 data bits) from a data source, two DSI



1	HOOD	5040-6071
2	CONNECTOR	1251-2518
3	SELF-TAPPING SCREW,	0624-0098
4	PAN-HEAD SCREW 4-40 x .562	2200-0091
5	HEX NUT, .187	2260-0002
6	SET SCREW	3030-0143
7	MOUNTING BLOCK	5040-6072
8	LARGE CABLE CLAMP	5040-6003

Figure 2-1. Assembly Diagram for Connector Kit, HP Part No. 5060-8339

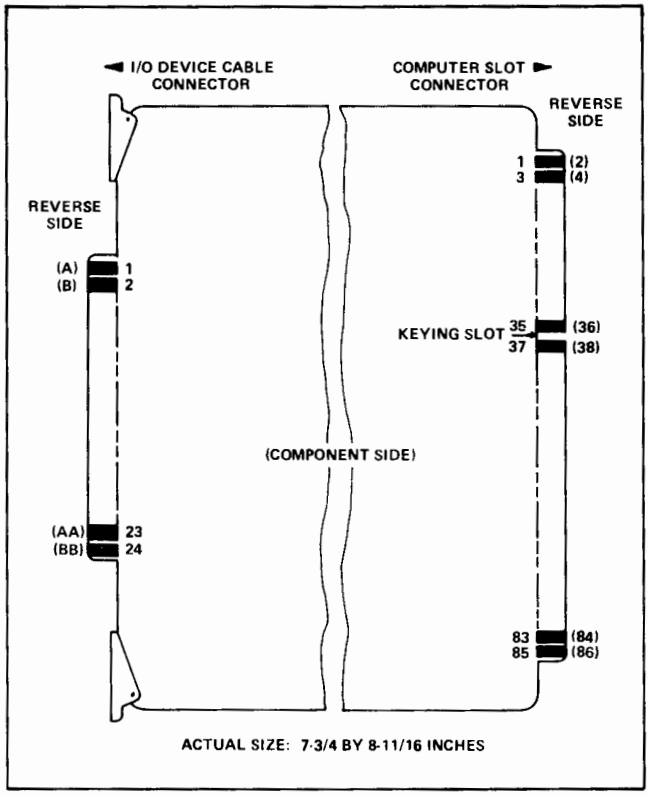


Figure 2-2. Orientation of Connector Pins

Table 2-1. DSI Pin Assignments and Leadwire Connections

DSI CONN. PIN	SIGNAL	DATA BIT	DATA SOURCE CONNECTOR PINS FOR HP CABLES 1 2					
			12604-60002	02116-6153	12604-60008	12604-60004	12604-60007	02116-6114
4	10^0 (1)	0	3	1	17	3	1	5
B	10^0 (2)	1	4	2	16	4	2	6
J	10^0 (4)	2	28	26	15	28	26	30
L	10^0 (8)	3	29	27	18	29	27	31
T	10^1	4	5	3	6	5	3	7
V	10^1	5	6	4	7	6	4	8
6	10^1	6	30	28	8	30	28	32
8	10^1	7	31	29	5	31	29	33
2	10^2	8	7	5	F	7	5	9
D	10^2	9	8	6	H	8	6	10
F	10^2	10	32	30	J	32	30	34
N	10^2	11	33	31	E	33	31	35
R	10^3	12	9	7	R	9	7	11
X	10^3	13	10	8	N	10	8	12
Z	10^3	14	34	32	M	34	32	36
10	10^3	15	35	33	P	35	33	37
5	10^4	16	11	9	L	--	9	13
C	10^4	17	12	10	9	--	10	14
K	10^4	18	36	34	10	--	34	38
M	10^4	19	37	35	K	--	35	39
U	10^5	20	13	11	11	--	11	15
W	10^5	21	14	12	13	--	12	16
7	10^5	22	38	36	14	--	36	40
9	10^5	23	39	37	12	--	21	41
3	10^6	24	15	13	S	11	17	17
E	10^6	25	16	14	V	12	15	18
H	10^6	26	40	38	U	36	16	42
P	10^6	27	41	39	T	37	40	3
S	10^7	28	1	15	--	1	13	1
Y	10^7	29	2	16	--	2	14	2
AA	10^7	30	26	40	--	26	38	26
11	10^7	31	27	41	--	27	18	27
14	+Ref.		25	25	3,C	25	25	25
13	+Hold		22	22	B	22	--	22
16	+Rec. Com.		23	23	4	23	--	23
20	-Ref.		24	24	1*	24	24	24
15	-Hold		47	47	2	--	47	47
17	-Rec. Com.		--	48	D	--	48	48
12	-Encode		--	--	--	--	46	--
18	+Encode		46	--	--	--	--	--
24,BB	Ground		50	50	A	43	50	50
A	IOI Output		†	†	†	†	†	†
1	IOI Return		†	†	†	†	†	†

1 12604-60002 for HP 2401C/2402A Digital Voltmeter

02116-6153 for discrete counters

12604-60008 for I.C. counters

12604-60004 for HP 3440A Digital Voltmeter

12604-60007 for HP 3450A Multi-Function Meter

02116-6114 for HP 3460A/B Digital Voltmeter

2 12604-60005 (discontinued) for HP 3450A Multi-Function Meter; same as 12604-60007 except pin 9 of 48-pin connector is connected to pin 37 of 50-pin connector.

*Pin 1 tied to pin A at 36-pin connector.

†Pin A tied to pin 1 at 48-pin connector.

cards can be used. The External Low Set lines (pin 21) must be connected together through the 48-pin connectors. This connection causes both DSI cards to begin the data transfer with the low-order digits first.

2-8. JUMPER PLACEMENT AND SWITCH SETTINGS

2-9. Jumpers W1 through W8 on the DSI card (see Figure 2-3) must be placed by the user so as to complete the interface circuits required by a particular data source.* The function of each jumper is as follows:

W1 enables the -Record Command to apply the Hold signals;

W2 (in position A) allows the -Record Command to remove the Encode signals;

W2 (in position B) allows the +Record Command to remove the Encode signals;

W3 enables the +Record Command to apply the Hold signals;

W4 enables the -Encode signal;

W5 enables the +Encode signal;

W6 enables automatic removal of Encode signals (after 60 to 80 μsec);

W7 controls data line settling time:

In - 1.0ms (900 μsec for Option 028)

Out - 100μsec (10μsec for Option 028);

W8 (in position A) enables only STC (Set Control) to apply Encode signals;

W8 (in position B) enables either STC or CLF (Clear Flag) to apply Encode Signals.

NOTE

Jumpers W1 through W5 and W8 are soldered in; jumpers W6 and W7 are plug-in types and can be stored at the top of the card near the 86-pin connector.

*If the DSI card was furnished as part of an HP subsystem, jumpers W1 through W8 will be placed correctly for the subsystem data source.

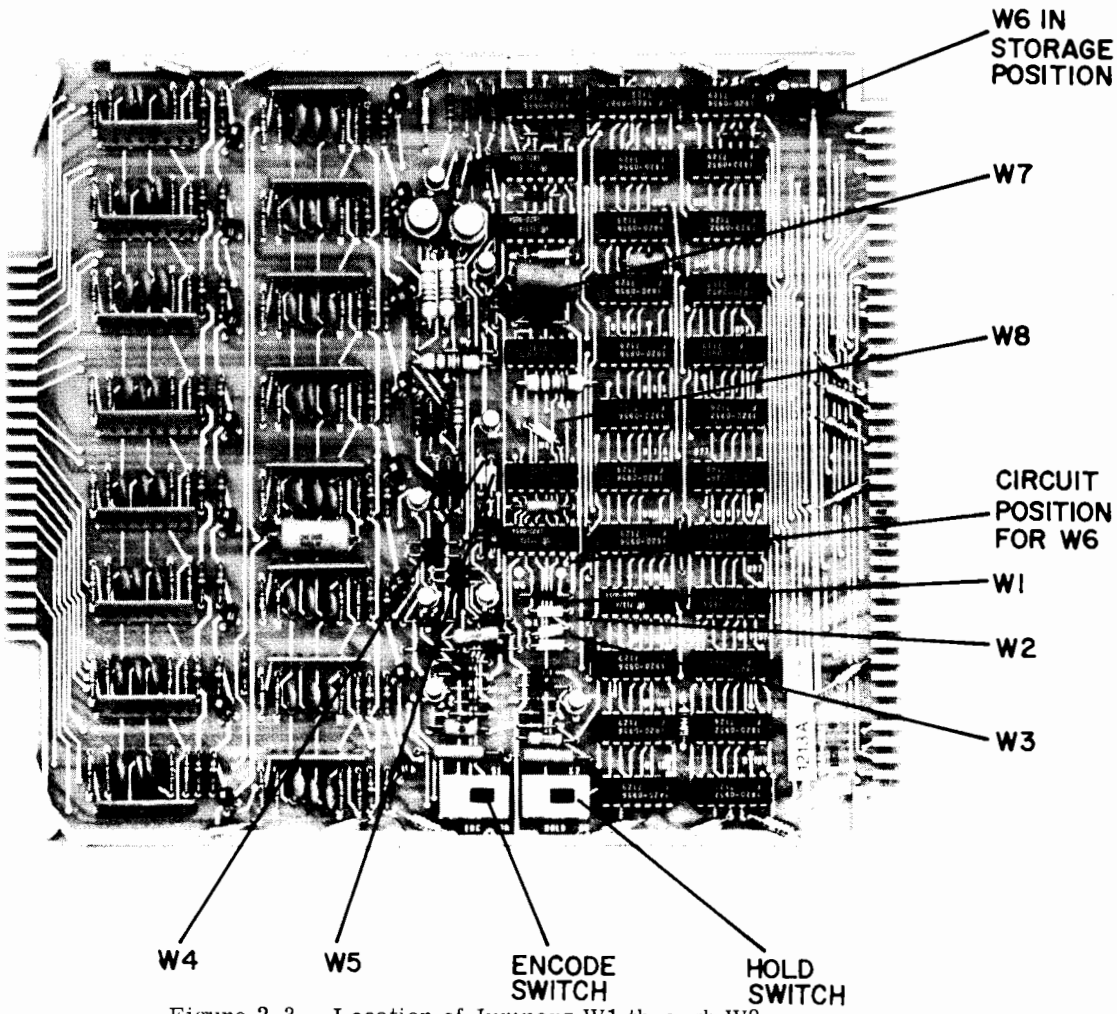


Figure 2-3. Location of Jumpers W1 through W8

2-10. When the DSI card is shipped from the factory the jumpers are placed as shown in Figure 2-3 (W2 is in position B, and W8 in position A). Generally, jumper W7 should be installed when the data lines have a high impedance; typical sources with this characteristic are those having discrete components instead of integrated circuits. The DSI card mounts two slide switches: ENCODE and HOLD; one of these two switches must be turned on whenever data source measurements are controlled by either the Encode or Hold signal from the DSI card. Refer to Table 2-2 for information on in-circuit placement of jumpers W6 and W7 and on the appropriate setting of the ENCODE and HOLD switches for several HP instruments. For instruments not listed in Table 2-2, refer to the specifications in the instrument manual for the Encode (or Hold) signal requirements.

2-11. INSTALLATION

2-12. Before installing an interface card, verify that the computer power supply has adequate capacity to accommodate the additional current demands of the card. Refer to the Input/Output System Operation volume of the computer manual for the information required to calculate power supply capacity.

2-13. The DSI card plugs into any of the input/output (I/O) slots of the computer and assumes the lower select code of the slot. To connect the data source to the computer, proceed as follows:

a. Turn the power off.

b. Open the computer for access to the I/O slots.

c. Plug the DSI card into the I/O slot assigned for the particular computer system. (Refer to Appendix B.)

d. Connect the interconnecting cable to the data source.

e. Pass the cable connector that mates with the DSI card through the opening at the rear of the computer. Slide the connector onto the card and close the computer.

2-14. For operating instructions for the data source, refer to the data source manual.

2-15. Refer to Table 2-1 for all leadwire connections in cables furnished with DSI Options 001 through 006.

2-16. PROGRAMMING

2-17. The 12604B DSI can be programmed in either the HP Assembler Language, FORTRAN, or ALGOL. Instructions for loading program tapes are given in the computer operating manual.

2-18. The BCS 8421 DSI Driver D.40 (HP Part No. 20008-60001) is furnished with the 12604B DSI for use in FORTRAN and ALGOL programming. If the user has a data source coded 4221, the BCS 8421/4221 DSI Driver D.40A (HP Part No. 20011-60001) can be ordered to replace the 8421 version. (Refer to Appendix B for information on generating a new BCS tape that includes either the D.40 or D.40A Driver.)

2-19. FLOWCHARTS. The flowcharts for Drivers D.40 and D.40A are shown in Figures B-1 and B-2 of Appendix B.

2-20. HP ASSEMBLER LANGUAGE

2-21. Table 2-3 shows a sample subroutine using HP Assembler Language programming to transfer 32 bits of data from a digital voltmeter into the computer. In this example, the multi-channel priority interrupt system of the computer is not used and the availability of input data is tested with an SFS (Skip If Flag Set) instruction.

Table 2-2. Placement of Jumpers W6 and W7 and of the Encode and Hold Switches for Typical HP Data Sources

HP DATA SOURCE	W6 (in circuit)	W7 (in circuit)	ENCODE (S1)	HOLD (S2)
2402A	no	no	ON	OFF
2401C	no	yes	OFF	ON
3440A	no	yes	OFF	ON
3450A	yes	no	ON	OFF
3460A/B	no	yes	OFF	ON
Discrete Counters	no	yes	OFF	ON
I.C. Counters	no	no	OFF	ON

NOTE:
When the 12604B DSI Card is used in an HP data acquisition subsystem such as the HP 2320A, refer to the subsystem manual for jumper placements and switch settings. When the 12567A DVM Program Card is used to program the HP 2402A Digital Voltmeter, set the ENCODE switch off.

Table 2-3. Sample 32-Bit Input Subroutine Program

LABEL	OPERATION	OPERAND	EXPLANATION
DSI	NOP		Entry point.
	STC	21B,C	Initiate a reading from the data source.
	SFS	21B	Input data ready?
	JMP	*-1	No, keep testing.
	LIA	21B	Yes, load the first 16 data bits into the A-register.
	LIB	21B	Load the second 16 data bits into the B-register.
	DST	DATA	Store the voltmeter reading (32 data bits) in memory.
	CLC	21B	Release the DSI card from the priority interrupt system.
	JMP	DSI,I	Return to main program.
	COM	DATA (2)	Common area for the reading placed in memory (two words).
For this example, the select code is 21_8.			

2-22. FORTRAN

2-23. The operation of Driver D.40 is as follows:

a. D.40 reads data in the following format:

Low order word $D_4\ D_3\ D_2\ D_1$

High order word $D_8\ D_7\ D_6\ D_5$

where each D_n is a 4-bit BCD number.

b. If a binary READ is requested (see Figure 2-4), the input data is transferred to the calling program with the low order word (D_4-D_1) in Buffer Address and the high order word (D_8-D_5) in Buffer Address +1.

c. If a formatted READ request is made (see Figure 2-5), data is returned as a 16 character (8 words) ASCII string with the following sequence:

$\underbrace{D_8\ D_7\ D_6\ D_5\ D_4\ D_3\ D_2\ D_1}\ \underbrace{E\ -\ \emptyset\ R\ \Delta\ \Delta\ FF}$

Converted from BCD to ASCII by the driver — Inserted by the driver

where R is equivalent to D_8. FF is the 2 character 8421 equivalent of the 4 bits that made D_7.

d. For a 4-digit voltmeter such as the HP 3440A, the program example shown in Figure 2-6 would apply where D_6 and D_5 are zero.

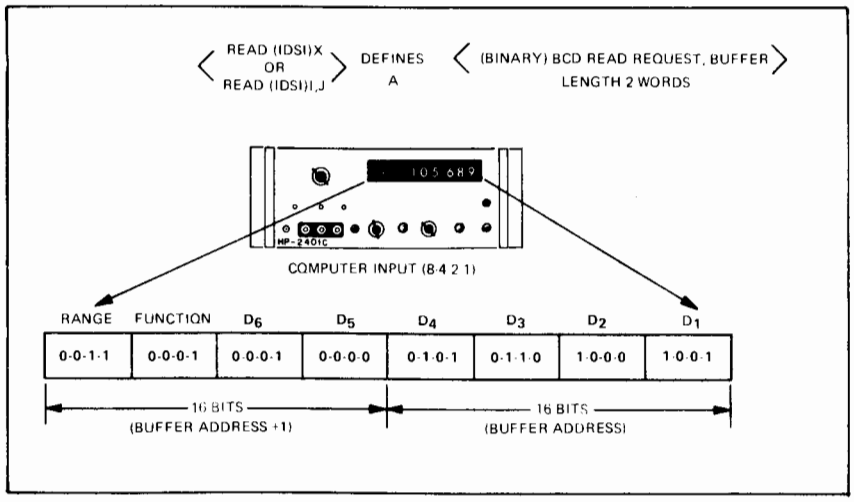


Figure 2-4. Binary Read Request

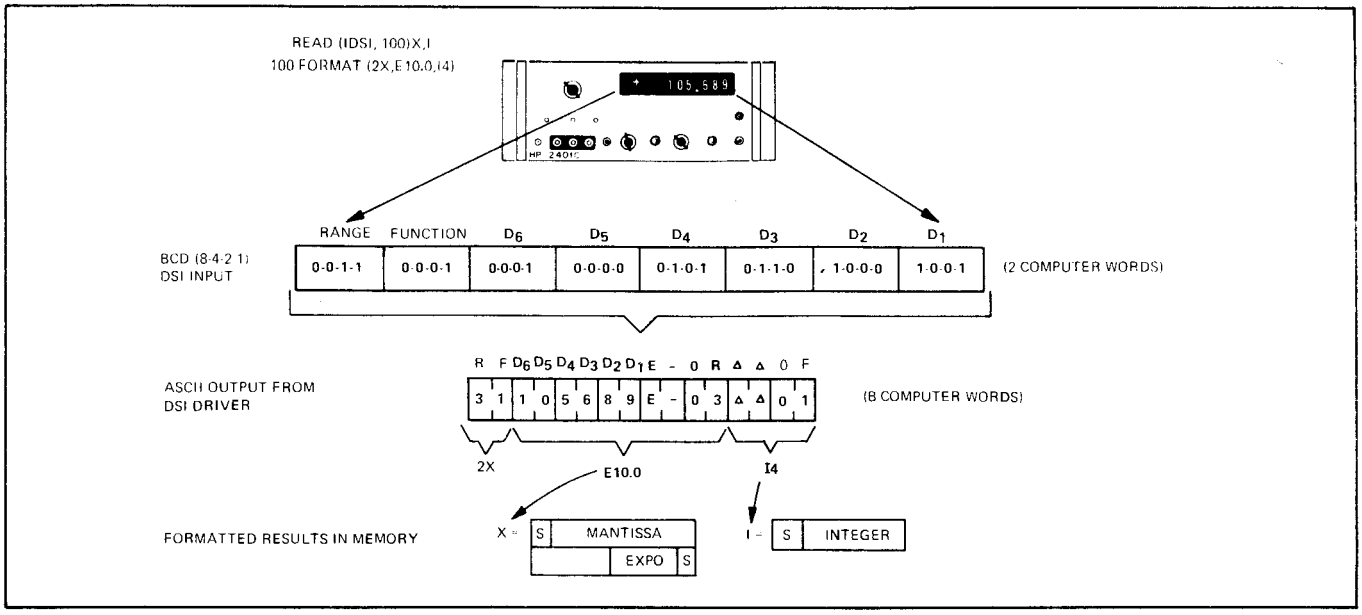


Figure 2-5. Formatted Read Request

e. For an 8-digit counter such as the HP 5245L, the following program would apply where range and function are not available because all 8 digits of counter information are desired.

```
      READ (CTR, 1ØØ) DATA
1ØØ   FORMAT (E11.Ø, 5X)
```

Counters with fewer digits would reduce the W specification of the E format and insert an NX to occupy the extra digits in front of the E. It should be remembered that resolution available in a computer floating point word is limited to seven significant digits. For example, the least significant digit of input data from an 8-digit counter will be ignored unless Extended Precision techniques are used.

f. For a 6-digit voltmeter with range and function, the following example would apply.

```
      READ (DVM, 1ØØ) DATA, IFUN
1ØØ   FORMAT (2X E1Ø.Ø, 2X, I2)
```

The programmer would then test IFUN for negative values and complement DATA for such values in addition to testing for overload. (See Figure 2-6.) Bear in mind that both the 8421 and 4221 versions of the driver convert the FUNCTION digit to the 2 character equivalent of 8421, not 4221.

g. For the 3450A Multi-Function Meter, the overload bit is in the range character. Since the Formatter will not convert an ASCII character with an octal value greater than 71 to an integer, a special technique must be used to test for overload on this voltmeter. A typical Data request to a 3450A is shown in Figure 2-7. Note that an "ASCII" constant is used to obtain the value of the range digit. This feature is not available in the 4K FORTRAN Library. Since the overload bit in the 3450A is connected to the 8 bit of the range digit, this digit will have an octal value of 70 or over whenever an overload occurs. The determination of what to do with an overloaded reading is the programmer's prerogative. When the driver returns the 8-word (16-character) ASCII string, the function code character of the first word may be any of those in the first column of Table 2-4 depending upon the data source. The appropriate code which produced the character is one of those in the next two columns. The value of FF (the last computer word) is the numeric value shown in the last column. Note that the "2X" format causes the first word to be skipped.

Table 2-4. Code Conversion

CHAR	4 2 2 1	8 4 2 1	FF
0	0 0 0 0	0 0 0 0	0 0
1	0 0 0 1	0 0 0 1	0 1
2	0 0 1 0	0 0 1 0	0 2
3	0 0 1 1	0 0 1 1	0 3
4	0 1 1 0	0 1 0 0	0 4
5	0 1 1 1	0 1 0 1	0 5
6	1 1 0 0	0 1 1 0	0 6
7	1 1 0 1	0 1 1 1	0 7
8	1 1 1 0	1 0 0 0	0 8
9	1 1 1 1	1 0 0 1	0 9
:	1 0 0 0	1 0 1 0	1 0
;	1 0 0 1	1 0 1 1	1 1
<	1 0 1 0	1 1 0 0	1 2
=	1 0 1 1	1 1 0 1	1 3
>	0 1 0 0	1 1 1 0	1 4
?	0 1 0 1	1 1 1 1	1 5

HEWLETT-PACKARD FORTRAN CODING FORM

```
FTN,B,L
      .
      .
      .
C ENCODE THE VOLTMETER
      WRITE (DVM)
C INPUT THE READING
      READ (DVM,100) IRNG,DATA,IFUN
100   FORMAT (A1,X,E10.0,I4)
C TEST FOR OVERLOAD IRNG>=70B
      IF (67B-IRNG) 10,20
C VOLTMETER IS IN OVERLOAD - SET DATA
C VERY LARGE
10    DATA=1.E+38
      WRITE (2,101)
101   FORMAT ("OVERLOAD LAST READING")
      GO TO 40
C READING IS VALID, TEST FOR NEGATIVE DATA
20    IF (IFUN-1) 40,30,40
C FUNCTION IS NEGATIVE, THEREFORE MAKE
C DATA NEGATIVE
30    DATA=-DATA
C CONTINUE PROGRAM
40    .
      .
      .
      .
```

Figure 2-6. Sample Program for HP 3440A Voltmeter

HEWLETT-PACKARD FORTRAN CODING FORM

```
FTN,B,L
      .
      .
      .
      READ (DVM,100) DATA,IFUN
100   FORMAT (4X,E8.0,I4)
10    IF (IFUN-1) 30,20,30
C FOR A FUNCTION VALUE OF 1 VOLTAGE IS
C NEGATIVE
20    DATA=-DATA
C CHECK FOR OVERLOAD
30    IF (IFUN-7) 40,35,35
35    WRITE (2,200)
200   FORMAT ("OVERLOAD")
40    CONTINUE
      .
      .
      .
      .
```

Figure 2-7. Sample Program for HP 3450A Multi-Function Meter

2-24. ALGOL

2-25. ALGOL will not accept a zero length binary WRITE call. However, Driver D.40 ignores any buffer specified for this particular request. Therefore, the DSI card control can be set through the use of a dummy argument in the WRITE request as follows:

WRITE (DSI, DUMMY);

where:

DSI is the EQT number of the DSI card;

DUMMY is any variable that has been declared previously.

The READ request is implemented in the same manner as a FORTRAN READ request but in ALGOL syntax. For a voltmeter, the following example would apply.

READ (DSI, FMT1, DATA, FUNCTION);

where:

DSI is the EQT number of the DSI card;

FMT1 is the format desired and has been included previously in the declarations;

DATA is the real variable where the data for the voltmeter reading will be stored;

FUNCTION is the integer variable where the voltmeter function digit will be stored.

The Format rules are identical to those of FORTRAN.

SECTION III
PRINCIPLES OF OPERATION

3-1. GENERAL

3-2. Figure 3-1 is a simplified logic diagram of the 12604B DSI Card. The circuitry of the DSI card can be divided into three basic sections; standard flag control and interrupt circuitry, data source control circuitry, and data transfer circuitry.

3-3. The data source control circuitry applies Encode Commands or Hold signals to the data source, receives a Record Command from the data source, and enables both the interrupt circuitry and the data transfer circuitry.

3-4. The flag control and interrupt circuitry is required for operation with the multi-channel priority interrupt system of HP computers. The priority interrupt system is turned on by a programmed Set Flag (STF) instruction having a select code of 00 (octal) and allows the DSI card to automatically inform the computer that data is available from the data source. If the priority interrupt system is not used, a "data-ready" check is made by looping on an SFS instruction addressed to the DSI card.

3-5. The BCD data from the data source is applied to the data transfer circuitry and transferred into the

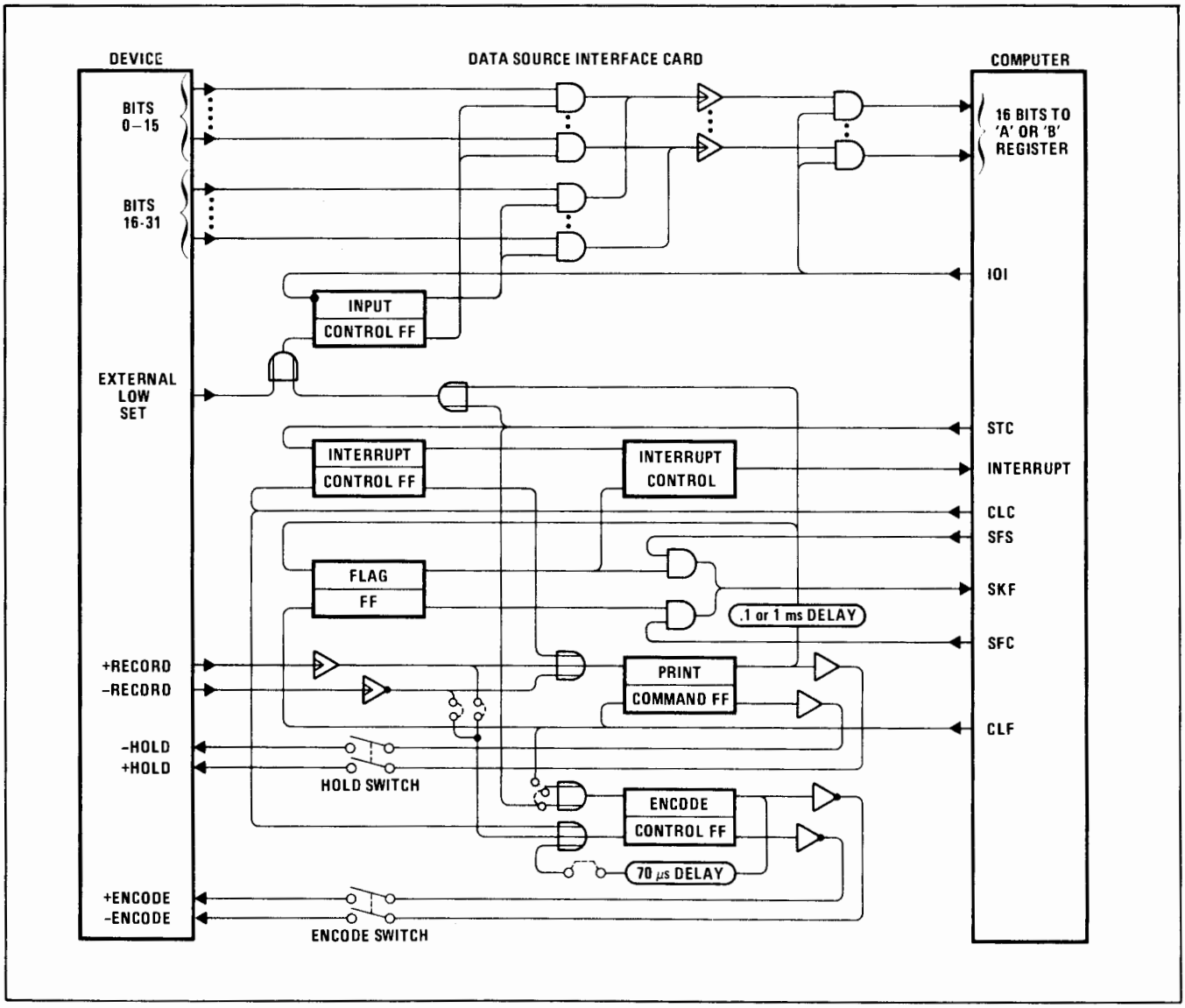


Figure 3-1. Simplified Logic Diagram, 12604B DSI Card

A or B Register of the computer by an IOI signal. The IOI signal is generated by a Load into A or Load into B (LIA/B) instruction. For 32 data bits, one LIA/B instruction transfers bits 0 through 15 and a second LIA/B instruction transfers bits 16 through 31. (The A and B Registers can contain only 16 data bits each. If only one register is used to input 32 bits of data, the first 16 bits must be stored in memory before the second 16 are loaded into the register.)

3-6. DSI OPERATION

3-7. During DSI operation, the general sequence of events is as follows:

a. An STC, CLF* instruction addressed to the DSI card causes the card to issue an Encode Command (or remove a Hold signal) to the data source. (Either Switch S1 or S2 is closed.)

b. The data source makes a measurement and returns a Record Command and BCD data to the DSI card.

c. The DSI card removes the Encode Command (or applies the Hold signal) to the data source and initiates either a 1.0 ms or 0.1 ms delay for settling time on the data lines (900μsec or 10μsec for Opt. 028).

d. After the line-settling delay, the Input Control FF is reset to enable transfer of the first 16 data bits to the computer. Additionally, the Flag FF is set to inform the computer that measurement data is available from the data source.

e. The computer, responding to a programmed LIA/B instruction, generates an IOI signal which transfers 16 data bits from the data source, through the DSI card, and into either the A or B Register of the computer. If there are more than 16 data bits, the computer generates a second IOI signal.

3-8. DETAILED PRINCIPLES OF OPERATION

3-9. INITIAL TURN-ON

3-10. Figure 3-4 is the logic diagram of the 12604B DSI Card. When power is initially applied by the POWER switch on the front panel of the computer, the POPIO and CRS signals are received simultaneously by the DSI card from the computer I/O control card. These signals place the DSI card in a "standby" condition. The POPIO signal sets the Flag Buffer FF through gate U77C and resets the Input Control FF through U77C and diode CR10. At time T2 of the machine timing cycle, the ENF signal from the I/O control card resets the IRQ FF through gate U77A. The output of U77A and the output of the Flag Buffer FF enable gate U107A to set the Flag FF. The CRS (Control Reset) signal resets both the Interrupt Control FF (through gate U77D) and the Encode Command FF (through gates U77D and U85B).

*Shown in Table 2-3 as "STC 21B,C", where 21B is the I/O location of the DSI card.

3-11. DSI CARD SELECT

3-12. The programmed select code of the DSI card allows the data input operations to be initiated. The LSCM, LSCL, and IOG(B) signals enable gate U87C which provides a high input to each of several gates that allow the input of various control signals.

3-13. INPUT OPERATIONS

3-14. The programmed STC, CLF instruction activates the flag control and interrupt circuitry and initiates data input operations. The STC signal enables gate U57B which sets the Interrupt Control FF. The output of the Interrupt Control FF is a high input to gate U57C. The other inputs to this gate are the +4.5 VDC and the high IEN signal (generated by the set output of the Interrupt System Enable flip-flop on the computer I/O control card). The Interrupt Control FF also applies high inputs to gate U25C and the Print Command FF. The CLF signal enables gate U87B, goes through diode CR15, and resets the Flag Buffer FF. (When jumper W8 is in the B position, the CLF signal also sets the Encode Command FF through gate U85C.) The STC signal, gated through U57B and U15A, resets the Input Control FF, ensuring that the 16 least significant data bits are transferred first. STC is also gated through U57B and U85A to set the Encode Command FF.

3-15. The two outputs of the Encode Command FF cause transistors Q4 and Q5 to conduct, producing the minus and plus Encode Commands. The output of gate U25C is buffered through gates U25A and U25D to cut off transistor Q8, which cuts off Q9 while Q10 starts conducting. This removes the plus and minus Hold signals from the data source. (Depending on the particular data source being used, either switch S1 or S2 must be closed.) When the appropriate Encode Command is received (or the Hold signal removed), the data source makes a measurement. The output of gate U25A also causes transistor Q3 to conduct and discharge capacitor C6 (and C7 if jumper W7 is installed).

3-16. If jumper W6 is installed, the output at pin 8 of gate U75B in the Encode Command FF cuts off transistor Q6. Capacitor C5 begins to charge through resistor R21. When the increasing voltage at the base of Q7 overcomes the reverse bias applied to the emitter by Zener diode CR8, Q7 conducts and develops a voltage on R22. The voltage on R22 is the input to gate U85D and when the voltage reaches the threshold level of the gate, U85D resets the Encode Command FF. This occurs approximately 70μsec after the Encode Command FF was set.

3-17. After the data source makes a measurement, it sends a plus or minus Record Command to the DSI card. A +Record Command cuts off emitter follower Q2, producing an output that is inverted by gate U96D to set the Print Command FF. A -Record Command cuts off emitter follower Q1, producing an output that is buffered through gates U96C and U96B to set the Print Command FF. Capacitors C2 and C4 provide noise rejection for the Record Command circuits by preventing circuit response to a pulse width of less

than 10μsec. The circuit response is inconsistent when the Record Command pulse width is between 10μsec and the specified 20μsec (minimum). Depending on the placement of jumper W2, the output of either U96D or U96B resets the Encode Command FF.

3-18. The output of the Print Command FF inhibits gate U25C, which enables the Hold circuit (via U25A and U25D) to restore Hold signals to the data source. When the Encode Command is removed (or the Hold signal applied), the data source is prevented from making another measurement.

3-19. The negative-going output of gate U25A also activates the line-settling delay circuit by cutting off transistor Q3, allowing capacitor C6 (and C7) to charge. At time T_1 (see Figure 3-2), the voltage build-up on C6 reaches a level that causes the current through Zener diode CR9 to develop a voltage on resistor R27 equal to the threshold level of gate U35B. With resistor R28 providing feedback, gates U35B and U35D function as a Schmitt Trigger and produce a positive step at the output of U35D. The output of U35D is applied to gates U35C and U35A, causing the output of U35A to go negative. After a delay caused by the discharge of C8, the inverted output of U35C inhibits U35A, causing the output of U35A to go positive again. The result is a negative-going pulse of approximately 200 nanoseconds at the output of U35A. The pulse is inverted by U25B and gated through U15B to ensure reset of the Input Control FF (through diode CR10) and to set the Flag Buffer FF, initiating an interrupt request (or enabling a flag check) which informs the computer that data is available on the DSI card. The delay time is 1.0 ms (900 μsec for Opt. 028) if capacitor C7 is included in the circuit (jumper W7 installed), and 0.1 ms (10 μsec for Opt. 028) if C7 is not included.

3-20. INTERRUPT REQUEST

3-21. The output of the Flag Buffer FF (see Figure 3-4) provides a high input to gates U107A and U47C. The next ENF (T2) signal enables gate U107A to set the Flag FF. The Flag FF output enables gate U47B; and the output of U47B enables gate U47A if a device of higher priority has not requested an interrupt (PRH high). The output of U47A is applied to gate U47C and the next SIR (T5) pulse enables U47C through U77B. The output of U47C sets the IRQ FF, which enables gates U37B and U17B for an interrupt request and provides a high input to gate U107B. The IRQL and FLGL outputs cause the computer I/O control card to request an interrupt program to load in digital data from the DSI card. The interrupt acknowledge (IAK) signal from the I/O control card enables gate U107B which resets the Flag Buffer FF to prevent further interrupt requests. The computer interrupt program provides a combination of two LIA/B instructions, each of which generates an IOI signal.

3-22. FLAG CHECK

3-23. When the priority interrupt system is not used, the status of the Flag FF is checked by an SFS (Skip if Flag Set) instruction in the subroutine program. (Refer to Table 2-3.) When the Flag FF is set, gate U127A in the Flag FF applies a high input to gate U97C. The SFS signal enables U97C, producing an SKF (Skip on Flag) output via gate U36A. The SKF signal causes the computer to skip the next instruction in the subroutine program and proceed to the first LIA/B instruction, generating an IOI signal.

3-24. DATA TRANSFER

3-25. The IOI signal is routed across the DSI card and through the 48-pin cable connector to the Input Control FF. The first IOI signal is "anded" with the reset output of the Input Control FF by gate U26B and applied to the data transfer circuits as a transfer pulse. The IOI is also gated through U36B.

3-26. Each data input bit is applied to the input of a transfer circuit (Figure 3-3) where it provides forward or reverse bias to a diode gate, depending on whether the bit is a logic "1" or "0", respectively. The bias on each diode gate is determined by the combination of input bit level and reference voltage applied to the gate. The transfer pulse generated by the first IOI signal is applied to 16 of the 32 diode

NOTE: C6 is removed for Options 028 and 029.

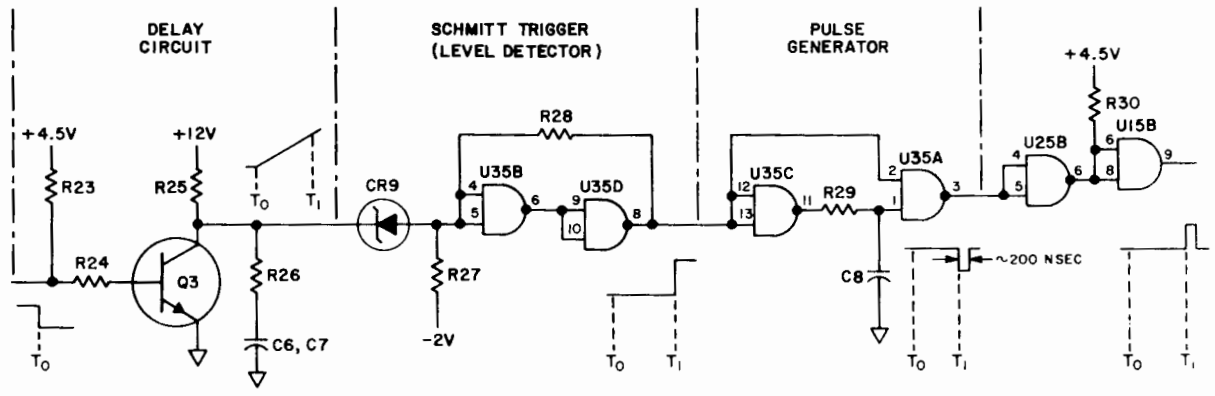


Figure 3-2. Delay Circuit

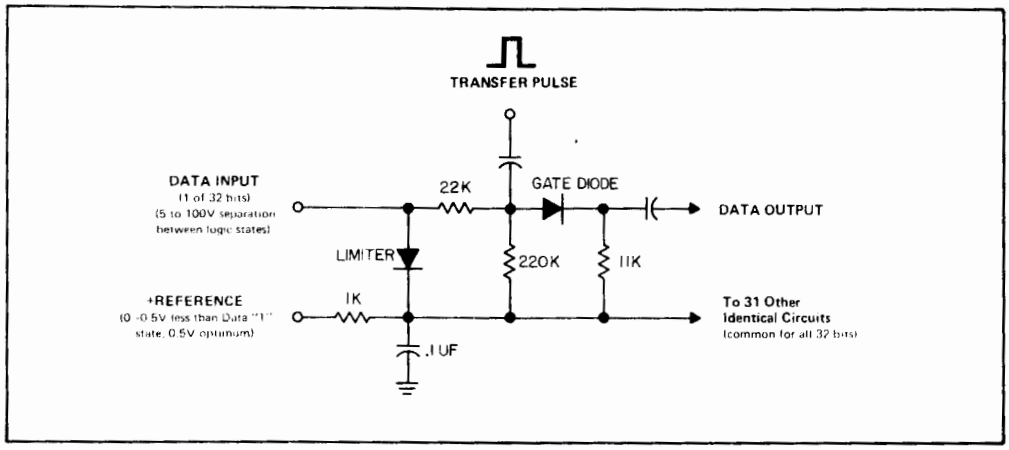


Figure 3-3. Typical Data Input Circuit

gates and enables those that are either forward (or zero) biased or only slightly reverse biased. (Bias is zero in the absence of BCD input or when the BCD and reference levels are equal.)

3-27. The IOI pulse gated through U36B (see Figure 3-4) is applied as a high input to a gate at the output of each of the 32 transfer circuits. If the corresponding diode gate is enabled, the transfer circuit output is true and a logic "1" is gated to the computer. If the diode gate is not enabled, the transfer circuit output remains false and the inhibited output gate provides a logic "0" to the computer.

3-28. The 16 data bits for the four least significant BCD digits (10^0 through 10^3) are gated through the transfer circuits and onto the IOBI-0 through IOBI-15 lines by the first IOI signal. The trailing edge of this IOI signal sets the Input Control FF. The second IOI signal is "anded" with the set output of the Input Control FF by gate U26A to produce the transfer pulse for the other 16 diode gates. The output of gates U26A and U36B enable the transfer of the second 16 data bits (BCD digits 10^4 through 10^7). The trailing edge of this IOI signal resets the Input Control FF.

3-29. Little or no current is drawn from the data source by a diode gate that is forward biased. When a diode gate is reverse biased, current drawn from the source is equal to the voltage difference between the data-bit "0" level and the positive reference voltage divided by approximately 243 kilohms.

3-30. A CLF instruction is required to remove the Hold signal (or apply Encode) to the data source and thus initiate another input operation. At the completion of the input operations, a CLC instruction should be programmed to reset the Interrupt Control FF and thus release the DSI card from the priority interrupt system. Note that after the CLC, another CLF signal can still apply an Encode signal to the data source (with the ENCODE switch closed). The output of the Interrupt Control FF, however, also inhibits gate U25C which prevents both the removal of a Hold signal to the data source and effective circuit response to a Record Command from the data source. Note that CLF can apply the Encode signal only when jumper W8 is in position B.

3-31. Refer to the Input/Output System Operation volume of the computer manual for a more detailed description of the following circuits:

a. Flag logic;

b. Control logic;

c. Select Code logic;

d. Skip Flag logic;

e. Interrupt logic.

3-32. Figure 3-5 contains logic diagrams of the integrated circuits according to HP part number. Appendix A provides a key to the logic symbology used in this manual.

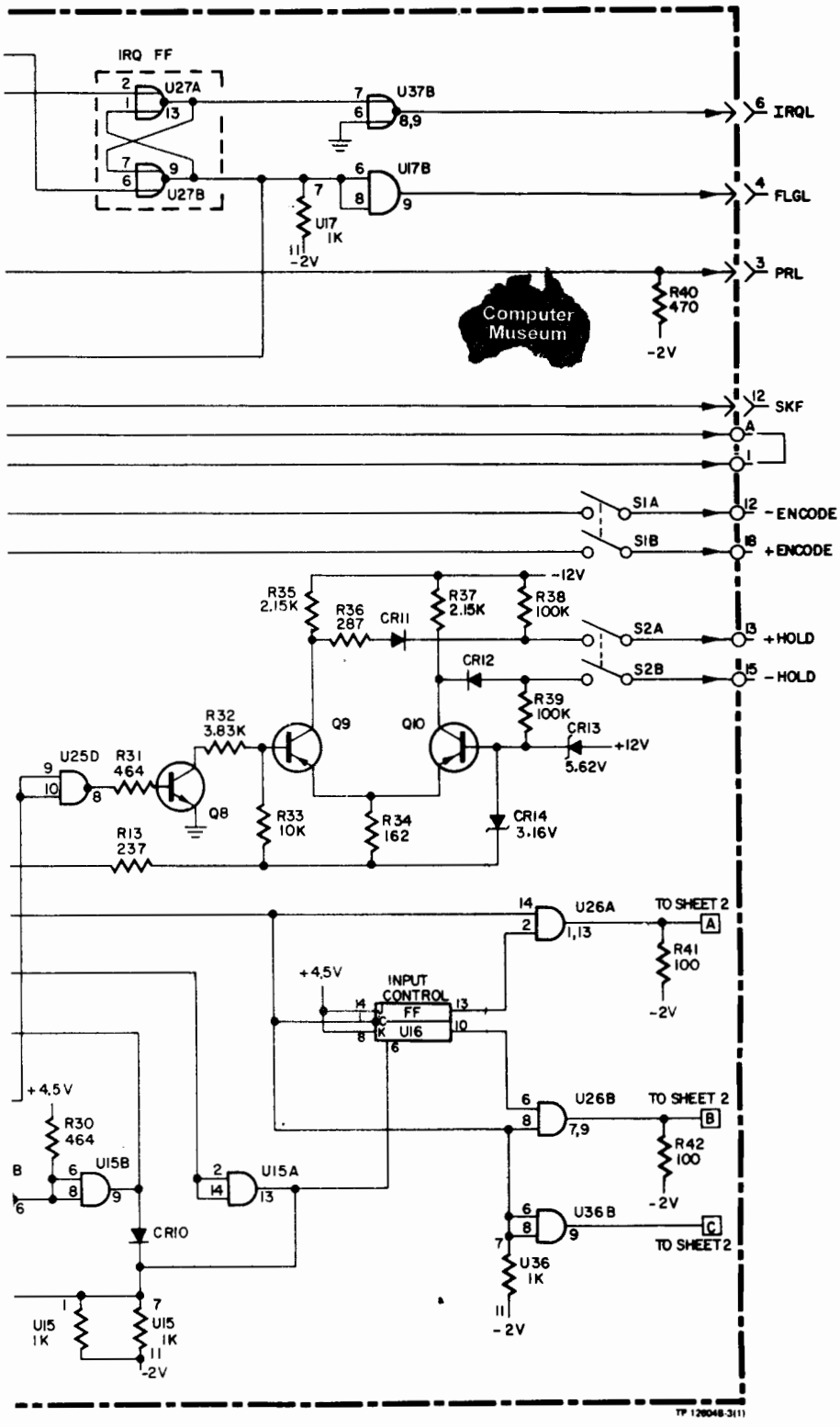
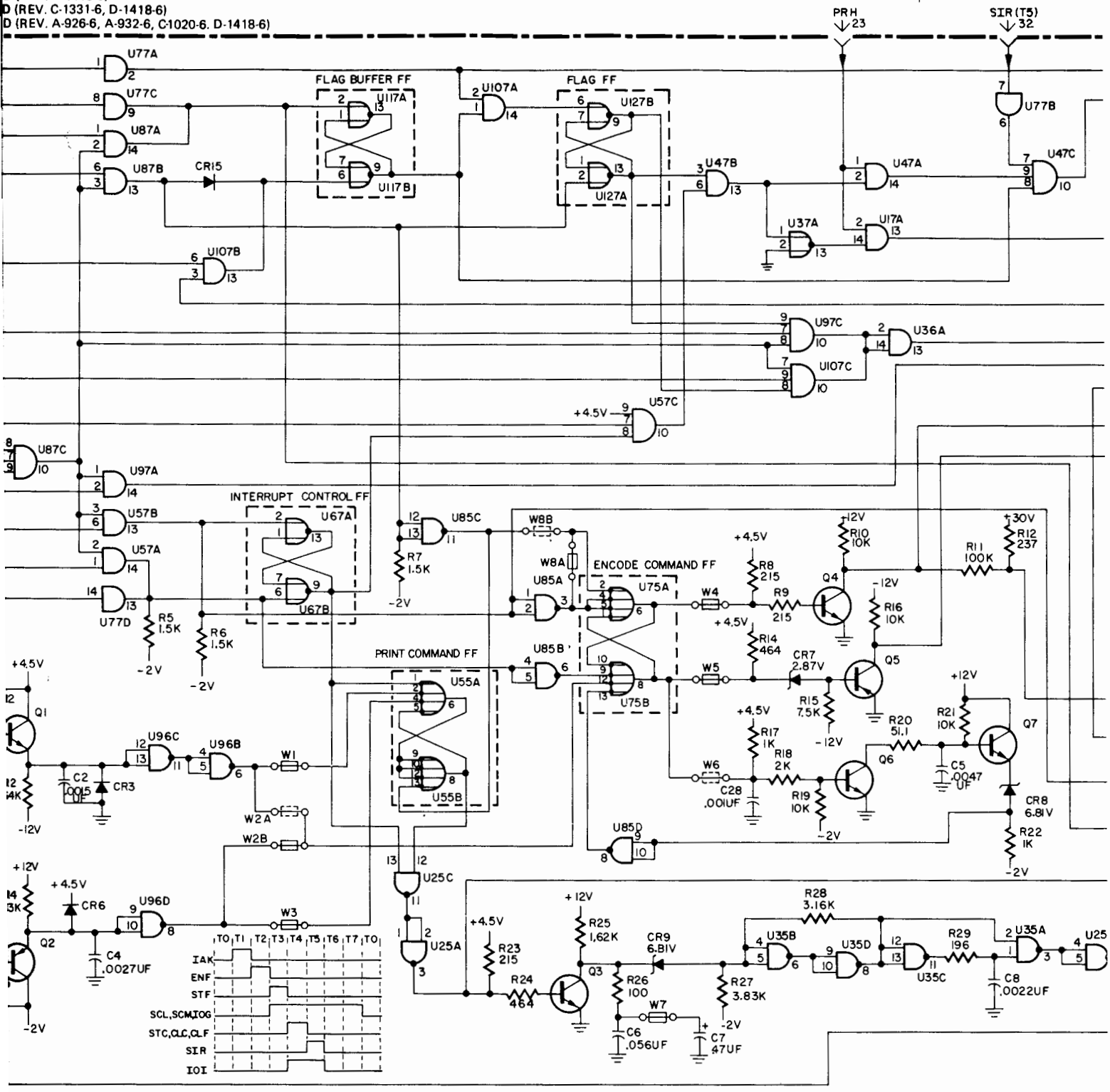


Figure 3-4. 12604B Data Source Interface
(Sheet 1 of 2)

D (REV. D-1418-6)
D (REV. C-1331-6, D-1418-6)
D (REV. A-926-6, A-932-6, C-1020-6. D-1418-6)



TES

D DENOTES 48 PIN CONNECTOR. ON REV. A-926-6, R1 IS 100K (NOT COMPATIBLE WITH HP 3450A)

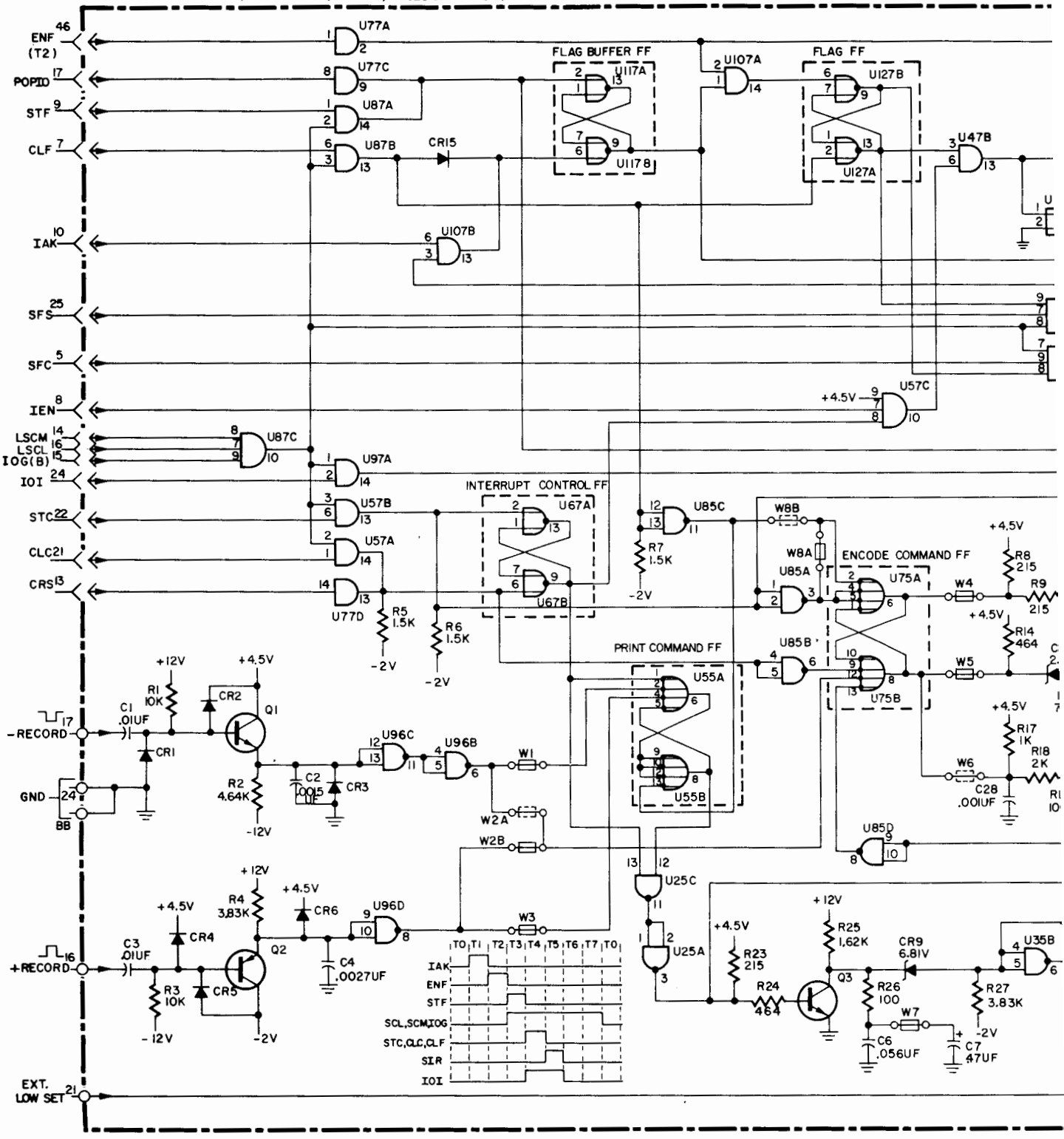
IS EQUIVALENT TO

3. REVISION C-1020-6 ADDED W8.

4. FOR OPTION 028, C6 IS REMOVED. ALSO, CAPACITANCE VALUES SHOWN ON SHEET 2 OF 2 FIGURE 3-4, CIRCUITS A AND B ARE CHANGED AS FOLLOWS: C100 AND C102 ARE CHANGED TO 330pf. THIS CHANGE IS THE SAME THROUGH EACH OF THE 16 CIRCUITS.

5. CR254 IS USED ONLY ON 12604-60011. R62 IS 100 OHMS ON 12604-60011.

12604-60011 DSI CARD (REV. D-1418-6)
12604-60010 DSI CARD (REV. C-1331-6, D-1418-6)
12604-60001 DSI CARD (REV. A-926-6, A-932-6, C-1020-6, D-1418-6)



NOTES

○ DENOTES 48 PIN CONNECTOR.

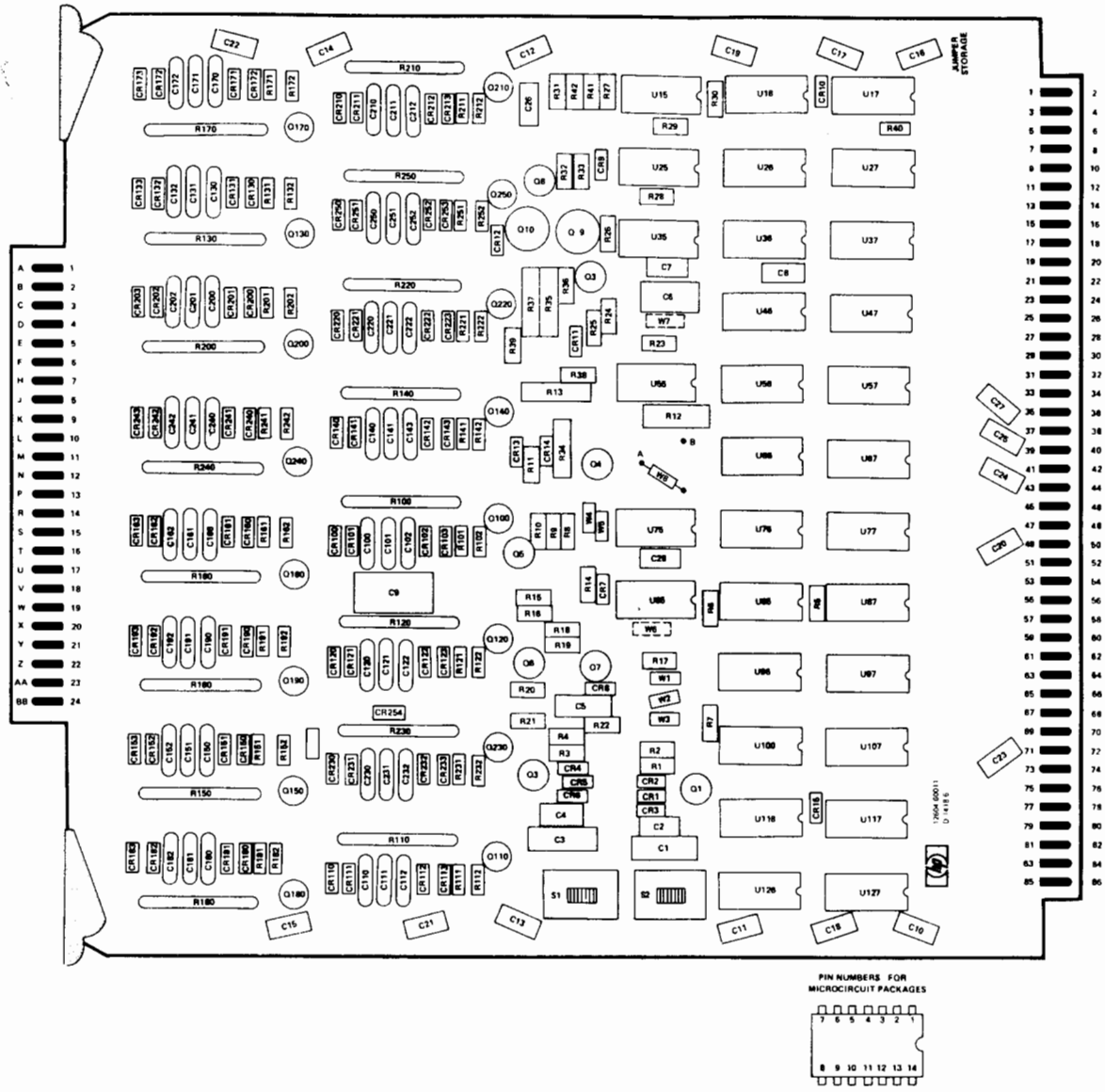
1. ON REV. A-926-6, R1 IS 100K (NOT COMPATIBLE WITH HP 3450A)

2. IS EQUIVALENT TO

3. REVISION C-1020-6 ADDED W8.

4. FOR OPTION 028, C6 IS REMOVED. ALSO, CAPACITANCE VALUES SHOWN ON SHEET 2 OF 2 FIGURE 3-4, CIRCUITS A AND B ARE CHANGED AS FOLLOWS: C100 AND C102 ARE CHANGED TO 330pf. THIS CHANGE IS THE SAME THROUGH EACH OF THE 16 CIRCUITS.

5. CR254 IS US
R62 IS 100 O



PART NO. 12604-60011 (Option 029)

NOTE:

This illustration is also applicable to assemblies 12604-60001 and 12604-60010 (Option 029) with the exception of C6, CR254, and W8. See schematic notes 3, 4, and 5 on this page for details.

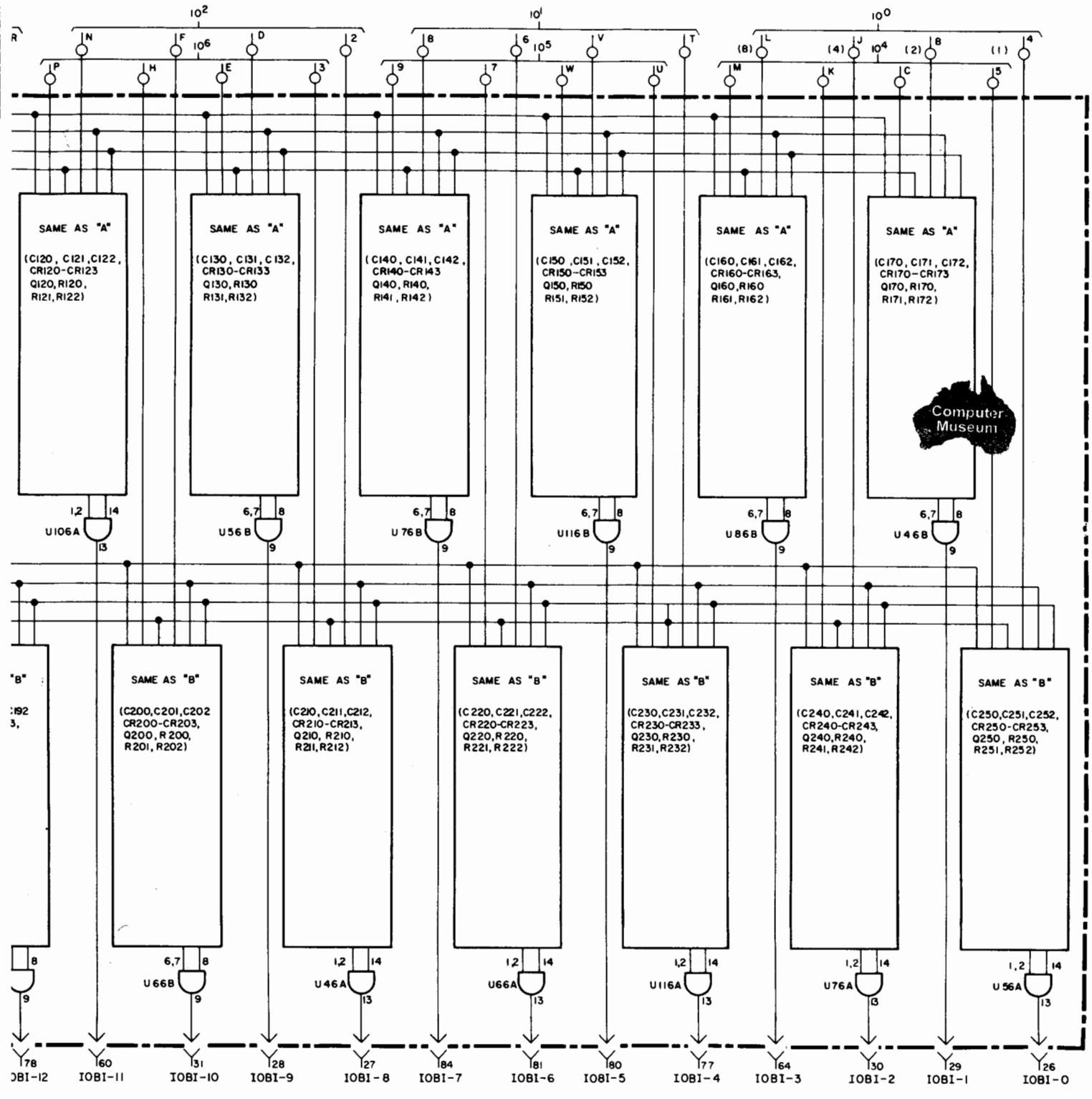
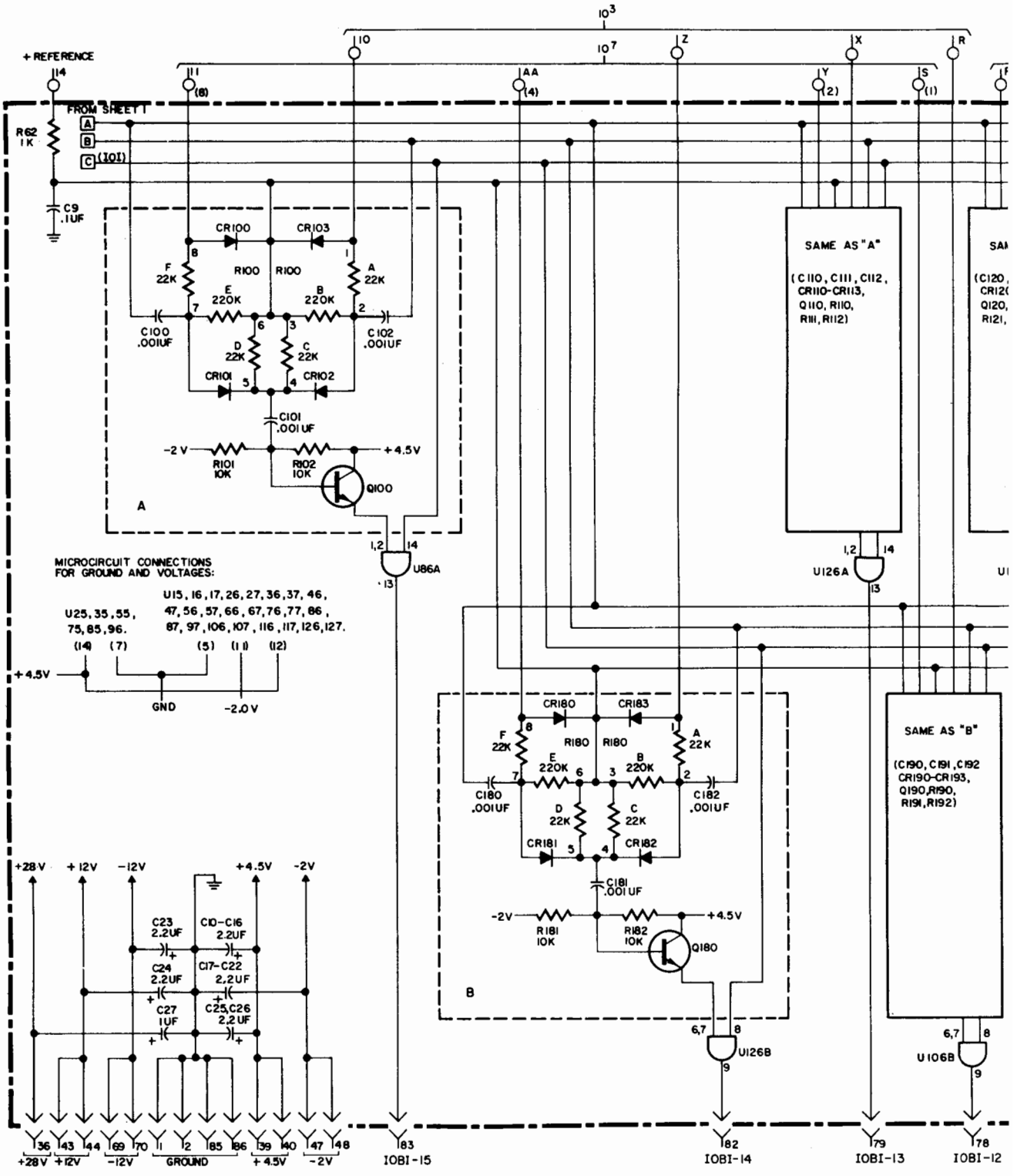
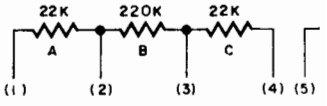


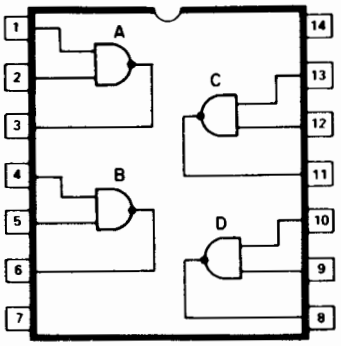
Figure 3-4. 12604B Data Source Interface (Sheet 2 of 2)



SEE SHEET 1 FOR NOTES.

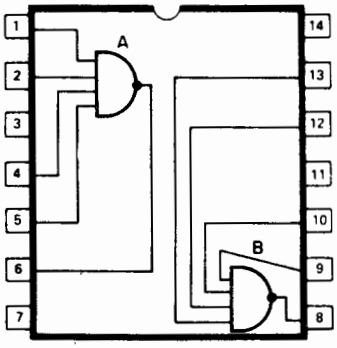
RESISTOR PACK





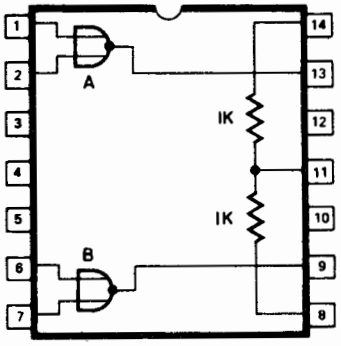
1820-0054
Type: TTL

Vcc = Pin 14
GND = Pin 7



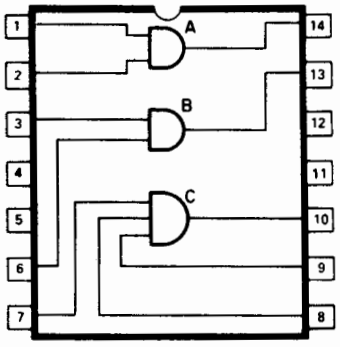
1820-0071
Type: TTL

Vcc = Pin 14
GND = Pin 7



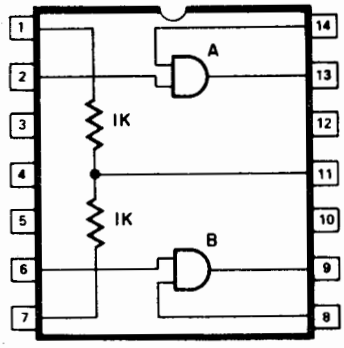
1820-0952
Type: CTL

Vcc = Pin 12
GND = Pin 5



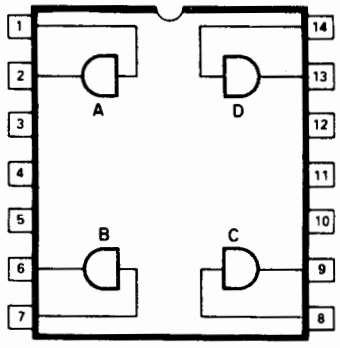
1820-0953
Type: CTL

Vcc = Pin 12
GND = Pin 5



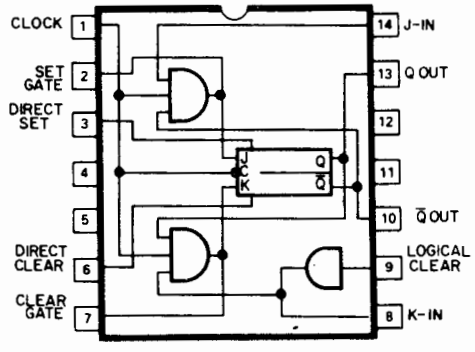
1820-0956
Type: CTL

Vcc = Pin 12
GND = Pin 5



1820-0965
Type: CTL

Vcc = Pin 12
GND = Pin 5



1820-0967
Type: CTL

Description: Dual-rank J-K flip-flops with direct set and clear inputs and complementary Q and $\overline{Q}$ outputs. If the J input is high, the output flip-flop is set (Q high, $\overline{Q}$ low) by the trailing edge of the clock pulse. If the K input is high, the clock pulse trailing edge resets the output flip-flop. If both the J and K inputs are high, the clock pulse trailing edge switches the flip-flop's initial state (set or reset) to the opposite state.

Vcc = Pin 12
VEE = Pin 11
GND = Pin 5

Figure 3-5. Logic Diagrams for Integrated Circuits, Top View

SECTION IV
MAINTENANCE

4-1. INTRODUCTION

4-2. This section contains the diagnostic test procedure, troubleshooting tables, and timing diagrams (Figures 4-1 through 4-11.) Flowcharts for the diagnostic program are in Appendix D.

4-3. DIAGNOSTIC TEST DESCRIPTION

4-4. The diagnostic test is used to check the HP 12604B Data Source Interface Card for correct operation and to aid in troubleshooting. The program for the diagnostic test consists of a background control program which calls test routines as requested through the SWITCH REGISTER, or DISPLAY REGISTER in the HP 2100/21MX, and the service routines. The service routines configure the program with respect to the select code of the DSI card and the model of HP computer being used. Diagnostic messages and requests to the operator are printed on a teleprinter.

4-5. TEST ROUTINES

4-6. There are six test routines which are called directly from the SWITCH REGISTER, or DISPLAY REGISTER, and three additional routines which are called indirectly. The routines called directly are:

a. Initial Test, which checks the condition of the card following Preset;

b. Basic Timing Test, which checks the flag, control, and interrupt circuitry;

c. Time Delay Test, which measures the line-settling time delay;

d. Input Test, which transfers data from the peripheral device (i.e., data source);

e. Hold Command Scope Loop, which removes and applies the Hold signal;

f. Encode Command Scope Loop, which removes and applies the Encode Command.

4-7. The three routines called indirectly are scope loops. Two of these routines check flag operation and are entered through the Basic Timing Test routine. The third is a scope loop for checking the line-settling time delay and is called through either the Basic Timing Test or the Time Delay Test.

4-8. HARDWARE REQUIRED

4-9. The hardware required to perform the diagnostic test of the DSI card is as follows:

a. An HP computer (HP 2100, HP 21MX, HP 2114, HP 2115, or HP 2116).

b. Teleprinter (an HP 2752A which is a modified Teletype Model ASR-33 or an HP 2754B which is a modified Teletype Model ASR-35) or CRT Terminal (HP 2640A) and associated interface card.

c. An input device to enter the program into memory (e.g., an HP 2748B High Speed Punched Tape Reader) and required interface card and cable. (The teleprinter is used if a faster input device is not available.)

d. Peripheral device (e.g., HP 2402A Integrating Digital Voltmeter) and its associated data cable.

e. DSI card with its jumpers (W1 through W8) in the proper positions for the particular peripheral device being used, and with the ENCODE and HOLD switches (S1 and S2) properly set. (Refer to Paragraph 2-8 and Table 2-2.)

NOTE

For Option 028, jumper W7 must be installed to avoid invalid error messages. The 20 sec time delay obtained with W7 removed can be checked by the time delay scope loop.

f. An HP 180A Oscilloscope (or equivalent) for viewing the waveforms in the timing diagrams.

4-10. SOFTWARE REQUIRED

4-11. The software required to test the DSI card is as follows:

a. A binary program tape (DSI Diagnostic Test Tape, HP Part No. 20337-60001).

b. System Input/Output (SIO) Buffered Teleprinter Driver Tape (HP Part No. 24127-60001).

4-12. INSTALLATION

4-13. Install the DSI card and teleprinter interface card in the computer, as follows:

a. Place the DSI card in an I/O slot of the computer such that every slot of higher priority has either another I/O card or a priority jumper card in it. If troubleshooting, use an extender card between the computer and the DSI card.

b. Connect the peripheral device to the card using the data cable. Turn the device on and set its controls for automatic (external) operation. (Note: For HP digital voltmeters this does not include external programming of range and function.)

c. Place the teleprinter interface card in an appropriate I/O slot.

d. Connect the teleprinter to its interface card.

4-14. PRELIMINARY PROCEDURES

4-15. The following procedures describe the basic load and run operations for the HP family of computers. Refer to the procedures in Paragraphs 4-15A, 4-16, 4-18, and 4-20 for the HP 21MX, HP 2100, HP 2114, HP 2115, and HP 2116 respectively.

4-15A. MODEL HP 21MX

4-15B. The following is the preliminary procedure for the Model HP 21MX Computer.

a. Turn on the HP 21MX Computer and the peripherals.

b. Place the SIO Teleprinter Driver tape in the Tape Reader.

c. Press Register Select, as required, to select the S-register for display in the Display Register. The light associated with the S-register will be on once the S-register is selected.

d. Press CLEAR DISPLAY to clear the contents of the Display Register. Since bits 15 and 14 are cleared at this time, the paper tape loader ROM will be selected.

e. Change bits 6 through 11 of the Display Register to the octal select code of the paper tape reader. Pressing the upper half of the corresponding Display Register switch sets that bit to a '1' (the associated light will be on), while pressing the lower half of the switch sets that bit to a '0' (the associated light will be off).

Since bits 0 through 5, 12, and 13 are not used in conjunction with the paper tape loader, they are ignored.

f. Press STORE to store the contents of the Display Register in the S-register.

g. Press IBL to load the contents of the paper tape loader ROM into the uppermost 64 locations in the first 32K of directly addressable memory.

A successful load is indicated if the OVERFLOW light remains off. An unsuccessful load is indicated if the OVERFLOW light is on; this will occur if the select code programmed in step c was less than 10 (octal) or if a memory hardware fault is detected.

h. Press PRESET to initialize the computer.

i. Press RUN to start the paper tape loader program. The associated light will be on and the program will be loaded from the paper tape reader into memory.

When the processor halts, the associated light will be turned off and the T-register will automatically be selected for display in the Display Register. A successful program load is indicated if the contents of the Display Register are 102077 (octal). If the halt code displayed is not 102077 (octal), one of two possible error condition halt codes will be displayed. If the halt code displayed is 102055 (octal), an address error is indicated. Check to ensure that the proper tape was used or that the tape was not installed backwards. If the halt code displayed is 102011 (octal), a checksum error is indicated. Check for a possible defective or dirty tape or tape reader.

j. Remove and rewind the SIO Teleprinter Driver tape.

k. Place the Diagnostic tape in the Tape Reader.

l. Sequentially press the following:

1. IBL
2. PRESET
3. RUN

m. The computer loads the tape and stops as described in step i above.

n. Remove and rewind the Diagnostic tape.

NOTE

In order to avoid loading two tapes each time the diagnostic test is run, a combined tape may be generated by using the combining procedure (SIO sump) given in the computer operating manual. If a combined tape is prepared, perform steps a through i above.

o. Select P-register for display and set display to 000002.

p. Press STORE.

q. Select S-register for display and set the display to the Teleprinter I/O address (octal Select Code).

r. Sequentially press the following:

1. STORE
2. PRESET
3. RUN

The computer halts with 102077 in the Display Register.

4-16. MODEL HP 2100

4-17. The following is the preliminary procedure for the model HP 2100 Computer.

a. Turn on the HP 2100 Computer and the peripherals.

b. Place the SIO Teleprinter Driver tape in the Tape Reader.

c. Press S pushbutton to select the S-Register and to display the S-Register contents in the DISPLAY REGISTER.

d. Press CLEAR DISPLAY pushbutton to clear the S-Register.

e. Press P pushbutton to select the P-Register and display the P-Register contents on the DISPLAY REGISTER.

f. Set DISPLAY REGISTER to the starting address of the basic binary loader. See Table 4-1.

g. Press EXTERNAL PRESET and INTERNAL PRESET pushbuttons.

h. Press LOADER ENABLE, and then press RUN pushbuttons.

The computer loads the tape and stops. The LOADER ENABLE and the RUN lights go out, the HALT and the MEMORY DATA lights go on, and the DISPLAY REGISTER should indicate 102077. If the halt code is not 102077 when the device stops, there has been an error in the loading process. Two possible error conditions are indicated by the loader, which changes the halt code to identify the type of error. A halt code of 102055 indicates an address error; check if the proper tape is being read, or if it is in backwards. A halt code of 102011 indicates a checksum error; check for a bad or dirty tape or tape reader.

Table 4-1. Loader Starting Addresses

MEMORY SIZE	STARTING ADDRESS OF LOADER
4K	0 7 7 0 0
8K	1 7 7 0 0
12K	2 7 7 0 0
16K	3 7 7 0 0
24K	5 7 7 0 0
32K	7 7 7 0 0

i. Remove and rewind the SIO Teleprinter Driver tape.

j. Place the diagnostic tape in the Tape Reader.

k. Sequentially, press the following pushbuttons:

1. EXTERNAL PRESET
2. INTERNAL PRESET
3. LOADER ENABLE
4. RUN

The computer loads the tape and stops as described in step h.

l. Remove and rewind the diagnostic tape.

NOTE

In order to avoid loading two tapes each time the diagnostic test is run, a combined tape may be generated by using the combining procedure (SIO dump) given in the computer operating manual. If a combined tape is prepared, perform steps a through h above.

m. Press P pushbutton and set DISPLAY REGISTER to 000002.

n. Press S pushbutton and set the DISPLAY REGISTER to the teleprinter I/O address (octal select code).

o. Press EXTERNAL PRESET, INTERNAL PRESET, and then RUN. The computer halts with the MEMORY DATA pushbutton on and 102077 in the DISPLAY REGISTER.

4-18. MODEL HP 2114

4-19. The following is the preliminary procedure for the model HP 2114 Computer.

a. Turn on the computer and peripherals.

b. Place the SIO Teleprinter Driver tape in the Tape Reader.

c. Press CLEAR REGISTER.

d. Press PRESET and LOAD simultaneously.

The computer loads the tape, lights the HALT touchbutton, and indicates 102077 in the MEMORY DATA REGISTER. If the MEMORY DATA REGISTER does not read 102077 when the device stops, there has been an error in the loading process. Two possible error conditions are indicated by the loader, which changes the halt code to identify the type of error. A halt code of 102055 indicates an address error; check if the proper tape is being read, or if it is in backwards. A halt code of 102011 indicates a checksum error; check for a bad or dirty tape or tape reader.

e. Remove and rewind the SIO Teleprinter Driver tape.

f. Place the diagnostic tape in the Tape Reader.

g. Press PRESET and LOAD simultaneously. Computer loads the tape, lights the HALT touchbutton, and indicates 102077 in the MEMORY DATA REGISTER.

h. Remove and rewind the diagnostic tape.

NOTE

In order to avoid loading two tapes each time the diagnostic test is run, a combined tape may be generated by using the combining procedure (SIO dump) given in the computer operating manual. If a combined tape is prepared, perform steps a through d above.

i. Set SWITCH REGISTER to 000002.

j. Press LOAD ADDRESS.

k. Set teleprinter I/O address (octal select code) into the SWITCH REGISTER.

l. Press RUN. Computer halts with 102077 in the MEMORY DATA REGISTER.

4-20. MODELS HP 2115 AND HP 2116

4-21. The following preliminary procedures are applicable to both models HP 2115 and HP 2116.

a. Turn on the computer and the peripherals.

b. Place the SIO Teleprinter Driver tape in the Tape Reader.

c. Set the SWITCH REGISTER to the starting address of the basic binary loader. See Table 4-1.

d. Press LOAD ADDRESS.

e. Set LOADER switch to ENABLED.

f. Press PRESET, then press RUN. Computer loads the tape and halts with 102077 in the T-REGISTER. If the T-REGISTER does not read 102077 when the device stops, there has been an error in the loading process. Two possible error conditions are indicated by the loader, which changes the halt code to identify the type of error. A halt code of 102055 indicates an address error; check if the proper tape is being read, or if it is in backwards. A halt code of 102011 indicates a checksum error; check for a bad or dirty tape or tape reader.

g. Remove and rewind the SIO Teleprinter Driver tape.

h. Place the diagnostic tape in the Tape Reader.

i. Press PRESET, then press RUN. Computer loads the tape and halts with 102077 in the T-REGISTER.

j. Set LOADER switch to PROTECTED.

k. Remove and rewind the diagnostic tape.

NOTE

In order to avoid loading two tapes each time the diagnostic test is run, a combined tape may be generated by using the combining procedure (SIO dump) given in the computer operating manual. If a combined tape is prepared, perform steps a through f, above, to load the tape and then perform steps j and k; omit steps l through o, below.

l. Set the SWITCH REGISTER to 000002.

m. Press LOAD ADDRESS.

n. Set teleprinter I/O address (octal select code) into the SWITCH REGISTER.

o. Press RUN. Computer halts with 102077 in the T-REGISTER.

4-22. DIAGNOSTIC TEST PROCEDURE

4-23. After completing the preliminary procedure (Paragraphs 4-14 through 4-21), perform the diagnostic test applicable to the type computer.

4-23A. MODEL HP 21MX

4-23B. The following is the diagnostic procedure for the HP 21MX Computer.

a. Select P-register for display.

b. Set the Display Register to 000100.

c. Sequentially press the following:

1. STORE
2. CLEAR DISPLAY
3. PRESET
4. RUN

d. The teleprinter will print:

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WHAT COMPUTER MODEL?

e. Use the teleprinter and type "21MX", followed by a line termination (Carriage RETURN, LINE FEED).

f. The teleprinter will print:

I/O CHANNEL?

g. Type the address (octal select code) of the DSI card, followed by a line termination.

h. The teleprinter will print:

TYPE "1" FOR 1.0 MSEC DELAY.

TYPE "0" FOR 0.1 MSEC DELAY.

i. Type a 1 or a 0, followed by a line termination. The delay referred to is the line settling delay which is 1.0 msec if jumper W7 is in place and is 0.1 msec if W7 is removed.

j. The teleprinter will print the following and then halt:

CONNECT PERIPHERAL DEVICE AND PUSH RUN

k. With the peripheral device connected, press RUN.

l. The program will loop until a desired test is selected by using the DISPLAY REGISTER. Refer to Program Control (Paragraph 4-30).

m. When the Initial Test is selected (pushbutton 3 lit) the teleprinter will print the following and halt:

PUSH PRESET THEN RUN

n. Push PRESET, and then push RUN. If no errors are detected (refer to Error Messages, Paragraph 4-44), the teleprinter will print the following and halt:

STATIC TEST FOR STATE OF FLIP-FLOPS AND LEVELS OF HOLD AND ENCODE LINES

The proper flip-flop states and line levels are listed in Tables 4-2 and 4-3.

o. When any other test is selected it is performed with no teleprinter messages unless an error is detected (refer to Paragraph 4-44).

4-24. MODEL HP 2100

4-25. The following is the diagnostic procedure for the model HP 2100 Computer.

a. Press the P pushbutton.

b. Set the DISPLAY REGISTER to 000100.

c. Sequentially, press the following pushbuttons:

1. S
2. CLEAR DISPLAY
3. EXTERNAL PRESET
4. INTERNAL PRESET
5. RUN

d. The teleprinter will print:

12604 DIAGNOSTIC PROGRAM - date of version

WHAT COMPUTER MODEL?

e. Use the teleprinter and type "2100", followed by a line termination (Carriage RETURN, LINE FEED).

f. The teleprinter will print:

I/O CHANNEL?

g. Type the address (octal select code) of the DSI card, followed by a line termination.

h. The teleprinter will print:

TYPE "1" FOR 1.0 MSEC DELAY.

TYPE "0" FOR 0.1 MSEC DELAY.

i. Type a 1 or a 0, followed by a line termination. The delay referred to is the line settling delay which is 1.0 msec (Opt. 028 is 900 μsec) if jumper W7 is in place, and is 0.1 msec (Opt. 028 is 10 μsec) if W7 is removed.

j. The teleprinter will print the following and then halt:

CONNECT PERIPHERAL DEVICE AND PUSH RUN

k. With the peripheral device connected, press RUN.

l. The program will loop until a desired test is selected by using the DISPLAY REGISTER. Refer to Program Control (Paragraph 4-30).

m. When the Initial Test is selected (pushbutton 3 lit) the teleprinter will print the following and halt:

PUSH PRESET THEN RUN

n. Push INTERNAL PRESET, and then push RUN. If no errors are detected (refer to Error Messages, Paragraph 4-44), the teleprinter will print the following and halt:

STATIC TEST FOR STATE OF FLIP-FLOPS AND LEVELS OF HOLD AND ENCODE LINES

The proper flip-flop states and line levels are listed in Tables 4-2 and 4-3.

o. When any other test is selected it is performed with no teleprinter messages unless an error is detected (refer to Paragraph 4-44).

4-26. MODEL HP 2114

4-27. The following is the diagnostic procedure for the model HP 2114 Computer.

Table 4-2. State of Flip-Flops After Preset

FLIP-FLOP	REFERENCE DESIGNATOR	STATE	PINS WITH LOGIC "1"	PINS WITH LOGIC "0"
Flag Buffer	U117	Set	1, 9	2, 6, 7, 13
Flag	U127	Set	7, 13	1, 2, 9
Interrupt Request (IRQ)	U27	Reset	7, 13	1, 2, 9
Interrupt Control	U67	Reset	7, 13	1, 2, 6, 9
Print Command	U55	Set	2, 4, 6, 9, 10, 12, 13	1, 5, 8
Encode Command	U75	Reset	1, 2, 4, 5, 8, 9, 12, 13	6, 10
Input Control	U16	Reset	8, 10, 14	1, 6, 13

NOTE: A logical "1" is approximately +3.0 Vdc and a logical "0" is approximately 0 Vdc or ground.

a. Set the SWITCH REGISTER to 000100 (this is the starting address).

b. Sequentially, press the following pushbuttons:

1. LOAD ADDRESS
2. CLEAR REGISTER
3. PRESET
4. RUN.

c. The teleprinter will print:

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WHAT COMPUTER MODEL?

d. Using the teleprinter keyboard, type "2114", followed by a line termination (Carriage RETURN, LINE FEED).

e. The teleprinter will print:

I/O CHANNEL?

f. Type the address (octal select code) of the DSI card, followed by a line termination.

g. The teleprinter will print:

TYPE "1" FOR 1.0 MSEC DELAY.

TYPE "0" FOR 0.1 MSEC DELAY.

h. Type a 1 or a 0, followed by a line termination. The delay referred to is the line settling delay which is 1.0 msec (Opt. 028 is 900 μsec) if jumper W7 is in place, and is 0.1 msec (Opt. 028 is 10 μsec) if W7 is removed.

i. The teleprinter will print the following and then halt:

CONNECT PERIPHERAL DEVICE AND PUSH RUN

j. With the peripheral device connected, press RUN.

k. The program will loop until a desired test is selected by using the SWITCH REGISTER. Refer to Program Control (Paragraph 4-30).

l. When the Initial Test is selected (touchbutton 3 lit) the teleprinter will print the following and halt:

PUSH PRESET THEN RUN

m. Push PRESET, and then push RUN. If no errors are detected (refer to Error Messages, Paragraph 4-45), the teleprinter will print the following and halt:

STATIC TEST FOR STATE OF FLIP-FLOPS AND LEVELS OF HOLD AND ENCODE LINES

The proper flip-flop states and line levels are listed in Tables 4-2 and 4-3.

n. When any other test is selected it is performed with no teleprinter messages unless an error is detected (refer to Paragraph 4-44).

Table 4-3. Levels of Hold and Encode Lines

FUNCTION	LEVEL (UNLOADED)	48-PIN CONNECTOR
+Encode	-12V	Pin 18
-Encode	+13.5V	Pin 12
+Hold	+17V	Pin 13
-Hold	-11V	Pin 15

4-28. MODELS HP 2115 AND HP 2116

4-29. The following is the diagnostic procedure for the models HP 2115 and HP 2116 Computers.

a. Set the SWITCH REGISTER to 000100 (this is the starting address).

b. Press LOAD ADDRESS, then clear the SWITCH REGISTER.

c. Press PRESET, then press RUN.

d. The teleprinter will print:

12604 DIAGNOSTIC PROGRAM - date of version

WHAT COMPUTER MODEL?

e. Using the teleprinter keyboard, type the model number of the computer being used for the test ("2115" or "2116"), followed by a line termination (Carriage RETURN, LINE FEED).

CAUTION

Timing is quite different for the HP 2115 and HP 2116. Take care to type the correct number.

f. The teleprinter will print:

I/O CHANNEL?

g. Type the address (octal select code) of the DSI card, followed by a line termination.

h. The teleprinter will print:

TYPE "1" FOR 1.0 MSEC DELAY.

TYPE "0" FOR 0.1 MSEC DELAY.

i. Type a 1 or a 0, followed by a line termination. The delay referred to is the line settling delay which is 1.0 msec (Opt. 028 is 900 μsec) if jumper W7 is in place, and is 0.1 msec (Opt. 028 is 10 μsec) if W7 is removed.

j. The teleprinter will print the following and then halt:

CONNECT PERIPHERAL DEVICE AND PUSH RUN

k. With the peripheral device connected, press RUN.

l. The program will loop until a desired test is selected by using the SWITCH REGISTER. Refer to Program Control (Paragraph 4-30).

m. When the Initial Test is selected (switch 3 up) the teleprinter will print the following and halt:

PUSH PRESET THEN RUN

n. Push PRESET, and then push RUN. If no errors are detected (refer to Error Messages, Paragraph 4-44), the teleprinter will print the following and halt:

STATIC TEST FOR STATE OF FLIP-FLOPS AND LEVELS OF HOLD AND ENCODE LINES

The proper flip-flop states and line levels are listed in Tables 4-2 and 4-3.

o. When any other test is selected it is performed with no teleprinter messages unless an error is detected (refer to Paragraph 4-44).

4-30. PROGRAM CONTROL

4-31. The diagnostic program is controlled by the SWITCH REGISTER as follows:

NOTE

For HP 2100 and HP 21MX Computers, switch X up corresponds to DISPLAY REGISTER bit X lit. For HP 2114 Computers, switch X up corresponds to SWITCH REGISTER switch X lit.

Switch 0 Up — Throw this switch up at any time to halt at beginning of program. HP 2100 and HP 21MX Computers will halt with the MEMORY DATA pushbutton lit and 102000 in the DISPLAY REGISTER. The HP 2114 MEMORY DATA REGISTER = 102000. The HP 2115 and HP 2116 will halt with the A, B, and T-REGISTERS = 102000. Pushing RUN will restart the programs at Paragraphs 4-23B(f), 4-25f, 4-27e, and 4-29f for models HP 21MX, HP 2100, HP 2114, HP 2115, and HP 2116 respectively.

Switch 1 Up — This switch will cause a halt at the end of any scope loop test. If switch 2 is up, switch 1 will be ignored.

Switch 2 Up — This switch will cause the program to loop for oscilloscope testing.

Switch 3 Up — Selects the Initial Test routine.

Switch 4 Up — Selects the Basic Timing Test routine.

Switch 5 Up — Selects the Time Delay Test routine.

Switch 6 Up — Selects the Input Test routine.

Switch 7 Up — Selects the Hold Command Scope Loop routine.

Switch 8 Up — Selects the Encode Command Scope Loop routine.

Switches 9 through 13 — Not Used.

Switch 14 Up — Causes selected test or tests to be repeated continuously. This switch must be up before selecting the desired test.

Switch 15 Up — This switch will inhibit all teleprinter messages with one exception. The message "PUSH PRESET THEN RUN" which is printed at the beginning of the Initial Test routine will not be inhibited.

NOTE

Unless switch 14 is up, clear the SWITCH REGISTER or DISPLAY REGISTER before going from one test routine to another.

4-32. OSCILLOSCOPE TEST

4-33. For oscilloscope tests, set switch 2 up and then select the desired test. For example, to enter the time delay scope loop, set switch 2 up and select the Time Delay Test (switch 5 up).

4-34. BASIC TIMING TEST

4-35. By using switches 1 and 2 to step through the Basic Timing Test, a number of scope loops can be entered successively if no errors are detected. Some of the loops are repeated since they are associated with the condition being tested. The loops are as follows:

a. First flag scope loop (using the SFS instruction), Figures 4-1 and 4-2;

b. Second flag scope loop (using the SFC instruction), Figures 4-3 and 4-4;

c. First flag scope loop;

d. Second flag scope loop;

e. Time delay scope loop (same as called from the Time Delay Test), Figure 4-5;

f. Time delay scope loop;

g. Interrupt test one (invalid interrupt), Figures 4-6 and 4-7;

h. Interrupt test two (valid interrupt), Figures 4-8 and 4-9.

4-36. The procedure for stepping through the scope loops listed in the preceding paragraph is as follows:

a. To enter the first flag scope loop, set switches 1 and 2 up and select the Basic Timing Test (switch 4 up).

b. To step to the next loop, set switch 2 down. The computer halts at the exit of the loop it is in. Set switch 2 up and press RUN.

c. Repeat step b to step from one loop to the next until the desired loop is reached.

4-37. A second version of the Encode Command Scope Loop can be entered by using switches 1 and 2 as described above to step through the first version.

4-38. COMBINATION TESTS

4-39. If switch 14 is set up, the operator may then select any combination of the following tests to be repeated:

a. Initial Test - Switch 3 up

b. Basic Timing Test - Switch 4 up

c. Time Delay - Switch 5 up

d. Input Test - Switch 6 up

4-40. Any one or more of the above tests can be continuously repeated using switch 14. If the Initial Test is selected, the teleprinter will print "PUSH PRESET THEN RUN" and the computer will halt for this to be done each time the Initial Test is entered.

4-41. INPUT TEST

4-42. For useful operation of the Input Test, the program should loop such that the data can be read from the Teleprinter and compared with the known code from the peripheral device being used. The Teleprinter will output the two 16-bit words of the code as an 8-digit number. For the HP 2401C or HP 2402 DVM, this output is

RANGE	FUNC-TION	10^5	10^4	10^3	10^2	10^1	10^0
		DATA					

Switch 6 may be alternately turned on and off to change and observe the input data.

4-43. To terminate the test while computer is halted, select the S-register for display. Press CLEAR DISPLAY and RUN pushbuttons.

4-44. ERROR MESSAGES

4-45. There are two possible error messages printed by the Initial Test. These messages are quite self-explanatory.

a. FLAG NOT SET BY PRESET. Check for continuity of POPIO signal path. Another possibility is failure of the SFS or SFC signal paths which can be checked using the appropriate flag scope loop routine.

b. INT. CONT. FF NOT CLEARED BY PRESET. The CRS signal is not getting to the Interrupt Control FF. Both flag scope loop routines use the CRS signal for a scope trigger. This allows the troubleshooter to trace the CRS signal path.

4-46. In the Basic Timing Test, error messages are printed as follows:

ERROR XX

where XX is an octal number from 00 to 11. The error numbers are defined in Table 4-4. Timing diagrams are associated with each error number. The timing diagrams show the proper timing sequences that occur in the particular scope loop. By referring to the timing diagrams and the schematic diagram, the troubleshooter should be able to locate the faulty component. A logical "1" on the timing diagram is approximately +3.0 Vdc and a logical "0" is approximately 0 Vdc or ground.

4-47. There are two possible error messages that may be printed during the Time Delay Test. These are quite self-explanatory. The computer will halt after the message is printed and the operator should check to see that the correct time delay was specified in steps h and i of Paragraph 4-23B, steps h and i of Paragraph 4-25, g and h of Paragraph 4-27, and h and i of Paragraph 4-29. If the specified delay does not correspond to the condition of W7, set switch 0 up and press RUN to halt the computer at the beginning of the program. Then set switch 0 down and press RUN to enter the proper delay; repeat the Time Delay Test. If the delay was properly specified, set switch 2 up and press RUN. This causes the time delay scope loop to be entered. The proper timing diagram is shown in Figure 4-5. The error messages are:

a. DELAY TIME TOO SHORT.

b. DELAY TIME TOO LONG.

4-48. The only error detected by the computer during the Input Test is the lack of response from the peripheral device. The message printed is:

WAITING TOO LONG

This error message could be an indication of failure or improper set-up of the peripheral device. It could also indicate a failure in the Record Command circuitry of the DSI card. Check that the proper switch (ENCODE or HOLD) on the DSI card is "on" and the other switch "off". If these are correct, clear the SWITCH REGISTER and press RUN. Set switch 2 up and select either the Hold Command scope loop or the Encode Command scope loop (use the loop appropriate for the peripheral device being used). Observe the Record Command circuits with an oscilloscope. An error is detected if the Record Command occurs more than 1.3 seconds after the Encode or the removal of Hold on an HP 2100 Computer: 2.2 seconds when using an HP 2114 or HP 2115, or 1.7 seconds for the HP 2116 Computer, or 1.2 seconds for the HP 21MX Computer.

Table 4-4. Error Codes for Basic Timing Test

ERROR CODE	SCOPE LOOP ROUTINE	TIMING DIAGRAMS	POSSIBLE CAUSE
00	First Flag	Figures 4-1 and 4-2	SFS instruction causing a skip with flag cleared. Flag is not clearing.
01	Second Flag	Figures 4-3 and 4-4	SFC instruction not causing a skip with flag cleared.
02	First Flag	Figures 4-1 and 4-2	SFS instruction not causing a skip with flag set. Flag is not setting.
03	Second Flag	Figures 4-3 and 4-4	SFC instruction is causing a skip with flag set.
04	Time Delay	Figure 4-5	Time delay so short that setting the Print Command Flip-Flop immediately sets the flag.
05	Time Delay	Figure 4-5	Print Command FF not setting with CLC signal. Time delay too long (possibly infinite).
06	Time Delay	Figure 4-5	This is an unlikely error since it repeats error 04.
07	Time Delay	Figure 4-5	Print Command FF not setting with CRS signal.
10	Interrupt One	Figures 4-6 and 4-7	An interrupt is being generated with the flag cleared. Check operation of Interrupt Request (IRQ) FF.
11	Interrupt Two	Figures 4-8 and 4-9	The interrupt circuitry is not generating a desired interrupt. Check operation of IRQ FF and the gates which set it.
NOTE: In each case set switch 2 up and press RUN to enter loop routine.			

NOTE

For the diagnostic test, select a gate time of one second (or less) for the data source.

4-49. If the operator detects an error in the observed data input from the peripheral device, an oscilloscope can be used to trace the data lines while looping in the Input Test (switches 2 and 6 up).

4-50. Timing diagrams show the oscilloscope patterns expected in the Hold Command Scope Loop (Figure 4-10) and the Encode Command Scope Loop (Figure 4-11).

4-51. ADDITIONAL DIAGNOSTIC INFORMATION

4-52. If an error is detected and the test is continued without first correcting the error, additional error messages may be erroneous. An interrupt from any other I/O device at any time will halt the program. The address (octal select code) of the interrupting device is the last six bits of the T-REGISTER (MEMORY DATA Register).

4-53. If switch 15 is set up, the effects on the diagnostic test are:

a. All output messages are inhibited any time steps d through k of Paragraph 4-23B, steps j through q of Paragraph 4-25, steps c through j of Paragraph 4-27; and steps d through k of Paragraph 4-29. The program waits for the appropriate input messages in the proper order and then goes without halting to the appropriate step below:

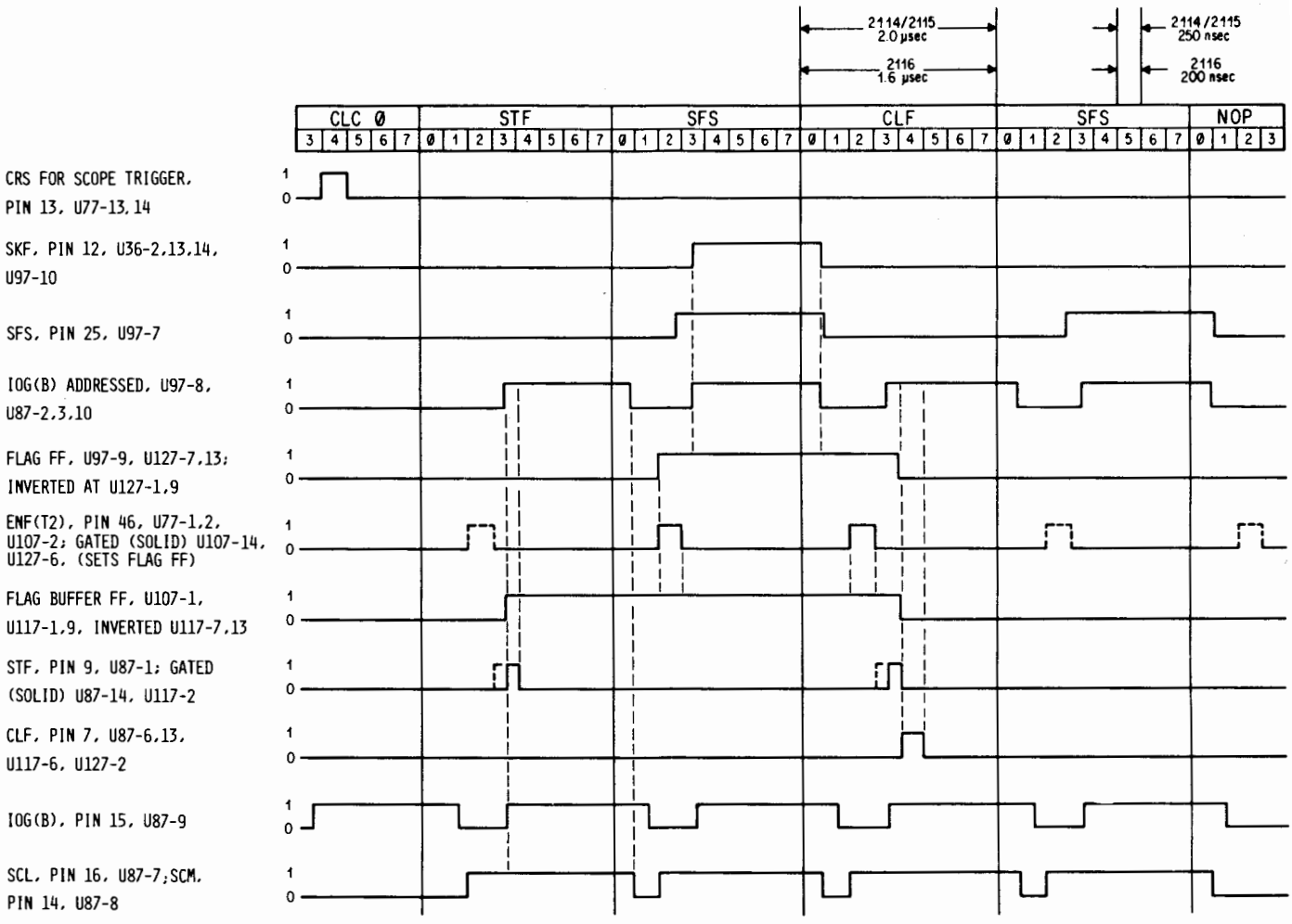
1. Paragraph 4-23B(l) for the HP 21MX
2. Paragraph 4-25(l) for the HP 2100
3. Paragraph 2-47(k) for the HP 2114
4. Paragraph 4-29(l) for the HP 2115 and HP 2116.

b. For the Basic Timing Test, the computer halts with the error number in the A-REGISTER when errors are detected. No error message is printed.

c. For the Initial Test, the error messages are not inhibited. The static test portion is skipped.

d. For the Time Delay Test, the computer halts with 102055 in the T-REGISTER (MEMORY DATA Register) for either long or short delay. No message is printed.

e. For the Input Test, the computer halts with 102066 in the T-REGISTER when the peripheral device does not respond. No message is printed.



NOTE: ALL "PIN" NUMBERS REFER TO 86 PIN CONNECTOR.

Figure 4-1. First Flag Scope Loop

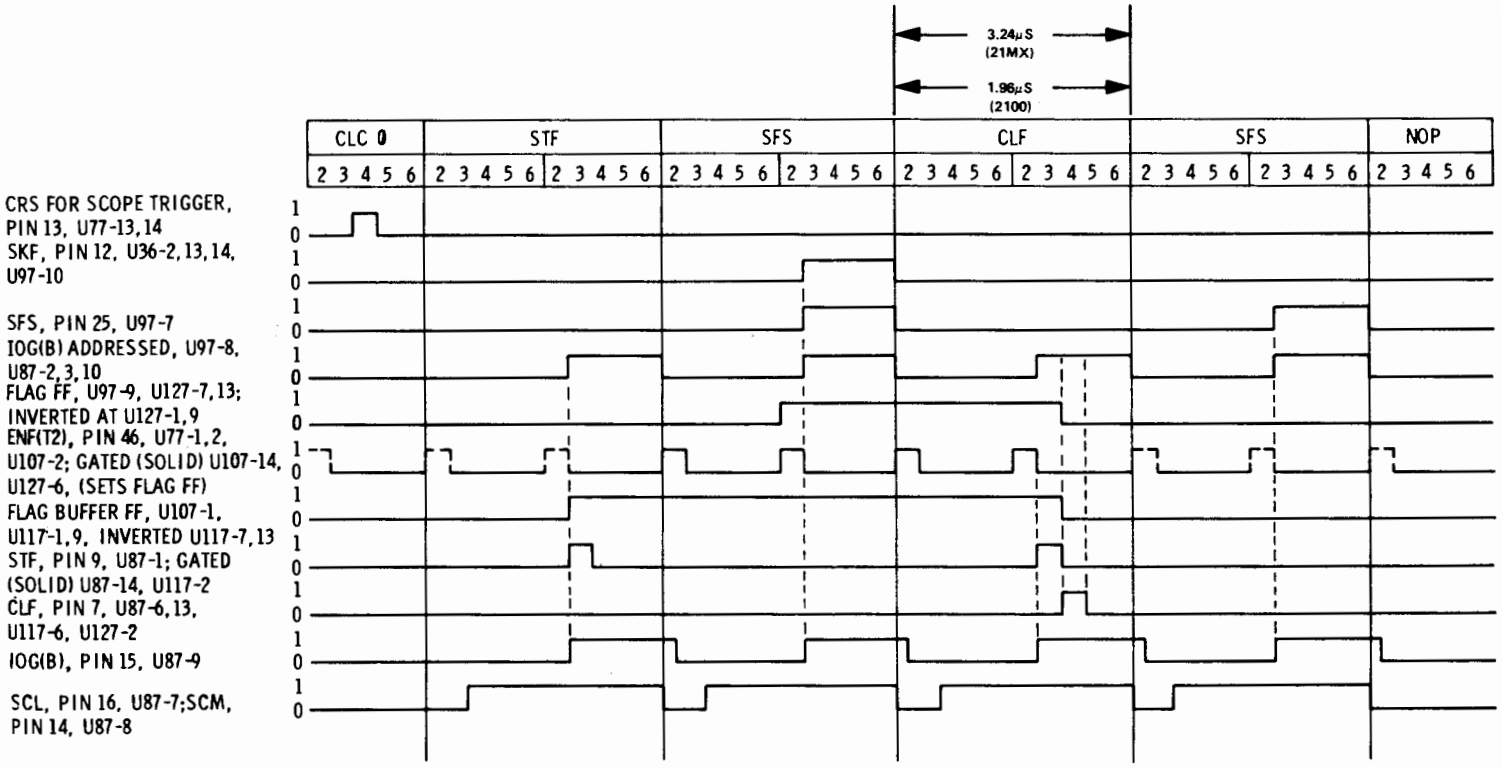
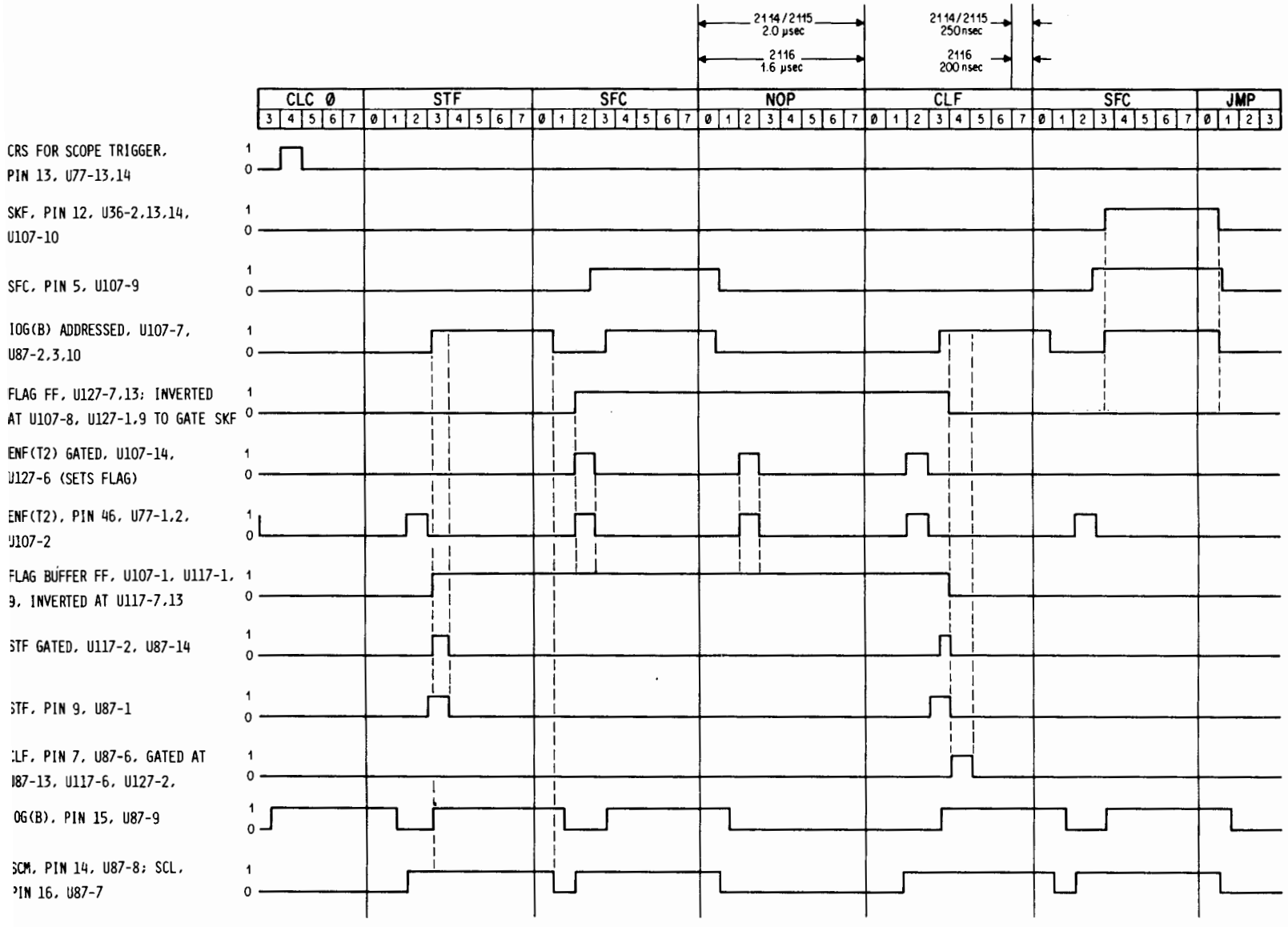
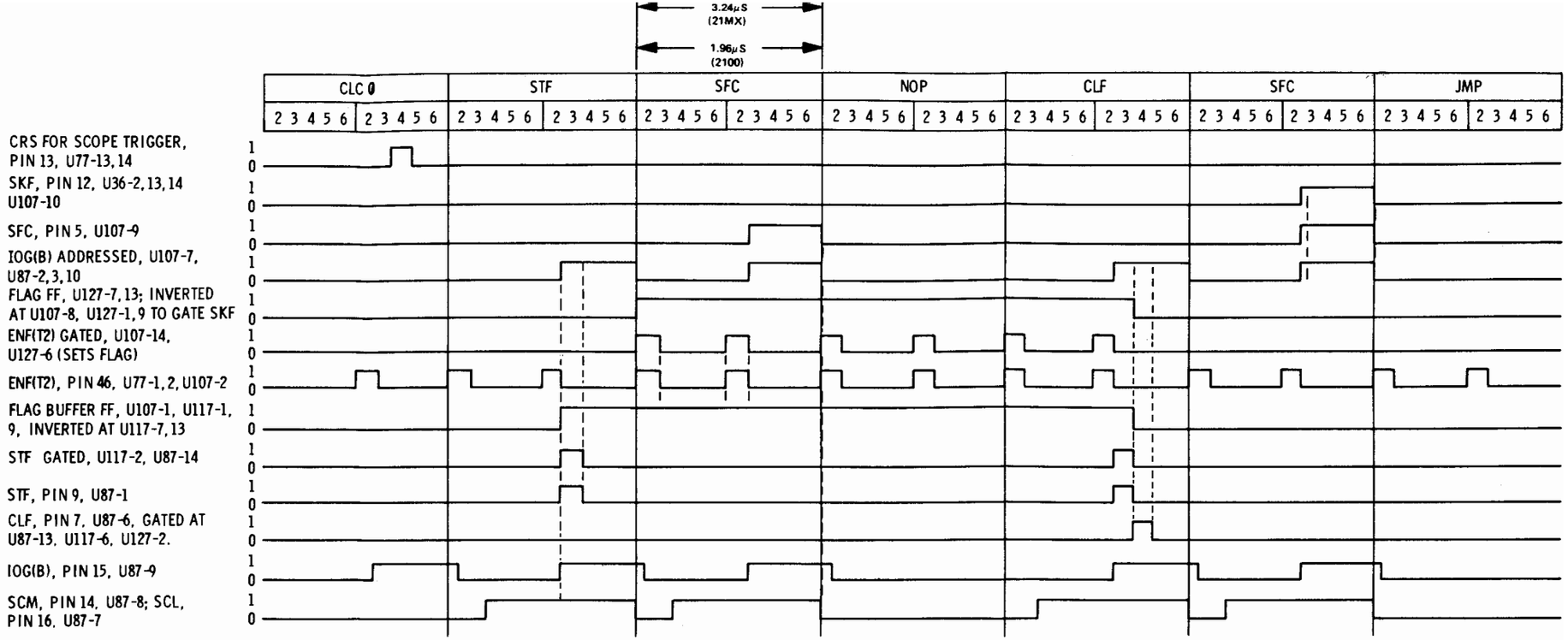


Figure 4-2. First Flag Scope Loop
(HP 2100 and HP 21MX Only)



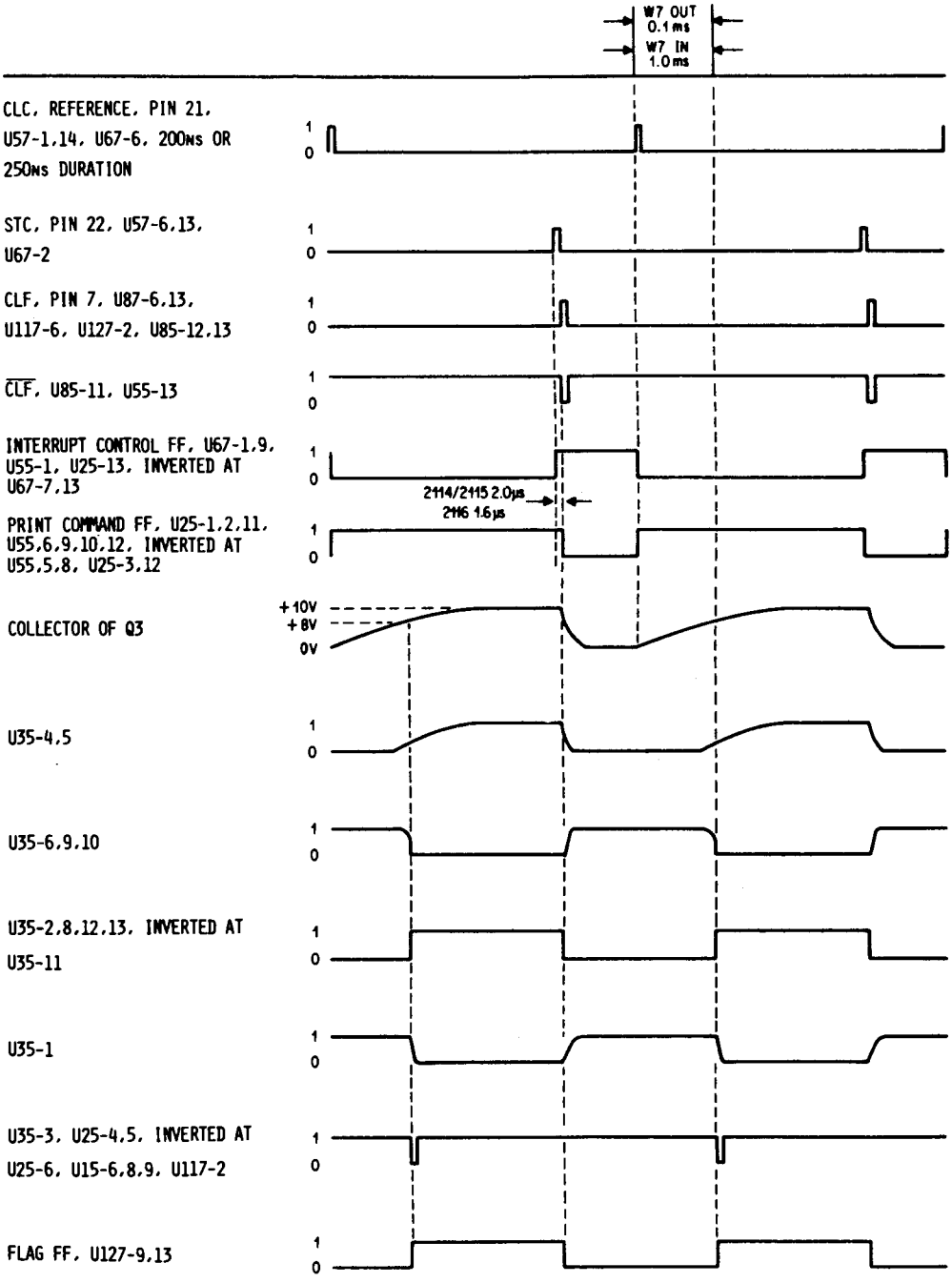
NOTE: ALL "PIN" NUMBERS REFER TO THE 86 PIN CONNECTOR.

Figure 4-3. Second Flag Scope Loop



NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR.

Figure 4-4. Second Flag Scope Loop (HP 2100 and HP 21MX Only)

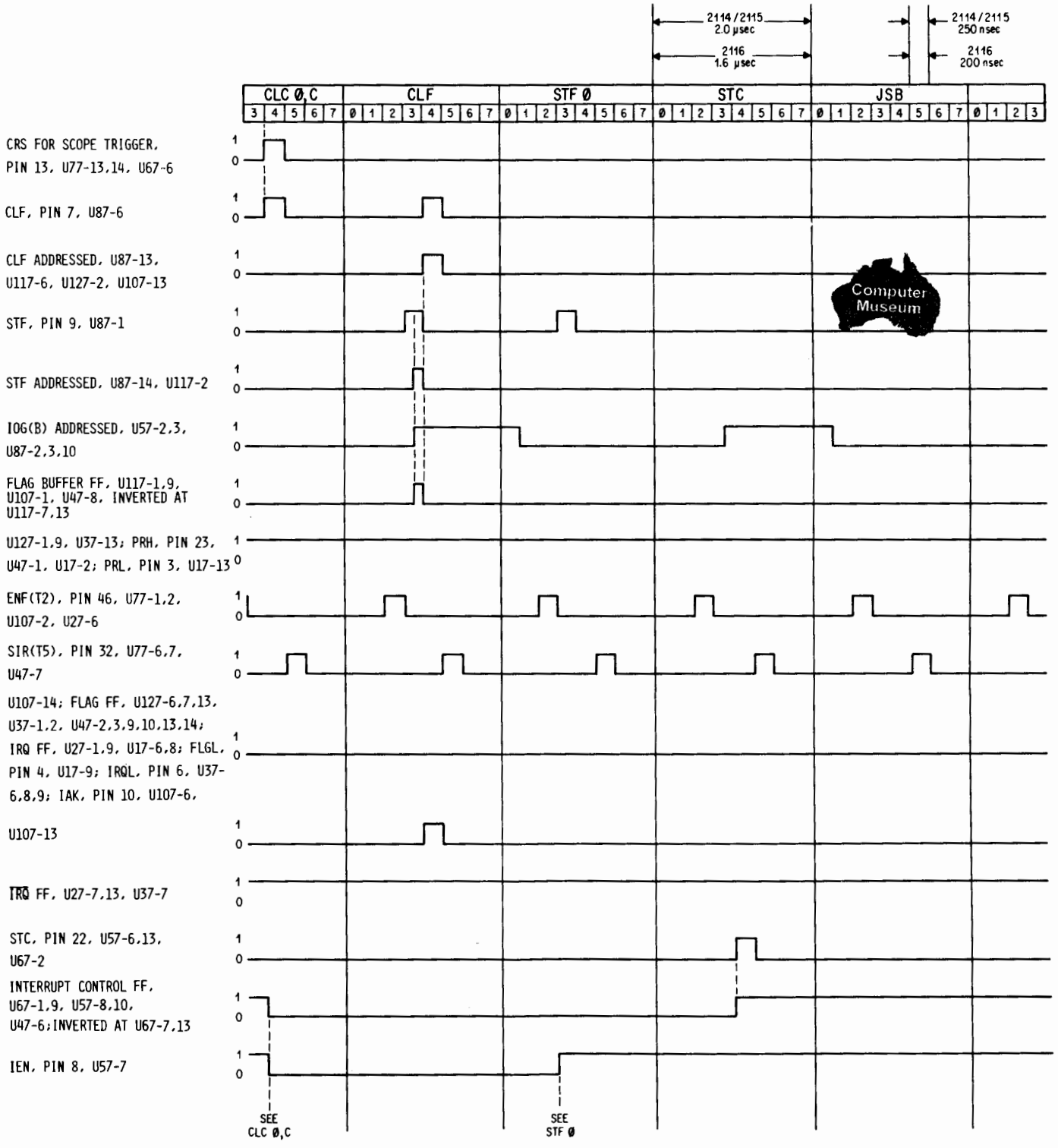


NOTES:

1. ALL "PIN" NUMBERS REFER TO THE 86 PIN CONNECTOR
2. FOR OPTION 028, TIME DELAYS ARE 10µSEC (W7 OUT) AND 900 µSEC (W7 IN)

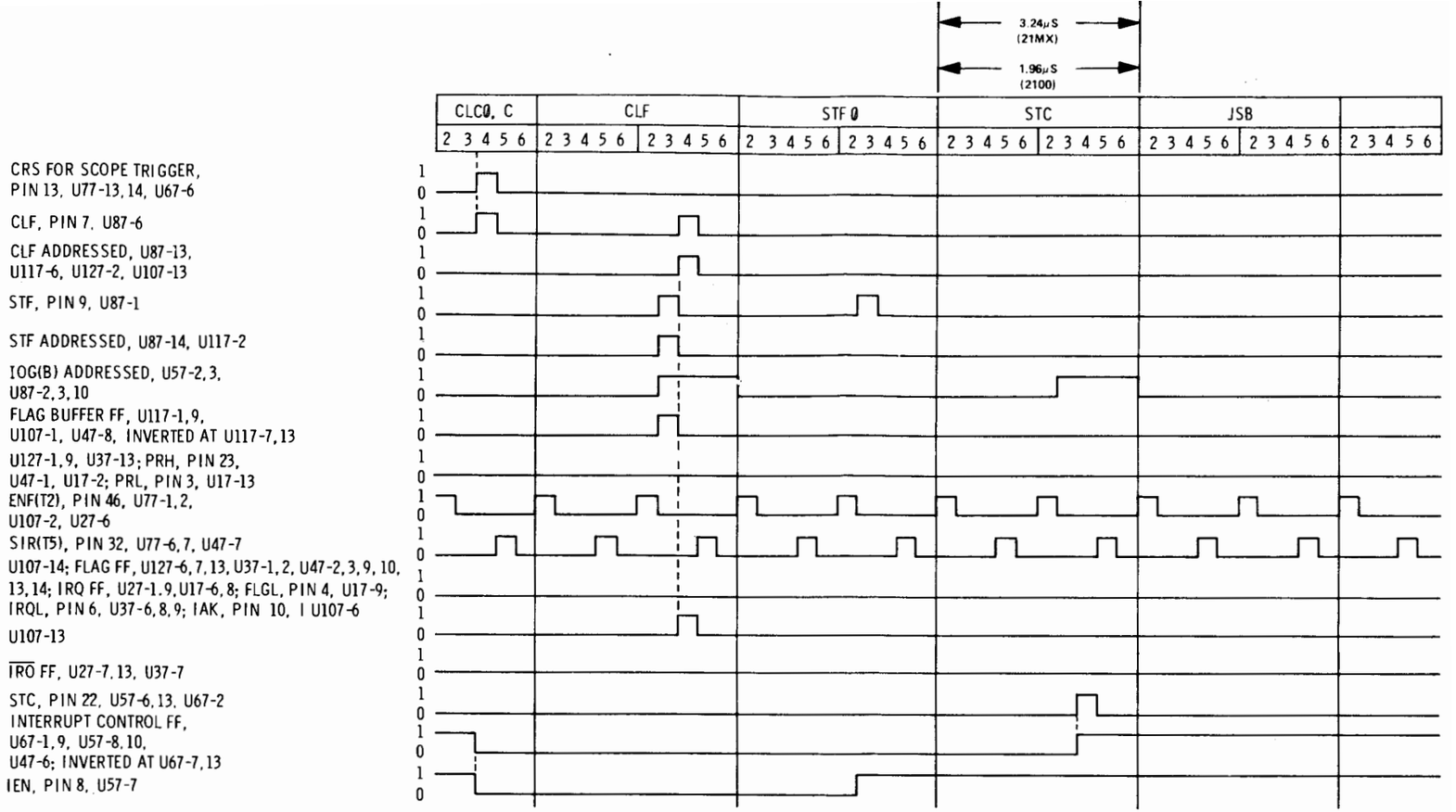
TP 126048-4

Figure 4-5. Time Delay Scope Loop



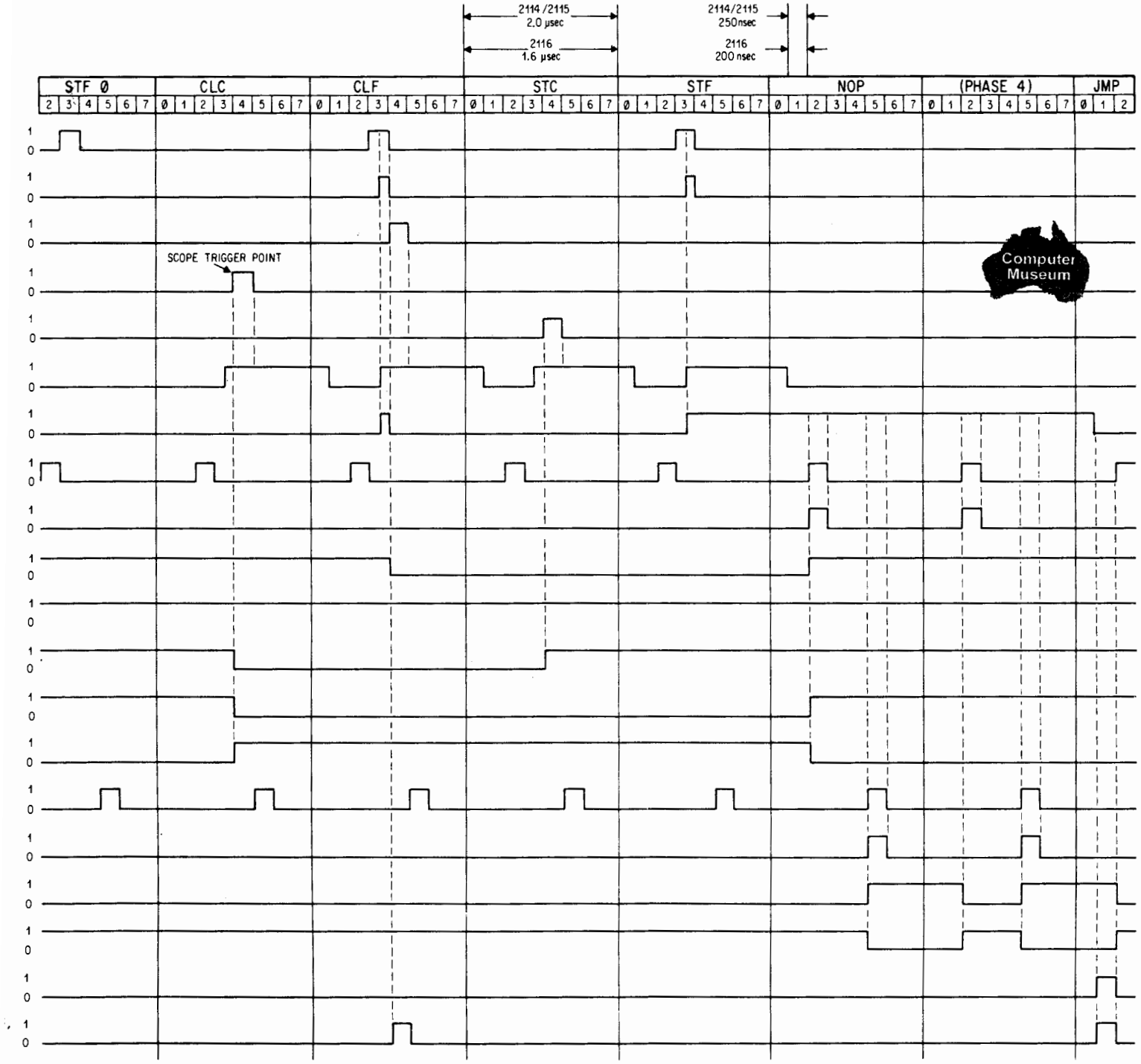
NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR.

Figure 4-6. Interrupt Test One Scope Loop



NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR.

Figure 4-7. Interrupt Test One Scope Loop (HP 2100 and HP 21MX Only)



-PIN CONNECTOR.

Figure 4-8. Interrupt Test Two Scope Loop

STF, PIN 9, U87-1

STF ADDRESSED, U87-14, U117-2

CLF, PIN 7, U87-6, ADDRESSED, U87-13,
U127-2, (ALSO SEE IAK BELOW)

CLC, PIN 21, U57-1, ADDRESSED,
U57-14, U67-6

STC, PIN 22, U57-6, ADDRESSED,
U57-13, U67-2

IOG(B) ADDRESSED, U87-2,3,10,
U57-2,3

FLAG BUFFER FF, U117-1,9, U107-1,
U47-8, INVERTED AT U117-7,13

ENF(T2), PIN 46, U77-1,2,
U107-2, U27-6

ENF(T2) GATED, U107-14, U127-6

FLAG FF, U127-7,13, U47-3,
INVERTED AT U127-1,9

IEN, PIN 8, U57-7; PRH,
PIN 23, U47-1, U17-2

INTERRUPT CONTROL FF, U67-1,9, U57-8,10,
U47-6, INVERTED AT U67-7,13

U47-2,9,13,14, U37-1

U37-13, U17-14; PRL, PIN 3,
U17-13

SIR(T5), PIN 32, U77-6,7, U47-7

SIR(T5) GATED, U47-10, U27-2

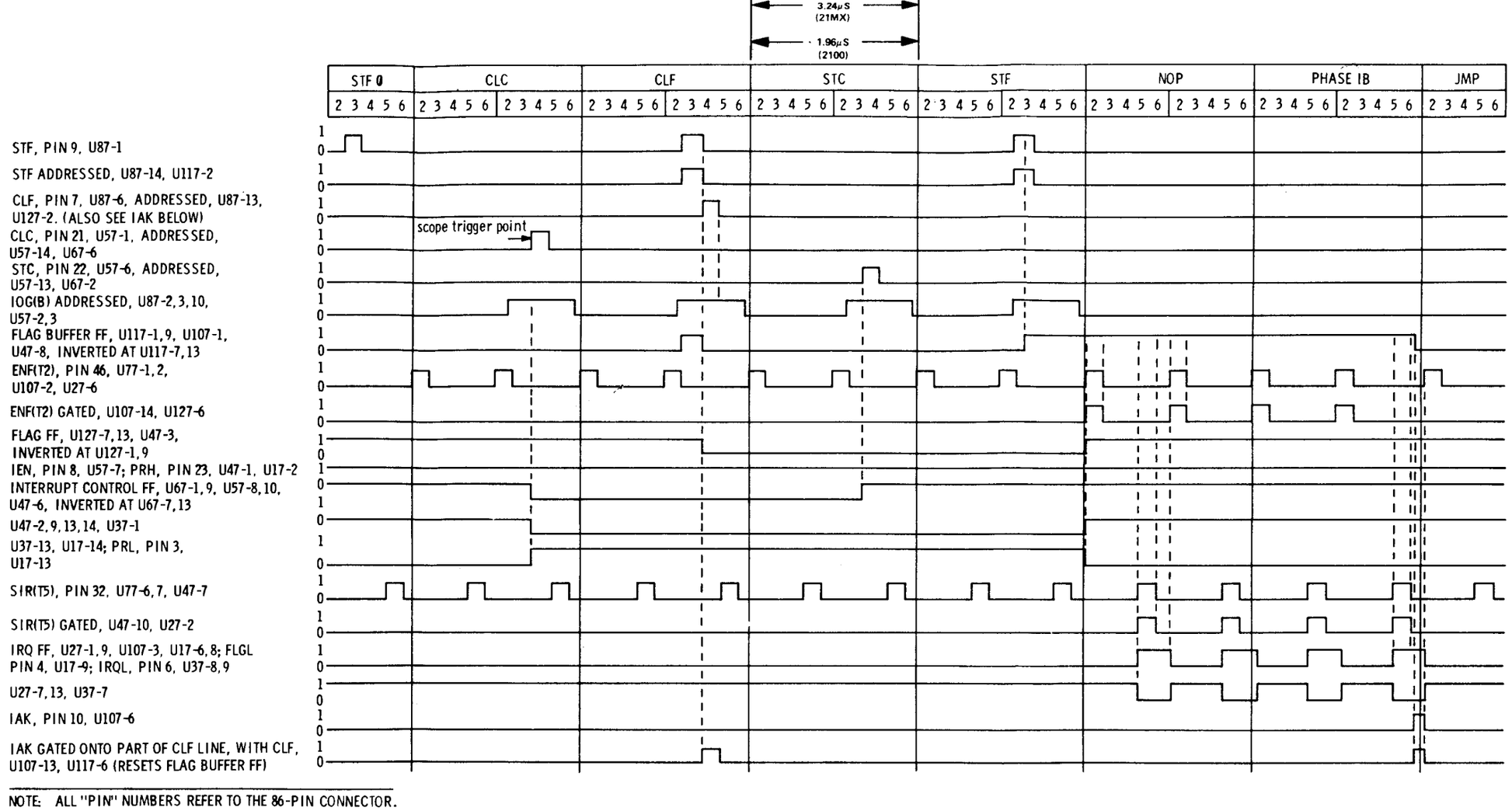
IRQ FF, U27-1,9, U107-3, U17-6,8; FLGL,
PIN 4, U17-9; IRQL, PIN 6, U37-8,9

U27-7,13, U37-7

IAK, PIN 10, U107-6

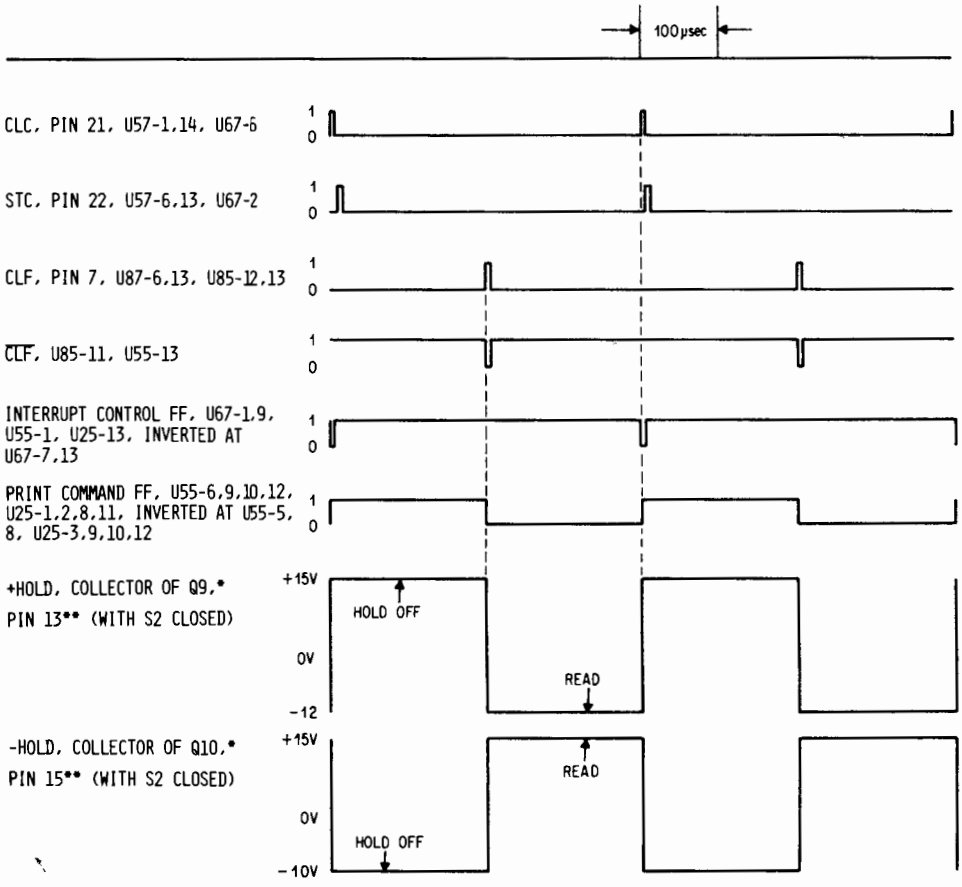
IAK GATED ONTO PART OF CLF LINE, WITH CLF
U107-13, U117-6,(RESETS FLAG BUFFER FF)

NOTE: ALL "PIN" NUMBERS REFER TO THE 86



NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR.

Figure 4-9. Interrupt Test Two Scope Loop (HP 2100 and HP 21MX Only)

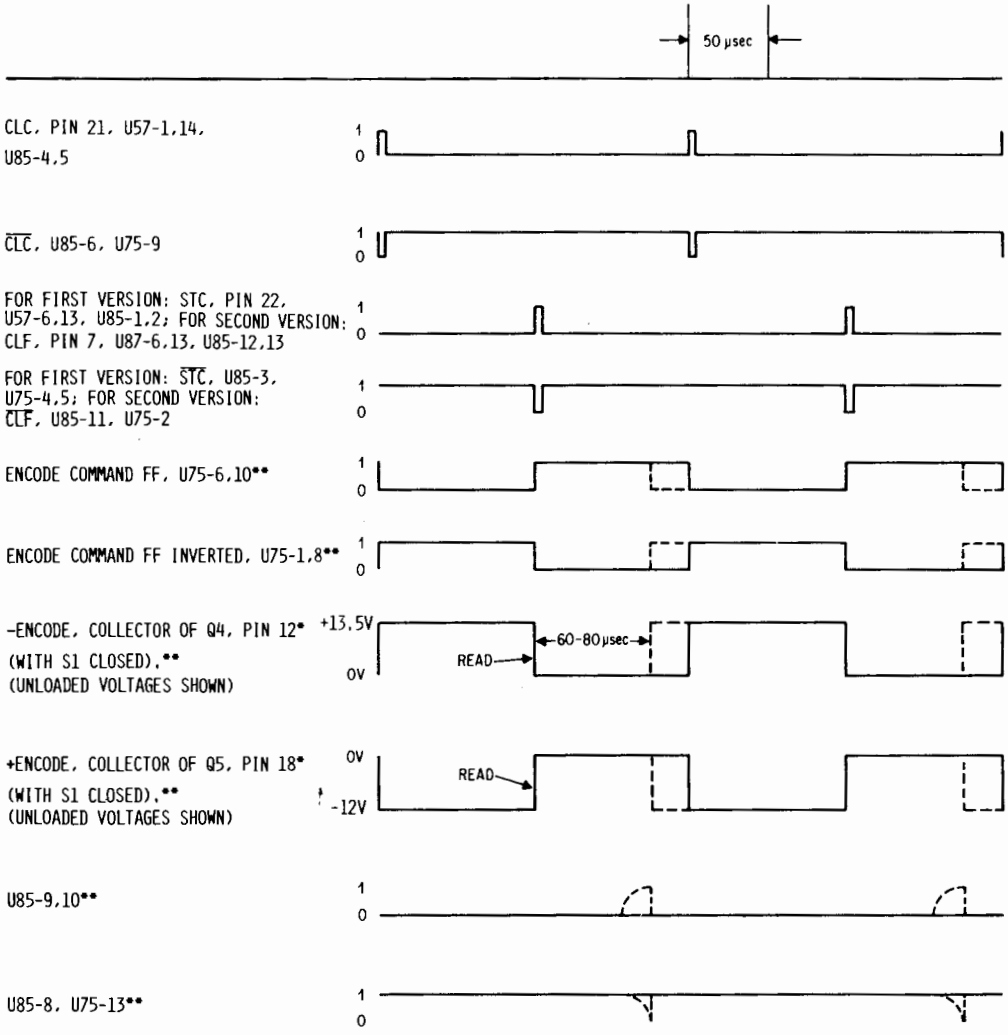


NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR UNLESS OTHERWISE NOTED.

*COLLECTORS OF Q9 AND Q10 ARE TIED TO THEIR CASES.

** "PIN 13" (+HOLD) AND "PIN 15" (-HOLD) REFER TO THE 48-PIN CONNECTOR.

Figure 4-10. Hold Command Scope Loop



NOTE: ALL "PIN" NUMBERS REFER TO THE 86-PIN CONNECTOR, UNLESS OTHERWISE NOTED.

*PIN 12 (-ENCODE) AND PIN 18 (+ENCODE) REFER TO THE 48-PIN CONNECTOR.

**DASHED LINES SHOW PULSED ENCODE (W6 IN PLACE).

Figure 4-11. Encode Command Scope Loop

SECTION V
REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains two lists of information for ordering replacement parts. Table 5-1 lists parts alpha-numerically by reference designator. It provides HP stock numbers, a general description of the parts, and any applicable notes. Miscellaneous parts not indexed by reference designation are listed at the end of this table.

5-3. Table 5-2 lists parts alpha-numerically by their HP stock numbers, and provides the following information on each part:

a. General description of the part.

b. Typical manufacturer of the part expressed as a five-digit code. (A list of manufacturers and their code numbers appear in Table 5-3.)

c. Manufacturer's part, stock, or drawing number.

d. Total quantities used.

5-4. ORDERING INFORMATION.

5-5. When ordering replacement parts, each part must be identified by the Hewlett-Packard stock number. To order a part that is not listed in the tables, include the following information.

a. Interface kit number.

b. Option number, if any.

c. Description of the part.

d. Function and location of the part.

5-6. Address your order or inquiry to your local Hewlett-Packard field office (listed at the rear of this manual).

5-7. If parts are ordered from the original manufacturer, a complete description should be included with each manufacturer's part number. Many numbers listed are type numbers only, and descriptions are needed to facilitate selection.

REFERENCE DESIGNATIONS

A	assembly	F	fuse	MP	mechanical part	TP	test point
B	motor	FL	filter	P	plug	U	integrated circuit
BT	battery	J	jack	Q	transistor	V	vacuum tube, neon bulb, photocell, etc.
C	capacitor	K	relay	R	resistor		
CP	coupler	L	inductor	RT	thermistor	VR	voltage regulator
CR	diode	LS	loudspeaker	S	switch	W	cable; jumper
DL	delay line	M	meter	T	transformer	X	socket
DS	device signaling (lamp)	MK	microphone	TB	terminal board	Y	crystal
E	misc electronic part					Z	tuned cavity: network

ABBREVIATIONS

A	amperes	GL	glass	N/C	normally closed	RH	right hand
AFC	automatic frequency control	GND	ground(ed)	NE	neon	RMO	rack mount only
AL	aluminum	H	henries	NI PL	nickel plate	RMS	root-mean-square
AMPL	amplifier	HDW	hardware	N/O	normally open	RWV	reverse working voltage
BFO	beat frequency oscillator	HEX	hexagonal	NOM	nominal	S-B	slow-blow
BE CU	beryllium copper	HR	hour(s)	NPO	negative positive zero (zero temperature coefficient)	SCR	silicon-controlled rectifier
BP	bandpass	HZ	hertz			SE	selenium
BRS	brass	IC	integrated circuit	NPN	negative-positive-negative	SECT	section(s)
BWO	backward wave oscillator	IMPG	impregnated	NRFR	not recommended for field replacement	SEMICOND	semiconductor
CCW	counterclockwise	INCAND	incandescent	NSR	not separately replaceable	SI	silicon
CD PL	counterclockwise	INCL	include(s)			SIL	silver
CD PL	cadmium plate	INS	insulation(ed)			SL	slide
CER	ceramic	INT	internal	OBD	order by description	SPG	spring
CL	capacitive logic	INTCON	interconnecting	OH	oval head	SPL	special
CMO	cabinet mount only	K	kilo (10^3)	OX	oxide	SST	stainless steel
COM	common	LH	left hand	P	pico (10^{-12})	STL	steel
COMP	composition	LIN	linear	PC	printed circuit	TA	tantalum
COMPL	complete	LK WASH	lock wash	PHL	Phillips	TD	time delay
CONN	connector	LPF	low pass filter	PK	peak	TGL	toggle
CRT	cathode-ray tube	M	milli (10^{-3})	PK-PK	peak-to-peak	THD	thread
CTL	complementary transistor logic	MEG	meg (10^6)	PIV	peak inverse voltage	TI	titanium
CW	clockwise	MET FLM	metal film	PNP	positive-negative-positive	TOL	tolerance
DEPC	deposited carbon	MET OX	metallic oxide	P/O	part of	TRIM	trimmer
DTL	diode-transistor logic	MFR	manufacturer	POLY	polystyrene	TTL	transistor-transistor logic
ELECT	electrolytic	MHZ	megahertz	PORC	porcelain	TWT	traveling wave tube
ENCAP	encapsulated	MINTR	minature	POS	position(s)	U	micro (10^{-6})
EXT	external	MOM	momentary	POT	potentiometer	V	volts
F	farads	MOS	metal oxide semiconductor	PT	point	VAR	variable
FH	flat head	MTG	mounting	PWV	peak working voltage	VDCW	dc working volts
FIL H	fillister head	MY	mylar	RECT	rectifier	W/	with
FXD	fixed	N	nano (10^{-9})	RF	radio frequency	W	watts
G	giga (10^9)					WIV	working inverse voltage
GE	germanium					WW	wirewound
						W/O	without

Table 5-1. Reference Designation Index

Reference Designation	Part No.	Description #	Note
	12604-60001	**BASIC 12604 DATA SOURCE INTERFACE (DSI)**	
C1	0160-0161	C:FXD MY 0.01 UF 10% 200VDCW	
C2	0160-0298	C:FXD MY 0.0015 UF 10% 200VDCW	
C3	0160-0161	C:FXD MY 0.01 UF 10% 200VDCW	
C4	0160-0300	C:FXD MY 0.0027 UF 200VDCW	
C5	0160-0157	C:FXD MY 0.0047 UF 10% 200VDCW	
C6	0160-0165	C:FXD MY 0.056 UF 10% 200VDCW	
C7	0180-0376	C:FXD ELECT 0.47 UF 10% 35VDCW	
C8	0160-0154	C:FXD MICA MY 0.0022 UF 10% 200VDCW	
C9	0160-0168	C:FXD MY 0.1 UF 10% 200VDCW	
C10-C26	0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	
C27	0180-0230	C:FXD ELECT 1.0 UF 20% 50VDCW	
C28	0160-0153	C:FXD MY 0.001 UF 10% 200VDCW	
C100-C102	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C110-C112	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C120-C122	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C130-C132	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C140-C142	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C150-C152	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C160-C162	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C170-C172	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C180-C182	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C190-C192	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C200-C202	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C210-C212	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C220-C222	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C230-C232	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C240-C242	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
C250-C252	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
CR1	1901-0050	DIODE:SILICON 75V	
CR2	1901-0050	DIODE:SILICON 75V	
CR3	1901-0096	DIODE:SILICON 120V	
CR4	1901-0050	DIODE:SILICON 75V	
CR5	1901-0050	DIODE:SILICON 75V	

 # See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	℗ Part No.	Description #	Note
CR6	1901-0096	DIODE:SILICON 120V	
CR7	1902-3024	DIODE:BREAKDOWN 2.87V 5%	
CR8	1902-0048	DIODE:BREAKDOWN 6.81V 5%	
CR9	1902-0048	DIODE:BREAKDOWN 6.81V 5%	
CR10	1910-0022	DIODE:GE 5WIV	
CR11	1901-0050	DIODE:SILICON 75V	
CR12	1901-0050	DIODE:SILICON 75V	
CR13	1902-3104	DIODE:BREAKDOWN 5.62V 5%	
CR14	1902-3036	DIODE:BREAKDOWN 3.16V 5%	
CR15	1910-0022	DIODE:GE 5WIV	
CR100-CR103	1901-0096	DIODE:SILICON 120V	
CR110-CR113	1901-0096	DIODE:SILICON 120V	
CR120-CR123	1901-0096	DIODE:SILICON 120V	
CR130-CR133	1901-0096	DIODE:SILICON 120V	
CR140-CR143	1901-0096	DIODE:SILICON 120V	
CR150-CR153	1901-0096	DIODE:SILICON 120V	
CR160-CR163	1901-0096	DIODE:SILICON 120V	
CR170-CR173	1901-0096	DIODE:SILICON 120V	
CR180-CR183	1901-0096	DIODE:SILICON 120V	
CR190-CR193	1901-0096	DIODE:SILICON 120V	
CR200-CR203	1901-0096	DIODE:SILICON 120V	
CR210-CR213	1901-0096	DIODE:SILICON 120V	
CR220-CR223	1901-0096	DIODE:SILICON 120V	
CR230-CR233	1901-0096	DIODE:SILICON 120V	
CR240-CR243	1901-0096	DIODE:SILICON 120V	
CR250-CR253	1901-0096	DIODE:SILICON 120V	
Q1	1854-0045	Q:SI NPN	
Q2	1853-0010	Q:SI PNP(SELECTED FROM 2N3251)	
Q3	1854-0045	Q:SI NPN	
Q4	1854-0045	Q:SI NPN	
Q5	1853-0010	Q:SI PNP(SELECTED FROM 2N3251)	
Q6	1854-0045	Q:SI NPN	
Q7	1854-0045	Q:SI NPN	
Q8	1854-0045	Q:SI NPN	
Q9	1853-0012	Q:SI PNP	
Q10	1853-0012	Q:SI PNP	

 # See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	Part No.	Description #	Note
Q100	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q110	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q120	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q130	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q140	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q150	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q160	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q170	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q180	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q190	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q200	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q210	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q220	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q230	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q240	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
Q250	1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	
R1	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R2	0698-3155	R:FXD MET FLM 4.64K 1% 1/8W	
R3	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R4	0698-3153	R:FXD MET FLM 3.83K 1% 1/8W	
R5	0757-0427	R:FXD MET FLM 1.5K 1% 1/8W	
R6	0757-0427	R:FXD MET FLM 1.5K 1% 1/8W	
R7	0757-0427	R:FXD MET FLM 1.5K 1% 1/8W	
R8	0698-3441	R:FXD MET FLM 215 OHM 1% 1/8W	
R9	0698-3441	R:FXD MET FLM 215 OHM 1% 1/8W	
R10	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R11	0757-0465	R:FXD MET FLM 100K 1% 1/8W	
R12	0698-3102	R:FXD MET FLM 237 OHM 1% 1/2W	
R13	0698-3102	R:FXD MET FLM 237 OHM 1% 1/2W	
R14	0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	
R15	0757-0440	R:FXD MET FLM 7.50K 1% 1/8W	
R16	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R17	0757-0280	R:FXD MET FLM 1K OHM 1% 1/8W	
R18	0698-5490	R:FXD MET FLM 2K 1% 1/8W	
R19	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R20	0757-0394	R:FXD MET FLM 51.1 OHM 1% 1/8W	
R21	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R22	0757-0280	R:FXD MET FLM 1K OHM 1% 1/8W	
R23	0698-3441	R:FXD MET FLM 215 OHM 1% 1/8W	
R24	0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	
R25	0757-0428	R:FXD MET FLM 1.62K 1% 1/8W	
R26	0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	
R27	0698-3153	R:FXD MET FLM 3.83K 1% 1/8W	
R28	0757-0279	R:FXD MET FLM 3.16K OHM 1% 1/8W	
R29	0698-3440	R:FXD MET FLM 196 OHM 1% 1/8W	
R30	0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	
R31	0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	
R32	0698-3153	R:FXD MET FLM 3.83K 1% 1/8W	
R33	0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	
R34	0698-5529	R:FXD MET FLM 162 OHM 1% 1/4W	
R35	0698-3408	R:FXD MET FLM 2.15 1% 1/2W	

 # See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	℗ Part No.	Description #	Note
R36	0698-3443	R:FXD MET FLM 287 OHM 1% 1/8W	
R37	0698-3408	R:FXD MET FLM 2.15 1% 1/2W	
R38	0757-0465	R:FXD MET FLM 100K 1% 1/8W	
R39	0757-0465	R:FXD MET FLM 100K 1% 1/8W	
R40	0683-4715	R:FXD COMP 470 OHM 5% 1/4W	
R41	0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	
R42	0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	
R62	0683-1025	R:FXD COMP 1000 OHM 5% 1/4W	
R100	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R101	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R102	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R110	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R111	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R112	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R120	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R121	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R122	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R130	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R131	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R132	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R140	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R141	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R142	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R150	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R151	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R152	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R160	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R161	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R162	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R170	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R171	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R172	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R180	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R181	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R182	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R190	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R191	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R192	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R200	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R201	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R202	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R210	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R211	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R212	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R220	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R221	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R222	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R230	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R231	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R232	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R240	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	
R241	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R242	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R250	1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	

 # See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	Part No.	Description #	Note
R251	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
R252	0683-1035	R:FXD COMP 10K OHM 5% 1/4W	
S1	3101-0860	SWITCH:SLIDE MINIATURE DPDT	
S2	3101-0860	SWITCH:SLIDE MINIATURE DPDT	
U15	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U16	1820-0967	IC:CTL DUAL RANK J-K FLIP-FLOP	
U17	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U25	1820-0054	IC:TTL QUAD 2-INPUT NAND GATE	
U26	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U27	1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	
U35	1820-0054	IC:TTL QUAD 2-INPUT NAND GATE	
U36	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U37	1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	
U46	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U47	1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	
U55	1820-0071	IC:TTL DUAL 4-INPUT NAND BUFFER	
U56	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U57	1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	
U66	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U67	1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	
U75	1820-0071	IC:TTL DUAL 4-INPUT NAND BUFFER	
U76	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U77	1820-0965	IC:CTL QUAD 2-INPUT AND GATE	
U85	1820-0054	IC:TTL QUAD 2-INPUT NAND GATE	
U86	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U87	1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	
U96	1820-0054	IC:TTL QUAD 2-INPUT NAND GATE	
U97	1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	
U106	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U107	1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	
U116	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U117	1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	
U126	1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	
U127	1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	
W1-W5,8	8159-0005	JUMPER WIRE	
W6	5040-1485	CONDUCTOR ASSEMBLY:PLUG-IN JUMPER	
W7	5040-1485	CONDUCTOR ASSEMBLY:PLUG-IN JUMPER	
	02116-6178	CONN ASSY:48CON PC(HP#1251-0335)W/HOOD	
	20008-60001	TAPE:BCS DRIVER D.40	
	20337-60001	TAPE:DIAGNOSTIC	

 # See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	Part No.	Description #	Note
		FOR OPTION 01, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	12604-60002	CABLE:INTCON FOR 2401C/2402A DVM	
		FOR OPTION 02, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	02116-6153	CABLE:INTCON FOR HP COUNTERS (8-DIGIT)	
		FOR OPTION 03, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	12604-60003	CABLE:INTCON FOR HP COUNTERS (7-DIGIT)	
		FOR OPTION 04, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	12604-60004	CABLE:INTCON FOR 3440A DVM	
		FOR OPTION 05, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	12604-60006	CABLE:INTCON FOR 3450A MULTI-METER	

See introduction to this section for ordering information

Table 5-1. Reference Designation Index (Continued)

Reference Designation	Part No.	Description #	Note
		FOR OPTION 06, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
	02116-6178	CONN ASSY:CONN 48-PIN PC W/HOOD	
		ADD THE FOLLOWING:	
	02116-6114	CABLE:INTCON FOR 3460A DVM	
		FOR OPTION 20, MAKE THE FOLLOWING CHANGE TO THE STANDARD 12604B PARTS LIST:	
		ADD THE FOLLOWING:	
	29100-60041	TAPE:DRIVER DVR40	
	12604-60010	12604 DSI CARD OPTION 028	
		FOR OPTION 028, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
C6	0160-0165	C:FXD MY 0.056 UF 10% 200VDCW	
		DELETE THE FOLLOWING:	
C100,C102	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	
		ADD THE FOLLOWING:	
C100,C102	0160-2208	C:FXD MICA 330PF 5% 300VDCW	
C102	0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000 VDCW	
		THIS CHANGE IS FOR EACH OF THE 16 SETS OF CAPACITORS FROM C100 TO C250.	
	12604-60011	DSI CARD OPTION 029	
		FOR OPTION 029, MAKE THE FOLLOWING CHANGES TO THE STANDARD 12604B PARTS LIST:	
		DELETE THE FOLLOWING:	
C6	0160-0165	C:FXD MY 0.056 UF 10% 200VDCW	
		DELETE THE FOLLOWING:	
R62	0683-1025	R:FXD COMP 1000 OHM 5% 1/4W	
		ADD THE FOLLOWING:	
R62	0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	
CR254	1902-3036	DIODE:BREAKDOWN 3.16V 5%	
		DELETE THE FOLLOWING:	
C100-C102	0150-0050	C:FXD CER DISC 1000 PF +80 -20% 1000VDCW	
		ADD THE FOLLOWING:	
C100-C102	0160-2208	C:FXD 330 PF 5% 300 VDCW	
		THIS CHANGE IS FOR EACH OF THE 16 SETS OF CAPACITORS C100-C102 THRU C250-C252.	

 # See introduction to this section for ordering information

Table 5-2. Replaceable Parts

℗ Part No.	Description #	Mfr.	Mfr. Part No.	TQ
0150-0050	C:FXD CER DISC 1000 PF +80-20% 1000VDCW	56289	C067B102E102ZE19-C0H	48
0160-0153	C:FXD MY 0.001 UF 10% 200VDCW	56289	192P10292-PTS	1
0160-0154	C:FXD MICA MY 0.0022 UF 10% 200VDCW	56289	192P22292-PTS	1
0160-0157	C:FXD MY 0.0047 UF 10% 200VDCW	56289	192P47292-PTS	1
0160-0161	C:FXD MY 0.01 UF 10% 200VDCW	56289	192P10392-PTS	2
0160-0165	C:FXD MY 0.056 UF 10% 200VDCW	56289	192P56392-PTS	1
0160-0168	C:FXD MY 0.1 UF 10% 200VDCW	56289	192P10492-PTS	1
0160-0298	C:FXD MY 0.0015 UF 10% 200VDCW	56289	192P15292-PTS	1
0160-0300	C:FXD MY 0.0027 UF 200VDCW	56289	192P27292-PTS	1
0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2-DYS	17
0180-0230	C:FXD ELECT 1.0 UF 20% 50VDCW	56289	150D105X0050A2-DYS	1
0180-0376	C:FXD ELECT 0.47 UF 10% 35VDCW	56289	150D474X9035A2-DYS	1
0683-1025	R:FXD COMP 1000 OHM 5% 1/4W	01121	CB 1025	1
0683-1035	R:FXD COMP 10K OHM 5% 1/4W	01121	CB 1035	32
0683-4715	R:FXD COMP 470 OHM 5% 1/4W	01121	CB 4715	1
0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	14674	C4	4
0698-3102	R:FXD MET FLM 237 OHM 1% 1/2W	91637	MFF-1/2-10	2
0698-3153	R:FXD MET FLM 3.83K 1% 1/8W	91637	MFF-1/10-32	3
0698-3155	R:FXD MET FLM 4.64K 1% 1/8W	91637	MFF-1/10-32	1
0698-3408	R:FXD MET FLM 2.15 1% 1/2W	91637	MFF-1/2-10	2
0698-3440	R:FXD MET FLM 196 OHM 1% 1/8W	91637	MF-1/10-32	1
0698-3441	R:FXD MET FLM 215 OHM 1% 1/8W	91637	MF-1/10-32	3
0698-3443	R:FXD MET FLM 287 OHM 1% 1/8W	91637	MF-1/10-32	1
0698-5490	R:FXD MET FLM 2K 1% 1/8W	14674	NC4	1
0698-5529	R:FXD MET FLM 162 OHM 1% 1/4W	91637	MF-1/8-34	1
0757-0279	R:FXD MET FLM 3.16K OHM 1% 1/8W	14674	C4	1
0757-0280	R:FXD MET FLM 1K OHM 1% 1/8W	14674	C4	2
0757-0394	R:FXD MET FLM 51.1 OHM 1% 1/8W	14674	C4	1
0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	14674	C4	3
0757-0427	R:FXD MET FLM 1.5K 1% 1/8W	14674	C4	3
0757-0428	R:FXD MET FLM 1.62K 1% 1/8W	14674	C4	1
0757-0440	R:FXD MET FLM 7.50K 1% 1/8W	14674	C4	1
0757-0442	R:FXD MET FLM 10.0K 1% 1/8W	14674	C4	7
0757-0465	R:FXD MET FLM 100K 1% 1/8W	14674	C4	3
1810-0018	RESISTOR:NETWORK MET FLM (6 RES)	56289	200C1365	16
1820-0054	IC:TTL QUAD 2-INPUT NAND GATE	01295	SN4342	4
1820-0071	IC:TTL DUAL 4-INPUT NAND BUFFER	01295	SN7440N	2
1820-0952	IC:CTL DUAL 2-INPUT NOR GATE	07263	SL3455	5
1820-0953	IC:CTL TRIPLE 2-2-3-INPUT AND GATE	07263	SL3456	5
1820-0956	IC:CTL DUAL 2-INPUT AND BUFFER	07263	SL3459	12
1820-0965	IC:CTL QUAD 2-INPUT AND GATE	07263	SL3462	1
1820-0967	IC:CTL DUAL RANK J-K FLIP-FLOP	07263	SL3464	1
1853-0010	Q:SI PNP(SELECTED FROM 2N3251)	28480	1853-0010	2
1853-0012	Q:SI PNP	80131	2N2904A	2
1854-0045	Q:SI NPN	04713	2N956	6
1854-0094	Q:SI NPN(SIMILAR TO 2N3053)	28480	1854-0094	16
1901-0050	DIODE:SILICON 75V	14433	S270	6
1901-0096	DIODE:SILICON 120V	01295	UG-888	66
1902-0048	DIODE:BREAKDOWN 6.81V 5%	04713	SZ10939-134	2
1902-3074	DIODE:BREAKDOWN 2.87V 5%	04713	SZ10939-26	1
1902-3036	DIODE:BREAKDOWN 3.16V 5%	04713	SZ10939-38	1
1902-3104	DIODE:BREAKDOWN 5.62V 5%	04713	SZ10939-110	1
1910-0022	DIODE:GE 5WIV	14433	G401	2

 # See introduction to this section for ordering information

Table 5-2. Replaceable Parts (Continued)

Part No.	Description #	Mfr.	Mfr. Part No.	TQ
20008-60001	TAPE:BCS DRIVER D.40	28480	20008-60001	1
20337-60001	TAPE:DIAGNOSTIC	28480	20337-60001	1
3101-0860	SWITCH:SLIDE MINIATURE DPDT	79727	G126-C064	2
5040-1485	CONDUCTOR ASSEMBLY:PLUG-IN JUMPER	28480	5040-1485	2
8159-0005	JUMPER WIRE	28480	8159-0005	6
02116-6178	CONN ASSY:48CON PC(HP#1251-0335)W/HOOD	28480	02116-6178	1
12604-60001	DATA SOURCE INTERFACE	04404	12604-60001	1

Table 5-3. Code List of Manufacturers

MFG. NO.	MANUFACTURER NAME	ADDRESS
01121	Allen Bradley Co.	Milwaukee, Wis. 53204
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas 75231
04404	Hewlett-Packard Co., Automatic Measurement Div./DAS	Palo Alto, Calif. 94306
04713	Motorola Inc., Semiconductor Prod. Div.	Phoenix, Arizona 85008
07263	Fairchild Camera & Instr. Corp., Semiconductor Div.	Mountain View, Calif. 94040
14433	ITT Semiconductor, a Div. of Int. Telephone & Telegraph Corp.	West Palm Beach, Fla. 33401
14674	Corning Glass Works	Corning, New York 14830
28480	Hewlett-Packard Co.	Palo Alto, Calif. 94304
56289	Sprague Electric Co.	North Adams, Mass. 01247
79727	Continental-Wirt Electronics Corp.	Warminster, Pa. 18974
80131	Electronic Industries Association*	Washington, D.C. 20006
91637	Dale Electronics, Inc.	Columbus, Nebr. 68601

*Any brand tube meeting EIA Standards.

APPENDIX A
KEY TO LOGIC SYMBOLOGY

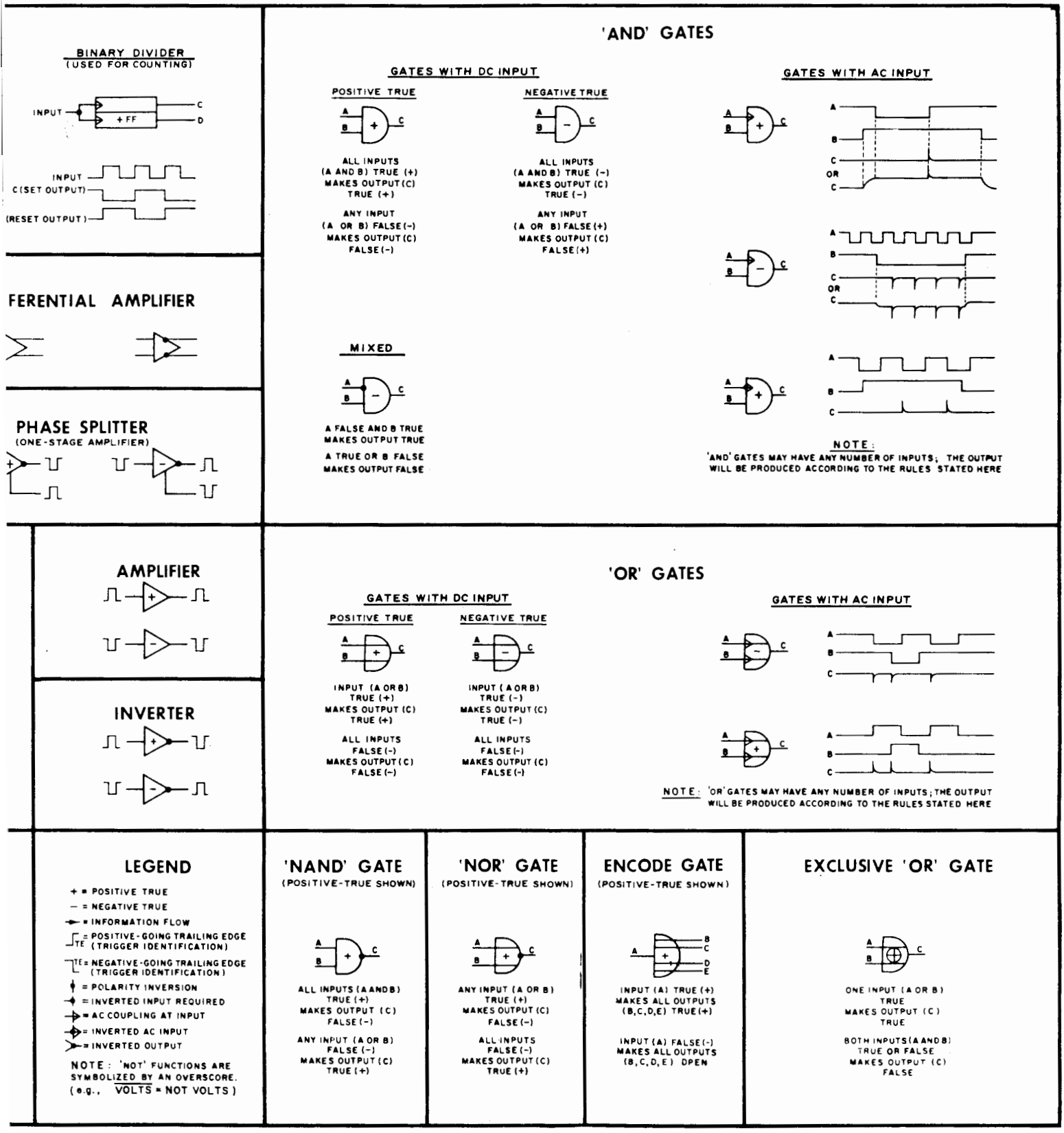
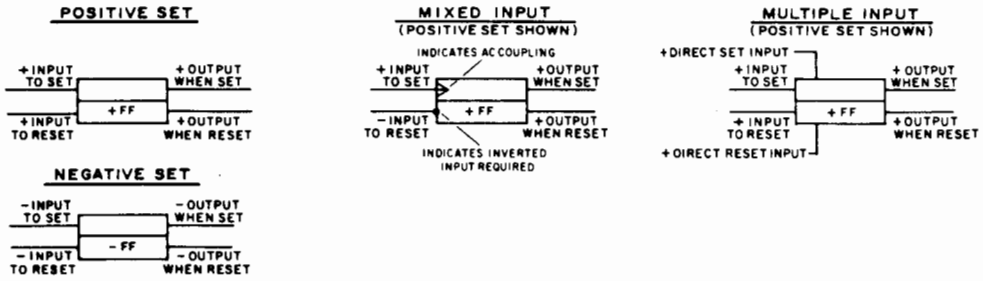
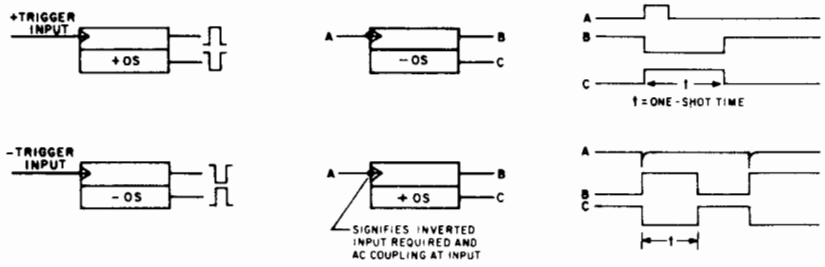


Figure A-1. Key to Logic Symbology

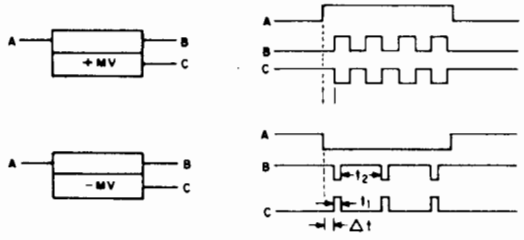
FLIP-FLOP



ONE-SHOT



ASTABLE MULTIVIBRATOR

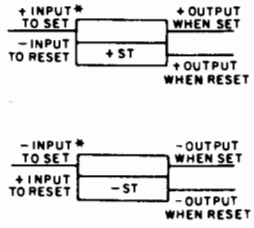


A IS INPUT REQUIRED FOR OPERATION; CORRESPONDS TO POLARITY (+MV OR -MV)

Δt IS DELAY OF FIRST TRANSITION

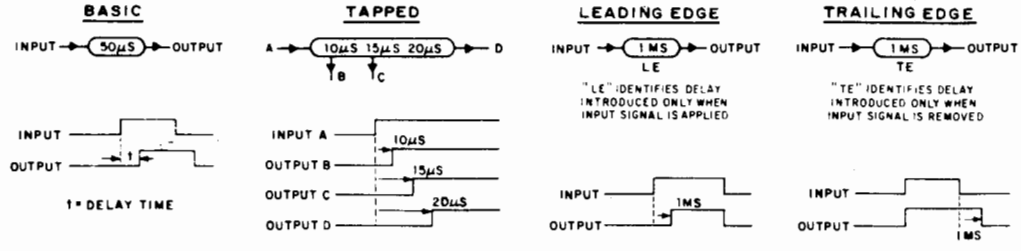
t_1-t_2 RATIO IS DETERMINED BY CIRUIT CONSTANTS

SCHMITT TRIGGER



* WITH RESPECT TO REFERENCE LEVEL

DELAY ELEMENTS



APPENDIX B
INSTRUCTIONS FOR INCORPORATING DRIVERS INTO BCS WITH D.40 AND D.40A FLOWCHARTS

APPENDIX B
INSTRUCTIONS FOR INCORPORATING DRIVERS INTO BCS

1-1. INTRODUCTION

1-2. This appendix supplements the Operating Procedures in the Prepare Control System (PCS) section of the HP Basic Control System Manual and the Computer Operating Manual. Please read that section in both manuals before attempting to configure your system. General instructions are included here to help you reconfigure your system and generate a new BCS tape. Specific instructions are included for incorporating drivers D.40 and D.40A into BCS. Flowcharts for drivers D.40 and D.40A are shown in Figures B-1 and B-2.

1-3. This appendix provides two worksheets on Figure B-3 that will aid you in planning a BCS configuration for your system. The Input/Output Configuration Worksheet is used to preplan the Standard Unit Table, the Equipment Table, Interrupt Locations, and Linkage Locations when configuring your system with I/O devices and their drivers. Also included is the First and Last Word of Available Memory. The PCS Worksheet is then completed using the entries from the I/O Worksheet. These are the responses to be made during PCS execution.

1-4. INPUT/OUTPUT PLANNING.

1-5. Input/output locations in all HP computers have the same sequence of priority addresses: the highest priority address is the lowest numbered Select Code (I/O location). The Select Codes start at 10_8 and continue through 17_8 in Model 2114A and 2115 Computers, 16_8 in Model 2114B Computers, 25_8 in Model 2100, and 27_8 in Model 2116 Computers.

1-6. Interface cards are assigned to priority addresses according to the type of device they operate. Interface cards for synchronous devices are usually assigned to higher priority addresses than those for asynchronous devices. Further, within the grouping for synchronous and asynchronous devices, the high-speed devices are assigned higher priority addresses than slow-speed devices. These relationships are vital for preservation of data transferring to and from the computer, as discussed in "Volumn 1, Specifications and Basic Operation", for the computer in use.

2-1. I/O CONFIGURATION WORKSHEET

2-2. Considering the factors given in the preceding paragraphs on Input/Output Planning, select the priority addresses for each interface card and use the following general instructions for completing the I/O worksheet. For any device that requires two interface cards, refer to the manual for the device to learn the respective positions required for the two cards.

a. Fill in the top portion of the table with the I/O card name under the appropriate select code (I/O slot).

b. Make Standard Unit Table assignments (1 thru 6) to I/O devices by placing a checkmark at the intersection of the standard unit table number (X-axis), and the I/O card select code (Y-axis).

NOTE

If a Standard Unit device has two interface cards, use only the high-priority Select Code column.

c. Starting with octal 7, write in Equipment Table numbers sequentially for each device. These numbers can be arbitrarily assigned to I/O devices and do not have to be written in a left to right order on this table. Order is attained when PCS asks for EQT?; the first entry made will be for Equipment Table No. 7, then 10 and so on.

NOTE

If a device has two interface cards, write in a number for only the high-priority interface card.

d. Write in the Driver Identification number, obtained from the software box, for each device.

NOTE

If a device has two interface cards, write the D.xx number under the high-priority card and a dash under the low-priority card.

e. Write in the Interrupt Location address for each device. This is normally the lower select code number of the I/O slot.

f. Write in the Linkage Location address for each device. These octal numbers usually begin with the next sequential number after the last Interrupt Location number written in step e.

g. Write in the Interrupt Entry Label which is usually the Driver Identification number preceded by an "I"; e.g., Teleprinter Interrupt Entry Label is I.ØØ. Note that some drivers do not interrupt and therefore do not have an "I." number. Refer to the last part of this appendix regarding your particular driver. For such drivers, write a dash in that space.

h. Determine the First and Last Word of Available Memory (FWAM and LWAM). FWAM is usually the next sequential address after the last Linkage Location; in magnetic tape systems, FWAM is 110B or higher. LWAM is given in Table B-1 for standard memory sizes up to 32K.

Table B-1. LWAM

MEMORY SIZE	LWAM	LWAM (in Magnetic Tape System)
4K	007677	
8K	017677	015677
16K	037677	035677
32K	077677	075677

3-1. PCS WORKSHEET

3-2. Once the system is planned, the actual configuration process takes place. This process is divided into five phases and is normally executed in the order presented on the PCS Worksheet. The PCS Worksheet should be completed in advance from the information entered on the I/O Worksheet so your replies are known and you do not waste computer time. The following general instructions will aid you in completing the worksheet. Actual operating instructions for PCS are found in the Computer Operating Manual.

3-3. INITIALIZATION.

3-4. Write in the select codes for the HS INP (photoreader) and HS PUN (high speed tape punch). Enter Ø if there is none. Write in the first and last words of available memory.

3-5. I/O DRIVERS.

3-6. Write the Driver Identification numbers into the D. spaces in the order used in the I/O Worksheet. The drivers may be entered in any order, however, it is recommended that synchronous drivers do not overlay page boundaries due to possible loss in time executing the indirect instructions required through base page links.

NOTE

This list specifies the order in which the drivers are to be loaded during PCS execution. If, in actually loading the drivers, an LØ4 error occurs, rearrange the order of loading the drivers to cut down on crossing page boundaries. Some drivers may be loaded external to BCS to reduce linkage area. Remember, DMA links are internal to .IOC. and are therefore internal to BCS. Drivers that use DMA cannot be loaded external to BCS.

3-7. EQT TABLE.

3-8. The unit-reference numbers in parenthesis serve as a guide in entering the correct select code numbers. Refer to the I/O Worksheet and write in the select code number and driver identification number corresponding to Equipment Table No. 7. Refer to the last part of this appendix for instructions concerning your particular driver.

Example: (7) 12, D. Ø1

3-9. This tells the computer that Equipment Table unit-reference number 7 is select code 12 and is driver D.Ø1 for the photoreader.

3-10. Continue writing in the select code and driver identification number for each of the Equipment Table unit-reference numbers on the I/O Worksheet. Drivers that use DMA are designated by ",D" (e.g., 17, D.40,D).

3-11. SQT TABLE.

3-12. The Standard Unit Table is cross-referenced to the Equipment Table here. In each space provided under each standard unit, write the Equipment Table number from the I/O Worksheet. Under DMA, write in the channel numbers (6 for one DMA channel; 6, 7 for two; Ø for none).

3-13. INTERRUPT LINKAGE.

3-14. The interrupt links are tied to the select code for input/output processing. Refer to the I/O Worksheet and write in the Interrupt Location, Linkage Location, Interrupt Entry Label letter and number.

NOTE

Some drivers do not interrupt and require a special instruction word here. Refer to the last part of this appendix regarding your particular driver.

Example: 1Ø, 16, I.21
11, 17, C.21

3-15. This example is for two interface cards and tells PCS that select code 10 is linked to memory location 16 which contains the address of the Mag tape data channel I.21. Select code 11 is linked to memory location 17 which contains the address of the Mag tape command channel C.21.

3-16. PCS can now be placed into operation as described in the Basic Control System manual. Type the entries and load the driver tapes as planned in Paragraphs 3-1 through 3-15.

4-1. 12604B DSI DRIVERS

4-2. This part of the appendix gives instructions for incorporating the D.40 and D.40A Drivers into BCS. It is assumed that in completing the worksheets, according to the instructions given in this appendix, you have included either D.40 or D.40A.

4-3. Driver D.40A checks the Equipment Table each time it is entered, and therefore, may be used for both 8421 and 4221 instruments in the same system. (Drivers D.40 and D.40A cannot both be incorporated into the same BCS tape; use only one or the other.) In the EQT TABLE column on the PCS Worksheet, write in the following information for the appropriate driver:

aa,D.40 (for D.40 or for D.40A with 4221-coded instrument);

or

aa,D.40, U1 (for D.40A with 8421-coded instrument).

Note that the driver's identifying suffix letter is not included; also, aa is the select code from the I/O Worksheet.

4-4. On the PCS Worksheet in the INTERRUPT LINKAGE column, write in the following information for the appropriate driver:

aa,1067 aa (for either D.40 or D.40A)

where aa is the select code and 1067 is a clear control (CLC) instruction to the DSI card.

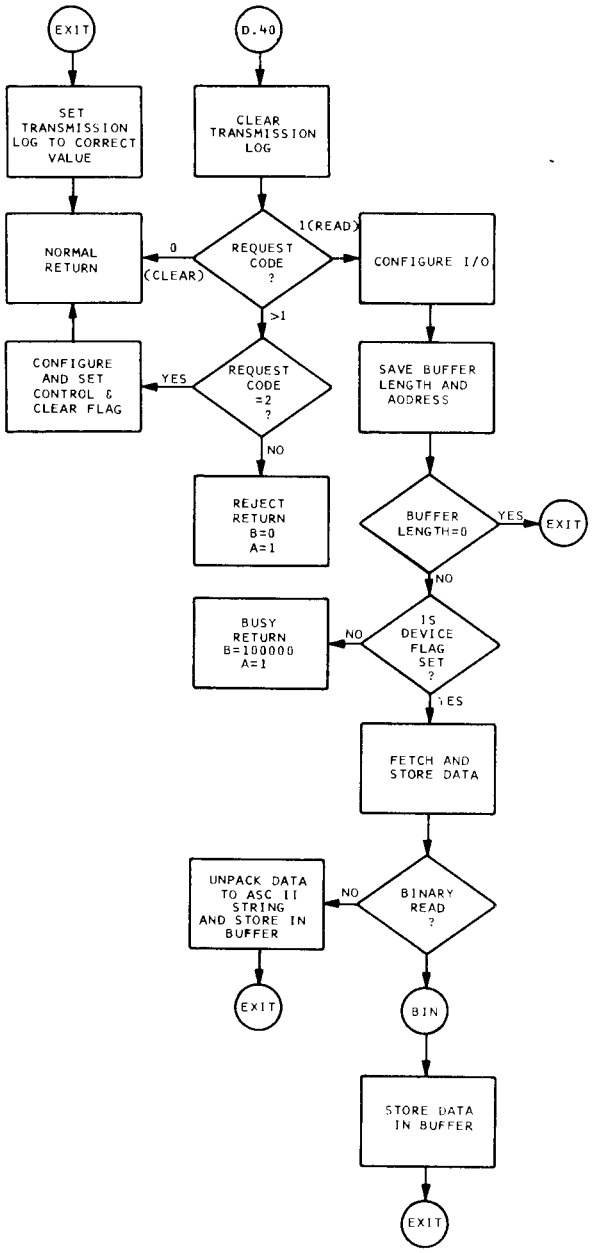


Figure B-1. D.40 Flowchart

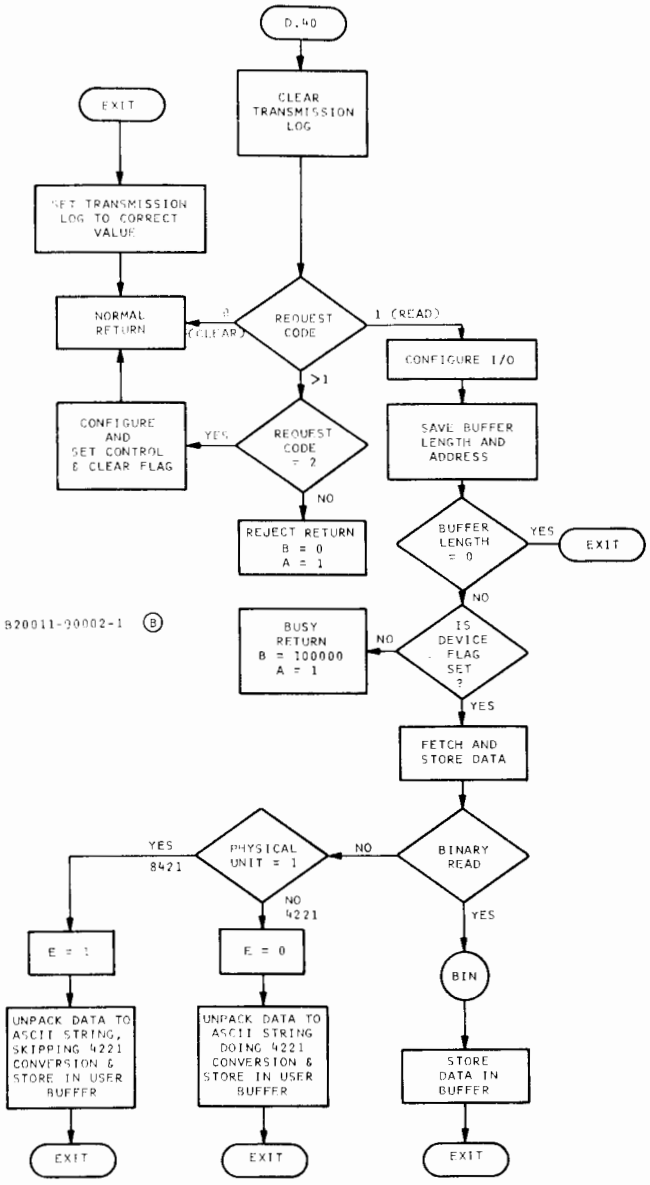


Figure B-2. D.40A Flowchart

P.C.S. WORKSHEET

SYSTEM SERIAL NO. ____________

TE ____________

25 24	26 25	27 26	30 27

HS INP?

HS PUN?

FWA MEM?

LWA MEM?

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
D.
xxxxx yyyyy

* LOAD
IOC
xxxxx yyyyy

* TABLE ENTRY

EQT?

(7) ________ , D. ________
(10) ________ , D. ________
(11) ________ , D. ________
(12) ________ , D. ________
(13) ________ , D. ________
(14) ________ , D. ________
(15) ________ , D. ________
(16) ________ , D. ________
(17) ________ , D. ________
(20) ________ , D. ________
(21) ________ , D. ________
(22) ________ , D. ________
(23) ________ , D. ________
(24) ________ , D. ________
(25) ________ , D. ________
(26) ________ , D. ________
(27) ________ , D. ________
(30) ________ , D. ________
(31) ________ , D. ________
(32) ________ , D. ________

/E
SQT?
-KYBD?

-TTY?

-LIB?

-PUNCH?

-INPUT?

-LIST?

DMA?

* LOAD

LOADR
xxxxx yyyyy

INTERRUPT LINKAGE?

________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
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________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
________ , ________ , ________
________ , ________ , ________

/E

NOTE: xxxxx yyyyy is the absolute lower and upper bounds of each program within BCS.

Figure B-3. PCS Worksheet

INPUT/OUTPUT CONFIGURATION WORKSHEET

SYSTEM SER # _____ PREPARED BY _____ DA

FIRST WORD OF AVAILABLE MEMORY (FWAM) _____

LAST WORD OF AVAILABLE MEMORY (LWAM) _____

STANDARD UNIT TABLE	I/O Interface Card Name	Select Code 11 10	12 11	13 12	14 13	15 14	16 15	17 16	20 17	21 20	22 21	23 22	24 23
1 KEY BOARD INPUT													
2 TELEPRINTER OUTPUT													
3 PROGRAM LIBRARY													
4 PUNCH OUTPUT													
5 INPUT													
6 LIST OUTPUT													
EQUIPMENT TABLE													

Driver Identification												
Interrupt Location												
Linkage Location												
Interrupt Entry Label												

APPENDIX C
INSTRUCTIONS FOR USING
DVR40 REAL-TIME EXECUTIVE DRIVER
WITH
HP 12604B DATA SOURCE INTERFACE KIT

APPENDIX C
INSTRUCTIONS FOR USING
DVR40 REAL-TIME EXECTIVE DRIVER
WITH
HP 12604B DATA SOURCE INTERFACE KIT

1-1. GENERAL INFORMATION

1-2. This appendix provides programming information and instructions for incorporating DVR40 into a Real-Time Executive (RTE) System. A sample FORTRAN program is included as Figure C-1 and the DVR40 Flowcharts are Figures C-2 and C-3. Detailed operating instructions for the RTE System are contained in the Real-Time Software Manual supplied with the system.

1-3. The RTE 12604B Data Source Interface (DSI) Driver DVR40 (HP Part No. 29100-60041) provides an interface for transferring up to 32 data bits into an HP Real-Time Executive System. The driver is entered through a FORTRAN or Assembler Language "call" to activate the DSI, take one 32 bit data reading, and store the data in a buffer defined by the calling program. The driver occupies 120 (octal) memory locations.

1-4. HARDWARE CONFIGURATION

1-5. The minimum RTE System hardware configuration is listed in the Real-Time Software Manual. No hardware modifications are required to either the DSI or the RTE System for proper operation of this driver.

2-1. PROGRAMMING

2-2. The driver, DVR40, is loaded into the RTE System during RTGEN execution as described in Section 7 of the Real-Time Software Manual. RTGEN entries for configuring a DSI into an RTE System are described starting at Paragraph 4-1 of this appendix. The following paragraphs describe some recommended methods for writing programs that use DVR40 in an RTE System.

2-3. CALLING SEQUENCES

2-4. The DVR40 driver can be called, via RTE, from FORTRAN or Assembler Language programs. A properly formatted program call to the driver causes: first, the calling program to be placed into I/O suspension; next, the driver to activate the DSI to take one 32 bit data reading which the driver then stores into the data buffer defined by the calling program; and, third, return of the calling program from I/O suspension to the RTE Scheduled List.

2-5. Three forms of FORTRAN calls can be used to activate the driver. The first two, binary READ statements, require the FORMATTER. The third form of call, although equivalent to the first two, does not require the FORMATTER. The FORTRAN calls are:

a. READ (IDRT) DATA

b. READ (IDRT) DATA, IFUN

c. CALL EXEC (1, IDRT, IDATA, L)

The Assembler Language call is:

```
      EXT EXEC
       .
       .
       .
      JSB EXEC
      DEF *+5
      DEF ONE
      DEF IDRT
      DEF IDATA
      DEF L
       .
       .
       .
```

Definitions of parameters:

ONE — A binary one. (This is the request code to both the driver and the RTE software. The latter interprets a request code of one as an I/O - READ request and passes the call list parameters to the driver in the proper format for DVR40.)

IDRT — The device reference number assigned to the DSI card.

DATA — A two-word variable in which two words (i.e., 32 bits) of DSI data are returned in the following order:

LOW-HALF : HIGH-HALF

IFUN — An integer variable which can be used if the DSI is interfacing an HP 2401C or HP 2402A Digital Voltmeter (DVM) to the RTE System. In this case, the four DVM function bits are returned in this additional integer variable. (If an HP 2402A overload occurs, a nine is returned as its function.)

IDATA — The name of the data buffer into which the DSI data is to be stored. (The buffer must be at least two words long--the length is specified by the next parameter, L.)

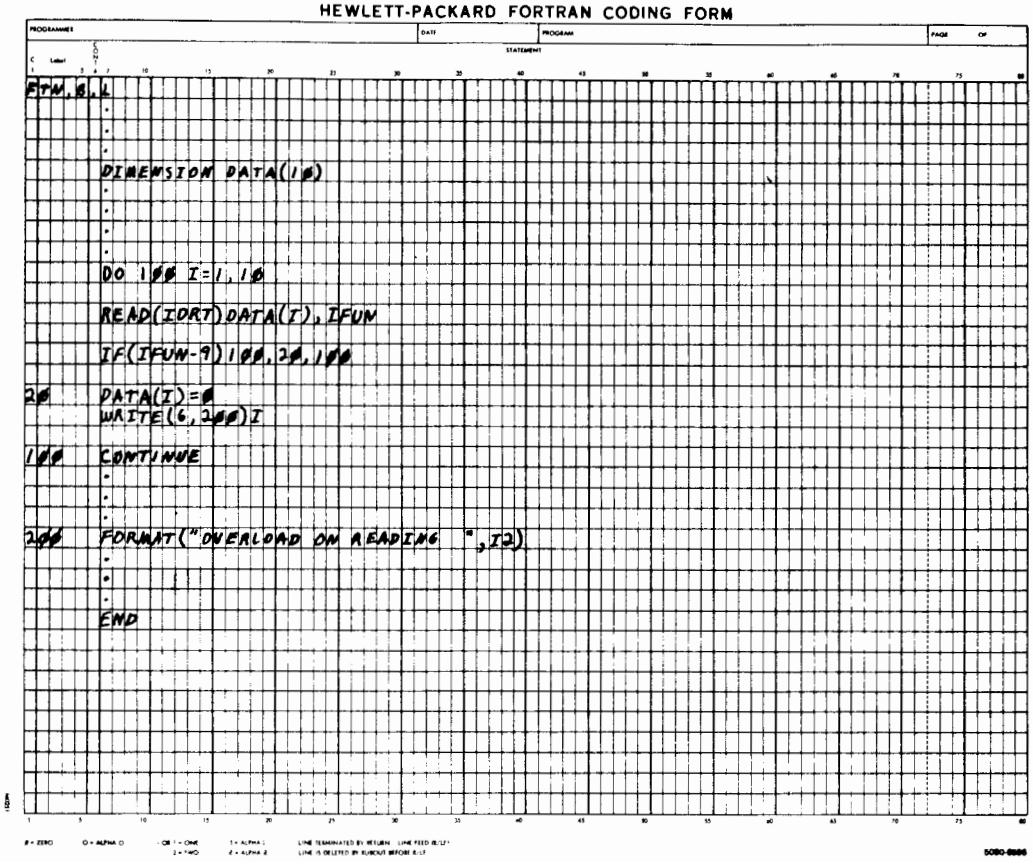

Figure C-1. Sample Program

L The length of the data buffer.

If L < 2, the READ request is rejected by the driver. If L = 2, the 32 bits of data from the DSI are stored as:

First Word input

Second Word input

If L > 2, the 32 bits are stored as in the L = 2 case, and additionally the DVM function bits are stored as the third buffer word to facilitate checking for DVM overload:

IDATA	D4	D3	D2	D1
IDATA+1	R	F	D6	D5
*IDATA+2				F

(Dn is a BCD digit, R is the DVM Range, and F is the DVM Function.)

2-6. SAMPLE PROGRAM

2-7. Figure C-1 illustrates a portion of a sample FORTRAN program which directs the DSI to take 10 readings, check each for overload, and store the data for later computations. In this particular case, the DSI card is interfacing a 2401C or 2402A DVM.

2-8. The DIMENSION statement reserves storage for the real array labeled DATA. Each of the 10 DSI data readings are stored in this array.

2-9. The next six statements form a DO loop which does the 10 DSI data readings.

2-10. READ is the statement which performs the operations as described in the calling sequence, Paragraph 2-4. Note that IFUN is to contain the 4 function bits of the DSI reading.

2-11. The IF statement checks the third word (IFUN) to determine if an overload condition exists (i.e., IFUN = 9). If overload is present, DATA (I) is set equal to zero and an overload message is printed on logical unit 6. If no overload is present, the 2 word BCD data reading is stored in DATA (I) for later computations.† The program then returns to the start of the DO loop for the next reading.

*In the case of 2402A overload--i.e., a Range of is returned--the variable IDATA+2 is set to 9 by DVR40.

†If the DSI is interfacing a 2401C or 2402A DVM, as in this case, the utility subroutine CONV (HP Part No. 20288-60001) can be used to convert the BCD data to floating point form.

3-1. PRINCIPLES OF OPERATION

3-2. Each DSI in the RTE System has one Equipment Table entry and one Interrupt Table entry. The DSI entry in the Equipment Table is busied for the duration of a single READ operation. Upon completion of the single 32 bit reading, the Equipment Table entry is set not-busy and the DSI is again available to any program in the RTE System. The driver is capable of controlling any number of DSI's in an RTE System.

3-3. The following paragraphs and flowcharts, Figures C-2 and C-3, provide a brief description of the driver operation.

3-4. Upon entry into the initiation section of DVR40 the driver first reconfigures the DSI trap cell. (The DSI trap cell is reconfigured so that entry is made to the driver upon DSI interrupt instead of to RTIOC. Refer to Paragraph 3-8, Special DSI Interrupt Processing for further explanation.)

3-5. The driver then determines that the Request Code is a "one" (READ) and a sufficient size buffer is defined by the calling program. If the request code and buffer size are correct, the DSI card is encoded and the driver exits to RTIOC.

3-6. When the DSI interrupts, the driver is entered. It disables the interrupt system, saves the registers in the interrupted program's ID segment, and enters RTIOC. RTIOC identifies the interrupting source and turns control over to the completion section of DVR40. The completion section is configured, a CLC DSI instruction executed, the data loaded from the DSI and stored into the buffer, and the transmission log stored into the B-Register. The driver then exits with an I/O-Completion indication to RTIOC.

3-7. Special DSI Interrupt Processing.

3-8. A "CLF DSI" instruction encodes the DSI. Ordinarily when any device interrupts the RTE, the CIC module of RTIOC is entered. CIC turns off the interrupt system, stores the registers into the interrupted program's ID Segment, and clears flag on the interrupting device. Because of this last action, it is necessary that, upon the DSI interrupt, entry be made not to CIC but to a routine which duplicates CIC except for the clear flag instruction. If the extraneous encode from CIC were permitted by allowing CIC to execute its "CLF DSI" instruction, the data on the DSI lines might be destroyed--depending on the instrument--when the Encode Switch on the DSI card is set so as to pass the encode on the instrument. To accomplish direct entry into the driver's own internal code upon DSI interrupt, the instruction in the trap cell corresponding to the DSI select code is changed by the initiation section of DVR40.

4-1. INCORPORATING DRIVER INTO RTE SYSTEM

4-2. During the execution of the RTGEN program, four things must be entered to configure the DSI into the RTE System being generated:

1. During Program Input Phase, the driver DVR40 must be loaded.

2. In the Disc Loading Phase, one Equipment Table entry must be made for each DSI:

```
*EQUIPMENT TABLE ENTRY
.
.
nn,DVR40
.
.
```

where "nn" is the select code of the DSI card.

3. A Device Reference Table entry must be made for each DSI:

```
*DEVICE REFERENCE TABLE
.
.
n = EQT# ?
m
.
.
```


where "n" is the device reference number to be assigned to the DSI and "m" is its position in the Equipment Table.

4. One entry must be made for each DSI in the Interrupt Table:

```
*INTERRUPT TABLE
.
.
nn,EQT,m
.
.
```

where "nn" is the select code of the DSI card and "m" is the position of the DSI entry in the Equipment Table.

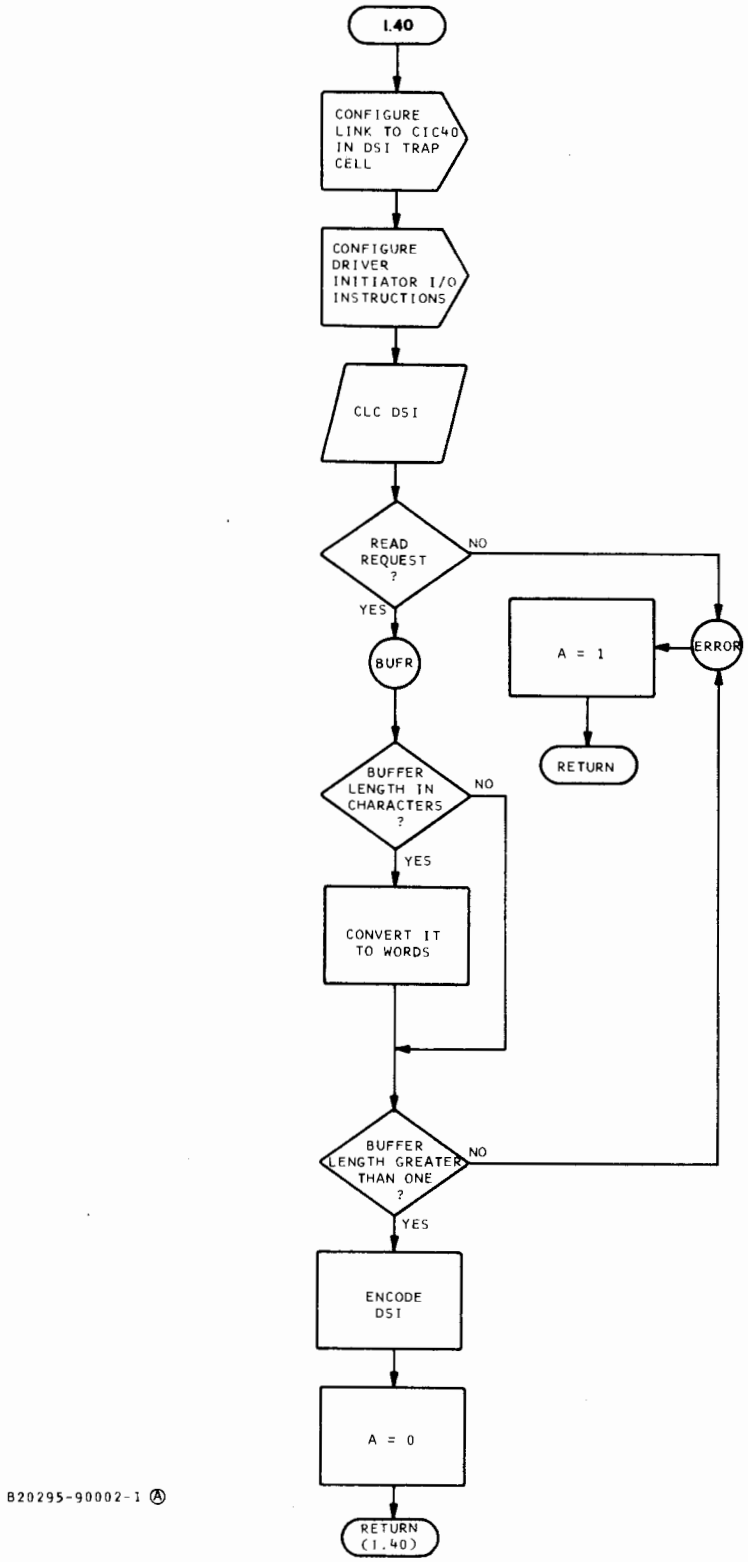

Figure C-2. Flowchart (Sheet 1 of 2)

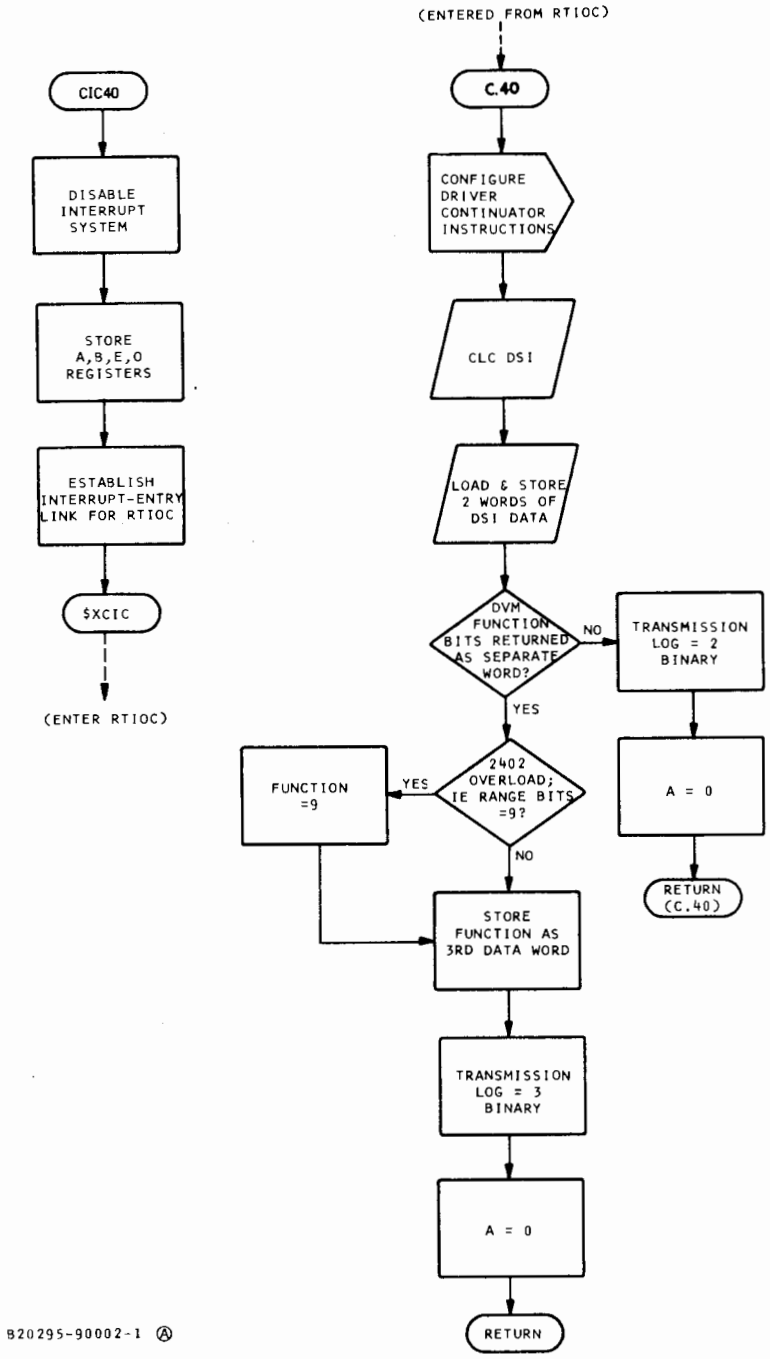

Figure C-2. Flowchart (Sheet 2 of 2)

APPENDIX D
FLOWCHARTS
FOR
HP 20337D DIAGNOSTIC PROGRAM

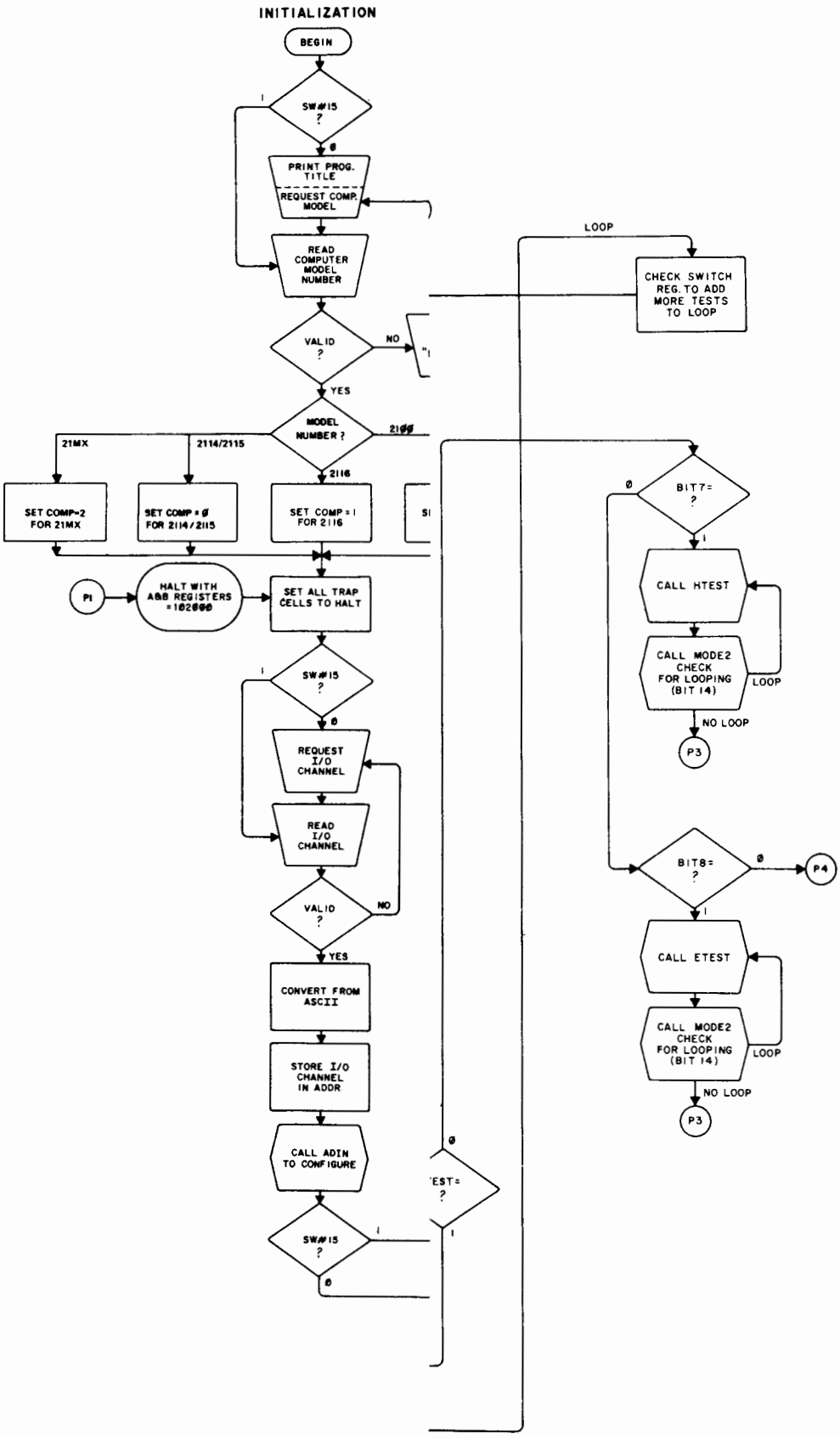

Figure D-1. Main Program

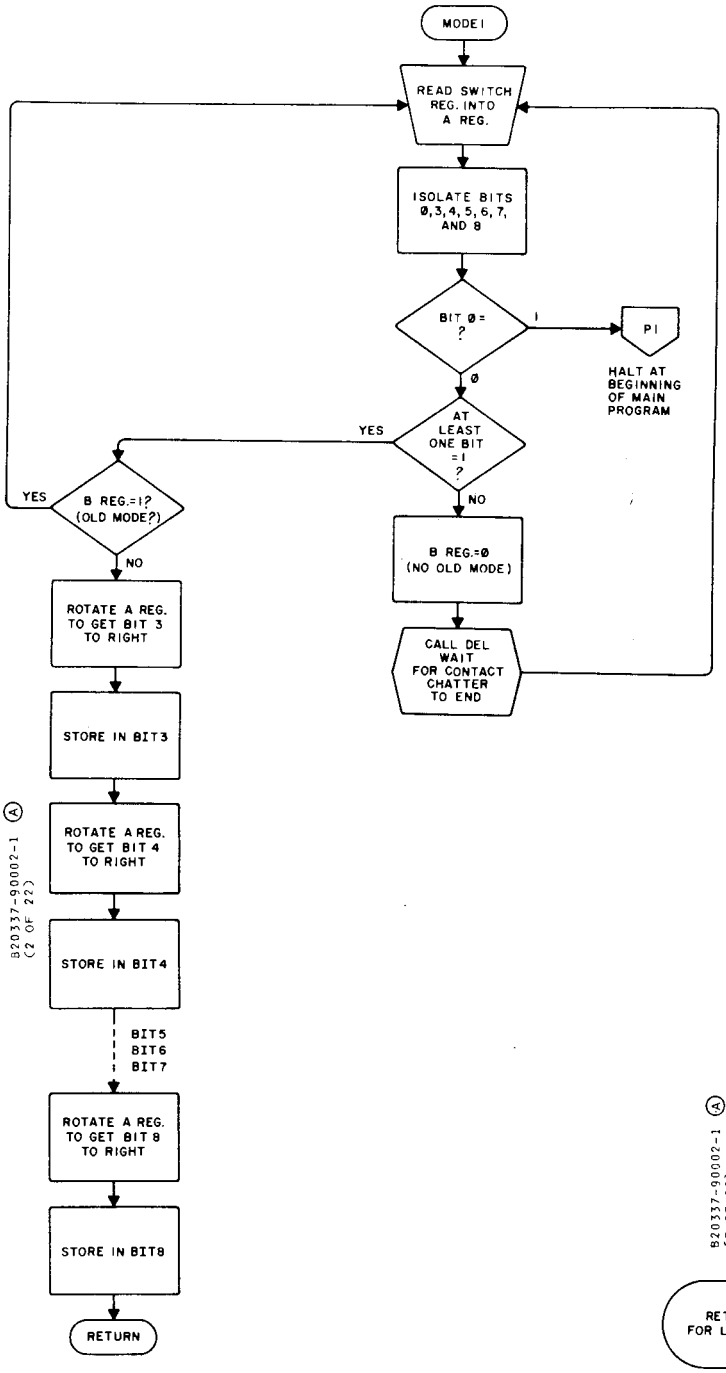

Figure D-2. Switch Register Storage Routine-One

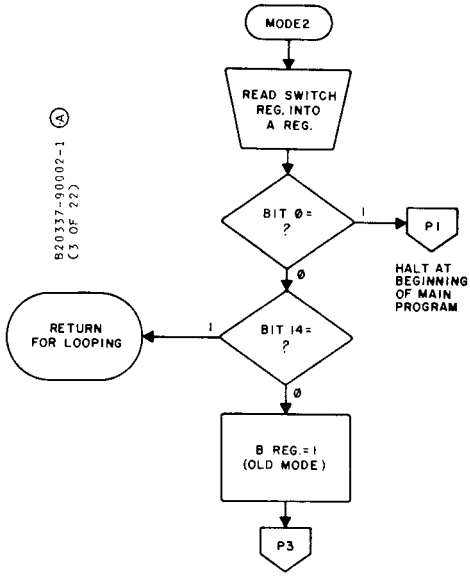

Figure D-3. Switch Register Storage Routine-Two

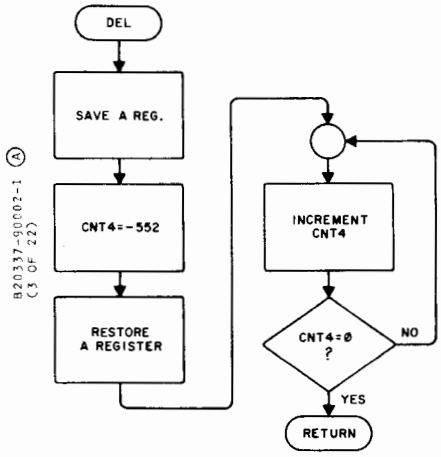

Figure D-4. Switch Register Chatter Delay Routine

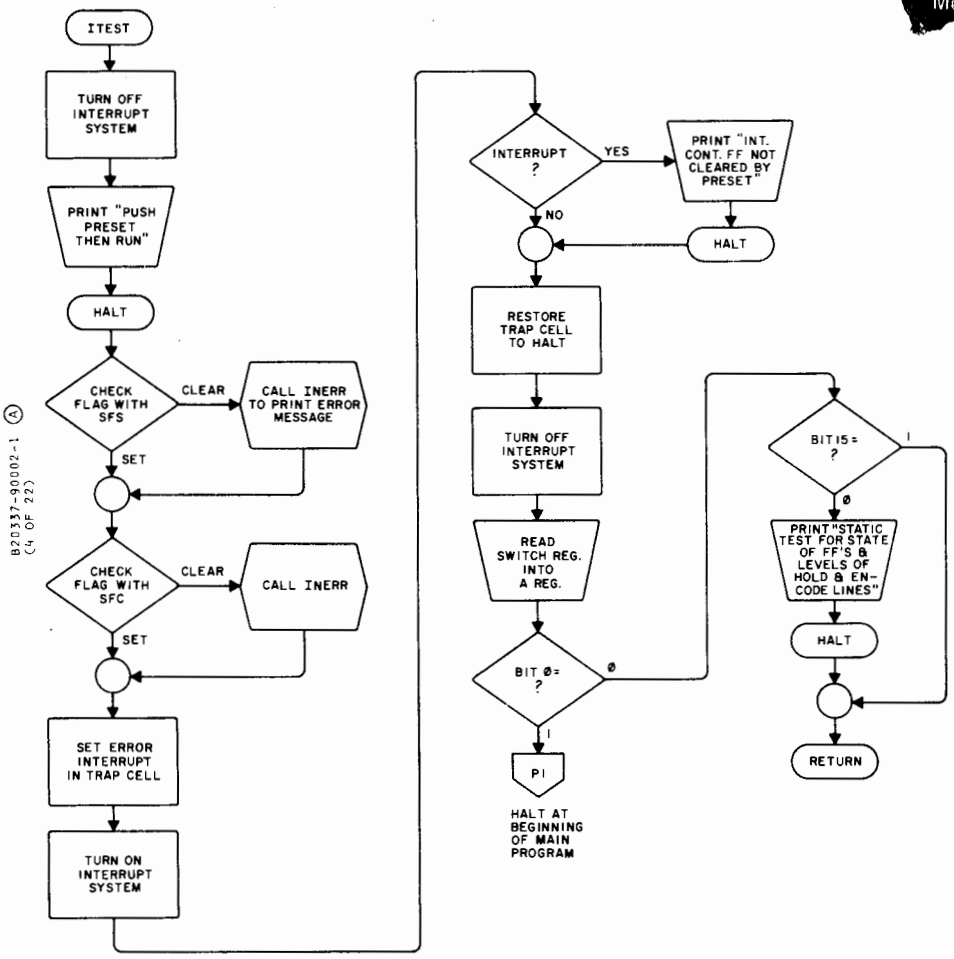

Figure D-5. Initial Test Routine

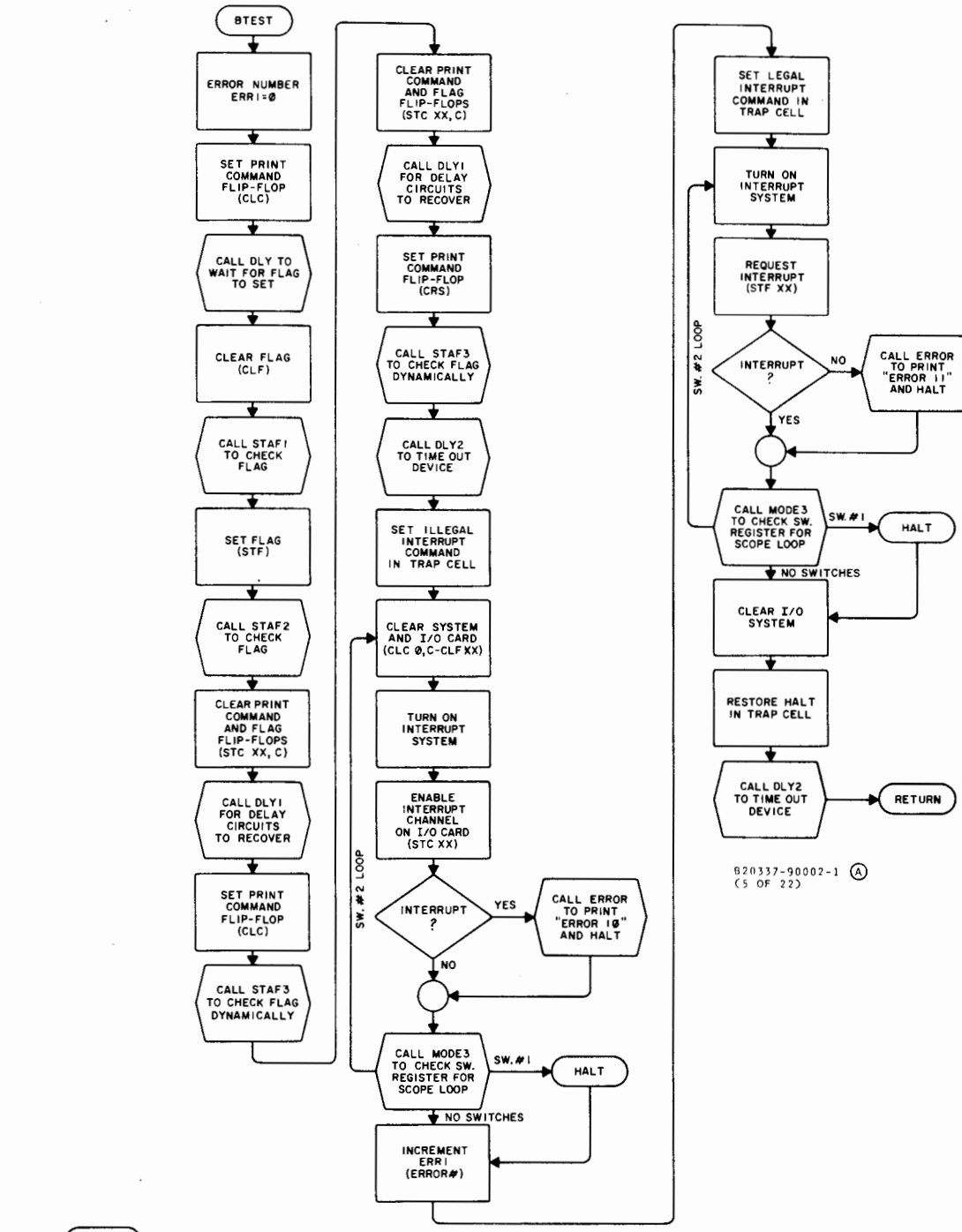

Figure D-7. Basic Timing Test Routine

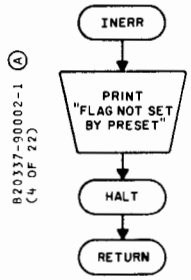

Figure D-6. Initial Test Error Routine

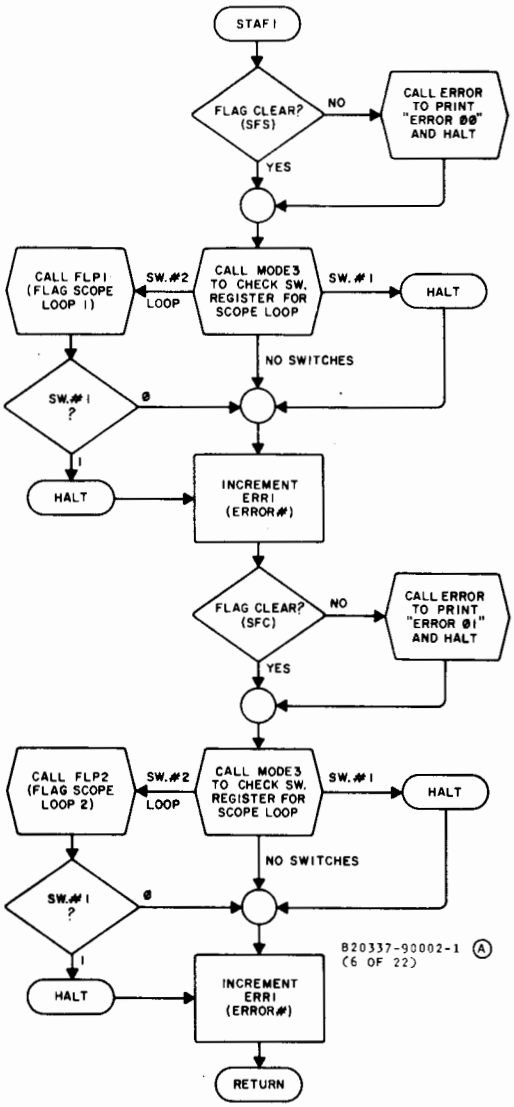

Figure D-8. Status Flag Check Routine-Clear

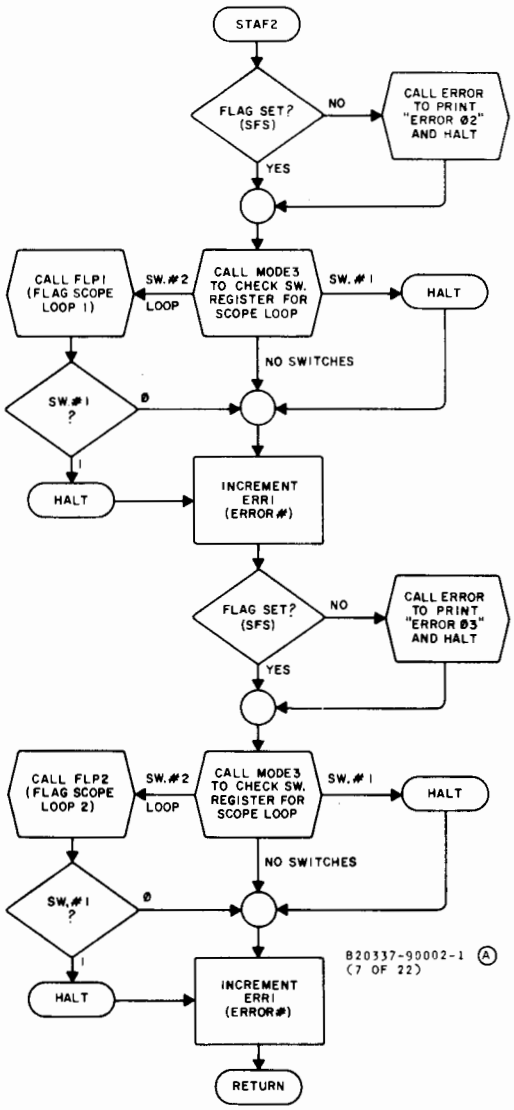

Figure D-9. Status Flag Check Routine-Set

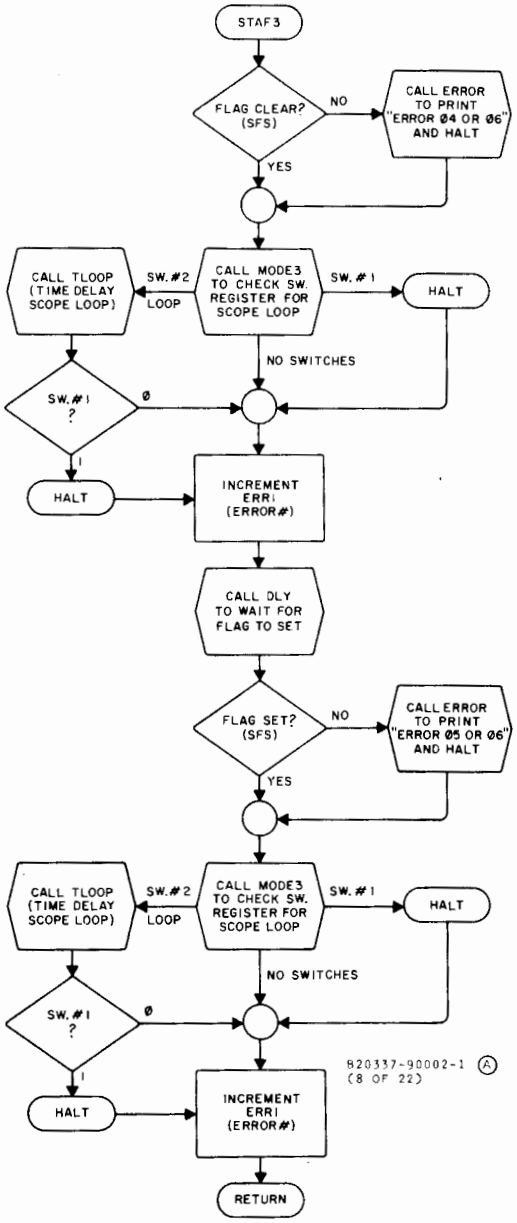

Figure D-10. Status Flag Check Routine-Dynamic

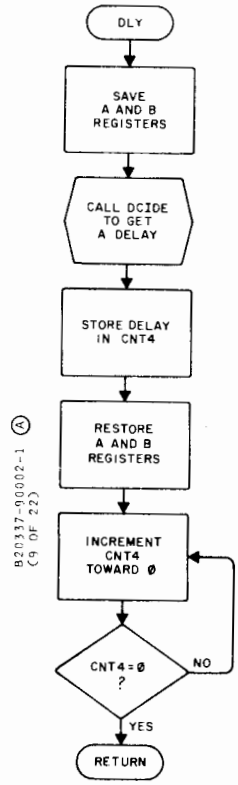

Figure D-11. Read Delay Routine - 0.2 or 2.0 Milliseconds

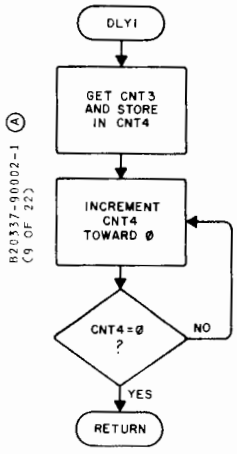

Figure D-12. Recovery Delay Routine - 50 or 300 Microseconds

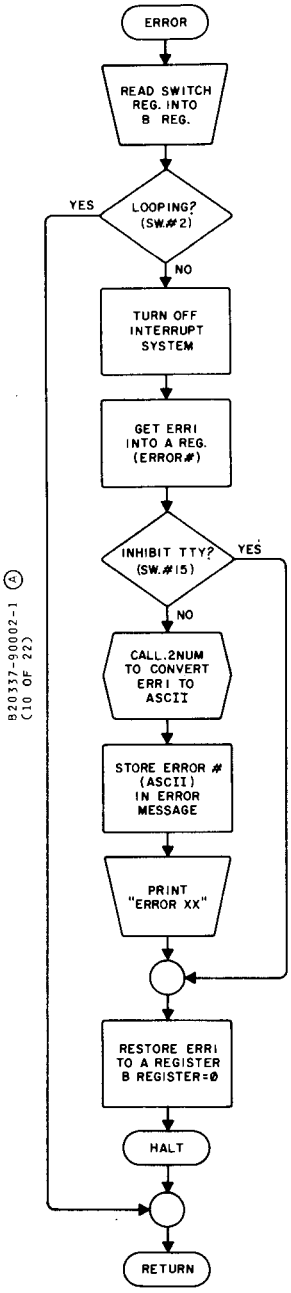

Figure D-13. Basic Timing Test Error Routine

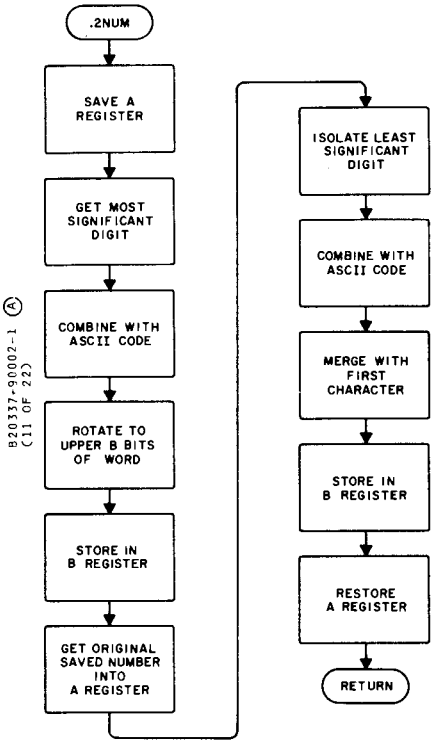

Figure D-14. Pack 2 ASCII Numbers Routine

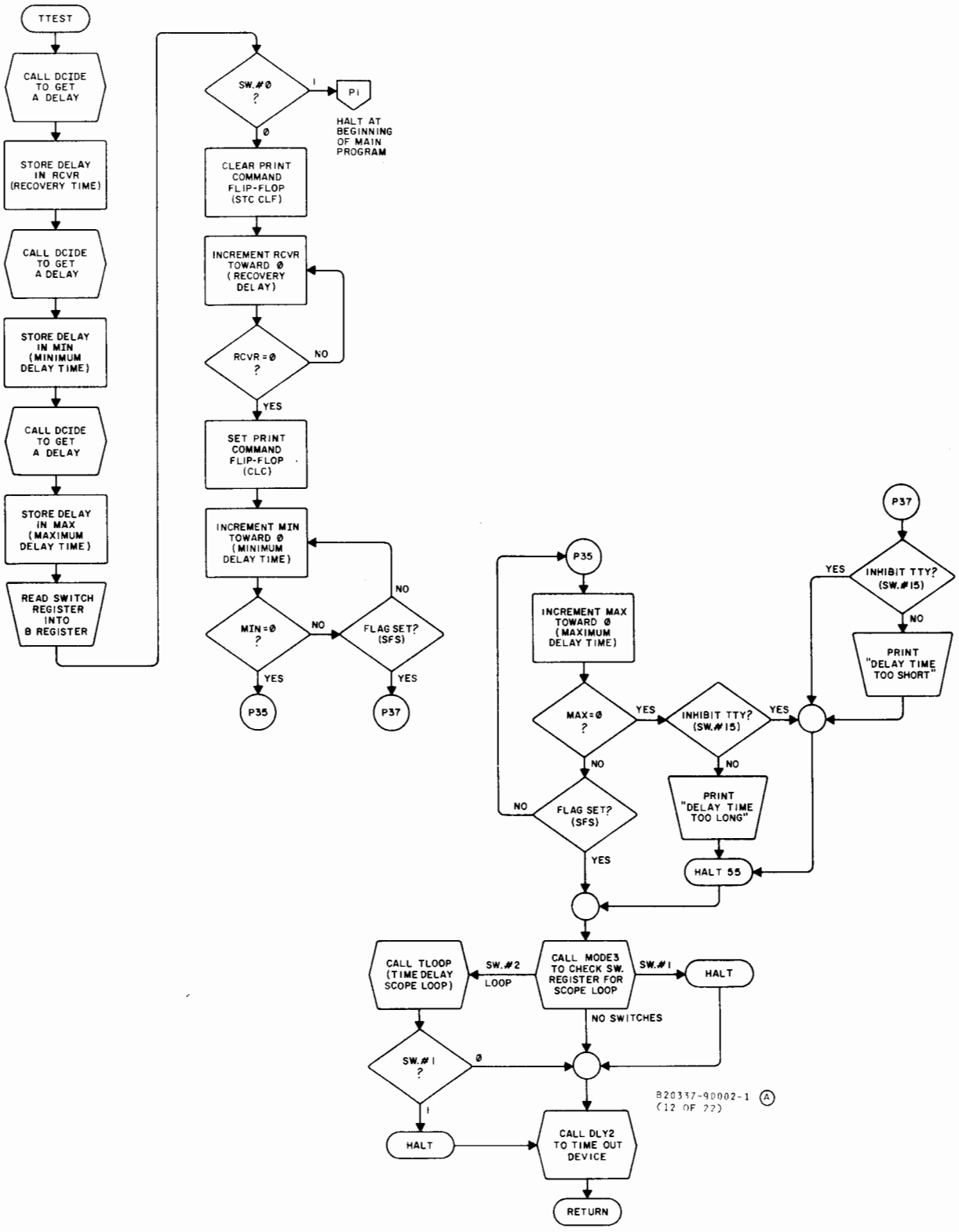

Figure D-15. Time Delay Test Routine

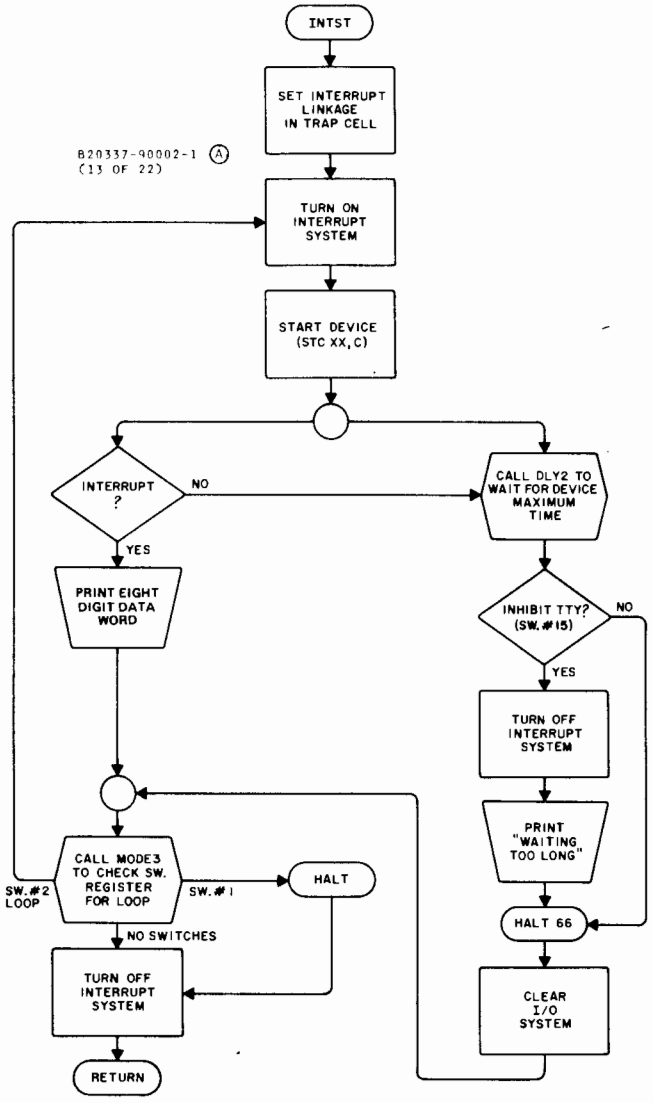

Figure D-16. Input Test Routine

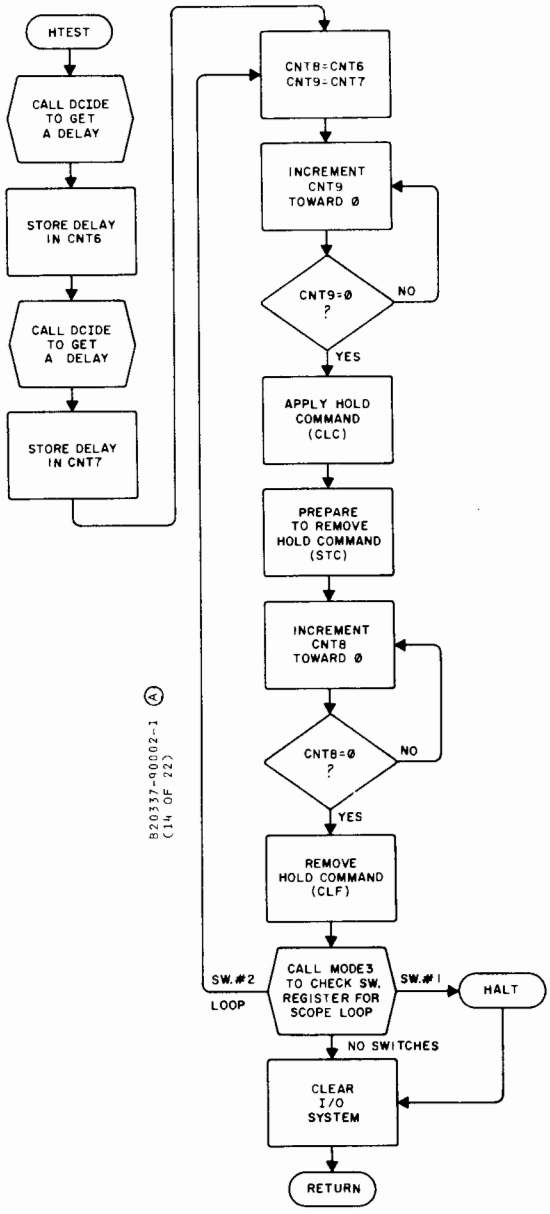

Figure D-17. Hold Command Scope Loop Routine

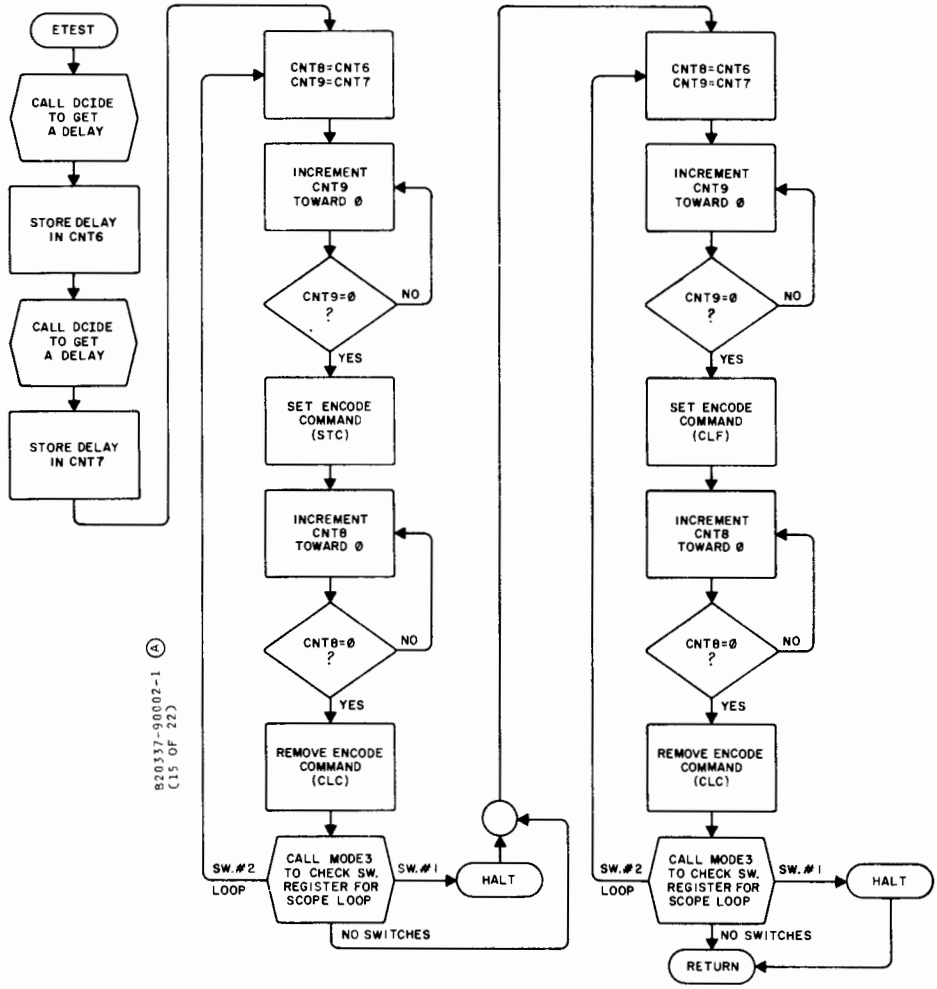

Figure D-18. Encode Command Scope Loop Routine

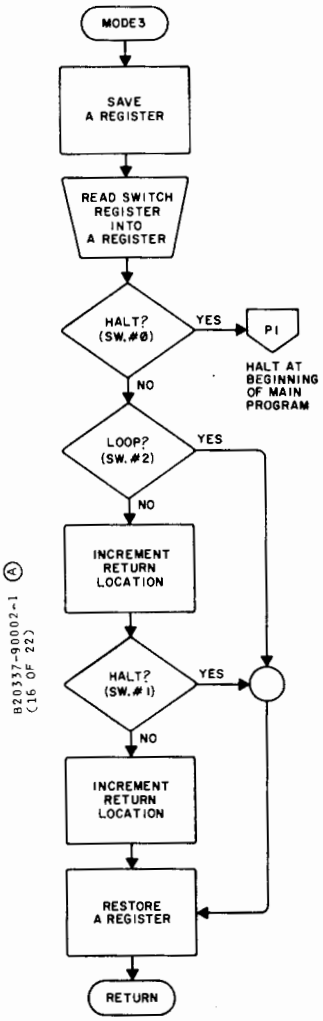

Figure D-19. Switch Register Storage Routine-Three

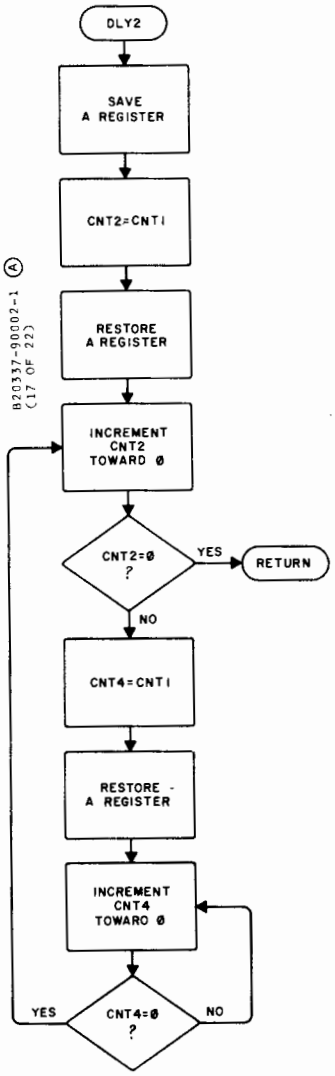

Figure D-20. Device Time-Out Delay Routine

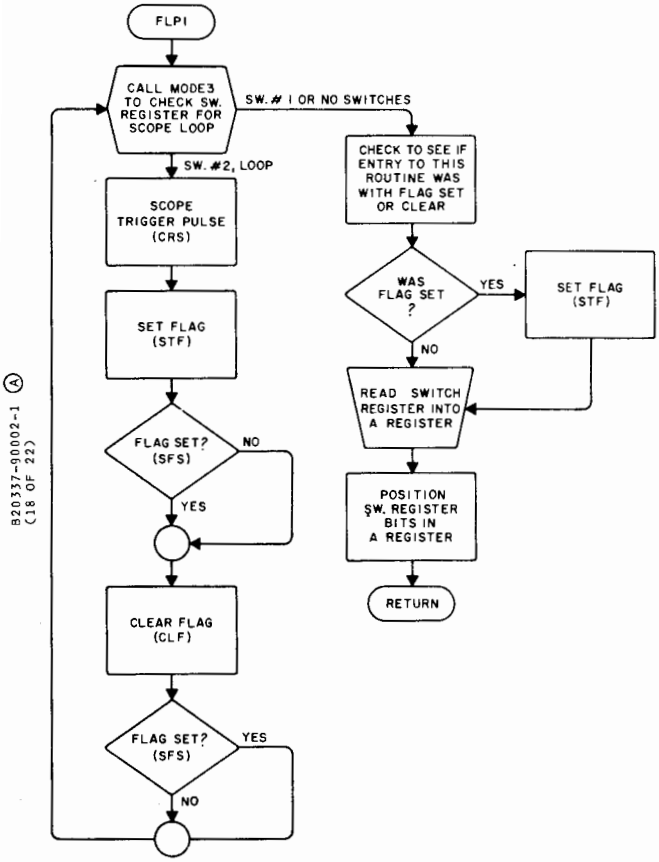

Figure D-21. Flag Scope Loop One

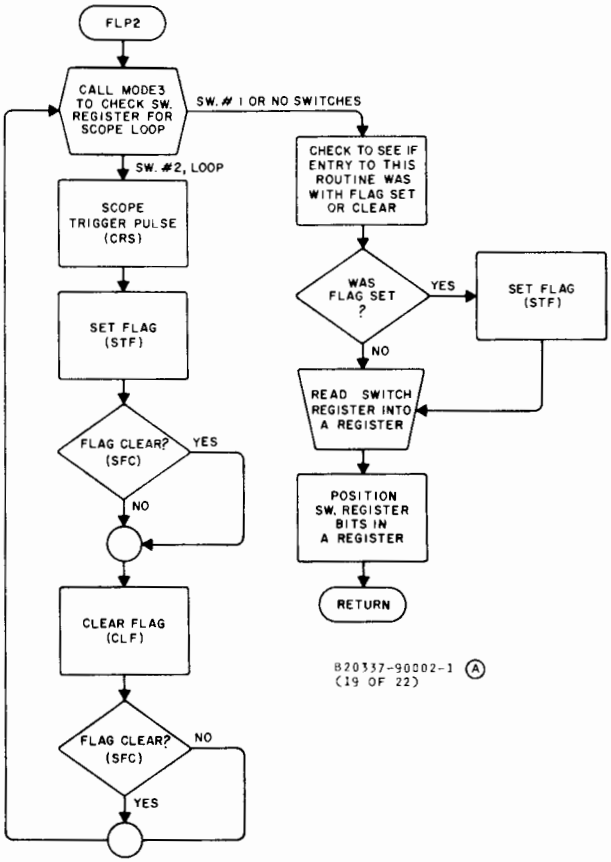

Figure D-22. Flag Scope Loop Two

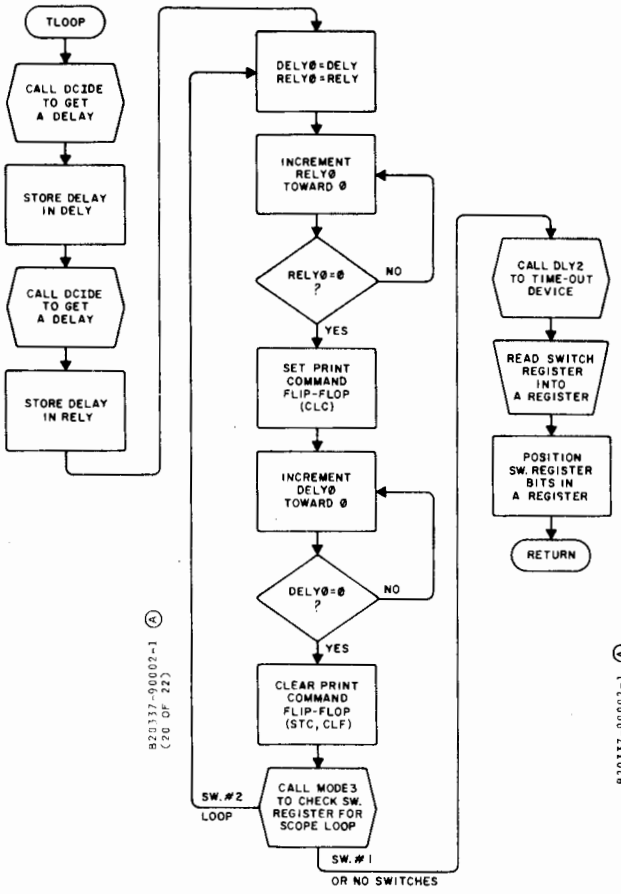

Figure D-23. Time Delay Scope Loop Routine

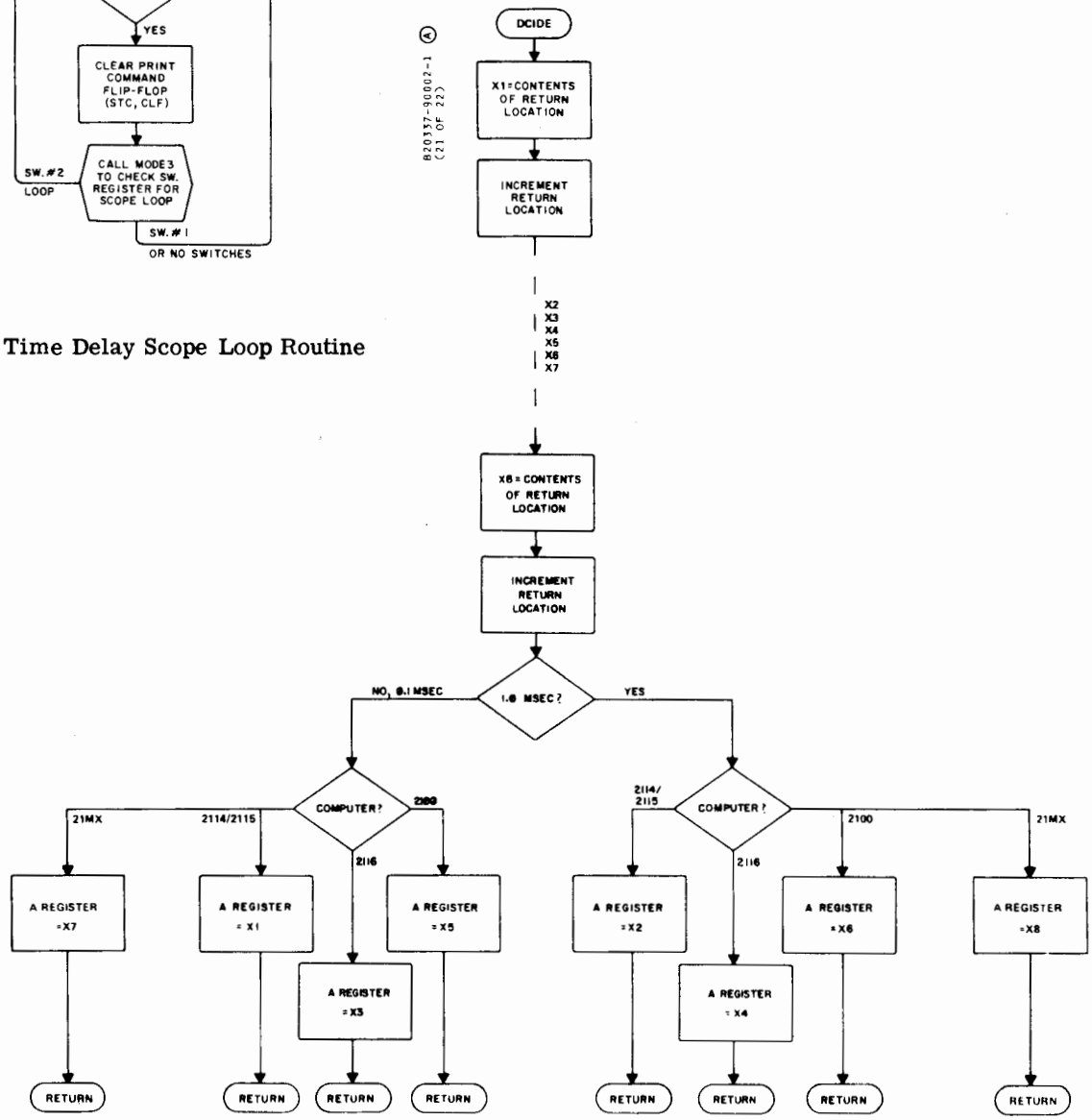

Figure D-24. Computer/Delay Decision Routine

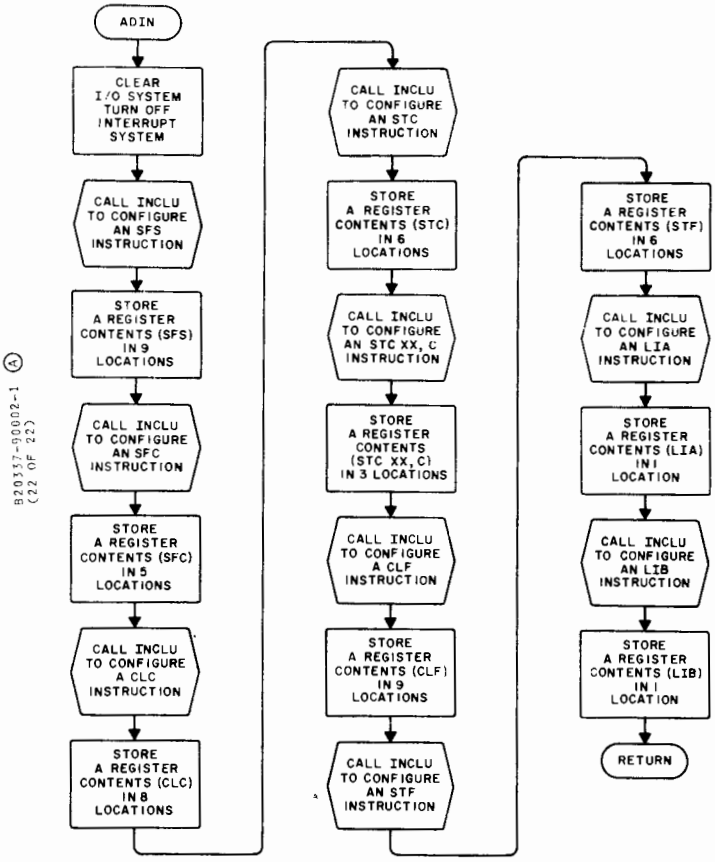

Figure D-25. Address Inclusion Routine

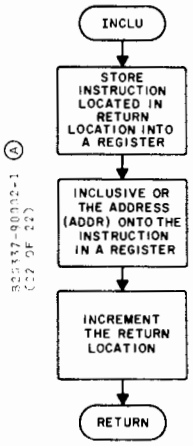

Figure D-26. Inclusion Routine