HEWLETT hp PACKARD

8-BIT DUPLEX REGISTER Interface Kit

model 12597A Including Options 01, 02, and 03

OPERATING AND SERVICING MANUAL 1 FEB 1969

SECTION I
INTRODUCTION AND DESCRIPTION

1-1. INTRODUCTION.

1-2. The Model 12597A 8-Bit Duplex Register Interface Kit provides a general-purpose interface between Hewlett-Packard Computers and an external device for 8-bit input or output operations. The HP 12597A Interface Kit is available in either positive or negative versions, and with various cables for interfacing to specific devices. The standard HP 12597A and basic options are described in Paragraphs 1-3 through 1-6.

1-3. STANDARD. The Standard HP 12597A Interface Kit consists of the following:

a. 8-Bit Duplex Register Interface Card, HP Part No. 12597-6001 (Positive-In/Positive-Out).

b. Connector Kit, 48-pin, HP Part No. 02116-6178.

c. Connector, 24-pin, HP Part No. 1251-0332.

d. 8-Bit Duplex Register Test Binary Tape, HP Part No. 20416C.

Note

Each tape has a suffix letter after the HP Accessory Number. This suffix letter is subject to change depending on the supplied version of the tape.

1-4. OPTION 01. Option 01 of the HP 12597A is identical to the standard kit except a Negative-in/Negative-out card, HP Part No. 12597-6002 replaces the Positive-in/Positive-out card.

1-5. OPTION 02. Option 02 adds to the standard kit an interconnecting cable (HP Part No. 12597-6004) for connecting to an HP 2748A Tape Reader and HP 2758A Tape Reader Reroller.

1-6. OPTION 03. Option 03 adds to the standard kit an interconnecting cable (HP Part No. 12597-6005) for connecting to an HP 2753A Tape Punch.

1-7. Sections II through IV provide installation and programming, theory of operation and replaceable parts information for the 8-Bit Duplex Register Card. A supplement to this manual contains a description of the diagnostic program contained in the 8-Bit Duplex Register Test Binary tape and diagnostic listing.

1-8. DESCRIPTION.

1-9. This card permits bidirectional transfer of data between the HP Computer and I/O device and operates with the I/O interrupt system. This card contains two eight-bit data storage registers, control and interrupt logic, and provides an Encode Command (action) signal to the I/O device and a Device Flag (action completed) signal from the I/O device. The card is a single address I/O card and plugs into any of the I/O slots of the Computer. The Data Registers operate with bits 0 through 7 of the Computer word. The supplied diagnostic test binary tape, used with a 24-pin jumper plug enables verification of the interface card without using the external I/O device.

1-10. The Connector Kit contains the connector (and its hood) which mates with the 48-pin side of the 8-Bit Duplex Register Card. The external-device connector and cabling may be supplied by the user.

1-11. SPECIFICATIONS.

1-12. Input/Output specifications are outlined in Table 1-1.

12597-9002

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Table 1-1. 8-Bit Duplex Register Specifications

CHARACTERISTICS	POSITIVE-IN/POSITIVE-OUT HP 12597A, HP 12597A-02, HP 12597A-03	NEGATIVE-IN/NEGATIVE-OUT HP 12597A-01
Output Levels		
"1" state	0 to +0.5V, 12 ma sink max.	-12V, 10K source
"0" state	+12V, 10K source	0 to +0.5V, 12 ma sink max.
Input Levels		
"1" state	0 to +0.5V, 12 ma sink max.	-8V
"0" state	+8V	0 to +0.5V, 12 ma sink max.
Bias and Impedance	+8V through 700 ohms	-8V through 700 ohms
Current Requirements		
+12V	0.05A	0.02A
-12V	0.02A	0.05A
-2V	0.05A	0.05A
+4.5V	0.75A	0.75A
Encode Output	Command signal to external device. Data ready in output register. Terminated by a Device Flag input.	
Device Flag Input	External device command to interface card. Signal strobes data into input storage register and sets Flag flip-flop on interface card.	
Dimensions		
Width	7-3/4 inches (196,8 mm)	
Height	8-11/16 inches (220,7 mm)	

SECTION II
INSTALLATION AND PROGRAMMING

2-1. INSTALLATION.

2-2. Plug the 8-Bit Duplex Register card into the I/O slot assigned for the particular Computer system. Run the Duplex Register diagnostic program described in the supplement using the 24-pin connector. If the diagnostic program is completed without error, the system operates properly.

2-3. Since the Duplex Register card is designed for use as an interface card for various external devices, an interconnecting cable must be prepared for the particular device being used. Table 2-1 lists the parts which are supplied by the connector kit and Figure 2-1 depicts the Connector Kit assembly diagram which must be prepared by the user. The 48-pin connector slides onto the end of the Duplex Register card containing the 48 printed-circuit paths (24 on each side of the card). As an aid in the preparation of the interconnecting cable, Table 2-2 lists the signals to and from the external I/O device and their pin assignments. Table 2-3 lists the pin connections from the 2748A and 2758A Readers to the interface card and Table 2-4 lists the pin connections from the 2753A to the interface card. After the cable is fabricated, connect the I/O device to the Computer as follows:

a. Turn power off.

b. Open the Computer for access to the I/O cards.

c. Pass the cable connector from the I/O device through the Computer opening and to the 48-pin connector of the card. Slide the connector onto the Duplex Register card, and close cover of the Computer.

2-4. PROGRAMMING.

2-5. The programs listed in Tables 2-5 through 2-7 are examples of input, output, and combined input/output through the 8-Bit Duplex Register using Assembly Language. The Duplex Register is assumed to be assigned select code GPR.

2-6. INPUT.

2-7. Command the external device to acquire and transfer 8 bits of information to the Computer. The results are left in the A-Register.

2-8. OUTPUT.

2-9. Output 8 bits of information from the A-Register to the external device and command it to accept the data.

2-10. COMBINED INPUT/OUTPUT.

2-11. Output 8 bits of command information, command the external device to take action, then read in 8 bits from the device. Command data is retained in the A-Register; input data is read into the B-Register.

2-12. CIRCUIT BOARD JUMPERS.

2-13. Table 2-8 lists the wire jumpers present on the 8-Bit Duplex Register card and the required positions for the indicated functions. See Figure 3-2 for the physical positions of the jumpers.

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HEWLETT PACKARD

DIAGNOSTIC TEST
for
8-BIT DUPLEX REGISTER
Computer Interface Kit

model
12597A
Including Options
01, 02, and 03

UPDATING SUPPLEMENT 15 SEPT 1969

MANUAL IDENTIFICATION

Manual Serial Prefixed:

Manual Printed: 1 Feb. 1969

Manual Part Number: 12597-9002

SUPPLEMENT DESCRIPTION

The purpose of this supplement is to correct manual errors (Errata) and to adapt the manual to instruments containing production improvements made subsequent to the printing of the manual. Enter the new information (or the Change Number, if more convenient) into the appropriate places in the manual, identified at left.

Changes 1 through 3 dated 15 September 1969.

CHANGE	DESCRIPTION
1	Change the diagnostic cover sheet title (top center of page DS-1) to read as follows: DIAGNOSTIC TEST for the 8-BIT DUPLEX REGISTER CARD
2	Change the NOTE on the cover sheet to read as follows: NOTE This diagnostic test program tests only the 8-Bit Duplex Register Card and not interconnecting cables or external devices to which the card may be connected. References in this program to the 16-Bit Duplex Register Card also apply to the 8-Bit Duplex Register Card.
3	On page DS-2, paragraph 6, step "c", change (12597-6001) to read: (12597-6001 and 12597-6002).

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Table 2-1. 48-Pin Connector Kit Parts List

ITEM	QTY	DESCRIPTION	PART NO.
1	1	Hood	02116-4001
2	2	Tapping Screw	0624-0096
3	1	Connector, 48-pin	1251-0335
4	1	Set Screw	3030-0143
5	1	Cable Clamp	02116-4003

Table 2-2. Connector Pin Assignments (Standard and Option 01)

TO I/O DEVICE		FROM I/O DEVICE	
PIN	SIGNAL	PIN	SIGNAL
A	Bit 0	1	Bit 0
B	Bit 1	2	Bit 1
C	Bit 2	3	Bit 2
D	Bit 3	4	Bit 3
E	Bit 4	5	Bit 4
F	Bit 5	6	Bit 5
H	Bit 6	7	Bit 6
J	Bit 7	8	Bit 7
		21	Status Enable
AA	Device Encode	23	Device Flag
BB	Ground	24	Ground

Table 2-3. 2748A and 2758A Connector Pin Assignments (Option 02)

48-PIN CONNECTOR	READER CONNECTOR	SIGNAL
1	B	Bit 1
2	F	Bit 2
3	L	Bit 3
4	R	Bit 4
5	V	Bit 5
6	Z	Bit 6
7	d	Bit 7
8	j	Bit 8
AA	AA	Read
23	FF	Feed Hole
24 BB	HH	Ground

Table 2-4. 2753A Connector Pin Assignments (Option 03)

48-PIN CONNECTOR	TAPE PUNCH CONNECTOR	SIGNAL
A	B	Bit 1
B	F	Bit 2
C	L	Bit 3
D	R	Bit 4
E	V	Bit 5
F	Z	Bit 6
H	d	Bit 7
J	j	Bit 8
AA	DD	Punch
23	FF	Flag
6	AA	Lo Tape
21 24 BB	HH	Ground

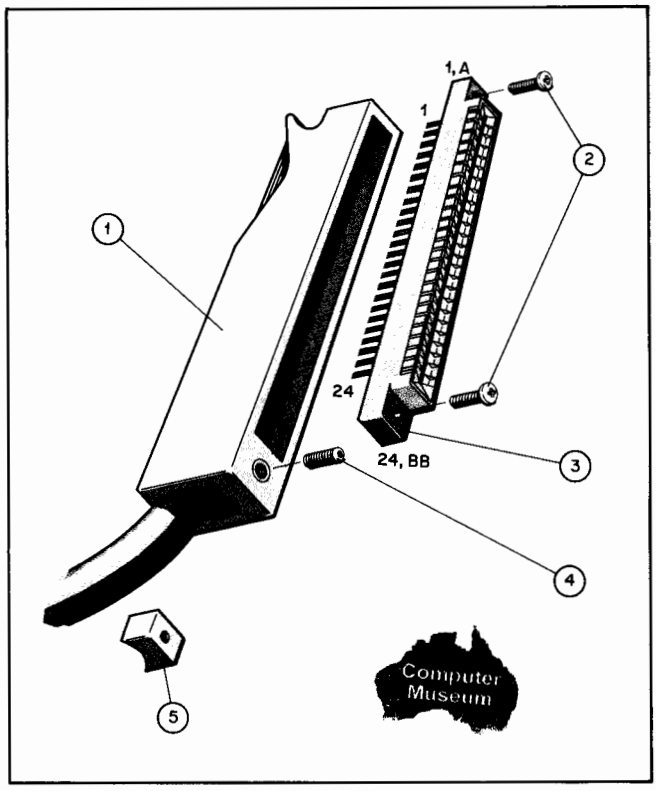


Figure 2-1. Connector Kit Assembly Diagram

Table 2-5. Input Program

```
MAIN PROGRAM
Label       Operation   Operand
                :
            JSB         INPUT       Jump to input subroutine.
            STA         CODE        Store A-Register contents in memory location CODE.
                :
SUBROUTINE
INPUT       NOP                     Entry point.
            STC         GPR,C       Encode external device to perform its function.
            SFS         GPR         Is operation complete?
            JMP         *-1         No, jump back to SFS instruction.
            LIA         GPR         Yes, transfer input data to A-Register.
            JMP         INPUT,I     Jump to main program.
```

Table 2-6. Output Program

```
MAIN PROGRAM
Label       Operation   Operand
                :
            LDA         N           Load A-Register with contents of memory location N.
            JSB         OUTPT       Jump to output subroutine.
                :
SUBROUTINE
OUTPT       NOP                     Entry point.
            SFS         GPR         Is External device busy?
            JMP         *-1         Yes, jump back to SFS instruction
            OTA         GPR         No, transfer output data to duplex register.
            STC         GPR,C       Encode external device to accept the data.
            JMP         OUTPT,I     Jump to main program.
```

Table 2-7. Input/Output Program

```
MAIN PROGRAM
Label       Operation   Operand
                :
            LDA         N           Load A-Register with contents of memory location N.
            JSB         IOSB        Jump to input/output subroutine.
            STB         CODE        Store B-Register contents in memory location CODE.
                :
SUBROUTINE
IOSB        NOP                     Entry point.
            OTA         GPR         Transfer data to duplex register.
            STC         GPR,C       Encode external device to accept or act on the data.
            SFS         GPR         Is External device busy?
            JMP         *-1         Yes, jump back to SFS instruction.
            LIB         GPR         No, transfer input data to B-Register.
            JMP         IOSB,I      Jump to main program.
```

Table 2-8. Jumper Strappings

JUMPER	POSITION	FUNCTION
W1	A	Clear Command, - signal
	B	Clear Command, + signal
W2	A	Flag, - signal
	B	Flag, + signal
W3		Negative going Device Encode signal (see W8)
W4		Gates data into input register when there is a Device Flag signal
W5	-12V	Positive-In/Positive-Out
	Open	Negative-In/Negative-Out
W6	-2V	Positive-In/Positive-Out
	Open	Negative-In/Negative-Out
W7	+12V	Positive-In/Positive-Out
	Open	Negative-In/Negative-Out
W8		Positive-going Device Encode signal (see W3)
W9		Gates data into input register with STF instruction
W10	Open	Positive-In/Positive-Out
	+12V	Negative-In/Negative-Out
W11	Open	Positive-In/Positive-Out
	-12V	Negative-In/Negative-Out
W12	Open	Positive-In/Positive-Out
	-12V	Negative-In/Negative-Out

SECTION III
THEORY OF OPERATION

3-1. GENERAL THEORY OF OPERATION.

3-2. INPUT OPERATIONS.

3-3. Refer to Figure 3-3 for the logic diagram of the standard (Positive-In/Positive-Out) HP 12597A interface card, and to Figure 3-4 for the logic diagram of the Option 01 (Negative-In/Negative-Out) interface card. A Set Control, Clear Flag (STC,CLF) instruction initiates the input of 8 bits of data from the I/O device. To enable the interrupt system a Set Flag (STF) instruction with a Select Code of 00 (octal) must be programmed. This sets the Interrupt System Enable flip-flop on the I/O Control Card.

3-4. The STC portion of the STC,CLF instruction sets the Command flip-flop which applies an Encode signal to the device, initiating its input function. The STC portion of the instruction also sets the Control flip-flop which provides an enable signal to the Interrupt Control logic on the 8-Bit Register Card. The CLF portion of the instruction resets the Flag flip-flop to prevent an interrupt signal from being sent to the Computer before the I/O device has transferred data to the Duplex Register Card.

3-5. When the I/O device is ready to transfer data to the Duplex Register Card, it applies a Device Flag signal to the card. This Flag signal enters data into the Input Storage Register and sets up a request for service (Skip Flag, SKF, if interrupt system is not being used, or Interrupt Request, IRQ). At time T2, the Duplex Register Card receives the Enable Flag (ENF) signal from the Computer. This signal and the output from the set-side of the Flag Buffer flip-flop sets the Flag flip-flop. If a device of higher priority has not requested an interrupt, the Flag flip-flop output initiates an interrupt signal to the Computer, indicating that data is available in the Input Storage Register.

3-6. The Computer must now accept the data from the Input Storage flip-flops of the Duplex Register Card by a Load Into A (LIA), Load Into B (LIB), Merge Into B (MIB) instruction before another input operation is initiated. If it is not accepted before another STC, CLF instruction is issued, the data will be lost. The IOI signal to the Duplex Register Card from the Computer, as a result of the LIA, LIB, or MIA, MIB instruction, enables the data on the input "and" gates (bits 0-7) of the Card to the Computer.

3-7. The set or reset condition of the Flag flip-flop may also be tested with a Skip on Flag Set (SFS) or Skip on Flag Clear (SFC) instruction to determine data availability to the Computer. When using this method, the Interrupt System Enable flip-flop on the I/O Control Card must be reset by a CLF instruction with a Select Code of 00 (octal).

3-8. OUTPUT OPERATIONS.

3-9. Refer to the applicable logic diagram, Figure 3-3 or Figure 3-4. The interrupt system is assumed to be enabled by previously setting the Interrupt System Enable flip-flop on the I/O Control Card with a Set Flag (STF) instruction and a Select Code of 00 (octal). This makes the input pin 8 (IEN) go true.

3-10. An Output from A (OTA) or an Output from B (OTB) instruction must be issued by the Computer program to output 8 data bits (0-7) from the A or B Register of the Computer to the Duplex Register Card and then to the I/O device. The IOO signal to the card, as a result of the OTA/B instruction, sets the Output Storage Register flip-flops. This transfers the data from the Computer into the Storage Register on the Duplex Register Card and makes the data available to the I/O device.

3-11. An STC,CLF instruction must then be issued by the Computer program. The STC portion of the instruction sets the Command flip-flop on the Register Card which applies a Device Encode signal to the I/O device, indicating that output data is available. The STC portion of the instruction also sets the Control flip-flop which provides an enable signal to the Interrupt Control logic on the Duplex Register Card. The CLF portion of the instruction resets the Flag and Flag Buffer flip-flops to prevent an interrupt signal from being sent to the Computer before the I/O device has accepted data and performed its operations. A CLF instruction is not necessary if no response is required back from the external device.

3-12. The device must now respond with a Device Flag signal to tell the Computer that the I/O device is ready for additional data. At time T2, the Duplex Register Card receives the ENF signal from the Computer. The ENF signal and the output from the set-side of the Flag Buffer flip-flop sets the Flag flip-flop. If a device of higher priority has not requested an interrupt, the Flag flip-flop initiates an interrupt signal to the Computer.

3-13. To output additional data, the Computer must transfer the new data to the Duplex Register Card before issuing another STC,CLF instruction. If the STC,CLF instruction precedes the output of new data, erroneous data may be received by the I/O device.

3-14. The set or reset condition of the Flag flip-flop may also be tested with an SFS or a SFC instruction to determine the readiness of the I/O device to accept data from the Computer. When using this method, the Interrupt System Enable flip-flop on the I/O Control Card must be reset by a CLF instruction with a Select Code of 00 (octal).

3-15. DETAILED THEORY OF OPERATION.

3-16. GENERAL.

3-17. Figure 3-3 depicts the logic diagram for the standard positive-in/positive-out 8-Bit Duplex Register Card and Figure 3-4 (Option 01) depicts the negative-in/negative-out logic diagram. For leadwire connections between the interface card and applicable I/O device, refer to Figure 3-3 or 3-4 and to Table 2-1. Figure 3-2 depicts the parts location diagram for both cards.

3-18. Logic diagram reference designations preceded by MC are identified by part number in Section IV and the logic diagram for each Microcircuit Package is shown in Figure 4-1.

3-19. COMPUTER POWER-ON.

3-20. When power is initially applied by the POWER switch, on the front panel of the Computer, the POPIO and CRS signals are received simultaneously by the interface card from the Computer. These signals establish initial conditions for operation of the interface card. The POPIO signal sets the Flag Buffer flip-flop through "nand" gate MC27C (the input to the flip-flop is inverted). At time T2, the ENF signal from the I/O Control card enables "nand" gate MC57C resetting the IRQ flip-flop. The output of gate MC57C is also transferred through "nand" gate MC57D, and with the output of the Flag Buffer flip-flop sets the Flag flip-flop. The POPIO signal is also transferred through "nand" gate MC66A strobing the Output Storage Register. The IOBO0 through 7 lines are at logic 0, therefore the register is set to logic 0. This means that the Output Storage Register is at logic 0 after Power turn-on. The Control Reset (CRS) signal is received at pin 13 and inverted by "nand" gate MC37B. The output from this gate resets the Control and Command flip-flops.

3-21. FLAG AND CONTROL LOGIC.

3-22. A programmed STC instruction with the Select Code of the 8-Bit Duplex Register Card initiates the output operation. This provides STC, LSCL, LSCM, and IOG signals to the Duplex Register Card. The STC signal is applied as one true input to "nand" gate MC37C. The LSCL, LSCM, and IOG signals are applied to "nand" gate MC36D, transferred through "nand" gate MC56A providing the second true input to gate MC37C. The false output of gate MC37C sets the Control and Command flip-flops. The set-side output of the Control flip-flop is applied as one true input to "nand" gate MC15A. The other inputs to this gate are the true IEN signal (generated by the set Interrupt System Enable flip-flop on the I/O Control Card) and the true output of the set-side of the Flag flip-flop. The output of "nand" gate MC15A is applied to "nand" gate MC25C and "and" gate MC47A. Gate MC47A will have a true output after the Flag flip-flop is reset and a device of higher priority has not requested an interrupt. Gate MC35A will have a false output at time T5 (SIR), when a device of higher priority has not requested an interrupt (PRH true), the Flag flip-flop is set (true), and the Flag Buffer flip-flop is set (true). The output of "nand" gate MC35A, is inverted setting the Interrupt Request flip-flop (IRQ). This flip-flop is reset at the next time T2 (ENF) to prevent further interrupts from this board. The set-side output of the IRQ flip-flop provides the FLGL (lower priority flag) and the IRQL (lower priority interrupt request) signals to the HP Computer. The Interrupt Acknowledge (IAK) signal from the I/O Control Card and the set-

side output of the IRQ flip-flop is applied to "nand" gate MC17D. The output of this "nand" gate or the output of "nand" gate MC37A resets the Flag Buffer flip-flop to prevent further interrupt requests.

3-23. DEVICE COMMAND.

3-24. The true set-side output of the Command flip-flop may be transferred through jumper W3 which puts a positive voltage on the base of transistor Q17. This turns Q17 on which transfers a negative going Device Encode signal to pin AA of the 48-pin connector. To change the negative-going Device Encode signal to a positive-going Device Encode signal, disconnect jumper W3 and connect jumper W8. This transfers the true set-side output of the Command flip-flop to the input of "nand" gate MC46A. The false output of this gate is transferred through jumper W8 which puts a negative potential, developed across resistor R117, on the base of transistor Q17. This turns Q17 off which transfers a positive going Device Encode signal to pin AA of the 48-pin connector. The Command flip-flop is cleared by the Device Flag signal through "nand" gate MC86A, or by a CLC instruction or by a CRS signal.

3-25. DEVICE FLAG.

3-26. The Device Flag signal is received from the I/O device, at pin 23, and responds to either a positive going or negative going signal. Jumper W1 sets up the condition that clears the Command flip-flop and jumper W2 sets up the condition that sets the Flag Buffer flip-flop. Jumper W2 also allows data to be strobed, through jumper W4, to the Input Storage Register. Figure 3-1 depicts the timing diagram for the Device Flag circuit.

3-27. DEVICE FLAG POSITIVE BOARD. When a negative going (positive voltage to ground) Device Flag signal is received at pin 23, transistor Q18 is turned off. A positive output from the collector of Q18 is applied to "nand" gate MC94A. The output from MC94A (ground) is transferred through the delay network consisting of R26, R27 and C19 to "nand" gate MC94C. This causes the output of MC94C to go positive and the output of MC94D to go to ground. This ground signal is transferred through speed-up resistor R28 and applied to MC94C. This Schmitt Trigger action helps speed-up the signal applied at MC94D. The ground output from MC94D is transferred to the B position of jumpers W1 and W2, and also inverted by "nand" gate MC94B and applied to the A position of jumpers W1 and W2. Therefore for a negative going Device Flag signal, position A of jumper W1 clears the Command flip-flop and position A of jumper W2 sets the Flag Buffer flip-flop and strobes data into the Input Storage Register.

3-28. The two pulse generator circuits MC86B and MC86A, MC86C and MC86D, respond only to a signal which is at ground and goes positive. Capacitor C20 and resistor R30 or capacitor C21 and resistor R31 determine the pulse width of the output pulse which is approximately 300 nanoseconds. Therefore, for a negative going input Device Flag signal (+ voltage to ground) jumper W1 and W2 must be in A position.

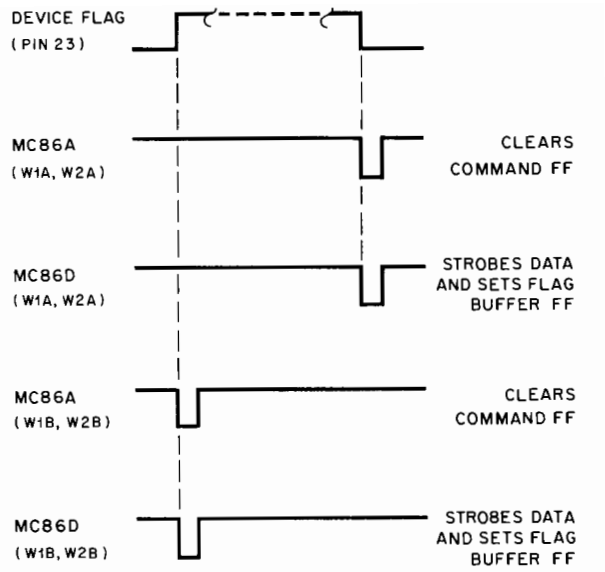


Figure 3-1. Device Flag Timing Diagram

When the signal is transferred through W1A the Command flip-flop is cleared and when the signal is transferred through W2A the Flag Buffer flip-flop is set and data is strobed into the Input Storage Register through jumper W4.

3-29. When a positive going (ground to positive voltage) Device Flag signal is received at pin 23, transistor Q18 is turned on. A negative output from the collector of Q18 is applied to "nand" gate MC94A. The output from MC94A (positive) is transferred through the Delay network consisting of R26, R27 and C19 to "nand" gate MC94C. This causes a ground output from MC94C and the output from MC94D to go positive. This positive signal is transferred through speed-up resistor R28 and applied to MC94C. This Schmitt Trigger action helps speed-up the signal applied at MC94D. The positive output from MC94D is transferred to the B position of jumpers W1 and W2, and also inverted by "nand" gate MC94B and applied to the A position of W1 and W2 as a ground output. Therefore for a positive going Device Flag signal, position B of jumper W1 clears the Command flip-flop and position B of jumper W2 sets the Flag Buffer flip-flop and strobes data into the Input Storage Register.

3-30. Jumpers W1 and W2 do not have to be set for the same polarity signal. These jumpers may be set in either position. Example: An input Device Flag signal (pin 23) can clear the Command flip-flop on the positive edge and on the negative edge set the Flag Buffer flip-flop and strobe the input data into the Input Storage Register.

3-31. DEVICE FLAG NEGATIVE BOARD. With negative going Device Flag signal (ground to negative) applied at pin 23, the output of "nand" gates MC94A and MC94D go to ground and jumpers W1A and W2A should be used. With a positive going Device Flag signal (negative to ground) applied at pin 23, the output of "nand" gates MC94A and MC94B go positive and jumpers W1B and W2B should be used.

3-32. The Status Enable line, pin 21, enables the user to input data to the card without gating it from a Device Flag signal. A ground is required on pin 21 to enable the Input Storage Register.

3-33. POSITIVE-IN/POSITIVE-OUT STORAGE REGISTERS.

3-34. Input and output logic levels from the external I/O device or to the external I/O device are as follows:

Logic "1" = ground
Logic "0" = + voltage

3-35. OUTPUT REGISTER. When IOBO signals are transferred from the Computer (via backplane wiring) to the Output Storage Register, -0.5 volts (logic 0) or +2.5 volts (logic 1) is received at the input to the storage register. Since all IOBO circuits are identical, only IOBO0 will be explained.

3-36. A logic 1 from the Computer, received through connector pin 35, will set the Bit 0 flip-flop, MC44A when IOO + POPIO signal is transferred from the Computer, to pin 4 of MC44A. This latches the data into the flip-flop where the positive voltage (logic 1) is output on pin 16 of the Bit 0 flip-flop. This positive voltage is transferred to the base of transistor Q9, turning the transistor on, and data (ground) is transferred to the I/O device through pin A of the 48-pin connector. This signal is capable of sinking 12 milliamperes from an external positive source.

3-37. A logic 0 from the Computer, received through connector pin 35, resets the Bit 0 flip-flop, MC44A, during IOO. The Bit 0 flip-flop is latched when IOO goes false. The set-side output of this flip-flop is at ground and is applied to the base of transistor Q9, turning the transistor off. With transistor Q9 in the off state a logic 0 is transferred to the I/O device through pin A of the 48-pin connector, as a positive voltage.

3-38. INPUT REGISTER. When Bit 0 through Bit 7 signals are transferred from the I/O device to the Input Storage Register, a ground potential (external transistor on) or positive voltage (external transistor off) is received at the input to the register. Since the Bit 0 through Bit 7 circuits are identical, only Bit 0 will be explained.

3-39. A ground potential capable of sinking at least 12 milliamperes is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 is cut-off which applies a positive voltage to pin 2 of the Bit 0 flip-flop, MC34A. A Device Flag signal is transferred from the I/O device through the Device Flag circuit, jumper W4 and "nand" gate MC66B to pin 4 of MC34A. This strobes the data through the flip-flop where the positive voltage output at pin 16 is transferred as one true input to pin 14 of "and" gate MC45A. The other true signal is the IOI · [LSCM · LSCL · IOG] signal. This enables "and" gate MC45A, and data (positive voltage) is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBI0 signal (logic 1).

3-40. A positive-voltage or open circuit is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 conducts which applies a ground potential to pin 2 of the Bit 0 flip-flop, MC34A. When the Device Flag signal occurs, data is stored. Therefore, the set-side output of MC34A is at a ground level, which is transferred to pin 14 of "and" gate MC45A. With this false input to "and" gate MC45A, the output (pin 13) is also ground which is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBI0 signal (logic 0).

3-41. NEGATIVE-IN/NEGATIVE-OUT STORAGE REGISTERS.

3-42. Input and output logic levels from the external I/O device or to the external I/O device are as follows:

Logic "1" = - voltage
Logic "0" = ground

3-43. OUTPUT REGISTER. When IOBO signals are transferred from the Computer (via backplane wiring) to the Output Storage Register, -0.5 volts (logic 0) or +2.5 volts (logic 1) is received at the input to the storage register. Since all IOBO circuits are identical, only IOBO0 will be explained.

3-44. A logic 1 from the Computer, received through connector pin 35, will set the Bit 0 flip-flop, MC44A when IOO + POPIO signal is input, from the Computer, to pin 4 of MC44A. This latches the data into the flip-flop and the positive voltage (logic 1) is output on pin 16 of the Bit 0 flip-flop. This positive voltage is transferred to the base of transistor Q9, turning the transistor off. With Q9 in the off state, a negative voltage is transferred to the I/O device, through pin A of the 48-pin connector.

3-45. A logic 0 from the Computer, received through connector pin 35, resets the Bit 0 flip-flop, MC44A, during IOO. The Bit 0 flip-flop is latched when IOO goes false. The set-side output of this flip-flop is at ground and is applied to the base of transistor Q9, turning the transistor on. With transistor Q9 in the on state, a ground potential is transferred to the I/O device, through pin A of the 48-pin connector. This signal is capable of sinking 12 milliamperes from an external negative source.

3-46. INPUT REGISTER. When Bit 0 through Bit 7 signals are transferred from the I/O device to the Input Storage Register, a ground potential (external transistor on) or negative voltage (external transistor off) is received at the input to the register. Since the Bit 0 through Bit 7 circuits are identical, only Bit 0 will be explained.

3-47. A negative voltage or open circuit is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 is cut-off which applies a logic 1 (positive voltage) to pin 2 of the Bit 0 flip-flop, MC34A. A Device Flag signal is input from the I/O device, through the Device Flag circuit, jumper W4, and "nand" gate MC66B to pin 4 of MC34A. This strobes the data through the flip-flop where a positive potential is output on pin 16 and transferred to pin 14

of "and" gate MC45A. The other true signal is the IOI·[LSCM·LSCL·IOG] signal. This enables "and" gate MC45A and data (logic 1) is transferred to the Computer through pin 26 of the 86-pin connector, as an IOBI0 signal (logic 1).

3-48. A ground potential capable of sinking at least 12 milliamperes is transferred through connector pin 1 to the base of transistor Q1. Transistor Q1 conducts which applies a ground potential to pin 2 of the Bit 0 flip-flop, MC34A. Therefore, the set-side of MC34A is at a false level which is transferred to pin 14 of "and" gate MC45A. When the Device Flag signal occurs data is stored. With this false input to "and" gate MC45A, the output (pin 13) is also at a ground potential which is transferred to the Computer, through pin 26 of the 86-pin connector, as an IOBI0 signal (logic 0).

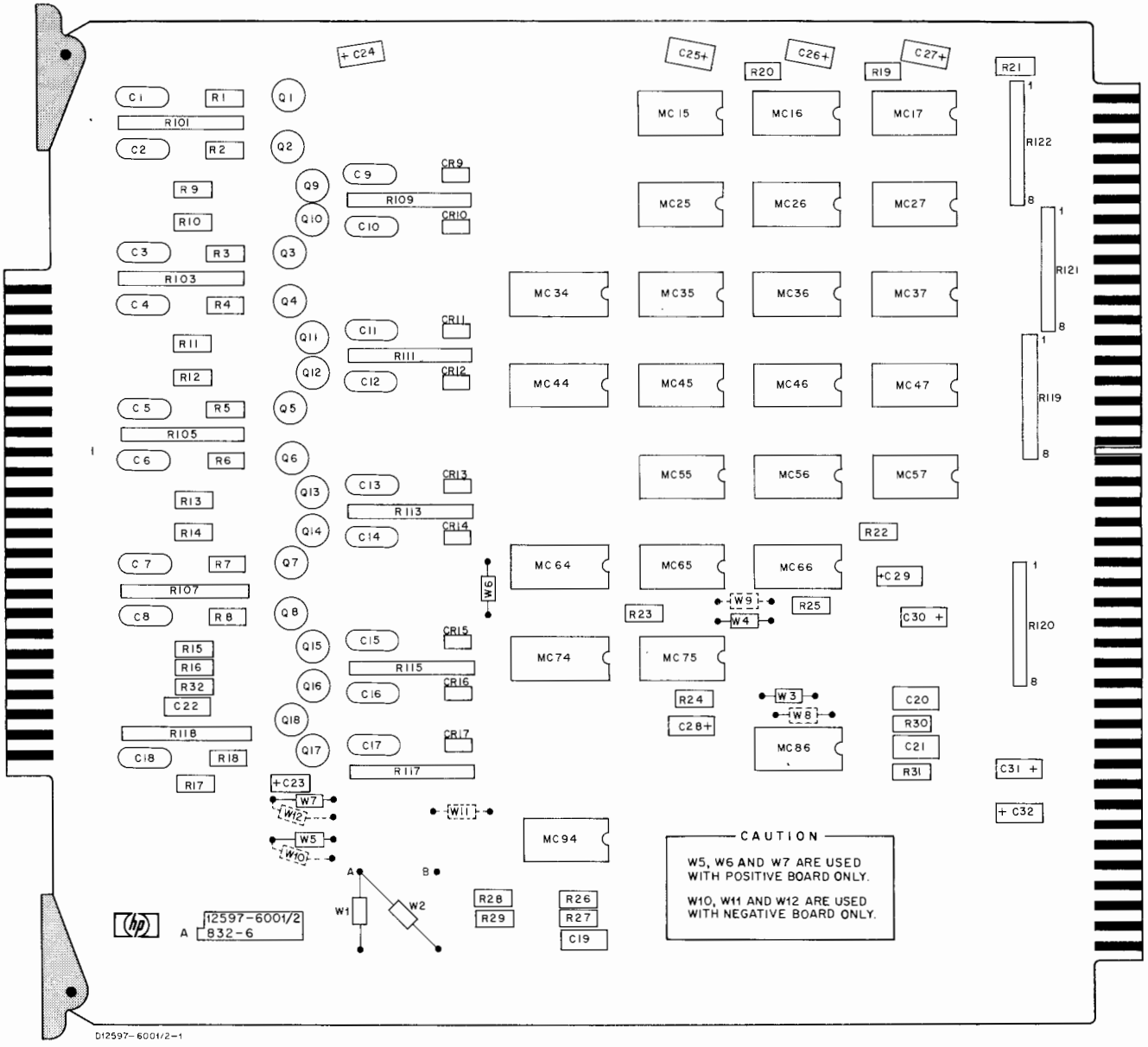


Figure 3-2. 8-Bit Duplex Register, Part Location Diagram

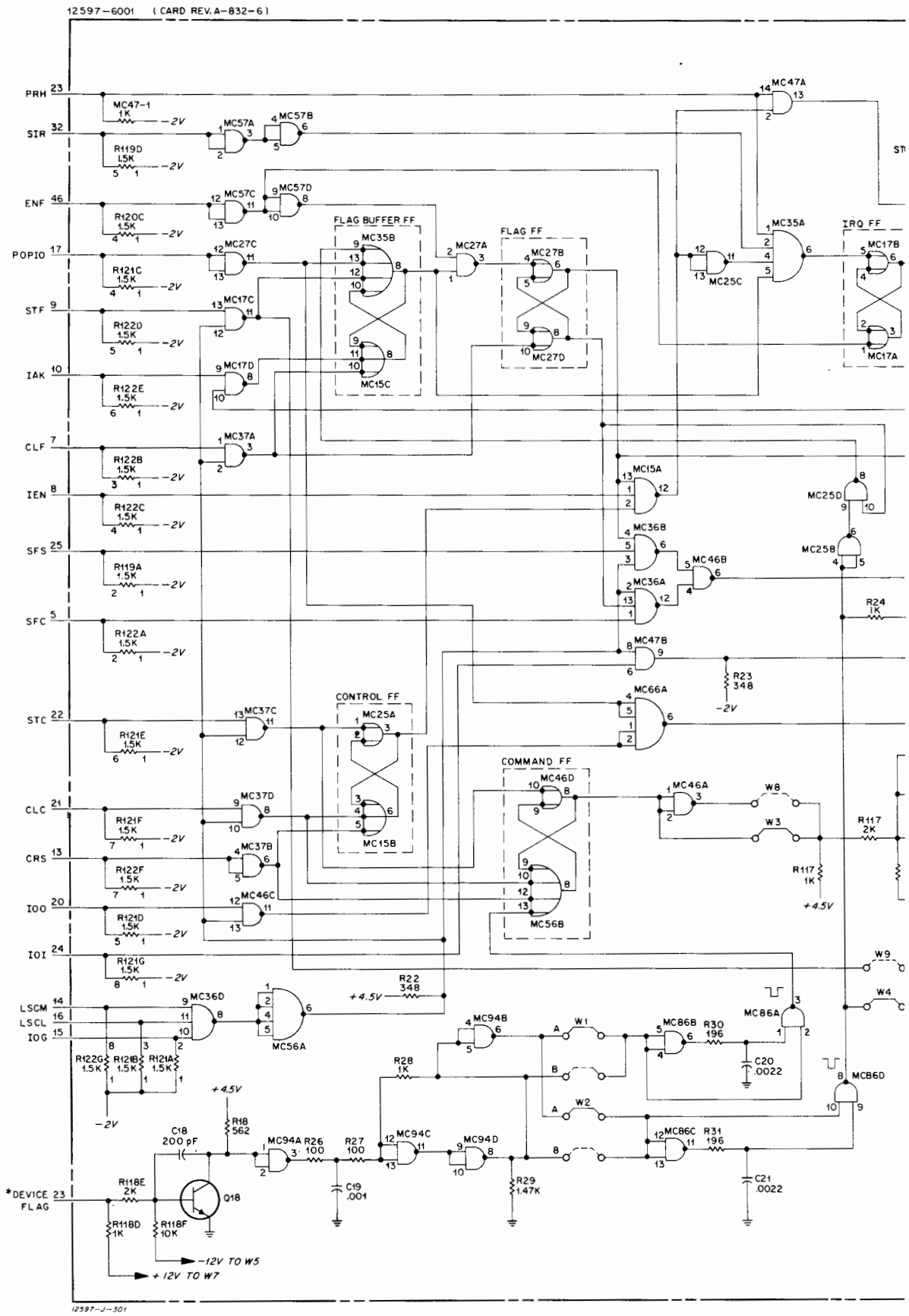
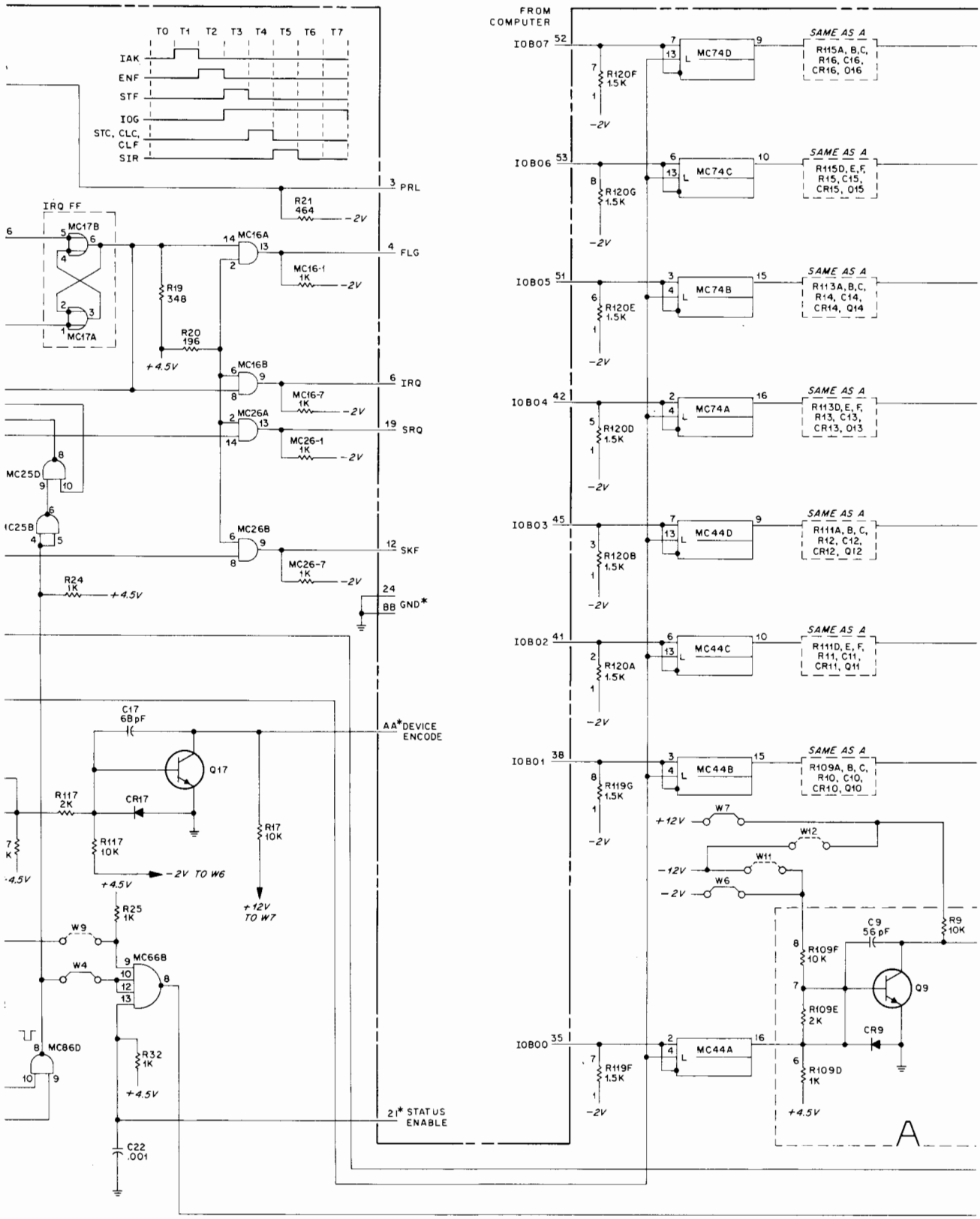
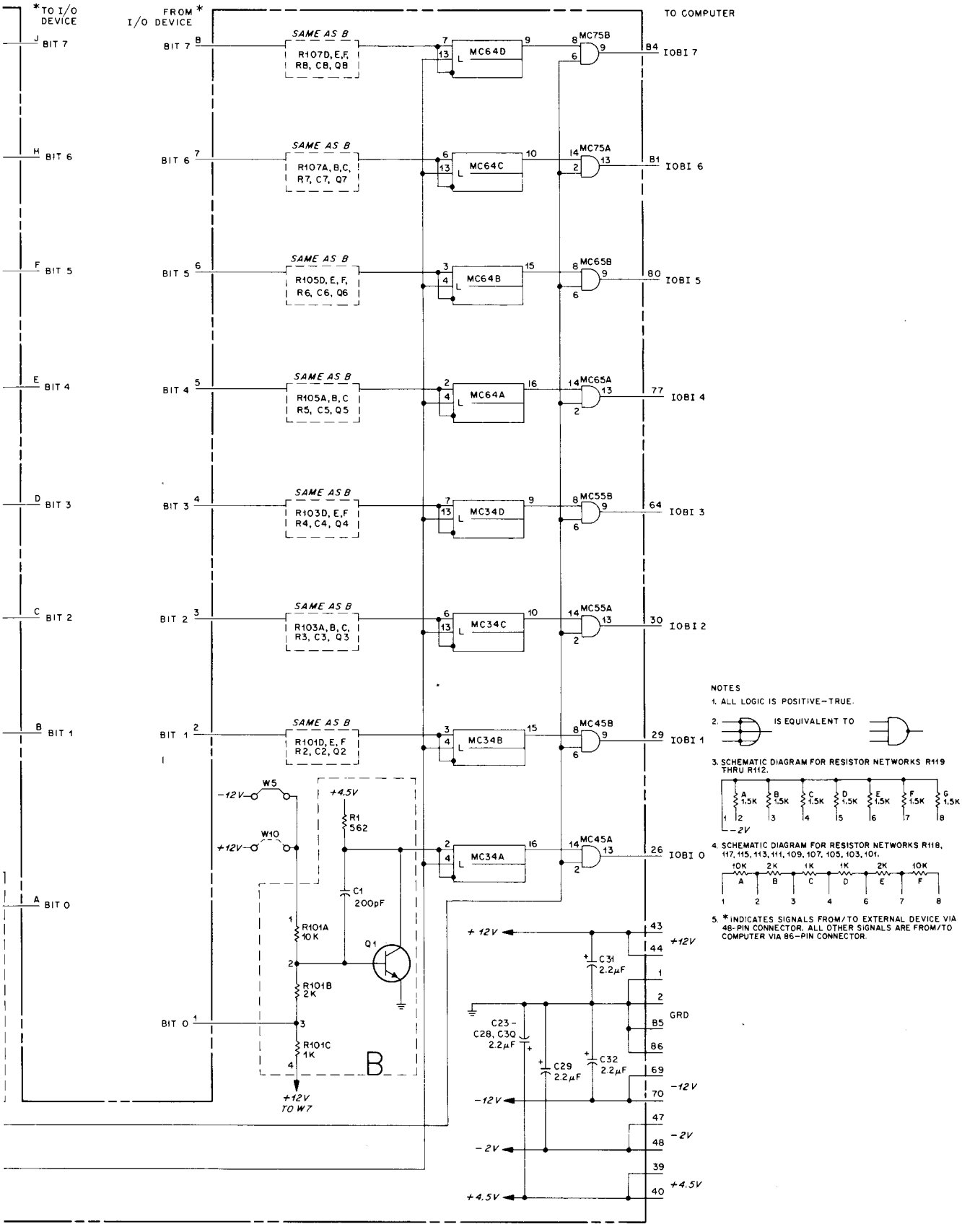


Figure 3-3. Positive-in/Positive-out Logic Diagram


T0 T1 T2 T3 T4 T5 T6 T7
IAK
ENF
STF
IOG
STC, CLC, CLF
SIR
IRQ FF
MC17B
MC17A
MC16A
MC16B
MC26A
MC26B
MC25D
MC25B
MC86B
MC86D
R21 464
R19 348
R20 196
R24 1K
R25 1K
R32 1K
R117 2K
R117 10K
R17 10K
MC16-1 1K
MC16-7 1K
MC26-1 1K
MC26-7 1K
C17 68pF
C22 .001
Q17
CR17
+4.5V
-2V
-2V TO W6
+12V TO W7
3 PRL
4 FLG
6 IRQ
19 SRQ
12 SKF
24 BB GND*
AA* DEVICE ENCODE
21* STATUS ENABLE
W9
W4
FROM COMPUTER
IOB07 52
IOB06 53
IOB05 51
IOB04 42
IOB03 45
IOB02 41
IOB01 38
IOB00 35
MC74D
MC74C
MC74B
MC74A
MC44D
MC44C
MC44B
MC44A
R120F 1.5K
R120G 1.5K
R120E 1.5K
R120D 1.5K
R120B 1.5K
R120A 1.5K
R119G 1.5K
R119F 1.5K
SAME AS A
R115A, B, C, R16, C16, CR16, Q16
R115D, E, F, R15, C15, CR15, Q15
R113A, B, C, R14, C14, CR14, Q14
R113D, E, F, R13, C13, CR13, Q13
R111A, B, C, R12, C12, CR12, Q12
R111D, E, F, R11, C11, CR11, Q11
R109A, B, C, R10, C10, CR10, Q10
+12V
-12V
-2V
W7
W12
W11
W6
C9 56 pF
R9 10K
R109F 10K
R109E 2K
R109D 1K
CR9
Q9
+4.5V
A

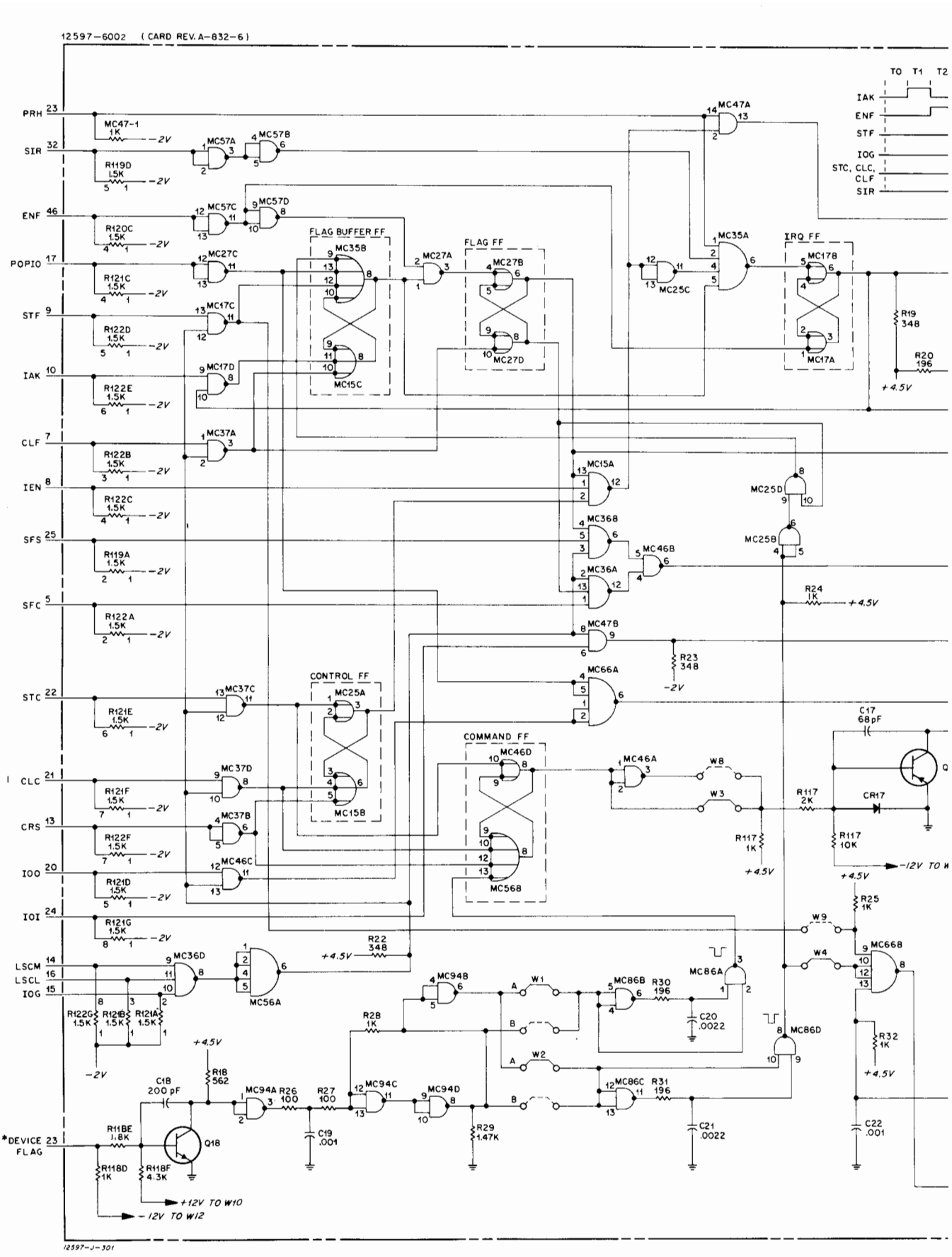


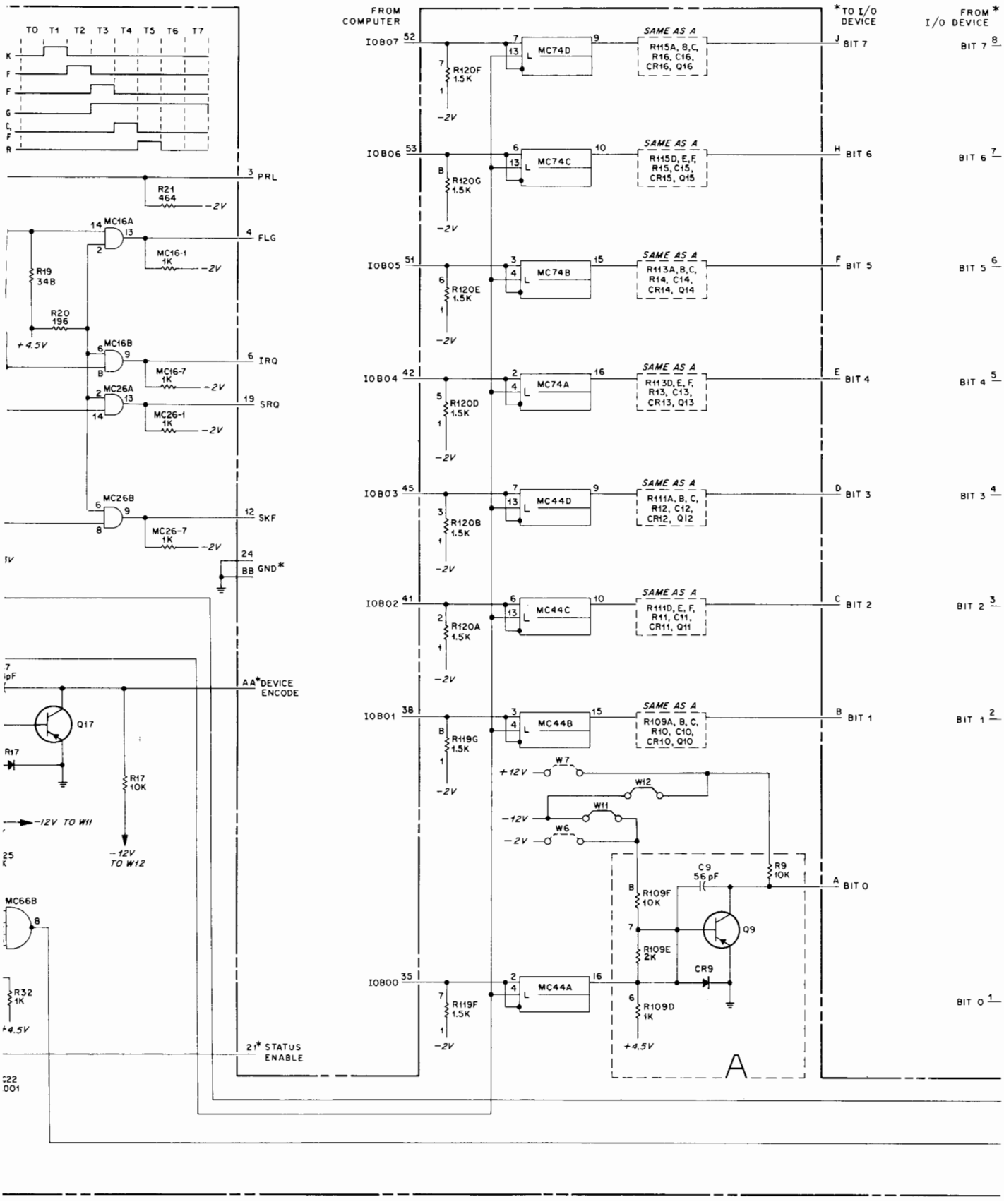
NOTES

1. ALL LOGIC IS POSITIVE-TRUE.
2. IS EQUIVALENT TO
3. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R119 THRU R112.

4. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R118, 117, 115, 113, 111, 109, 107, 105, 103, 101.

5. *INDICATES SIGNALS FROM/TO EXTERNAL DEVICE VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.


12597-6002 (CARD REV. A-832-6)
PRH 23
SIR 32
ENF 46
POPIO 17
STF 9
IAK 10
CLF 7
IEN 8
SFS 25
SFC 5
STC 22
CLC 21
CRS 13
IOO 20
IOI 24
LSCM 14
LSCL 16
IOG 15
*DEVICE FLAG 23
MC47-1 1K -2V
R119D 1.5K -2V
R120C 1.5K -2V
R121C 1.5K -2V
R122D 1.5K -2V
R122E 1.5K -2V
R122B 1.5K -2V
R122C 1.5K -2V
R119A 1.5K -2V
R122A 1.5K -2V
R121E 1.5K -2V
R121F 1.5K -2V
R122F 1.5K -2V
R121D 1.5K -2V
R121G 1.5K -2V
R122G 1.5K
R121B 1.5K
R121A 1.5K
-2V
MC57A
MC57B
MC57C
MC57D
MC27C
MC17C
MC17D
MC37A
MC37C
MC37D
MC37B
MC46C
MC36D
MC56A
FLAG BUFFER FF
MC35B
MC15C
MC27A
FLAG FF
MC27B
MC27D
CONTROL FF
MC25A
MC15B
COMMAND FF
MC46D
MC56B
MC47A
MC35A
MC25C
IRQ FF
MC17B
MC17A
R19 348
R20 196
+4.5V
MC15A
MC36B
MC46B
MC47B
MC66A
MC25D
MC25B
R24 1K
R23 348
-2V
C17 68pF
Q
CR17
R117 2K
R117 10K
R117 1K
+4.5V
-12V TO W
MC46A
W8
W3
R25 1K
W9
W4
MC66B
R32 1K
C22 .001
MC94B
MC94A
MC94C
MC94D
MC86A
MC86B
MC86C
MC86D
W1
W2
A
B
R28 1K
R30 196
R31 196
C20 .0022
C21 .0022
R18 562
C18 200 pF
R26 100
R27 100
C19 .001
R29 1.47K
R11BE 1.8K
R118D 1K
R118F 4.3K
Q18
+12V TO W10
-12V TO W12
TO T1 T2
IAK
ENF
STF
IOG
STC, CLC, CLF
SIR
12597-J-301


FROM COMPUTER
*TO I/O DEVICE
FROM * I/O DEVICE
T0 T1 T2 T3 T4 T5 T6 T7
3 PRL
R21 464 -2V
4 FLG
MC16A
MC16-1 1K -2V
R19 34B
R20 196
+4.5V
6 IRQ
MC16B
MC16-7 1K -2V
MC26A
19 SRQ
MC26-1 1K -2V
MC26B
12 SKF
MC26-7 1K -2V
24 BB GND*
AA* DEVICE ENCODE
Q17
R17
R17 10K
-12V TO W11
-12V TO W12
MC66B
R32 1K
+4.5V
21* STATUS ENABLE
IOB07 52
MC74D
R120F 1.5K
SAME AS A
R115A, B, C, R16, C16, CR16, Q16
J BIT 7
BIT 7 8
IOB06 53
MC74C
R120G 1.5K
R115D, E, F, R15, C15, CR15, Q15
H BIT 6
BIT 6 7
IOB05 51
MC74B
R120E 1.5K
R113A, B, C, R14, C14, CR14, Q14
F BIT 5
BIT 5 6
IOB04 42
MC74A
R120D 1.5K
R113D, E, F, R13, C13, CR13, Q13
E BIT 4
BIT 4 5
IOB03 45
MC44D
R120B 1.5K
R111A, B, C, R12, C12, CR12, Q12
D BIT 3
BIT 3 4
IOB02 41
MC44C
R120A 1.5K
R111D, E, F, R11, C11, CR11, Q11
C BIT 2
BIT 2 3
IOB01 38
MC44B
R119G 1.5K
R109A, B, C, R10, C10, CR10, Q10
B BIT 1
BIT 1 2
IOB00 35
MC44A
R119F 1.5K
BIT 0 1
+12V
-12V
-2V
W7
W12
W11
W6
C9 56 pF
R9 10K
R109F 10K
Q9
R109E 2K
CR9
R109D 1K
+4.5V
A BIT 0
A

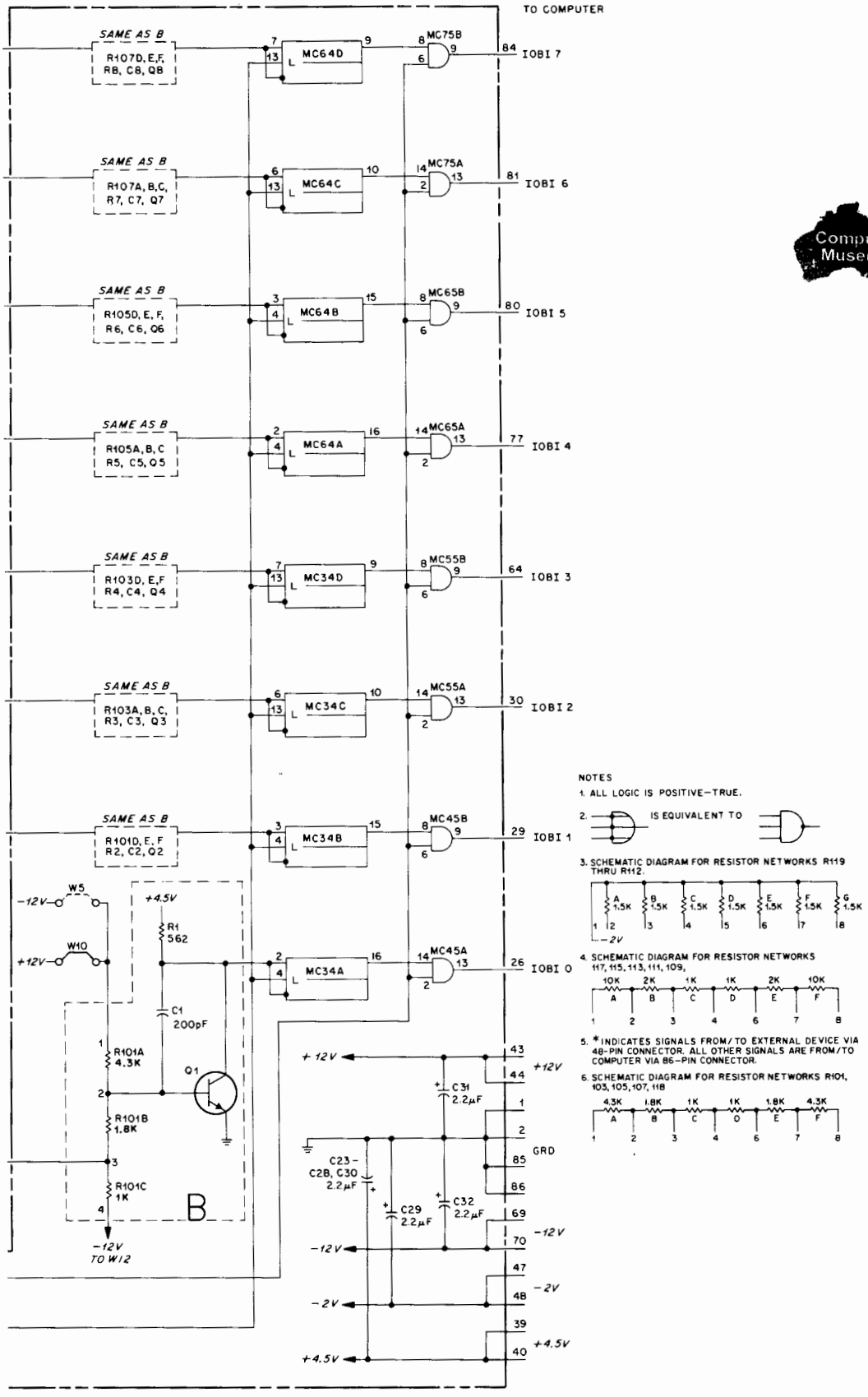


Figure 3-4. Negative-in/Negative-out Logic Diagram

SECTION IV
REPLACEABLE PARTS

4-1. INTRODUCTION.

4-2. This section contains information for ordering replacement parts for the 8-Bit Duplex Register Card. Refer to Table 4-1 for a list of replaceable parts in alphanumerical order of their reference designations, with a description and HP part number for each part. Table 4-2 lists parts alphanumerically by their HP part numbers.

4-3. ORDERING INFORMATION.

4-4. To order a replacement part, address the order or inquiry to your local Hewlett-Packard field office. See the list at the back of this manual for field office addresses.

4-5. Specify the following information for each part when ordering:

a. Hewlett-Packard part number

b. Circuit reference designation

c. Description

4-6. To order a part not listed in Tables 4-1 and 4-2, give a complete description of the part and include its function and location.

Table 4-1. Reference Designation Index

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION
C1-8,18	0140-0198	C:FXD MICA 200 PF 5%
C9-16	0140-0191	C:FXD MICA 56 PF 5%
C17	0140-0192	C:FXD MICA 68 PF 5%
C19,22	0160-0153	C:FXD MY 1000 PF 10% 200 VDCW
C20,21	0160-0154	C:FXD MYLAR 2200 PF 10%
C23-32	0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW
CR9-17	1901-0040	DIODE: SILICON 30 MA 30 WV
MC15,36	1820-0068	INTEGRATED CIRCUIT: TTL
MC16,26,47	1820-0956	INTEGRATED CIRCUIT: CTL
MC17,25,27,37,46,57,86,94	1820-0054	INTEGRATED CIRCUIT: TTL
MC34,44,64,74	1820-0301	INTEGRATED CIRCUIT: TTL
MC35	1820-0069	INTEGRATED CIRCUIT: TTL
MC45,55,65,75	1820-0974	INTEGRATED CIRCUIT: CTL
MC56,66	1820-0071	INTEGRATED CIRCUIT: TTL
Q1-18	1854-0215	TRANSISTOR: SILICON NPN 2N3904
*Q9-17	1853-0036	TRANSISTOR: SILICON PNP 2N3906
R1-8,18	0757-0417	R:FXD MET FLM 562 OHM 1% 1/8W
R9-17	0757-0442	R:FXD MET FLM 10.0K OHM 1% 1/8W
R19,22,23	0698-3445	R:FXD MET FLM 348 OHM 1% 1/8W
R20,30,31	0698-3440	R:FXD MET FLM 196 OHM 1% 1/8W
R21	0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W
R24,25,28,32	0757-0280	R:FXD MET FLM 1K OHM 1% 1/8W
R26-27	0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W
R29	0757-1094	R:FXD MET FLM 1.47K OHM 1% 1/8W
R101,103,105,107,109,111, 113,115,117,118	1810-0008	RESISTOR NETWORK: MET FLM (6 RES)
*R101,103,105,107,118	1810-0022	RESISTOR NETWORK: MET FLM (6 RES)
*R109,111,113,115,117	1810-0008	RESISTOR NETWORK: MET FLM (6 RES)
R119,120,121,122	1810-0020	RESISTOR NETWORK: MET FLM (7 RES)
W1-7	8159-0005	JUMPER WIRE

*12597-6002 8-Bit Duplex Register Board Only

Table 4-2. Replaceable Parts

HP PART NO.	DESCRIPTION	MFR.	MFR. PART NO.	TQ
0140-0191	C:FXD MICA 56 PF 5%	28480	0140-0191	8
0140-0192	C:FXD MICA 68 PF 5%	28480	0140-0192	1
0140-0198	C:FXD MICA 200 PF 5%	28480	0140-0198	9
0160-0153	C:FXD MY 1000 PF 10% 200VDCW	28480	0160-0153	2
0160-0154	C:FXD MYLAR 2200 PF 10%	28480	0160-0154	2
0180-0197	C:FXD ELECT 2.2 UF 10% 20VDCW	56289	150D225X9020A2	10
0698-0082	R:FXD MET FLM 464 OHM 1% 1/8W	28480	0698-0082	1
0698-3440	R:FXD MET FLM 196 OHM 1% 1/8W	28480	0698-3440	3
0698-3445	R:FXD MET FLM 348 OHM 1% 1/8W	28480	0698-3445	3
0757-0280	R:FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280	4
0757-0401	R:FXD MET FLM 100 OHM 1% 1/8W	28480	0757-0401	2
0757-0417	R:FXD MET FLM 562 OHM 1% 1/8W	28480	0757-0417	9
0757-0442	R:FXD MET FLM 10.0K OHM 1% 1/8W	28480	0757-0442	9
0757-1094	R:FXD MET FLM 1.47K OHM 1% 1/8W	28480	0757-1094	1
1810-0008	RESISTOR NETWORK: MET FLM (6 RES)	28480	1810-0008	*5,10
1810-0022	R:NETWORK MET FLM (6 RES)	28480	1810-0022	*5
1810-0020	RESISTOR NETWORK: MET FLM (7 RES)	28480	1810-0020	4
1820-0054	INTEGRATED CIRCUIT: TTL	28480	1820-0054	8
1820-0068	INTEGRATED CIRCUIT: TTL	28480	1820-0068	2
1820-0069	INTEGRATED CIRCUIT: TTL	28480	1820-0069	1
1820-0071	INTEGRATED CIRCUIT: TTL	28480	1820-0071	2
1820-0301	INTEGRATED CIRCUIT: TTL	28480	1820-0301	4
1820-0956	INTEGRATED CIRCUIT: CTL	28480	1820-0956	3
1820-0974	INTEGRATED CIRCUIT: CTL	28480	1820-0974	4
1853-0036	TRANSISTOR: SILICON PNP 2N3906	28480	1853-0036	*9
1854-0215	TRANSISTOR: SILICON NPN 2N3904	28480	1854-0215	*9,18
1901-0040	DIODE: SILICON 30 MA 30 WV	28480	1901-0040	9
8159-0005	JUMPER WIRE	28480	8159-0005	7
12597-6001	8-BIT DUPLEX REGISTER	04404	12597-6001	1
12597-6002	8-BIT DUPLEX REGISTER (-V)	04404	12597-6002	*1

*12597-6002 8-Bit Duplex Register Board Only

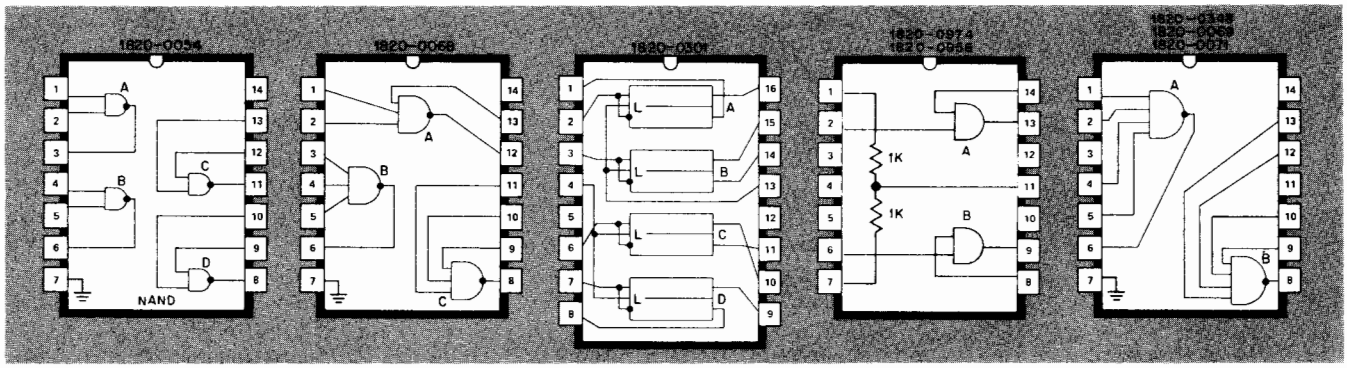


Figure 4-1. Microcircuit Packages, Top View

HEWLETT • PACKARD hp SALES AND SERVICE

UNITED STATES

ALABAMA
P.O. Box 4207
2003 Byrd Spring Road S.W.
Huntsville 35802
Tel: (205) 881-4591
TWX: 810-726-2204

ARIZONA
3009 North Scottsdale Road
Scottsdale 85251
Tel: (602) 945-7601
TWX: 910-950-1282

5737 East Broadway
Tucson 85716
Tel: (602) 298-2313
TWX: 910-952-1162

CALIFORNIA
1430 East Orangethorpe Ave.
Fullerton 92631
Tel: (714) 870-1000

3939 Lankershim Boulevard
North Hollywood 91604
Tel: (213) 877-1282
TWX: 910-499-2170

1101 Embarcadero Road
Palo Alto 94303
Tel: (415) 327-6500
TWX: 910-373-1280

2220 Watt Ave.
Sacramento 95825
Tel: (916) 482-1463
TWX: 910-367-2092

1055 Shafter Street
San Diego 92106
Tel: (714) 223-8103
TWX: 910-335-2000

COLORADO
7965 East Prentice
Englewood 80110
Tel: (303) 771-3455
TWX: 910-935-0705

CONNECTICUT
508 Tolland Street
East Hartford 06108
Tel: (203) 289-9394
TWX: 710-425-3416

111 East Avenue
Norwalk 06851
Tel: (203) 853-1251
TWX: 710-468-3750

DELAWARE
3941 Kennett Pike
Wilmington 19807
Tel: (302) 655-6161
TWX: 510-666-2214

FLORIDA
P.O. Box 24210
2806 W. Oakland Park Blvd.
Ft. Lauderdale 33307
Tel: (305) 731-2020
TWX: 510-955-4099

P.O. Box 20007
Herndon Station 32814
621 Commonwealth Avenue
Orlando
Tel: (305) 841-3970
TWX: 810-850-0113

P.O. Box 8128
Madeira Beach 33708
410 150th Avenue
St. Petersburg
Tel: (813) 391-0211
TWX: 810-863-0366

GEORGIA
P.O. Box 28234
450 Interstate North
Atlanta 30328
Tel: (404) 436-6181
TWX: 810-766-4890

ILLINOIS
5500 Howard Street
Skokie 60076
Tel: (312) 677-0400
TWX: 910-223-3613

INDIANA
3839 Meadows Drive
Indianapolis 46205
Tel: (317) 546-4891
TWX: 810-341-3263

LOUISIANA
P.O. Box 856
1942 Williams Boulevard
Kenner 70062
Tel: (504) 721-6201
TWX: 810-955-5524

MARYLAND
6707 Whitestone Road
Baltimore 21207
Tel: (301) 944-5400
TWX: 710-862-0850

P.O. Box 1648
2 Choke Cherry Road
Rockville 20850
Tel: (301) 948-6370
TWX: 710-828-9684

MASSACHUSETTS
32 Hartwell Ave.
Lexington 02173
Tel: (617) 861-8960
TWX: 710-326-6904

MICHIGAN
24315 Northwestern Highway
Southfield 48075
Tel: (313) 353-9100
TWX: 810-224-4882

MINNESOTA
2459 University Avenue
St. Paul 55114
Tel: (612) 645-9461
TWX: 910-563-3734

MISSOURI
11131 Colorado Ave.
Kansas City 64137
Tel: (816) 763-8000
TWX: 910-771-2087

2812 South Brentwood Blvd.
St. Louis 63144
Tel: (314) 962-5000
TWX: 910-760-1670

NEW JERSEY
W. 120 Century Road
Paramus 07652
Tel: (201) 265-5000
TWX: 710-990-4951

1060 N. Kings Highway
Cherry Hill 08034
Tel: (609) 667-4000
TWX: 710-892-4945

NEW MEXICO
P.O. Box 8366
Station C
6501 Lomas Boulevard N.E.
Albuquerque 87108
Tel: (505) 265-3713
TWX: 910-989-1665

156 Wyatt Drive
Las Cruces 88001
Tel: (505) 526-2485
TWX: 910-983-0550

NEW YORK
1702 Central Avenue
Albany 12205
Tel: (518) 869-8462
TWX: 710-441-8270

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HEWLETT hp PACKARD

DIAGNOSTIC TEST for 8-BIT DUPLEX REGISTER CARD

model 12597A Including Options 01, 02, and 03

MANUAL SUPPLEMENT 6 OCT 69

CONTENTS

NOTE

This diagnostic program tests only the 8-Bit Duplex Register Card and not interconnecting cables or external devices to which the card may be connected. References in this program to the 16-Bit Duplex Register Card also apply to the 8-Bit Duplex Register Card.

11000 Wolfe Road, Cupertino, California 95014, Area Code 408 257-7000, TWX 910-338-0221

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DIAGNOSTIC OPERATING PROCEDURE

1. INTRODUCTION.

2. PROGRAM DESCRIPTION.

3. The objective of this program is to check the 8-Bit Duplex Register Boards (HP 12597-6001 and HP 12597-6002).

4. The program consists of a background control program and three task routines. The background program obtains information via the Teletype and the Switch Register, and it controls message printout and directs task performance according to the information. The first task routine inserts the address of the Duplex Register into all Input/Output instructions. The second task routine checks the flag, control, and interrupt circuitry on the board. The third task routine checks the data buffers and associated discrete circuirty by outputting all possible combinations of 8 bits.

5. ENVIRONMENT.

6. Hardware requirements are as follows:

   a. HP Computer with 4K memory.

   b. Teleprinter (HP 2752A or HP 2754A) and associated interface register.

   c. 8-Bit Duplex Register Card (12597-6001 and 12597-6002) and a 24-pin connector to short all output pins to the adjacent input pins.

   d. An input device to enter the diagnostic into memory.

7. Software requirements are as follows:

   a. This diagnostic

   b. System Input/Output Teleprinter driver

8. DIAGNOSTIC TEST PROCEDURE

   a. Duplex Register

      (1) Short all output pins to the adjacent input pins with a 24-pin connector.

      (2) Place register (with connector) in an Input/Output slot such that every slot of higher priority has either another I/O board or a priority jumper board in it.

b. Teleprinter

(1) Put the Teleprinter Register in any I/O slot.

(2) Connect it to the Teleprinter.

c. Teleprinter Driver

(1) Read the SIO Teleprinter driver into memory.

(2) Put 000002 into the Switch Register.

(3) Push LOAD ADDRESS.

(4) Put the Teleprinter Register address into the Switch Register.

(5) Push RUN.

d. Duplex Register Diagnostic

(1) Read the diagnostic into memory.

(2) Put 000100 into the Switch Register.

(3) Push LOAD ADDRESS.

(4) Push RUN.

e. Program Operation

(1) The program will print: 16 BIT DUPLEX REGISTER DIAGNOSTIC

(2) The program will print: I/O CHANNEL?

(3) The operator must print (using Teleprinter keyboard) the address of the Duplex Register, followed by a line termination (RETURN, LINE FEED).

(4) The program will print: SET SW. REG. FOR DATA BITS TO BE TESTED.

(5) The program will halt with M and P REGS. = 203 and A, B, and T REGS. = 102002.

(6) The operator must set to "1" each bit of the Switch Register that corresponds to a bit on the Duplex Register which has both input and output circuits.

(7) Push RUN.

(8) The program will print: SET SW. REG. FOR DESIRED PROGRAM OPTIONS.

(9) The program will halt with M and P REGS. = 214 and A, B, and T REGS. = 102001.

(10) Use Table in Paragraph 10 to select operations to be performed. After setting Switch Register for program option, push RUN.

9. PROGRAM CONTROL.

10. From this point on, program control depends on the state of the Switch Register as follows:

BIT 4	3	2	1	0	
X	X	X	X	1	Throw this switch for an orderly halt. Program will halt, M and P REGS. = 122 A, B, and T REGS. = 102000, pushing run will enter at 2 of 8, e.
X	X	X	1	0	Program will go to 9 of 8, e.
X	X	1	0	0	Program will not print a message at the beginning and end of each test.
X	1	X	0	0	Program will perform BASIC TEST of flag, control, and interrupt circuitry.
1	X	X	0	0	Program will perform DATA BUFFER TEST.

11. ERROR CODES

a. An interrupt from any other I/O device will halt the program. The address of the interrupting device is the last six bits of the T-Register.

b. Basic Test Errors

CODE	MEANING
E01	SFS XX True after CLF XX instruction
E02	SFC XX False after CLF XX instruction
E03	SFS XX False after STF XX instruction
E04	SFC XX True after STF XX instruction
E05	SFS XX True after CLF XX instruction
E06	SFC XX False after CLF XX instruction
E07	SFS XX False after STC XX, C instruction
E10	SFC XX True after STC XX, C instruction
E11	Failure to interrupt after STF 0, STC XX, STF XX
E12	SFS XX False after interrupt test
E13	SFC XX True after interrupt test
E14	Program address = XXXXXX Illegal Interrupt from Duplex Reg.

c. Data Buffer Test Errors

(1) If the data which was output to the register does not equal the data read in from the register, the following code is printed:

OUTPUT = $XXXXXX_8$ INPUT = $XXXXXX_8$

(2) If the flag is not set within 12 μs after a STC XX,C instruction, the following is printed:

FLAG FAILURE IN DATA TEST.

(3) If any of the IOBI drivers is not working properly, the following is printed:

IOBI ERROR = $XXXXXX_8$.

Decoding the octal number to binary will show which drivers are bad.

8-BIT DUPLEX REGISTER

Binary Tape 20416C

Source Listing 20416CL

NOTE

This diagnostic listing is identical to the 16-Bit Duplex Register diagnostic listing.

```
0001                    ASMB,A,B,L
** NO ERRORS*
```

```
0001                    ASMB,A,R,L
0002*
0003*
0004*
0005*16 BIT DUPLEX REGISTER DIAGNOSTIC
0006*
0007*
0008*
0009*STARTING OCTAL ADDRESS = 100
0010*
0011*
0012*THE FOLLOWING SWITCH REGISTER SETTINGS
0013*ARE USED FOR PROGRAM CONTROL
0014*
0015******
0016*BIT 0 = 1   ->  HALT AT BEGINNING OF PROGRAM
0017*BIT 1 = 1   ->  HALT AT BEGINNING OF BASIC TEST
0018*BIT 2 = 1   ->  SUPPRESS SUPERFLUOUS MESSAGES
0019*BIT 3 = 1   ->  PERFORM BASIC TEST
0020*BIT 4 = 1   ->  PERFORM DATA BUFFER TEST
0021******
0022*
0023*
0024*MAIN PROGRAM
0025*
0026*
0027  00100                 ORG 100B
0028  00100 024110          JMP 110B
0029  00105                 ORG 105B
0030  00105 001337          DEF X           FIRST AVAIL MEMORY
0031  00110                 ORG 110B
0032  00110 107700          CLC 0,C       INTERRUPT OFF
0033  00111 014456          JSB EOL       LINE FEED
0034  00112 060311          LDA ML1       PRINT
0035  00113 064267          LDB MAD1        FIRST
0036  00114 114102          JSB 102B,I        MESSAGE
0037  00115 014456          JSB EOL       LINE FEED
0038  00116 024122          JMP *+4
0039  00117 060121  P1      LDA *+2       HALT AT
0040  00120 064121          LDB *+1         BEGINNING
0041  00121 102000          HLT 0             OF PROGRAM
0042  00122 064452          LDB M67       PREPARE
0043  00123 060457          LDA HIS         TRAP
0044  00124 070126          STA *+2           FOR
0045  00125 060450          LDA HI              ILLEGAL
0046  00126 070010          STA 10B               INTERRUPT
0047  00127 034126          ISZ *-1                 FROM
0048  00130 002004          INA                       ANY
0049  00131 006006          INB,SZB                     DEVICE
0050  00132 024126          JMP *-4
0051  00133 014456  P2      JSB EOL       LINE FEED
0052  00134 060321          LDA ML2       PRINT
0053  00135 064312          LDB MAD2        SECOND
0054  00136 114102          JSB 102B,I        MESSAGE
0055  00137 014466          JSB EOL       LINE FEED
0056  00140 060456          LDA RL1       RECEIVE
0057  00141 064454          LDB PAD1        FIRST
```

```
0058  00142 114104          JSB 104B,I       REPLY
0059  00143 060455          LDA REP1       CHECK FIRST CHARACTER
0060  00144 010453          AND MSK1         FOR VALIDITY
0061  00145 050465          CPA C1         VALID?
0062  00146 024150          JMP *+2        YES.
0063  00147 024133          JMP P2         NO.
0064  00150 060455          LDA REP1       CHECK SECOND
0065  00151 001727          ALF,ALF          CHARACTER
0066  00152 010463          AND MSK1           FOR VALIDITY
0067  00153 050465          CPA C1         VALID?
0068  00154 024156          JMP *+2        YES.
0069  00155 024133          JMP P2         NO.
0070  00156 002400          CLA            GENERATE
0071  00157 060455          LDA REP1         DUPLEX
0072  00160 010454          AND MSK2           REGISTER
0073  00161 070522          STA ADDR             ADDRESS
0074  00162 060455          LDA REP1
0075  00163 001727          ALF,ALF
0076  00164 010454          AND MSK2
0077  00165 001721          ALF,ARS
0078  00166 030522          IOR ADDR
0079  00167 070522          STA ADDR       ADDRESS COMPLETE
0080  00170 014533          JSB ADIN
0081  00171 060451          LDA IBAD       ILLEGAL INTERRUPT
0082  00172 070000  STA1    STA 0            TRAP
0083  00173 014456          JSB EOL
0084  00174 060347          LDA ML3        PRINT
0085  00175 064322          LDB MAD3         THIRD
0086  00176 114102          JSB 102B,I         MESSAGE
0087  00177 014456          JSB EOL
0088  00200 060202          LDA *+2        HALT
0089  00201 064202          LDB *+1          TO SET
0090  00202 102002          HLT 2              SW. REG.
0091  00203 102501          LIA 1          LOAD MASK FOR
0092  00204 071257          STA DAMSK        DATA TESTING
0093  00205 060375          LDA ML4        SET SW. REG.
0094  00206 064350          LDB MAD4         FOR DESIRED
0095  00207 114102          JSB 102B,I         PROGRAM OPTIONS
0096  00210 014456          JSB EOL
0097  00211 060213  P3      LDA *+2        HALT AT
0098  00212 064213          LDB *+1          BEGINNING
0099  00213 102001          HLT 1              OF BASIC TEST
0100  00214 014531  P4      JSB MODE       CHECK SW. REG.
0101  00215 060531          LDA BIT3       PERFORM
0102  00216 002011          SLA,RSS          BASIC TEST?
0103  00217 024241          JMP P5         NO.
0104  00220 060530          LDA BIT2       YES.  SUPPRESS
0105  00221 000010          SLA              MESSAGES?
0106  00222 024230          JMP *+6        YES.
0107  00223 014456          JSB EOL        NO.
0108  00224 060407          LDA ML5        PRINT FIRST
0109  00225 064376          LDB MAD5         BASIC TEST
0110  00226 114102          JSB 102B,I         MESSAGE
0111  00227 014466          JSB EOL
0112  00230 014523          JSB BAT        PERFORM BASIC TEST
0113  00231 060530          LDA BIT2       SUPPRESS
0114  00232 000010          SLA              MESSAGES?
```

```
0115  00233 024241          JMP *+6       YES.
0116  00234 014456          JSB EOL       NO.
0117  00235 060421          LDA ML6       PRINT SECOND
0118  00236 064410          LDB MAD6        BASIC TEST
0119  00237 114102          JSB 1028,I        MESSAGE
0120  00240 014456          JSB EOL
0121  00241 014501  P5      JSB MODE      CHECK SW. REG.
0122  00242 060532          LDA BIT4      PERFORM DATA
0123  00243 002011          SLA,RSS         BUFFER TEST?
0124  00244 024214          JMP P4        NO.
0125  00245 060530          LDA BIT2      YES.  SUPPRESS
0126  00246 000010          SLA             MESSAGES?
0127  00247 024255          JMP *+6       YES.
0128  00250 014456          JSB EOL       NO.
0129  00251 060436          LDA ML7       PRINT FIRST
0130  00252 064422          LDB MAD7        DATA TEST
0131  00253 114102          JSB 1028,I        MESSAGE
0132  00254 014466          JSB EOL
0133  00255 015120          JSB DAT       PERFORM DATA BUFFER TEST
0134  00256 060530          LDA BIT2      SUPPRESS
0135  00257 000010          SLA             MESSAGES?
0136  00260 024214          JMP P4        YES.
0137  00261 014456          JSB EOL       NO.
0138  00262 060453          LDA ML8       PRINT SECOND
0139  00263 064437          LDB MAD8        DATA TEST
0140  00264 114102          JSB 1028,I        MESSAGE
0141  00265 014466          JSB EOL
0142  00266 024214          JMP P4
0143*
0144*
0145  00267 000270  MAD1    DEF *+1
0146  00270 030466  MES1    ASC 17,16 BIT DUPLEX REGISTER DIAGNOSTIC
      00271 020102
      00272 044524
      00273 020104
      00274 052520
      00275 046105
      00276 054040
      00277 051105
      00300 043511
      00301 051524
      00302 042522
      00303 020104
      00304 044501
      00305 043516
      00306 047523
      00307 052111
      00310 041440
0147  00311 000042  ML1     DEC 34
0148*
0149  00312 000313  MAD2    DEF *+1
0150  00313 044457  MES2    ASC 6,I/O CHANNEL?
      00314 047440
      00315 041510
      00316 040516
      00317 047105
      00320 046077
```

```
0151   00321 000014   ML2    DEC 12
0152*
0153   00322 000323   MAD3   DEF *+1
0154   00323 051505   MES3   ASC 20,SET SW. REG. FOR DATA BITS TO BE TESTED
       00324 052040
       00325 051527
       00326 027040
       00327 051105
       00330 043456
       00331 020106
       00332 047522
       00333 020104
       00334 040524
       00335 040440
       00336 041111
       00337 052123
       00340 020124
       00341 047440
       00342 041105
       00343 020124
       00344 042523
       00345 052105
       00346 042040
0155   00347 000050   ML3    DEC 40
0156*
0157   00350 000351   MAD4   DEF *+1
0158   00351 051505   MES4   ASC 20,SET SW. REG. FOR DESIRED PROGRAM OPTION
       00352 052040
       00353 051527
       00354 027040
       00355 051105
       00356 043456
       00357 020106
       00360 047522
       00361 020104
       00362 042523
       00363 044522
       00364 042504
       00365 020120
       00366 051117
       00367 043522
       00370 040515
       00371 020117
       00372 050124
       00373 044517
       00374 047123
0159   00375 000050   ML4    DEC 40
0160*
0161   00376 000377   MAD5   DEF *+1
0162   00377 041105   MES5   ASC 8,BEGIN BASIC TEST
       00400 043511
       00401 047040
       00402 041101
       00403 051511
       00404 041440
       00405 052105
       00406 051524
```

```
0153   00407 000020   ML5    DEC 16
0154*
0155   00410 000411   MAD6   DEF *+1
0156   00411 042516   MES6   ASC 8,END    BASIC TEST
       00412 042040
       00413 020040
       00414 041101
       00415 051511
       00416 041440
       00417 052105
       00420 051524
0157   00421 000020   ML6    DEC 16
0158*
0159   00422 000423   MAD7   DEF *+1
0160   00423 041105   MES7   ASC 11,BEGIN DATA BUFFER TEST
       00424 043511
       00425 047040
       00426 042101
       00427 052101
       00430 020102
       00431 052506
       00432 043105
       00433 051040
       00434 052105
       00435 051524
0161   00436 000026   ML7    DEC 22
0162*
0163   00437 000440   MAD8   DEF *+1
0164   00440 042516   MES8   ASC 11,END    DATA BUFFER TEST
       00441 042040
       00442 020040
       00443 042101
       00444 052101
       00445 020102
       00446 052506
       00447 043105
       00450 051040
       00451 052105
       00452 051524
0165   00453 000026   ML8    DEC 22
0166*
0167   00454 000455   RAD1   DEF *+1
0168   00455 000000   REP1   OCT 0
0169   00456 000002   RL1    OCT 2
0170*
0171   00457 070010   HIS    STA 10B
0172   00460 102010   HI     HLT 10B
0173   00461 015045   IBAD   JSB ILINT
0174   00462 177711   M67    OCT 177711
0175   00463 000170   MSK1   OCT 170
0176   00464 000007   MSK2   OCT 7
0177   00465 000060   C1     OCT 60
0178*
0179*LINE FEED, CARRIAGE RETURN
0180*
0181   00466 000000   EOL    NOP           ENTER SUBROUTINE
0182   00467 070477          STA AS1       STORE
```

```
0193  00470 074500          STB BS1         A & B
0194  00471 002400          CLA           LINE
0195  00472 006400          CLB             FEED
0196  00473 114102          JSB 102B,I
0197  00474 060477          LDA AS1       RESTORE
0198  00475 064500          LDB BS1         A & B
0199  00476 124466          JMP EOL,I     EXIT SUBROUTINE
0200  00477 000000  AS1     OCT 0
0201  00500 000000  BS1     OCT 0
0202*
0203*MODE SUBROUTINE
0204*
0205  00501 000000  MODE    NOP           ENTER SUBROUTINE
0206  00502 070525          STA AS2       STORE A
0207  00503 102501          LIA 1         EACH BIT
0208  00504 070526          STA BIT0       FROM THE
0209  00505 001300          RAR              SWITCH REGISTER
0210  00506 070527          STA BIT1          IS ROTATED
0211  00507 001300          RAR                INTO THE
0212  00510 070530          STA BIT2            LEAST SIGNIFICANT
0213  00511 001300          RAR                  POSITION AND
0214  00512 070531          STA BIT3               STORED IN THE
0215  00513 001300          RAR                      STORAGE LOCATION
0216  00514 070532          STA BIT4                   BEARING ITS NAME
0217  00515 060526          LDA BIT0      HALT AT
0218  00516 000010          SLA             BEGINNING OF PROGRAM?
0219  00517 024117          JMP P1        YES.
0220  00520 060527          LDA BIT1      NO.  HALT AT
0221  00521 000010          SLA             BEGINNING OF BASIC TEST?
0222  00522 024211          JMP P3        YES.
0223  00523 060525          LDA AS2       NO.  RESTORE A
0224  00524 124501          JMP MODE,I    EXIT SUBROUTINE
0225  00525 000000  AS2     OCT 0
0226  00526 000000  BIT0    OCT 0
0227  00527 000000  BIT1    OCT 0
0228  00530 000000  BIT2    OCT 0
0229  00531 000000  BIT3    OCT 0
0230  00532 000000  BIT4    OCT 0
0231*
0232*
0233*ADDRESS INCLUSION ROUTINE
0234*
0235*
0236  00533 000000  ADIN    NOP           ENTER ROUTINE
0237  00534 107700          CLC 0,C       INTERRUPT SYSTEM OFF
0238  00535 014515          JSB INCLU     PUT DUPLEX REG. ADDR.
0239  00536 070000          STA 0           INTO STA INSTRUCTIONS
0240  00537 070172          STA STA1
0241  00540 070723          STA STA2
0242  00541 070732          STA STA3
0243  00542 014515          JSB INCLU     SAME FOR STC XX,C
0244  00543 103700          STC 0,C
0245  00544 070525          STA STCC1
0246  00545 070732          STA STCC2
0247  00546 071174          STA STCC3
0248  00547 014515          JSB INCLU     SAME FOR SFS XX
0249  00550 102300          SFS 0
```

```
0250  00551 070552          STA SFS1
0251  00552 070552          STA SFS2
0252  00553 070572          STA SFS3
0253  00554 070706          STA SFS4
0254  00555 070733          STA SFS5
0255  00556 071200          STA SFS6
0256  00557 014515          JSB INCLU     SAME FOR SFC XX
0257  00560 102200          SFC 0
0258  00561 070556          STA SFC1
0259  00562 070565          STA SFC2
0260  00563 070576          STA SFC3
0261  00564 070711          STA SFC4
0262  00565 070736          STA SFC5
0263  00566 014515          JSB INCLU     SAME FOR CLF XX
0264  00567 103100          CLF 0
0265  00570 070532          STA CLF1
0266  00571 070571          STA CLF2
0267  00572 014515          JSB INCLU     SAME FOR STF XX
0268  00573 102100          STF 0
0269  00574 070561          STA STF1
0270  00575 070716          STA STF2
0271  00576 071122          STA STF3
0272  00577 014515          JSB INCLU     SAME FOR CLC XX
0273  00600 106700          CLC 0
0274  00601 070715          STA CLC1
0275  00602 071154          STA CLC2
0276  00603 014515          JSB INCLU     SAME FOR STC XX
0277  00604 102700          STC 0
0278  00605 070724          STA STC1
0279  00606 014515          JSB INCLU     SAME FOR OTA XX
0280  00607 102500          OTA 0
0281  00610 071152          STA OTA1
0282  00611 014515          JSB INCLU     SAME FOR LIB XX
0283  00612 106500          LIB 0
0284  00613 071202          STA LIB1
0285  00614 124533          JMP ADIN,I    EXIT ROUTINE
0286*
0287*INCLUSION SUBROUTINE
0288*
0289  00615 000000  INCLU NOP             ENTER SUBROUTINE
0290  00616 160615        LDA INCLU,I     PUT ADDRESS
0291  00617 030622        IOR ADDR          INTO INSTRUCTION
0292  00620 034515        ISZ INCLU       EXIT
0293  00621 124615        JMP INCLU,I       SUBROUTINE
0294  00622 000000  ADDR  OCT 0           ADDRESS STORAGE
0295*
0296*
0297*BASIC TEST ROUTINE
0298*
0299*
0300  00623 000000  BAT   NOP             ENTER ROUTINE
0301  00624 107700        CLC 0,C
0302  00625 103700  STCC1 STC 0,C
0303  00626 061004        LDA C2
0304  00627 002006        INA,SZA
0305  00630 024527        JMP *-1
0306  00631 107700        CLC 0,C
```

```
0307  00632 103100  CLF1   CLF 0
0308  00633 102100         STF 0          INTERRUPT SYSTEM ON
0309  00634 006400         CLB            INITIALIZE
0310  00635 074767         STB E1           ERROR
0311  00636 074770         STB E2             BUFFER
0312  00637 074771         STB E3
0313  00640 074772         STB E4
0314  00641 074773         STB E5
0315  00642 074774         STB E6
0316  00643 074775         STB E7
0317  00644 074776         STB E10
0318  00645 074777         STB E11
0319  00646 075200         STB E12
0320  00647 075201         STB E13
0321  00650 075203         STB E14
0322  00651 006004         INB
0323  00652 102300  SFS1   SFS 0          FLAG SET?
0324  00653 024655         JMP *+2        NO.
0325  00654 074767         STB E1         YES.  ERROR 1
0326  00655 006004         INB            INCREMENT ERROR CODE
0327  00656 102200  SFC1   SFC 0          FLAG CLEAR?
0328  00657 074770         STB E2         NO.  ERROR 2
0329  00660 006004         INB            YES.
0330  00661 102100  STF1   STF 0          SET FLAG
0331  00662 102300  SFS2   SFS 0          FLAG SET?
0332  00663 074771         STB E3         NO.  ERROR 3
0333  00664 006004         INB            YES.
0334  00665 102200  SFC2   SFC 0          FLAG CLEAR?
0335  00666 024670         JMP *+2        NO.
0336  00667 074772         STB E4         YES.  ERROR 4
0337  00670 006004         INB
0338  00671 103100  CLF2   CLF 0          CLEAR FLAG
0339  00672 102300  SFS3   SFS 0          FLAG SET?
0340  00673 024675         JMP *+2        NO.
0341  00674 074773         STB E5         YES.  ERROR 5
0342  00675 006004         INB
0343  00676 102200  SFC3   SFC 0          FLAG CLEAR?
0344  00677 074774         STB E6         NO.  ERROR 6
0345  00700 006004         INB            YES.
0346  00701 107700         CLC 0,C        INTERRUPT SYSTEM OFF
0347  00702 103700  STCC2  STC 0,C        ENCODE
0348  00703 061004         LDA C2         WAIT
0349  00704 002006         INA,SZA          FOR
0350  00705 024704         JMP *-1            FLAG
0351  00706 102300  SFS4   SFS 0          FLAG SET?
0352  00707 074775         STB E7         NO.  ERROR 7
0353  00710 006004         INB            YES.
0354  00711 102200  SFC4   SFC 0          FLAG CLEAR?
0355  00712 024714         JMP *+2        NO.
0356  00713 074776         STB E10        YES.  ERROR 10
0357  00714 006004         INB
0358  00715 106700  CLC1   CLC 0          CLEAR CONTROL
0359  00716 102100  STF2   STF 0          SET FLAG
0360  00717 102100         STF 0          INTERRUPT SYSTEM ON
0361  00720 000000         NOP
0362  00721 000000         NOP
0363  00722 061005         LDA IOK
```

```
0364   00723 070000  STA2  STA 0
0365   00724 102700  STC1  STC 0          TEST
0366   00725 000000        NOP              INTERRUPT
0367   00726 000000        NOP                CIRCUITRY
0368   00727 074777        STB E11          ERROR 11 - FAILURE TO INTERRUPT
0369   00730 005004  P6    INB
0370   00731 060461        LDA IBAD
0371   00732 070000  STA3  STA 0
0372   00733 102300  SFS5  SFS 0            FLAG SET?
0373   00734 075000        STB E12          NO.  ERROR 12
0374   00735 006004        INB              YES.
0375   00736 102200  SFC5  SFC 0            FLAG CLEAR?
0376   00737 024741        JMP *+2          NO.
0377   00740 075001        STB E13          YES.  ERROR 13
0378   00741 005004        INB
0379   00742 103700        CLC 0,C          INTERRUPT SYSTEM OFF
0380   00743 060756        LDA ERBUF        CHECK ERROR BUFFER
0381   00744 164000  P7    LDB 0,I
0382   00745 006003        SZB,RSS          ERROR?
0383   00746 024755        JMP *+7          NO.
0384   00747 006007        INB,SZB,RSS      END OF ERROR BUFFER?
0385   00750 024757        JMP *+7          YES.
0386   00751 164000        LDB 0,I          NO.
0387   00752 071255        STA AS5          PRINT
0388   00753 015006        JSB ERR            OUT
0389   00754 061255        LDA AS5              ERROR
0390   00755 002004        INA                    CODE
0391   00756 024744        JMP P7
0392   00757 061003        LDA E14          INTERRUPT
0393   00760 002003        SZA,RSS            ERROR?
0394   00761 024765        JMP *+4          NO.
0395   00762 051117        LDA ML10         PRINT
0396   00763 065076        LDB MAD10          OUT
0397   00764 114102        JSB 102B,I           MESSAGE
0398   00765 124523        JMP BAT,I        EXIT ROUTINE
0399*
0400   00766 000767  ERBUF DEF *+1          ERROR BUFFER
0401   00767 000000  E1    OCT 0            SFS  TRUE AFTER CLF
0402   00770 000000  E2    OCT 0            SFC FALSE AFTER CLF
0403   00771 000000  E3    OCT 0            SFS FALSE AFTER STF
0404   00772 000000  E4    OCT 0            SFC  TRUE AFTER STF
0405   00773 000000  E5    OCT 0            SFS  TRUE AFTER CLF
0406   00774 000000  E6    OCT 0            SFC FALSE AFTER CLF
0407   00775 000000  E7    OCT 0            SFS FALSE AFTER STC   ,C
0408   00776 000000  E10   OCT 0            SFC  TRUE AFTER STC   ,C
0409   00777 000000  E11   OCT 0            FAILURE TO INTERRUPT
0410   01000 000000  E12   OCT 0            SFS FALSE AFTER INTERRUPT TEST
0411   01001 000000  E13   OCT 0            SFC  TRUE AFTER INTERRUPT TEST
0412   01002 177777        OCT 177777       ERROR BUFFER TERMINATION
0413   01003 000000  E14   OCT 0            ILLEGAL INTERRUPT
0414*
0415   01004 177774  C2    OCT 177774
0416   01005 024730  IOK   JMP P6
0417*
0418*BASIC TEST ERROR PRINTOUT SUBROUTINE
0419*
0420   01006 000000  ERR   NOP              ENTER SUBROUTINE
```

```
0421  01007 075020          STB BS2       STORE B
0422  01010 060001          LDA 1
0423  01011 015025          JSB .2NUM     PACK 2 NUMBERS
0424  01012 075023          STB MES9+1    PRINT
0425  01013 061024          LDA ML9         OUT
0426  01014 065021          LDB MAD9          ERROR
0427  01015 114102          JSB 102B,I          MESSAGE
0428  01016 065020          LDB BS2       RESTORE B
0429  01017 125006          JMP ERR,I     EXIT SUBROUTINE
0430  01020 000000  BS2     OCT 0
0431  01021 001022  MAD9    DEF *+1
0432  01022 042440  MES9    ASC 1,E
0433  01023 000000          OCT 0
0434  01024 000004  ML9     DEC 4
0435*
0436*PACK TWO ASCII NUMBERS SUBROUTINE
0437*
0438  01025 000000  .2NUM   NOP           ENTER SUBROUTINE
0439  01026 071044          STA AS3       STORE A
0440  01027 001323          RAR,RAR       FORMAT
0441  01030 001300          RAR             FIRST
0442  01031 010464          AND MSK2          NUMBER
0443  01032 030465          IOR C1
0444  01033 001727          ALF,ALF
0445  01034 070001          STA 1         STORE IT
0446  01035 061044          LDA AS3       FORMAT
0447  01036 010454          AND MSK2        SECOND
0448  01037 030465          IOR C1            NUMBER
0449  01040 030001          IOR 1         PACK THEM
0450  01041 070001          STA 1           INTO B
0451  01042 061044          LDA AS3       RESTORE A
0452  01043 125025          JMP .2NUM,I   EXIT SUBROUTINE
0453  01044 000000  AS3     OCT 0
0454*
0455*ILLEGAL DUPLEX REGISTER INTERRUPT SUBROUTINE
0456*
0457  01045 000000  ILINT   NOP           ENTER SUBROUTINE
0458  01046 071073          STA AS4       STORE
0459  01047 075074          STB BS3         A & B
0460  01050 061045          LDA ILINT     PACK
0461  01051 001700          ALF             FIRST
0462  01052 011775          AND MSK3          TWO
0463  01053 015025          JSB .2NUM           NUMBERS
0464  01054 075114          STB IA        STORE THEM
0465  01055 061045          LDA ILINT     PACK
0466  01056 001727          ALF,ALF         SECOND
0467  01057 001222          RAL,RAL           TWO
0468  01060 015025          JSB .2NUM      NUMBERS
0469  01061 075115          STB IA+1       STORE THEM
0470  01062 001700          ALF           PACK
0471  01063 001222          RAL,RAL         LAST TWO
0472  01064 015025          JSB .2NUM         NUMBERS
0473  01065 075116          STB IA+2      STORE THEM
0474  01066 002404          CLA,INA
0475  01067 071003          STA E14
0476  01070 061073          LDA AS4       RESTORE
0477  01071 065074          LDB BS3         A & B
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0478  01072 125745          JMP ILINT,I  EXIT SUBROUTINE
0479  01073 000000  AS4     OCT 0
0480  01074 000000  BS3     OCT 0
0481  01075 000017  MSK3    OCT 17
0482  01076 001077  MAD10   DEF *+1
0483  01077 042440  MES10   ASC 13,E 14   PROGRAM ADDRESS =
      01100 030464
      01101 020040
      01102 020120
      01103 051117
      01104 043522
      01105 040515
      01106 020101
      01107 042104
      01110 051105
      01111 051523
      01112 020075
      01113 020040
0484  01114 000000  IA      OCT 0,0,0
      01115 000000
      01116 000000
0485  01117 000040  ML10    DEC 32
0486*
0487*
0488*DATA BUFFER TEST ROUTINE
0489*
0490*
0491  01120 000000  DAT     NOP          ENTER ROUTINE
0492  01121 107700          CLC 0,C      INTERRUPT SYSTEM OFF
0493  01122 102100  STF3    STF 0
0494  01123 002400          CLA
0495  01124 015160  P8      JSB DOIC     OUTPUT A CHARACTER
0496  01125 003000          CMA          OUTPUT ITS
0497  01126 015160          JSB DOIC       COMPLEMENT
0498  01127 003000          CMA          OUTPUT THE
0499  01130 015160          JSB DOIC       CHARACTER AGAIN
0500  01131 002006          INA,SZA      INCREMENT CHARACTER.     = 0?
0501  01132 025124          JMP P8       NO.
0502  01133 102500          LIA 0        YES.  CHECK IOBI DRIVERS
0503  01134 002003          SZA,RSS      ANY ERRORS?
0504  01135 125120          JMP DAT,I    NO.  EXIT ROUTINE
0505  01136 071256          STA AS6      YES.
0506  01137 015025          JSB .2NUM    PACK
0507  01140 075335          STB MES13+9    A REG.
0508  01141 051256          LDA AS6          AND
0509  01142 001700          ALF                STORE
0510  01143 071256          STA AS6              IT IN THE
0511  01144 011775          AND MSK3               ERROR
0512  01145 015025          JSB .2NUM                MESSAGE
0513  01146 075333          STB MES13+7
0514  01147 061256          LDA AS6
0515  01150 001700          ALF
0516  01151 001222          RAL,RAL
0517  01152 015025          JSB .2NUM
0518  01153 075334          STB MES13+8
0519  01154 061336          LDA ML13     OUTPUT
0520  01155 065323          LDB MAD13      ERROR
```

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0521  01156 114102          JSB 1028,I        MESSAGE
0522  01157 125120          JMP DAT,I     EXIT ROUTINE
0523*
0524*DATA OUT, IN, AND COMPARE SUBROUTINE
0525*
0526  01160 000000  DOIC    NOP           ENTER SUBROUTINE
0527  01161 071255          STA AS5       STORE A
0528  01162 102600  OTA1    OTA 0         OUTPUT A
0529  01163 025170          JMP *+5
0530  01164 106700  CLC2    CLC 0
0531  01165 061276          LDA ML11      LOSS
0532  01166 065260          LDB MAD11       OF FLAG
0533  01167 114102          JSB 1028,I        MESSAGE
0534  01170 014501          JSB MODE      CHECK SW. REG.
0535  01171 060532          LDA BIT4      EXIT DAT
0536  01172 002011          SLA,RSS         ROUTINE?
0537  01173 125120          JMP DAT,I     YES.
0538  01174 103700  STCC3   STC 0,C       NO.  ENCODE
0539  01175 061004          LDA C2        WAIT
0540  01176 002006          INA,SZA         FOR
0541  01177 025176          JMP *-1           FLAG
0542  01200 102300  SFS6    SFS 0         FLAG SET?
0543  01201 025164          JMP CLC2      NO.  REPEAT ENCODING
0544  01202 106500  LIB1    LIB 0         YES.  READ DATA
0545  01203 060001          LDA 1         MASK OFF
0546  01204 011257          AND DAMSK       UNWANTED BITS
0547  01205 070001          STA 1
0548  01206 061255          LDA AS5       MASK OFF
0549  01207 011257          AND DAMSK       UNWANTED BITS
0550  01210 050001          CPA 1         OUTPUT = INPUT ?
0551  01211 025252          JMP P9        YES.
0552  01212 075254          STB BS4       NO.
0553  01213 071256          STA AS6
0554  01214 001700          ALF           PACK
0555  01215 011075          AND MSK3        OUTPUT
0556  01216 015025          JSB .2NUM         WORD
0557  01217 075305          STB MES12+5         AND
0558  01220 061256          LDA AS6               STORE
0559  01221 001727          ALF,ALF                 IT IN THE
0560  01222 001222          RAL,RAL                   ERROR
0561  01223 015025          JSB .2NUM                   MESSAGE
0562  01224 075306          STB MES12+6
0563  01225 001700          ALF
0564  01226 001222          RAL,RAL
0565  01227 015025          JSB .2NUM
0566  01230 075307          STB MES12+7
0567  01231 061254          LDA BS4       PACK
0568  01232 001700          ALF             INPUT
0569  01233 011075          AND MSK3          WORD
0570  01234 015025          JSB .2NUM           AND
0571  01235 075317          STB MES12+15          STORE
0572  01236 061254          LDA BS4                 IT IN THE
0573  01237 001727          ALF,ALF                   ERROR
0574  01240 001222          RAL,RAL                     MESSAGE
0575  01241 015025          JSB .2NUM
0576  01242 075320          STB MES12+16
0577  01243 001700          ALF
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0578   01244 001222          RAL,RAI
0579   01245 015025          JSB .2NUM
0580   01246 075321          STR MES12+17
0581   01247 061322          LDA ML12      OUTPUT
0582   01250 065277          LDB MAD12       ERROR
0583   01251 114102          JSB 1028,I        MESSAGE
0584   01252 061255  P9      LDA AS5       RESTORE A
0585   01253 125150          JMP DOIC,I    EXIT SUBROUTINE
0586   01254 000000  BS4     OCT 0
0587   01255 000000  AS5     OCT 0
0588   01256 000000  AS6     OCT 0
0589   01257 000000  DAMSK   OCT 0         DATA MASK STORAGE
0590*
0591   01260 001261  MAD11   DEF *+1
0592   01261 043114  MES11   ASC 13,FLAG FAILURE IN DATA TEST
       01262 040507
       01263 020106
       01264 040511
       01265 045125
       01266 051105
       01267 020111
       01270 047340
       01271 042101
       01272 052101
       01273 020124
       01274 042523
       01275 052440
0593   01276 000032  ML11    DEC 26
0594*
0595   01277 001340  MAD12   DEF *+1
0596   01340 047525  MES12   ASC 18,OUTPUT =              INPUT   =
       01341 052120
       01342 052524
       01343 020075
       01344 020040
       01345 020040
       01346 020040
       01347 020040
       01350 020040
       01351 020040
       01352 044516
       01353 050125
       01354 052440
       01355 020075
       01356 020040
       01357 020040
       01360 020040
       01361 020040
0597   01362 000044  ML12    DEC 36
0598   01363 001364  MAD13   DEF *+1
0599   01364 044517  MES13   ASC 10,IOBI ERROR =
       01365 041111
       01366 020135
       01367 051122
       01370 047522
       01371 020075
       01372 020040
```

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       01333 020040
       01334 020043
       01335 020040
0600   01336 000024   ML13   DEC 20
0601   01337          X      EQU *          FWAM
0602                         END
**  NO ERRORS*
```