



**OPERATING AND SERVICE
MANUAL**

12539C

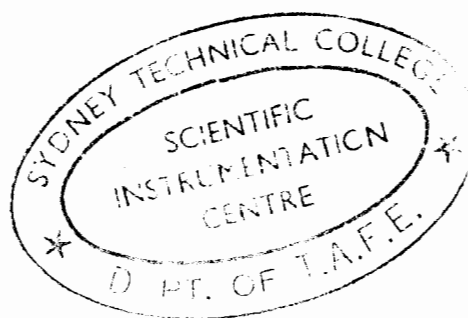
**TIME BASE GENERATOR
INTERFACE KIT**

For HP 1000 (M-, E-, & F-Series) and 2100-Series Computers

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GENERAL INFORMATION

SECTION

I

1-1. INTRODUCTION

1-2. This manual provides general information, installation and programming instructions, theory of operation, maintenance instructions, and replaceable parts information for the Hewlett-Packard 12539C Time Base Generator Interface Kit (figure 1-1).

1-3. DESCRIPTION

1-4. The HP 12539C Time Base Generator measures real-time intervals in decade steps from 0.1 millisecond to

1000 seconds (16.67 minutes). A three-bit control word transferred to the time base generator by programmed instruction selects the time interval to be measured. The 1-MHz crystal-controlled oscillator used as the frequency standard for the time base generator allows generation of timing signals accurate to within 2 seconds per 24-hour day.

1-5. KIT CONTENTS

1-6. The time base generator interface kit consists of a time base generator printed-circuit assembly, part no. 12539-60003, (manufactured until August 1980) or 12539-60005 currently being manufactured, and the operating and service manual, part no. 12539-90008.

1-7. IDENTIFICATION

1-8. This operating and service manual is identified on the title page by interface kit designation and nomenclature, printed-circuit assembly part number and series code, manual part number, and publication date. Refer to the information presented in the following paragraphs and ensure that this manual applies to the equipment being serviced.

1-9. Hewlett-Packard uses five digits and a letter (00000A) for standard interface kit designation. If the designation of your kit does not agree with that on the title page of this manual, there are differences between your kit and the kit described in this manual. The appropriate manual or manual supplement is available at the nearest HP Sales and Service Office listed at the back of this manual.

1-10. Printed-circuit assembly (PCA) revisions are identified by a letter, a series code, and a division code stamped on the board (e.g., A-1232-22). The letter code identifies the version of the etched trace pattern on the unloaded board. The series code (four middle digits) refers to the electrical characteristics of the loaded assembly and the positions of the components. The division code (last two digits) identifies the Hewlett-Packard division which manufactured the PCA. If the series code stamped on the PCA does not agree with the series code shown on the title page of this manual, there are differences between your PCA and the PCA described in this manual. These differences are described in change sheets and manual supplements available at the nearest HP Sales and Service Office.

1-11. Throughout this manual the term 12539C is used to refer to all part numbers and series code listed on

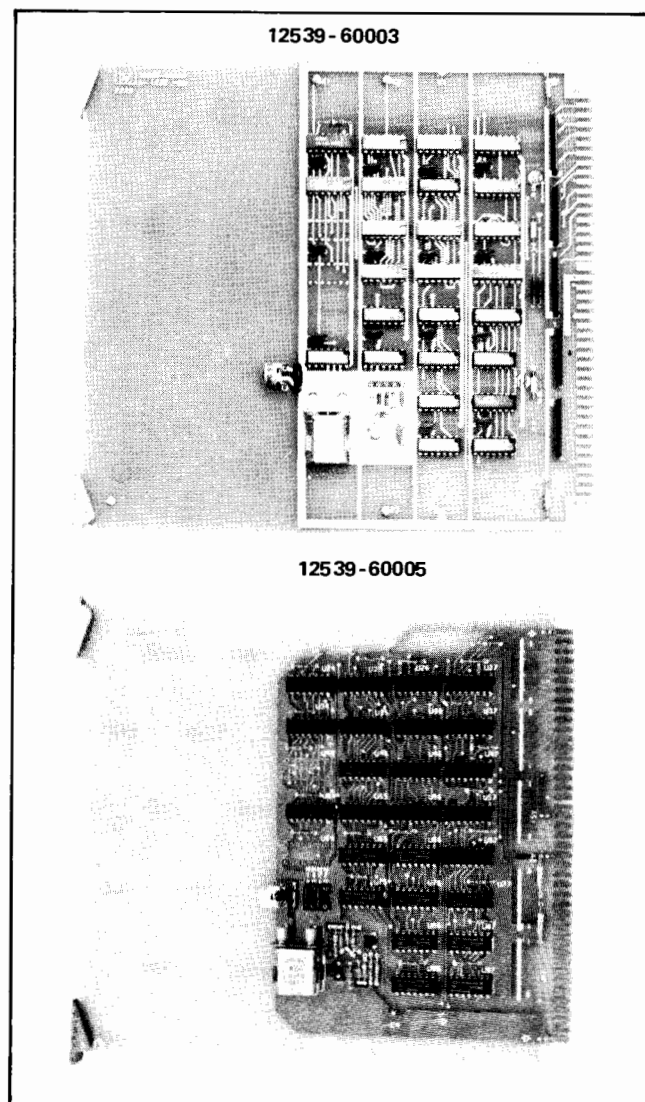


Figure 1-1. HP 12539C Time Base Generator Interface Kit

the cover page of this manual when the information presented pertains equally to all three. A particular part number is referred to only if the information presented is unique to that part number.

1-12. SPECIFICATIONS

1-13. Table 1-1 lists the specifications for the HP 12539C Time Base Generator Interface PCA.

Table 1-1. Time Base Generator Specifications

| CHARACTERISTICS | SPECIFICATIONS | CHARACTERISTICS | SPECIFICATIONS |
|----------------------|--|---|---|
| Time Base Intervals: | 0.1 millisecond 1 millisecond 10 milliseconds 100 milliseconds 1 second 10 seconds 100 seconds 1000 seconds | Stability: Aging: Temperature: Supply Voltage (4.5 - 5.5V) | ± 5 PPM/Yr ± 20 PPM ± 5 PPM |
| Time Base Accuracy: | 2 seconds per 24-hour day | Current Requirements from Computer Power Supply: -2V +5V | 0.016A 0.75A |
| | | Logic Levels: Logic 1 (high): Logic 0 (low): | +2.4 or greater +0.4V or less |

INSTALLATION AND PROGRAMMING

SECTION

II

2-1. INTRODUCTION

2-1. This section provides information for unpacking and inspection, reshipment, installation, and programming the HP 12539C Time Base Generator Interface Kit.

2-3. UNPACKING AND INSPECTION

2-4. If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the card is unpacked. Inspect the PCA for damage (cracks, broken components, etc.). If the PCA is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for repair or replacement of the damaged PCA without waiting for claims against the carrier to be settled.

2-5. RESHIPMENT

2-6. If an item of the kit is to be shipped to Hewlett-Packard for service or repair, attach a tag to the item identifying the owner and indicating the service or repair to be accomplished. Include the model number of the kit.

2-7. Pack the item in the original factory packing material if available. If the original material is not available, standard factory packing material can be obtained from the nearest Hewlett-Packard Sales and Service Office.

2-8. If standard packing material is not used, wrap the item in Air Cap TH-240 cushioning (manufactured by Sealed Air Corporation, Hawthorn, N.J.) or equivalent and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to ensure careful handling.

NOTE

In any correspondence, identify the kit by number. Refer any questions to the nearest Hewlett-Packard Sales and Service Office.

2-9. INSTALLATION

2-10. The time base generator PCA obtains its operating currents from the computer power supply. Before

installing the PCA, determine the current requirements of this PCA in combination with all other interface or accessory kits already installed in the computer. The computer system documentation defines the currents available from the computer and describes the procedures for calculating the total power supply current requirements. If the total current requirements exceed the limitations of the computer power supply, a Hewlett-Packard input/output extender unit must be used. See table 1-1 for the current requirements of the time base generator PCA.

2-11. After ensuring sufficient power, install the time base generator PCA as follows:

- a. Check jumpers on PCA. Jumpers should be installed across W1A and W2A. See paragraph 2-16 and 4-7 for further information.
- b. Turn power off at the computer.
- c. Insert the time base generator PCA in the computer I/O slot corresponding to the desired select code.
- d. Turn on power and perform the diagnostic test, manual part no. 12539-90011, to verify proper operation of the time base generator PCA.
- e. Check the oscillator output frequency at test point E4 using a Hewlett-Packard 5245L Electronic Counter or equivalent. The frequency should be $1\text{-MHz} \pm 0.5\text{ Hz}$. If the frequency is not within tolerance, adjust the frequency according to the oscillator adjustment procedures given in paragraph 4-10.

2-12. PROGRAMMING

2-13. CONTROL WORD

2-14. The desired time interval to be measured by the time base generator is selected by transferring a three-bit control word from the computer A- or B-register to the time base generator. Table 2-1 lists the possible control word bit combinations and the time interval selected by each. Note that the time intervals are selected in increments equal to 10^{n-1} milliseconds where n is the decimal equivalent of the three-bit control word. For non-decade time intervals a decade interval must be counted by software to form the desired interval. For example, if a time interval of three milliseconds is desired, a one millisecond interval must be counted by software three times, to obtain the desired interval.

2-15. ERROR CHECK

2-16. When more than one decade time interval is required for any given timing operation, the time base generator provides a means of ensuring that all selected intervals have been acknowledged by the computer. A status word, transferred from the time base generator to the computer A- or B-register by an LIA or LIB instruction, contains a single significant bit (bit 4). If this bit is a logic 1, at least one time interval has been lost. This status word should be checked by software after each decade time interval.

2-17. Jumper W1 on the PCA can be placed in position B to make bit 5 significant also. In this way, bit 5 can be checked by software to determine if a time interval has been lost.

2-18. SAMPLE PROGRAM

2-19. Table 2-2 is a sample program demonstrating the operation of the time base generator. Under control of this program, the time base generator will provide a measured time interval of 5 seconds. This is done by counting five

Table 2-1. Control Word Combinations and Time Intervals

| CONTROL WORD | | | SELECTED TIME INTERVAL |
|--------------|-------|-------|------------------------|
| BIT 2 | BIT 1 | BIT 0 | |
| 0 | 0 | 0 | 0.1 millisecond |
| 0 | 0 | 1 | 1 millisecond |
| 0 | 1 | 0 | 10 milliseconds |
| 0 | 1 | 1 | 100 milliseconds |
| 1 | 0 | 0 | 1 second |
| 1 | 0 | 1 | 10 seconds |
| 1 | 1 | 0 | 100 seconds |
| 1 | 1 | 1 | 1000 seconds |

NOTE: Bits 3 through 15 not used.

1-second intervals with a software counter. After each 1-second interval, the error status bit is checked to ensure that all of the 1-second intervals are acknowledged by the computer.

Table 2-2. Sample Program

| | | | | | |
|-------|--|--------|-------|-------|-------------------------------------|
| 0001 | ASMB,A,B,L,T | | | | |
| 0002* | | | | | |
| 0003* | THIS IS A SAMPLE PROGRAM TO DEMONSTRATE THE OPERATION OF THE | | | | |
| 0004* | TIME BASE GENERATOR. UNDER CONTROL OF THIS PROGRAM, THE TIME | | | | |
| 0005* | BASE GENERATOR WILL PROVIDE A MEASURED INTERVAL OF FIVE SECONDS. | | | | |
| 0006* | THIS REQUIRES THAT FIVE DECADE INTERVALS OF ONE SECOND EACH | | | | |
| 0007* | BE MEASURED AND COUNTED BY SOFTWARE. AFTER EACH DECADE INTERVAL | | | | |
| 0008* | IS MEASURED, THE ERROR STATUS IS CHECKED AND IF AN ERROR IS | | | | |
| 0009* | DETECTED, THE COMPUTER HALTS WITH A T-REGISTER DISPLAY OF | | | | |
| 0010* | 102066 OCTAL. | | | | |
| 0011* | | | | | |
| 0012 | 00100 | | ORG | 100B | |
| 0013* | | | | | |
| 0014 | 00100 | 000000 | START | NOP | |
| 0015 | 00101 | 060121 | LDA | .5 | INITIALIZE COUNTER TO COUNT |
| 0016 | 00102 | 070122 | STA | COUNT | FIVE DECADE INTERVALS. |
| 0017* | | | | | |
| 0018* | THIS PART OF THE PROGRAM OPERATES THE TIME BASE GENERATOR. | | | | |
| 0019* | | | | | |
| 0020 | 00103 | 060123 | LDA | CW | GET CONTROL WORD AND TRANSFER |
| 0021 | 00104 | 102615 | OTA | TBG | TO TIME BASE GENERATOR. |
| 0022 | 00105 | 102715 | STC | TBG | START TIME BASE GENERATOR |
| 0023 | 00106 | 103115 | CLF | TBG | ENABLE FLAG LOGIC. |
| 0024 | 00107 | 102315 | SFS | TBG | HAS DECADE INTERVAL ELAPSED? |
| 0025 | 00110 | 024107 | JMP | *-1 | NO. WAIT. |
| 0026 | 00111 | 024112 | JMP | STAT | YES. CHECK ERROR STATUS. |
| 0027* | | | | | |
| 0028* | THIS PART OF THE PROGRAM CHECKS ERROR STATUS AND INCREMENTS | | | | |
| 0029* | THE DECADE INTERVAL COUNTER. | | | | |
| 0030* | | | | | |
| 0031 | 00112 | 102515 | STAT | LIA | TBG |
| 0032* | GET STATUS WORD FROM TIME BASE | | | | |
| 0033 | 00113 | 050124 | CPA | ERR | GENERATOR |
| 0034 | 00114 | 102066 | HLT | 66B | DOES STATUS WORD INDICATE AN ERROR? |
| 0035 | 00115 | 034122 | ISZ | COUNT | YES. HALT COMPUTER. |
| 0036* | NO. INCREMENT COUNTER. IS TIME | | | | |
| 0037 | 00116 | 024106 | JMP | GO | INTERVAL COMPLETE? |
| 0038 | 00117 | 106715 | CLC | TBG | NO. START ANOTHER DECADE INTERVAL. |
| 0039 | 00120 | 102077 | HLT | 77B | YES. STOP DECADE COUNTERS. |
| 0040* | HALT COMPUTER. | | | | |
| 0041* | CONSTANT AND STORAGE INFORMATION. | | | | |
| 0042* | | | | | |
| 0043 | 00121 | 177773 | .5 | DEC | -5 |
| 0044 | 00122 | 000000 | COUNT | BSS | 1 |
| 0045 | 00123 | 000004 | CW | OCT | 4 |
| 0046 | 00124 | 000020 | ERR | OCT | 20 |
| 0047 | 00015 | | TBG | EQU | 158 |
| 0048* | | | | | |
| 0049 | | | END | START | |
| ** | NO ERRORS* | | | | |

THEORY OF OPERATION

SECTION

III

3-1. INTRODUCTION

3-2. This section provides functional and detailed theory of operation for the HP 12539C Time Base Generator Interface Kit.

3-3. FUNCTIONAL THEORY OF OPERATION

3-4. Figure 3-1 is a block diagram of the time base generator PCA and a flowchart showing the functional operation of the time base generator PCA. The program instructions shown in the flowchart are the same as those used in the sample program in table 2-2 in section II of this manual.

3-5. Operation of the time base generator begins with the transfer of a three-bit control word from the computer A- or B-register to the time base selection register with an OTA or OTB instruction. The next instruction (STC,C) causes a shaped 100-kHz signal to be gated to the decade divider circuits. This marks the beginning of the time interval.

3-6. An SFS instruction is used to determine if the selected time interval has elapsed. Before the time interval has elapsed, a JMP *-1 instruction is executed followed by the SFS instruction again. This wait loop continues until the selected time interval has elapsed.

3-7. At the end of the selected time interval, the time base generator supplies an SKF signal. The SKF signal causes the computer to skip the JMP *-1 instruction and proceed with the program. The time spent in the wait loop is the time selected by the control word that was initially transferred to the time base generator.

3-8. DETAILED THEORY OF OPERATION

3-9. Refer to the time base generator logic diagram, figure 4-2, in section IV of this manual while reading the detailed theory of operation discussion.

3-10. For an index of signals on the 86-pin edge of the time base generator PCA, refer to the computer system documentation.

3-11. All logic levels on the time base generator PCA are positive-true. The term "high" refers to a level of approximately +2.4V and "low" refers to approximately

+0.4V. These signal levels vary somewhat depending on the integrated circuit package involved.

3-12. POWER-ON LOGIC

3-13. When power is initially applied to the computer or the computer PRESET switch is pressed, the computer supplies a POPIO and a CRS signal to the time base generator PCA. The POPIO signal sets the Flag Buffer FF and the CRS signal clears the Control FF. An ENF signal at the next computer time T2 is gated with the set-side output of the Flag Buffer FF to set the Flag FF. The low set-side output of the Control FF is applied through U34D to the clear inputs of the decade dividers ensuring that they are initially in the clear state. The low set-side output of the Control FF also inhibits "and" gate U24C to prevent the 100-kHz signal from clocking the decade dividers. Also, the first ENF signal clears the IRQ FF. Because the output of the eight-to-one multiplexer circuit is low, the Time Flag FF clears when the first SIR signal is received at computer time T5.

3-14. TIME STANDARD LOGIC

3-15. The basic component of the time standard logic is a 1-MHz crystal oscillator accurate to 20 ppm (parts per million). The 1-MHz signal is applied to decade divider U75 to obtain a 100-kHz signal. "And" gate U24C allows the control logic to control the application of this 100-kHz signal to the decade dividers as described in paragraph 3-24.

3-16. The gated 100-kHz signal is applied to the first of the eight decade dividers. The decade dividers are wired externally to operate as binary coded decimal counters with a count added each time the input signal (pin 14) swings low. The output signal (pin 11) swings high on the eighth count then low on the tenth count. The low swing adds one count to the next divider stage. The output signals from each of the decade dividers are applied to the time base selection logic.

3-17. TIME BASE SELECTION LOGIC

3-18. The time base selection logic consists of three Time Base Selection FF's (BIT 0-3 FF's) and an eight-to-one multiplexer circuit.

3-19. The desired time interval to be measured by the time base generator PCA is encoded into a three-bit control word. This control word is transferred from the computer A- or B-register to the Time Base Selection FF's by

an OTA or OTB instruction with the select code of the time base generator. Either of these instructions supply high SCM, SCL, IOG, and IOO signals and the three-bit control word (IOBO 0, IOBO 1, and IOBO 2) to the time base generator.

3-20. When the IOO signal goes high at computer time T3, the three-bit control word is stored in the Time Base Selection FF's. The IOO signal also clears all nine decade dividers and the Control FF at this time.

3-21. The outputs of the Time Base Selection FF's control the eight-to-one multiplexer circuit. This circuit decodes the control word so that one of the eight decade dividers is selected as the time base (for time interval).

3-22. CONTROL LOGIC

3-23. After the control word has been loaded into the Time Base Selection FF's, the time base generator is ready to begin measuring the time period. An STC,C instruction with the select code of the time base generator marks the beginning of the time period. As a result of this instruction, the time base generator PCA receives high IOG, SCM, SCL, STC, and CLF signals from the computer.

3-24. The STC signal sets the Control FF. The high set-side output of the Control FF gates the 100-kHz signal to the decade dividers and provides one of the enabling signals to the time flag gate (U36C).

3-25. The CLF signal clears the Flag Buffer and Flag FF's. The high clear-side output of the Flag FF provides another enabling signal to the time flag gate. (Because the clear-side output of the Time Flag FF is also high, the output of the time flag gate goes high at this time. However, this has no effect since the CLF signal provides an overriding clear signal to the Flag Buffer FF.) The decade dividers are now counting the 100-kHz signal and continue to count until the selected time interval has elapsed.

3-26. FLAG LOGIC

3-27. The flag logic monitors the output of the eight-to-one multiplexer circuit for a signal indicating the end of the desired time interval.

3-28. For discussion purposes, assume that the control word specifies a time interval of one second. In this instance, the eight-to-one multiplexer selects the U86 decade divider as the time base. When the decade dividers have counted 0.8 second, the output of divider U86 goes high (paragraph 3-16). This signal is gated through the eight-to-one multiplexer circuit to the set input of the Time Flag FF. At the next computer time T5 (SIR), the Time Flag FF sets causing the output of the time flag gate to go low. At the count of one second, the output of divider U86 goes low. The Time Flag FF clears at the next SIR signal causing the output of the time flag gate to go high,

setting the Flag Buffer FF. At the next computer time T2 (ENF), the Flag FF sets.

3-29. When the Flag FF is in the set state, the time base generator PCA generates an SRQ signal and, if programmed to do so, generates FLG and IRQ signals or an SKF signal. These signals indicate to the computer that the requested time interval has ended. The following paragraphs describe how these signals are generated and how they are used by the computer.

3-30. **SKIP-ON-FLAG SIGNAL.** If the computer is programmed to wait for the Flag FF to be set (SFS instruction followed by a JMP *-1 instruction for example), the resulting SFS signal gated with the set side of the Flag FF generates an SKF signal. This causes the computer to skip the next programmed instruction (JMP *-1) and proceed with the program. Figure 3-2 illustrates the generation of an SKF signal by the time base generator PCA. Notice that SKF signal can also be generated when the Flag FF is in the clear state by programming a SFC instruction. Either way, the state of the Flag FF is being tested and the computer must be programmed to respond accordingly.

3-31. **INTERRUPT SIGNALS.** If the computer interrupt system has been enabled by an STF 00 instruction, the time base generator can be used to generate timed interrupts. Figure 3-3 illustrates the functions involved in an interrupt operation. To interrupt the main program at the end of a measured time interval, the following conditions must be met at the time base generator PCA:

- a. Control FF set (paragraph 3-24).
- b. Flag Buffer FF set (paragraph 3-28).
- c. Flag FF set (paragraph 3-28).
- d. IEN signal high (interrupt system enabled).
- e. PRH signal high (no higher priority interrupts).

3-32. When all of these conditions are established, an SIR signal at time T5 sets the IRQ FF which generates true FLG and IRQ signals. These signals are used by the computer I/O control and addressing circuits to generate an interrupt signal.

3-33. At time T2 following the interrupt, an ENF signal clears the IRQ FF. An SIR signal again sets the IRQ FF if the PRH signal is still high at time T5. The FLG and IRQ signals this time are used by the computer I/O control and addressing circuits to encode the interrupt address.

3-34. The next machine cycle will be under control of the instruction located at the interrupt address in memory. During this machine cycle, an IAK signal at time T6 clears the Flag Buffer FF and an ENF signal at time T2 clears the IRQ FF. The Flag FF remains set to inhibit lower priority interrupts by providing a low PRL signal.

3-35. At this point, the computer normally enters an interrupt subroutine. A CLC instruction is required at the

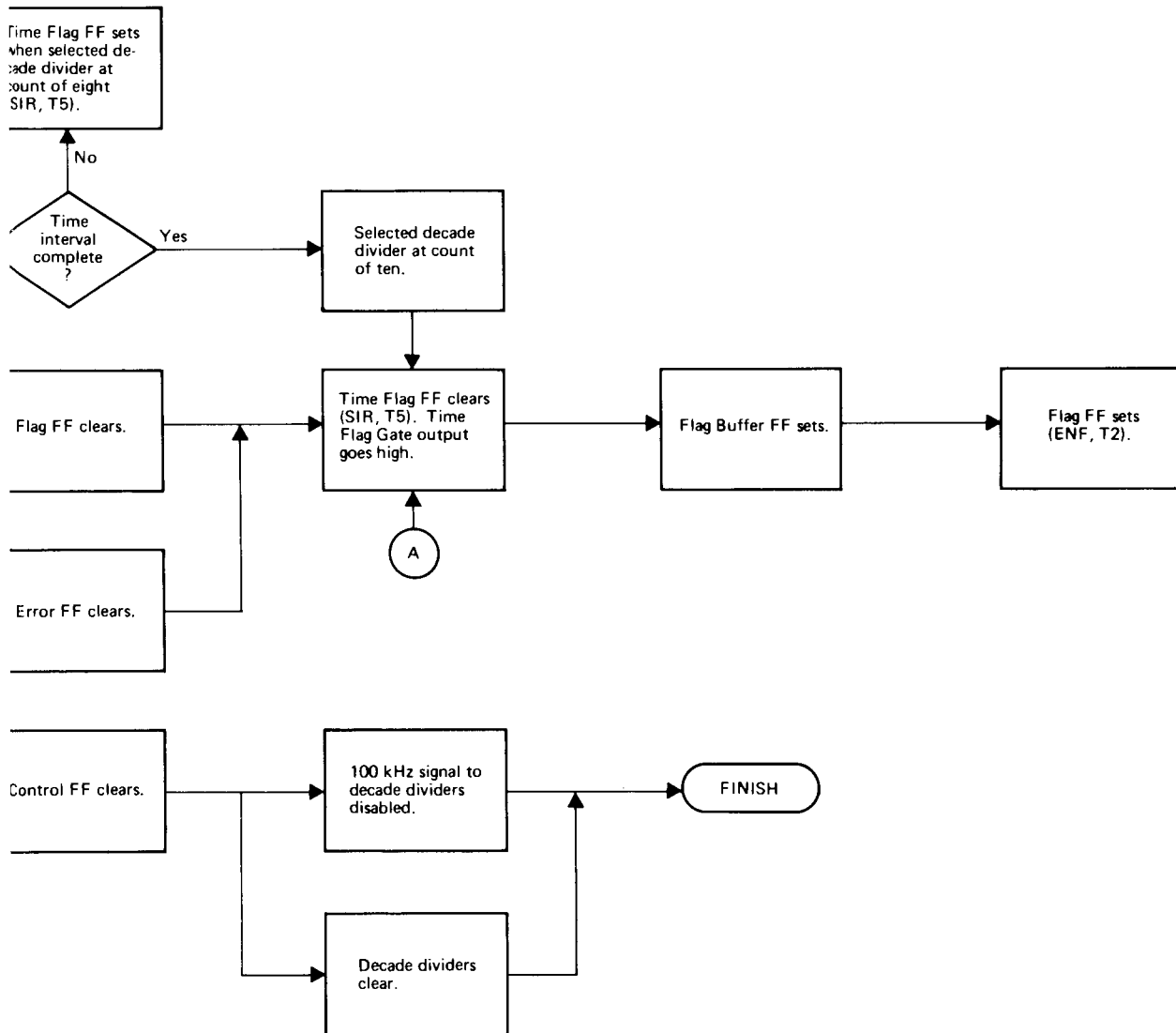


Figure 3-1. Time Base Generator Simplified Logic Diagram and Functional Operation Flowchart

— SRQ

— PRL

— FLG

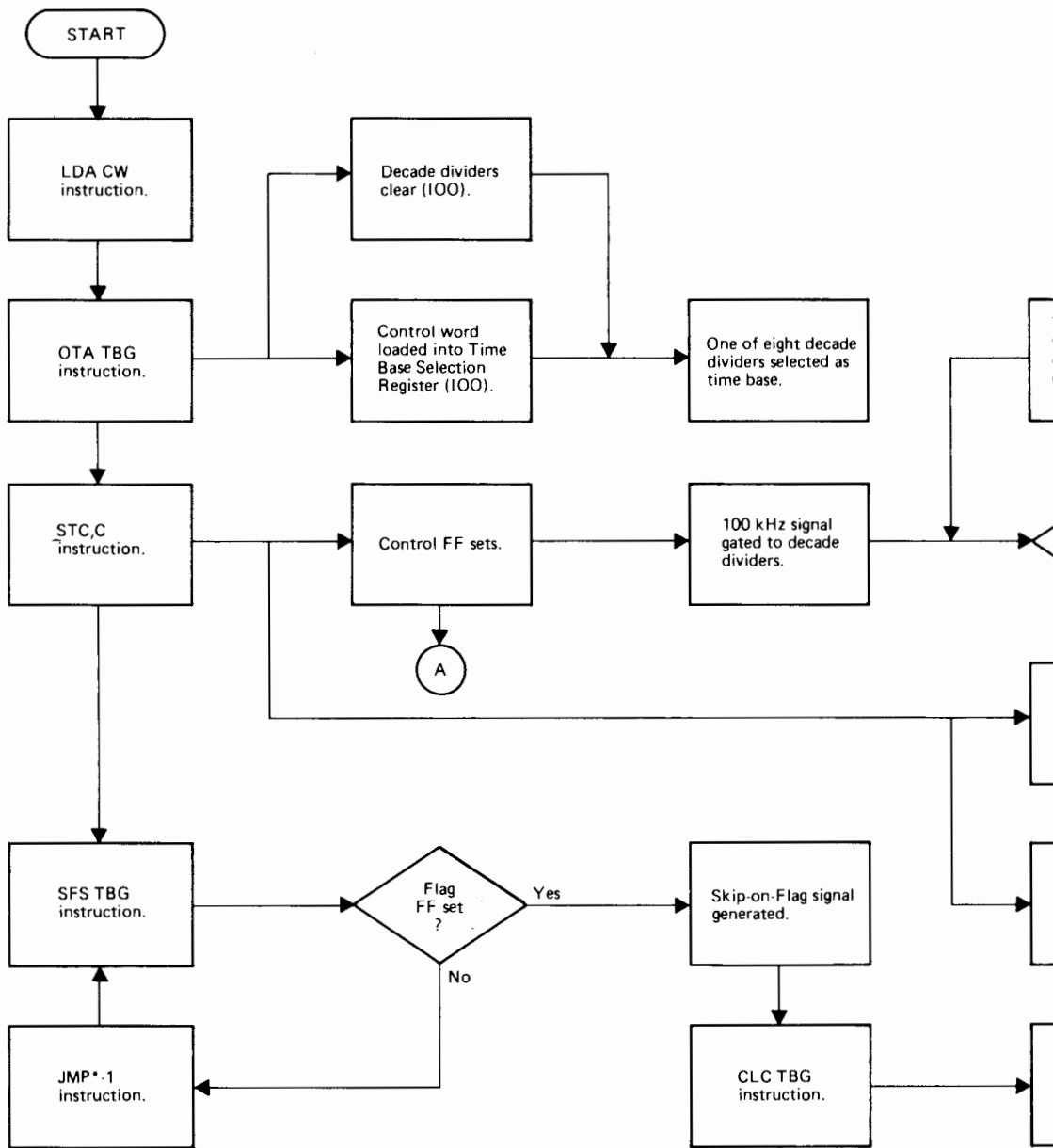
— IRQ

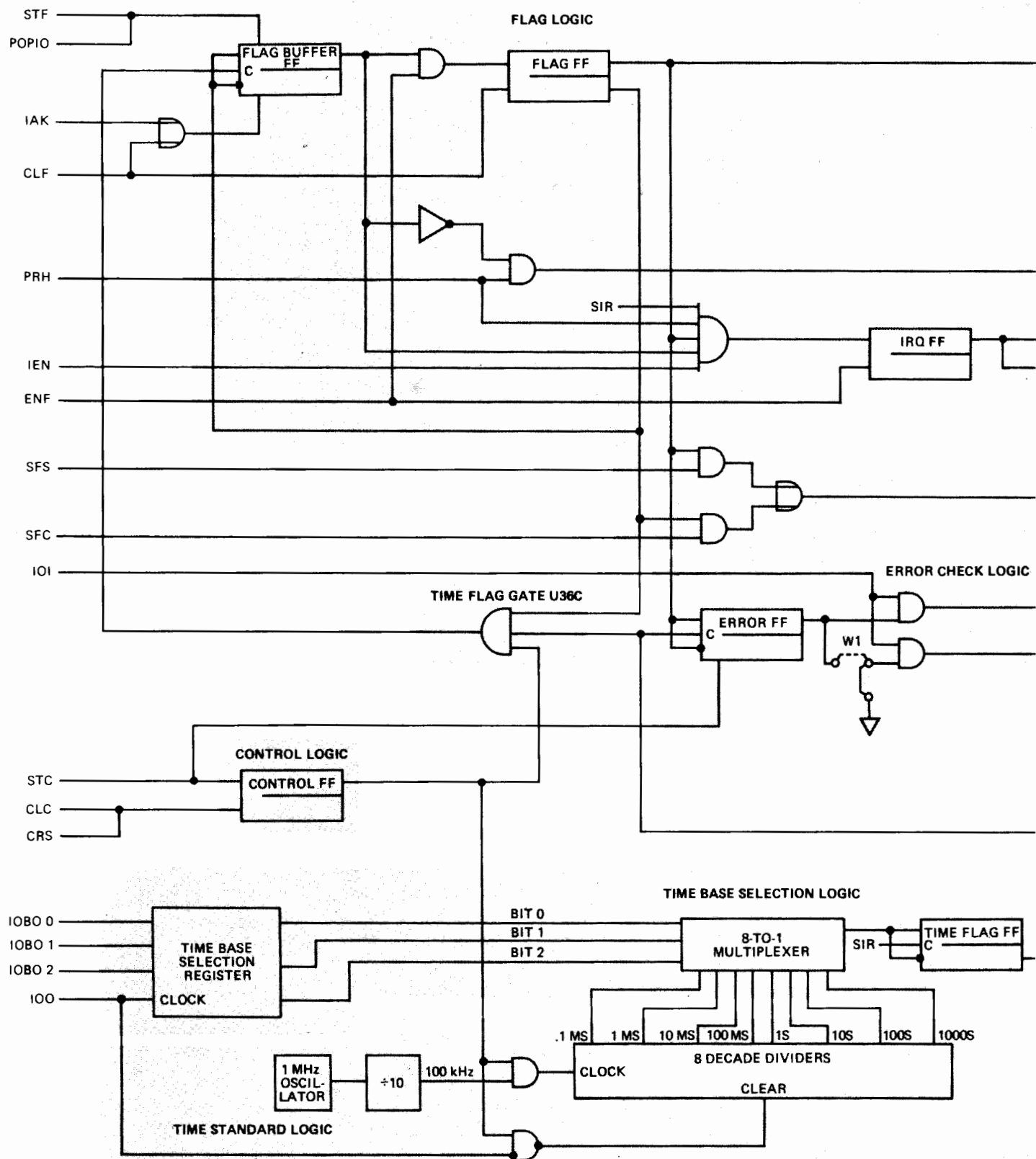
— SKF

— IOBI 4

— IOBI 5

[





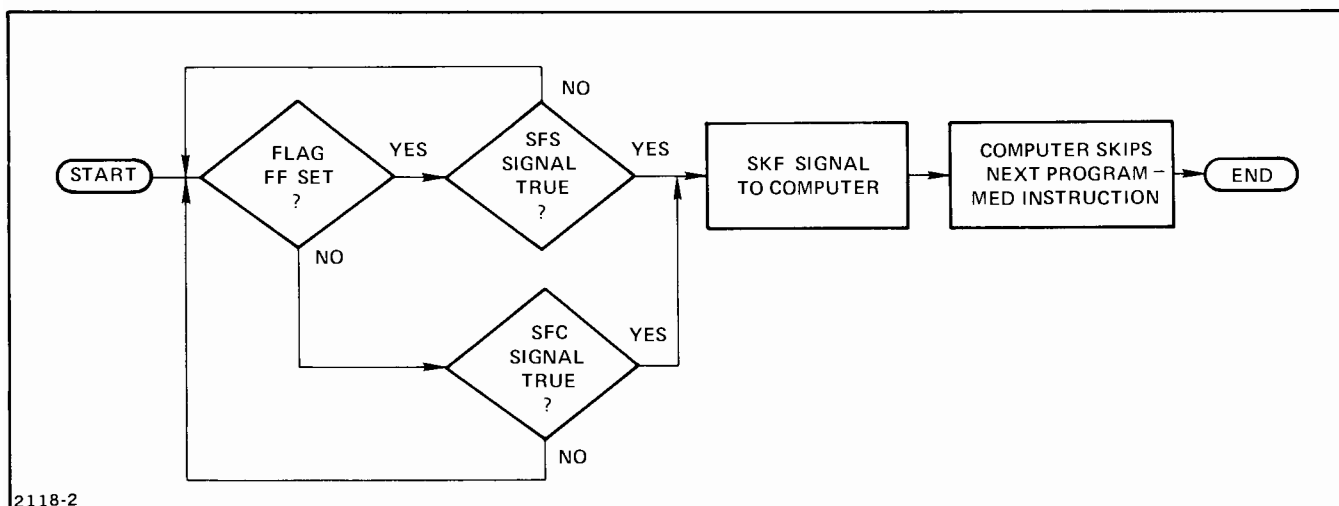


Figure 3-2. Skip-On-Flag Signal Generation Flowchart

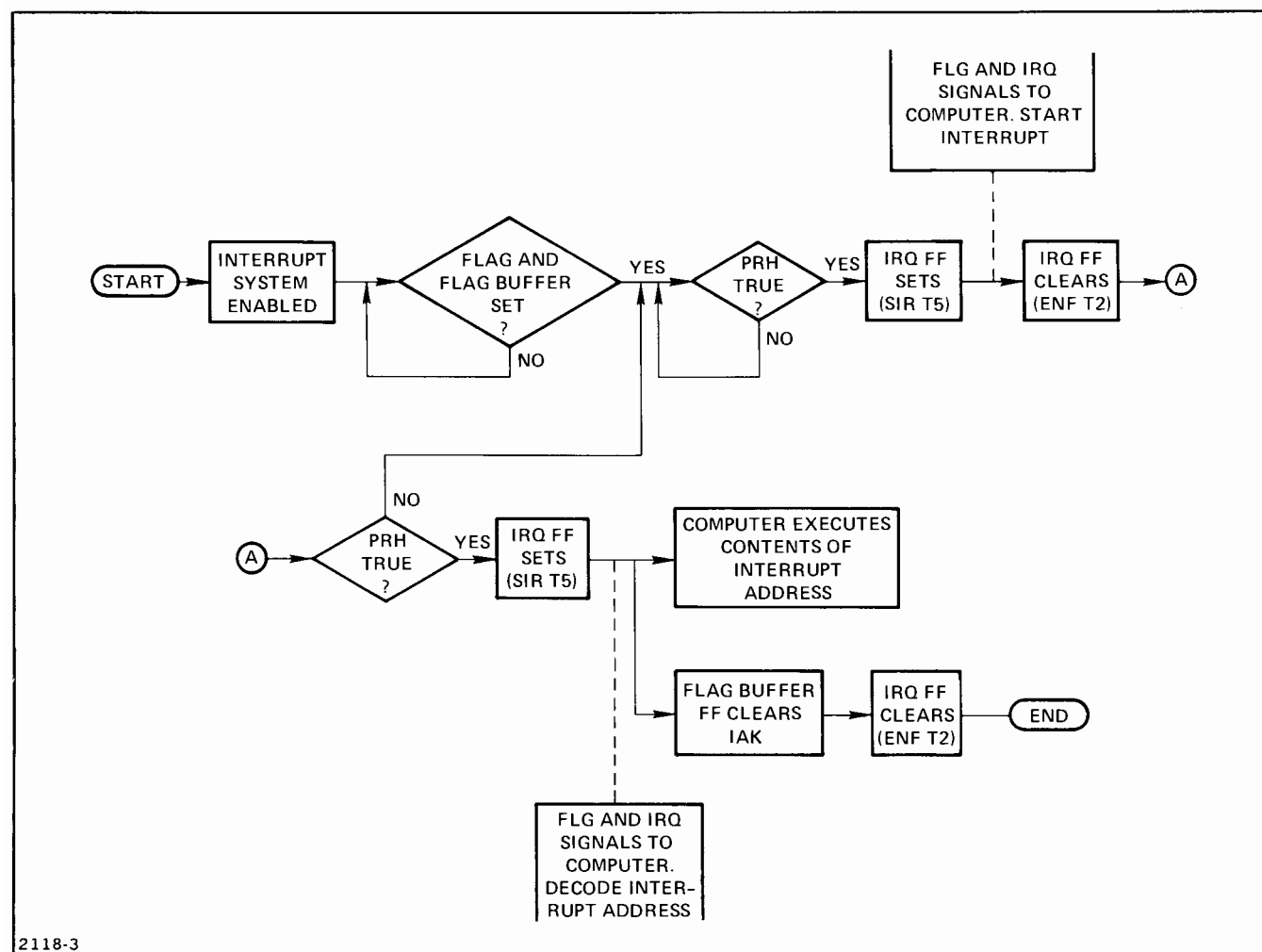


Figure 3-3. Interrupt Operation Flowchart

beginning of the subroutine to disable the decade dividers and prevent the Error FF (paragraph 3-37) from being set. Also, just before leaving the subroutine, a CLF instruction is required to enable lower priority interrupts.

3-36. ERROR CHECK LOGIC

3-37. The Error FF monitors the set-side output of the Flag FF and is clocked by the clear-side output of the Time

Base FF. If the Flag FF is set (indicating that the desired time interval has elapsed) and the selected divider output goes low a second time (causing the Time Flag FF to clear), the Error FF sets.

3-38. The state (set or cleared) of the Error FF is read onto the IOBI 4 line (and the IOBI 5 line if selected by jumper W1) and loaded into the computer A- or B-register by an LIA or LIB instruction addressed to the time base generator. Bit 4 (or 5) of the A- or B-register can then be checked by software for a possible error condition.

4-1. INTRODUCTION

4-2. This section provides maintenance information for the HP 12539C Time Base Generator Interface Kit. Included are preventive maintenance instructions, troubleshooting instructions, and maintenance data consisting of integrated circuit pin connections (figure 4-1), and a time base generator PCA parts location and logic diagram (figure 4-2). For PN 12539-60005 see figure 4-3 for PCA Parts Location and Logic Diagram.

4-3. PREVENTIVE MAINTENANCE

4-4. Incorporate preventive maintenance for the time base generator with the preventive maintenance routines for the computer system. Inspect the time base generator PCA for cracked, broken, or burned components, insulation, and connections.

4-5. TROUBLESHOOTING

4-6. Most malfunctions on the time base generator PCA can be traced by performing the diagnostic test, manual part no. 12539-90011, and analyzing error halts as they occur. Use the maintenance data contained in this section to isolate malfunctions to the component level.

4-7. To facilitate testing the decade dividers, jumper W2 can be moved to position B. This reduces the time interval required to operate the last four divider circuits. With jumper W2 in position B, the decade dividers for 0.1 millisecond (U77), 1 millisecond (U87), 10 milliseconds (U97), and 100 milliseconds (U96) operate normally. However, with jumper W2 in position B, the last four decade dividers operate at 1 millisecond (U86), 10 milliseconds (U76), 100 milliseconds (U66), and 1 second (U65).

NOTE

If jumper W2 is moved to position B, be sure to return jumper W2 to position A when testing is completed.

4-8. If crystal Y1 is replaced, check the oscillator output frequency at test point E4 using a Hewlett-Packard 5245L Electronic Counter or equivalent. The frequency should be 1-MHz ± 0.5 Hz. If the frequency is not within tolerance, adjust the frequency according to the oscillator adjustment procedures given in paragraph 4-10.

4-9. OSCILLATOR ADJUSTMENT

4-10. Using a Hewlett-Packard 5245L Electronic Counter or equivalent frequency measuring device, observe the oscillator output frequency at test point E4. Adjust capacitor C19 (C27 on PN 12539-60005) to obtain an output frequency of 1-MHz ± 0.5 Hz.

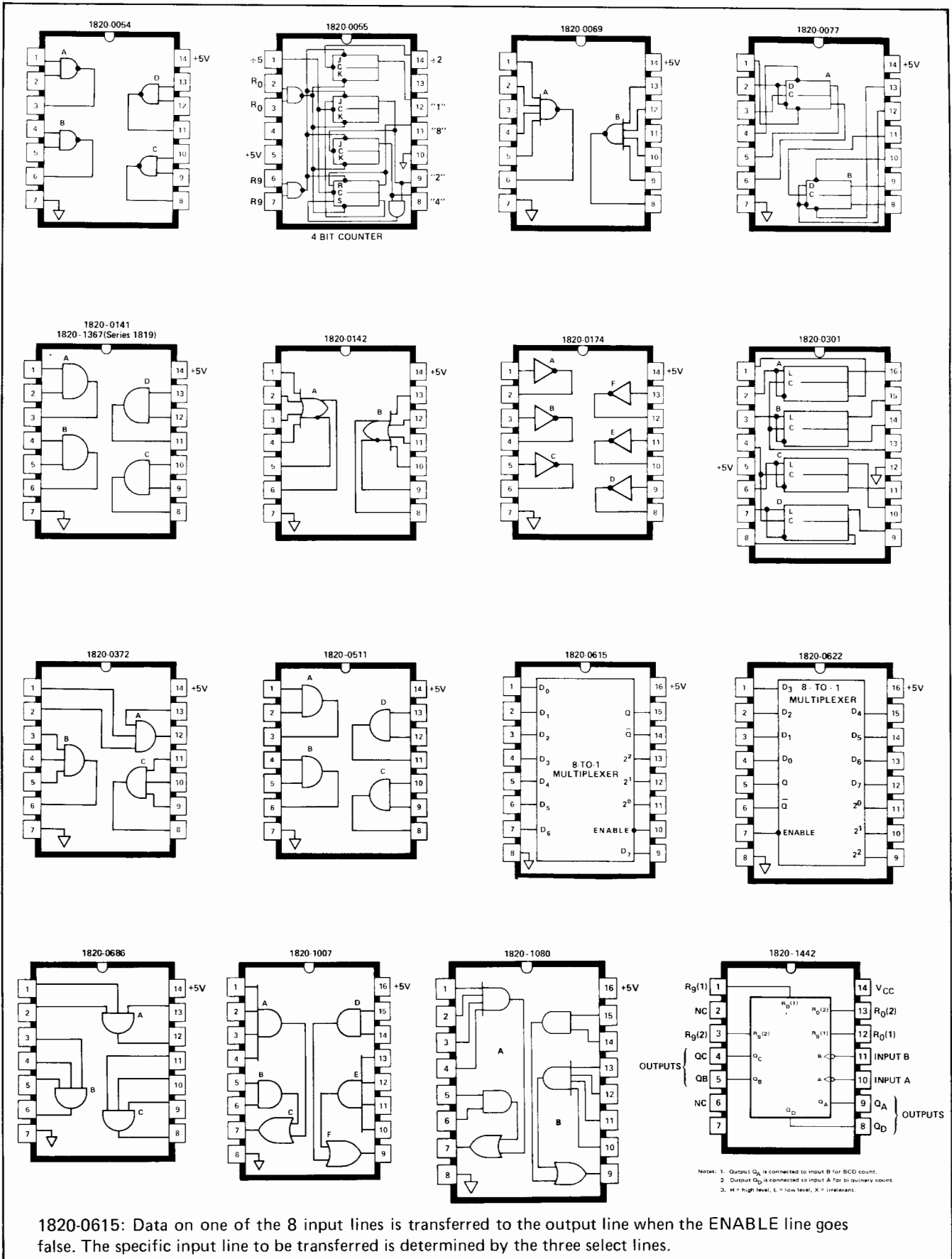


Figure 4-1. Integrated Circuit Pin Connection

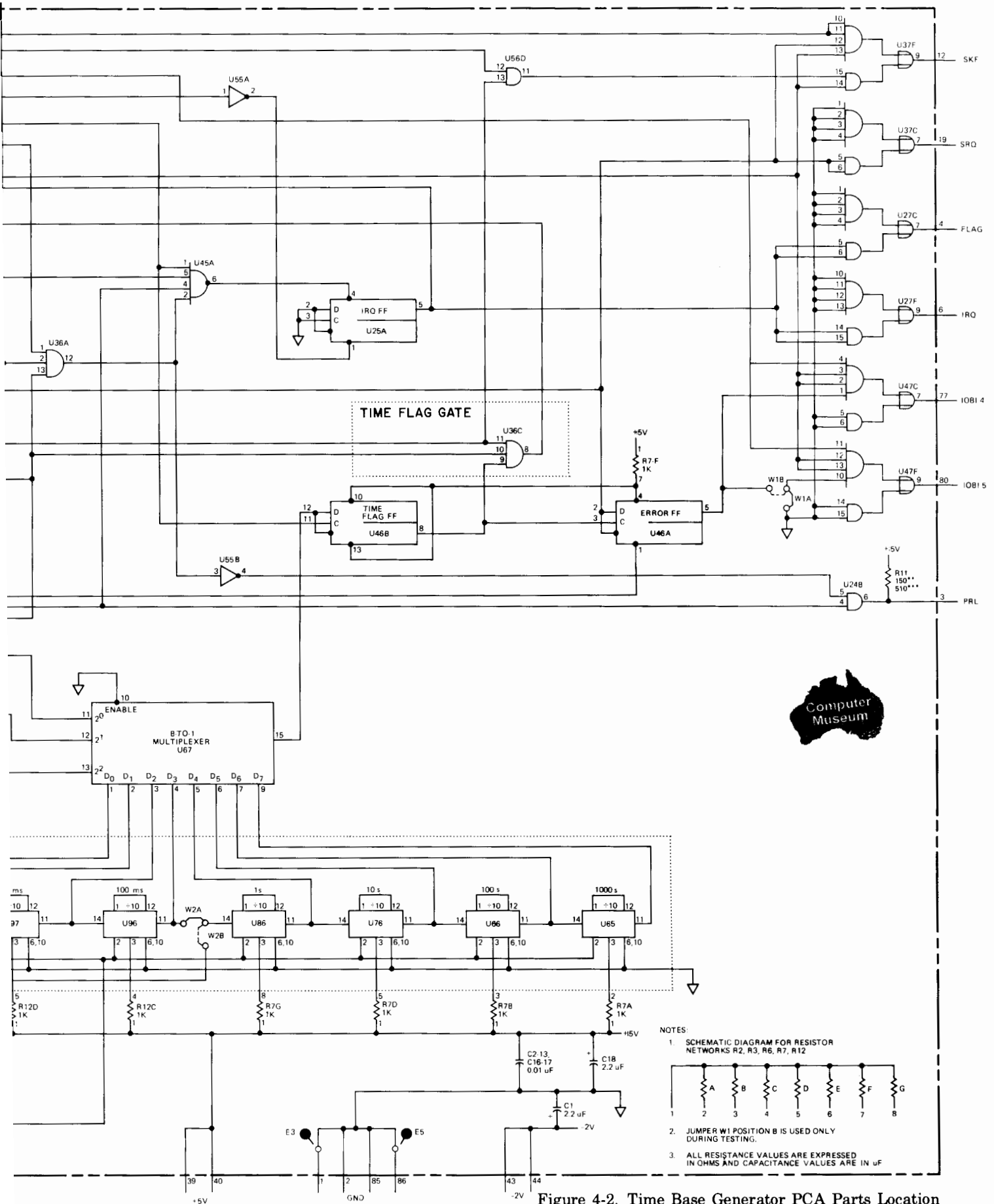
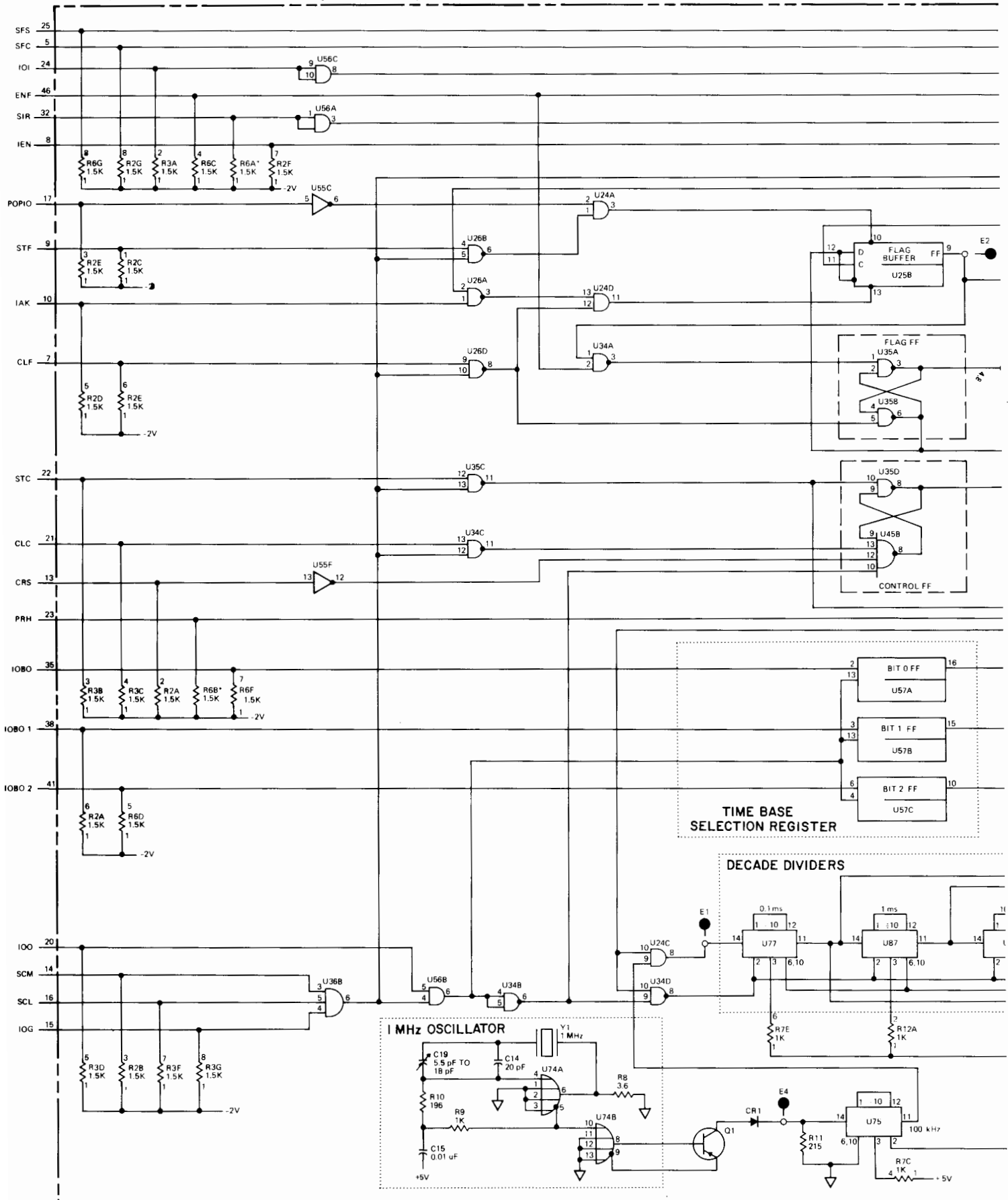


Figure 4-2. Time Base Generator PCA Parts Location and Logic Diagrams (PN 12539-60003)

TIME BASE GENERATOR (12539-60003, SERIES 1819)



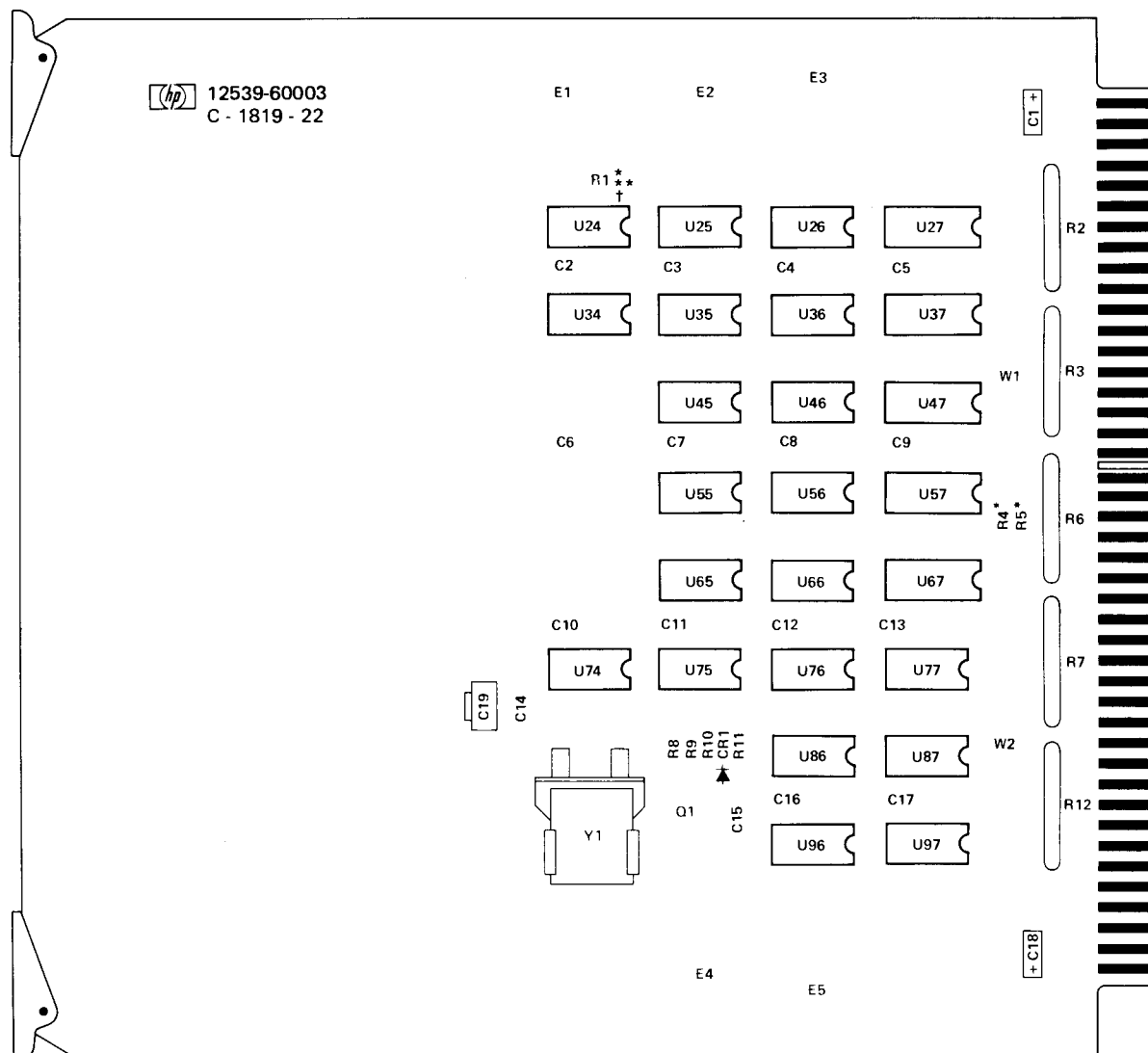
DWG REV. A

* R6A is R4, 750 ohms and R6B is R5, 750 ohms on PCA's with Series No. 1232.

** Used on PCA's with Series No. 1232.

*** Used only on PCA's with series no. 1819.

† Resistor removed on series no. 1945. If PCA is used in Select Code 17 of the computer mainframe, reinstall 150 ohm resistor in R1 slot located next to U24.



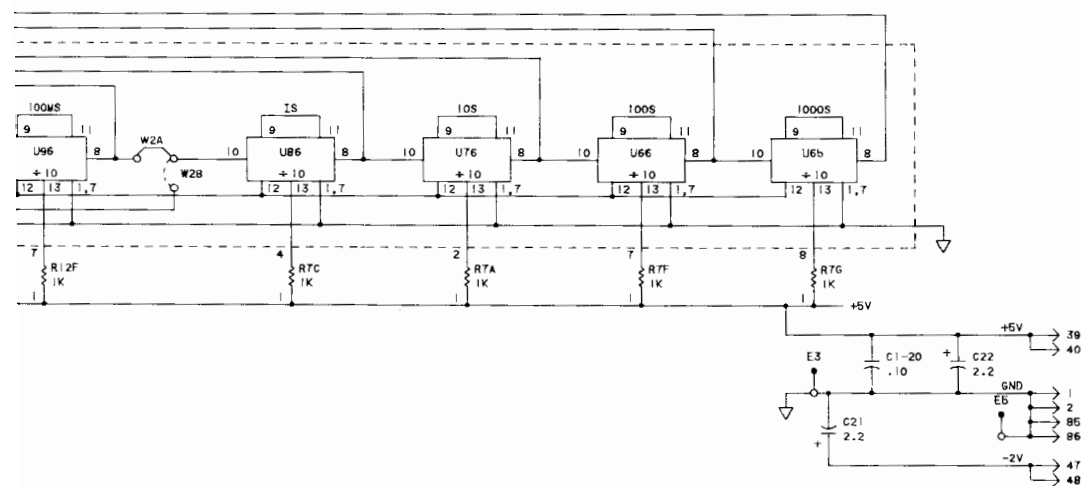
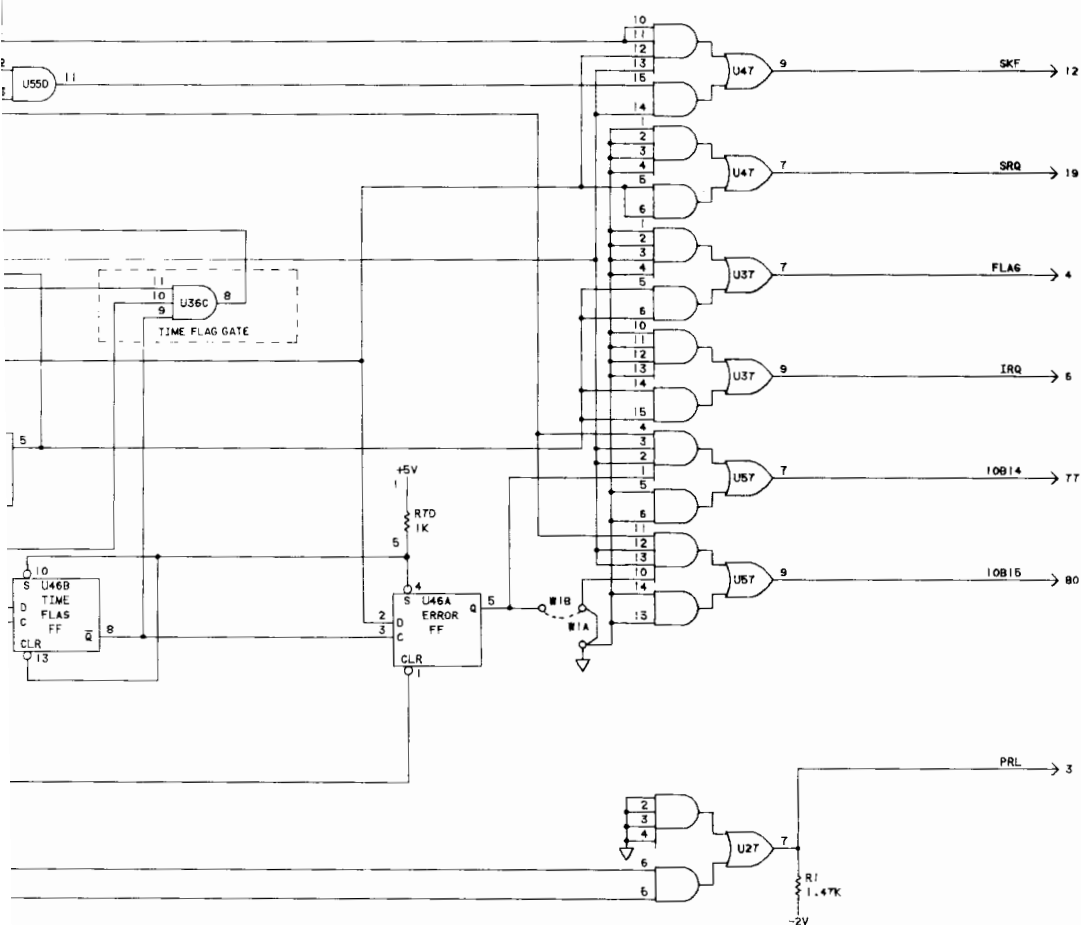
2238-5

*Used on Series Nos. 1232

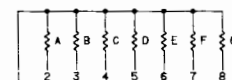
**Used on Series Nos. 1819

† Resistor removed on Series No. 1945

If PCA is used in Select Code 17 of the computer mainframe,
reinstall 150 ohm resistor in R1 slot located next to U24.



1. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R2, R3, R6, R7, R12

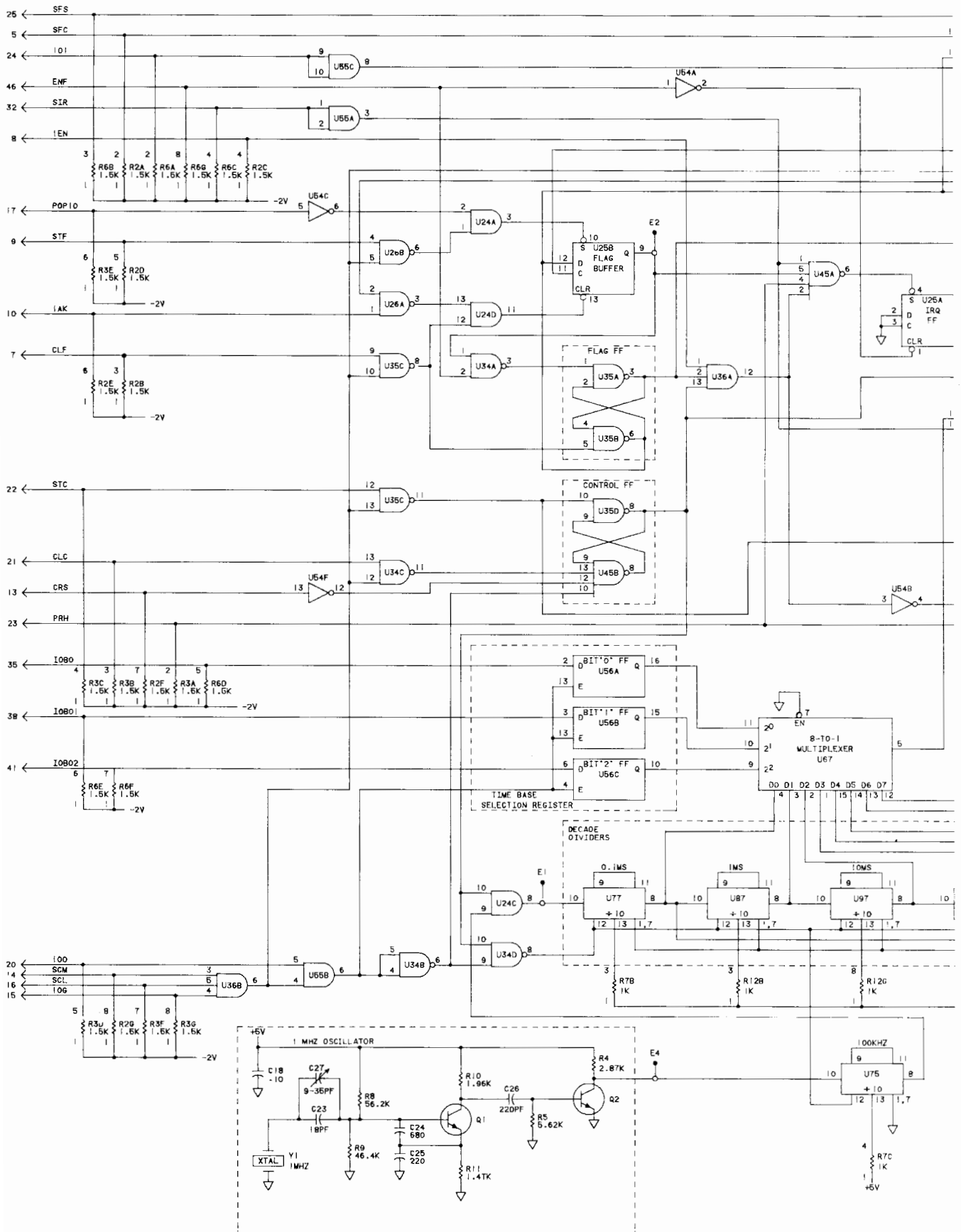


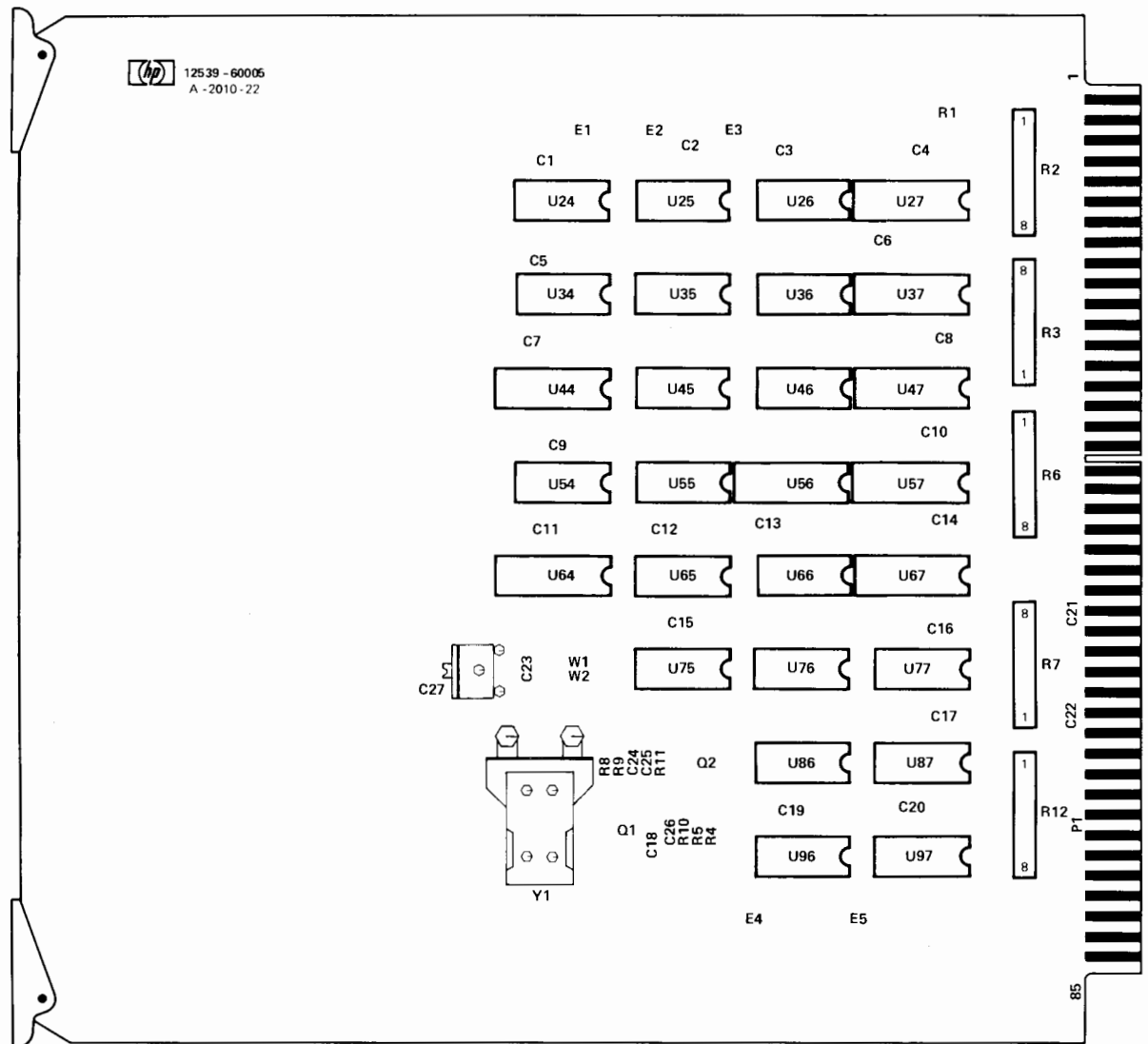
2. JUMPER W2 POSITION B IS USED ONLY DURING TESTING

3. ALL RESISTANCE VALUES ARE EXPRESSED IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS

Figure 4-3. Time Base Generator PCA Parts Location and Logic Diagrams (PN 12539-60005)

TIME BASE GENERATOR (12539-60005) SERIES 2010





REPLACEABLE PARTS

SECTION

V

5-1. INTRODUCTION

5-2. This section provides information for ordering replacement parts for the HP 12539C Time Base Generator Interface Kit. Table 5-1 (table 5-2 for PN 12539-60005) is a numerical listing of all replaceable parts in the interface kit.

5-3. A time base generator PCA parts location diagram is provided in section IV of this manual.

5-4. Figure 4-2 and 5-1 (figure 4-3 and 5-2 PN 12539-60005) list the following information for each replaceable part:

- a. Reference designation of the part (figure 4-2 or 4-3). Refer to table 5-4 for an explanation of the designations used in the REFERENCE DESIGNATION column.
- b. Hewlett-Packard part number.
- c. Description of the part. (Refer to table 5-4 for an explanation of the abbreviations used in the DESCRIPTION column.)

- d. A five digit code that corresponds to the manufacturer of the part. (Refer to table 5-3 for the code list of manufacturers.)
- e. Manufacturers part number.

5-5. ORDERING INFORMATION

5-6. To order replacement parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office. Refer to the list at the back of this manual for addresses. Specify the following information for each part ordered:

- a. Identification of the kit or assembly containing the part (refer to paragraphs 1-8 through 1-10).
- b. Hewlett-Packard part number for each part.
- c. Description of each part.
- d. Circuit reference designation for each part (if applicable).



| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|------------------------------------|----------|-----------------|
| #1 | 125R-0124 | 7 | 2 | PIN=PROGRAMING DUMPER ,30 CONTACT | 91506 | 8136-475G1 |
| #2 | 125R-0124 | 7 | | PIN=PROGRAMING DUMPER ,30 CONTACT | 91506 | 8136-475G1 |
| XW1 | 1200-0455 | 6 | 1 | SOCKET=IC 8=CONT DIP=SLDH | 28480 | 1200-0455 |
| Y1 | 0410-0478 | 7 | 1 | CRYSTAL=QUARTZ 1.000 MHZ | 28480 | 0410-0478 |
| | 1200-0484 | 1 | 1 | SOCKET=XTAL 2=CONT HC=6/U DIP=SLDR | 28480 | 1200-0484 |
| | 1480-0116 | 8 | 2 | PIN=GRV ,062-IN=DIA ,25-IN=LG STL | 28480 | 1480-0116 |

Table 5-3. Code List of Manufacturers

| The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements. | | | | | |
|--|----------------------------------|-------------------|----------|------------------------------------|------------------|
| CODE NO. | MANUFACTURER | ADDRESS | CODE NO. | MANUFACTURER | ADDRESS |
| 01295 | Texas Instr Inc Semicond. | | 28480 | Hewlett-Packard Co. | |
| | CMPNT Div. | Dallas, TX | | Corporate Headquarters | Palo Alto, CA |
| 04713 | Motorola Semiconductor | | 52763 | Stettner-Trush Inc. | Cazenovia, NY |
| | Products | Phoenix, AZ | 56289 | Sprague Electric Co. | North Adams, MA |
| 07263 | Fairchild Camera & Instr. Corp., | | 72136 | Electro Motive Mfg. Co., Inc. | Willimantic, CT |
| | Semiconductor Div. | Mountain View, CA | 80131 | Electronic Industries Assoc. | |
| 18324 | Signetics Corp | Sunnyvale, CA | | Any brand part meeting | |
| 24546 | Corning Glass (Bradford) | Bradford, PA | | EIA Standards | Washington, D.C. |
| | | | 91506 | Augat Inc | Attleboro, MA |

Table 5-4. Reference Designations and Abbreviations

| REFERENCE DESIGNATIONS | | |
|--|--|--|
| A = assembly B = motor, synchro BT = battery C = capacitor CB = circuit breaker CR = diode DL = delay line DS = indicator E = Misc electrical parts F = fuse FL = filter J = receptacle connector | K = relay L = inductor M = meter P = plug connector Q = semiconductor device other than diode or integrated circuit R = resistor RT = thermistor S = switch T = transformer | TB = terminal board TP = test point U = integrated circuit, non-repairable assembly V = vacuum tube, photocell, etc. VR = voltage regulator W = jumper wire X = socket Y = crystal Z = tuned cavity, network |
| ABBREVIATIONS | | |
| A = amperes ac = alternating current Ag = silver Al = aluminum ar = as required adj = adjust assy = assembly b = base bp = bandpass bpi = bits per inch blk = black blu = blue brn = brown brs = brass Btu = British thermal unit Be Cu = beryllium copper cpi = characters per inch coll = collector cw = clockwise ccw = counterclockwise cer = ceramic com = common crt = cathode-ray tube CTL = complementary-transistor logic cath = cathode Cd pl = cadmium plate comp = composition conn = connector compl = complete dc = direct current dr = drive DTL = diode-transistor logic depc = deposited carbon dpdt = double-pole, double-throw dpst = double-pole, single-throw em = emitter ECL = emitter-coupled logic ext = external encap = encapsulated elctlt = electrolytic F = farads FF = flip-flop flh = flat head flm = film fxd = fixed filh = fillister head G = giga (10^9) Ge = germanium gl = glass gnd = ground(ed) | gra = gray grn = green H = henries Hg = mercury hr = hour(s) Hz = hertz hdw = hardware hex = hexagon, hexagonal ID = inside diameter IF = intermediate frequency in. = inch, inches I/O = input/output int = internal incl = include(s) insul = insulation, insulated impgrg = impregnated incand = incandescent ips = inches per second k = kilo (10^3), kilohm lp = low pass m = milli (10^{-3}) M = mega (10^6), megohm My = Mylar mfr = manufacturer mom = momentary mtg = mounting misc = miscellaneous met. ox. = metal oxide mintr = miniature n = nano (10^{-9}) nc = normally closed or no connection Ne = neon no. = number n.o. = normally open np = nickel plated NPN = negative-positive-negative NPO = negative-positive zero (zero temperature coefficient) NSR = not separately replaceable NRFR = not recommended for field replacement OD = outside diameter OBD = order by description orn = orange ovh = oval head oxd = oxide p = pico (10^{-12}) PC = printed circuit | PCA = printed-circuit assembly PWB = printed-wiring board phh = phillips head pk = peak p-p = peak-to-peak pt = point prv = peak inverse voltage PNP = positive-negative-positive pwv = peak working voltage porc = porcelain posn = position(s) pozi = pozidrive rf = radio frequency rdh = round head rms = root-mean-square rww = reverse working voltage rect = rectifier r/min = revolutions per minute RTL = resistor-transistor logic s = second SB, TT = slow blow Se = selenium Si = silicon scr = silicon controlled rectifier sst = stainless steel stl = steel spcl = special spdt = single-pole, double-throw spst = single-pole, single-throw Ta = tantalum td = time delay Ti = titanium tgl = toggle thd = thread tol = tolerance TTL = transistor transistor logic U(μ) = micro (10^{-6}) V = volt(s) var = variable vio = violet Vdcw = direct current working volts W = watts ww = wirewound wht = white WIV = working inverse voltage yel = yellow |

READER COMMENT SHEET

OPERATING AND SERVICE MANUAL

12539C TIME BASE GENERATOR

INTERFACE KIT

PART NO. 12539-90008

AUG 1980

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