HP 1000 Computer Systems

HP 12040C
Eight-Channel Asynchronous Multiplexer Subsystem

Installation and Reference Manual

Card Assembly: 12040-60014

HEWLETT PACKARD

HEWLETT-PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

Update 1 (March 1988)
Manual Part No. 12040-90023
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12040-90023

First Edition ..... March 1986

Contents

Contents (continued)

Contents (continued)

Safety Considerations

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols

Instruction manual symbol: The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Servicing

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

General

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends on the type of material. Insulators can easily build up charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields.

The resulting damage can range from complete destruction to latent degradation. Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The PSI card is shipped in a transparent static shielding bag. The card should be kept in this bag at all times until it is installed in the system. Save this bag for storing or transporting the card. When installing the card in the system, do not touch any components. Hold the card only by its edges or extractor levers.

WARNING

SAFETY EARTH GROUND - The computer on which this product is installed is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety ground must be provided from the main source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and must be secured against any unintended operation.

Chapter 1
GENERAL INFORMATION

INTRODUCTION

This chapter describes the HP 12040C 8-Channel Asynchronous Multiplexer Subsystem (MUX) and associated RS-232-C panel. Related documentation and software part numbers are listed, and the multiplexer subsystem specifications are given.

GENERAL DESCRIPTION

The HP 12040C 8-Channel Asynchronous Multiplexer Interface and the RS-232-C Panel provide a complete HP 1000 A-Series hardware package for multiplexed terminal/device applications. These applications include communications to and from all currently supported HP terminals as well as line printer support for the HP 2631A, HP 2635A, and HP 7310A printers.

Other HP or non-HP devices may be used in conjunction with the multiplexer subsystem; it may be necessary, however, for you to write simple device drivers to supply the necessary control for certain devices. Consult the appropriate RTE Driver Reference Manuals for detailed information regarding user-written device drivers.

Hardware Operation

The HP 12040C 8-Channel Asynchronous Multiplexer Interface provides a method for interfacing HP 1000 Computers (using the A-Series backplane) to any RS-423 or RS-232-C compatible device. The interface supports hardwired or passive full-duplex modem connections in a point-to-point environment. Additionally, the 12040C supports active modems when connected through the HP 37214A modem card cage.

Device communication to and from the host system is provided through a microprocessor-based interface. An on-board Z-80A microprocessor, in conjunction with EPROM, RAM, DMA, and SIO support, manages the asynchronous TTY-like protocol of connected devices. Each of the eight channels is separately buffered (input and output). All backplane communications to and from the host are handled by the A-Series I/O Master.

In conjunction with RTE-A (A-Series processors only), port 0 on the 12040C can be selected to operate in the Virtual Control Panel (VCP) mode. In this mode, the terminal connected to port 0 can access and modify CPU registers and memory. VCP mode is further discussed in the RTE-A Operator's Guide.

Each MUX interface contains two on-board programmable baud rate generators (BRG's) which provide channel transmission speeds from 50 to 19.2K Baud. The flexibility in the multiplexer interface is enhanced by the ability to simultaneously distribute up to five different baud rates to external devices. The total aggregate throughput capability of the interface is processor and process dependent.

MUX Software

The HP 12040C Multiplexer Subsystem (hardware and software) operates in HP 1000 A-Series Processors/Systems in conjunction with the RTE-A operating system. Program development and program execution are supported on these systems.

The supporting software for the HP 12040C interface consists of an interface driver (1DM00) and two standard device drivers (DD.00 and DD.20). The interface driver manages the communications across the CPU backplane to and from the multiplexer interface printed circuit assembly (PCA). The device drivers perform the formatting of control and data strings (specifically, the inclusion of control characters) for external device requirements.

Flexibility is a key feature in the device software area of RTE. Customers may write their own device drivers to interface to other devices such as terminals, plotters, and "black boxes" that meet the RS-423-A or RS-232-C requirements.

MUX Panel and Custom Cabling

Up to eight terminals or devices can be connected to a single multiplexer interface through the RS-232-C Panel provided with the standard 12040C. Options to the product allow customers to construct a custom cabling scheme.

Virtually any number of interfaces will be supported in the operating system, up to the maximum number of available I/O slots. Future expansion can be built in at system generation time by allowing reserved slots for devices to be added as the need arises.

Since the MUX interface supports the standard RS-423-A electrical interface specifications (also compatible with RS-232-C), the RS-232-C Panel may be located at the CPU or up to 300 feet (91 meters) away from the main CPU (supported at channel speeds $\leq$ 9600 baud).

Devices may then be connected to the panel through EIA-standard 25-pin connectors on the panel. This remote location of the panel overcomes the typical 50-foot (15 meter) limitation imposed by RS-232-C specifications. Additionally, hardwired full-duplex modems may be employed on a channel-by-channel basis. No active modem control lines to or from the MUX interface are provided. However, this limitation is easily overcome by the use of the HP 32714A Modem Card Cage. The HP 32714A is a rack-mountable card cage containing a microprocessor-based modem control card and seven I/O slots.

EQUIPMENT SUPPLIED

Equipment supplied with the standard HP 12040C Multiplexer interface product is listed here:

DESCRIPTION	HP PART NUMBER
A-Series Multiplexer Interface	12040-60014
(Includes Firmware EPROM)	5180-7228
RS-232-C Panel	28658-60005
Cable, Card to RS-232-C Panel	28658-63005
Connector Kit for custom cables	1252-0508
Mounting Bracket, 19-inch rack	5001-5278
This manual	(see cover for part number)

Options

The following options are available:

Option 002: HP 37214A Interface. This option deletes the RS-232-C panel and the panel cable (part number 28658-63005). A 3-meter cable (part number 12828-60002) is substituted for the standard cable for connection to the HP 37214A Modem Card Cage.

Option 003: Custom Cable Option. The 28658-63005 cable is deleted, and an 80-pin card-edge connector kit (part number 8120- 4039) is added, allowing customers to fabricate their own cables.

ASSOCIATED SOFTWARE AND DOCUMENTATION

Software

- %IDM00 MUX Interface Driver (REV 2301) 12040-16002
- %DD.00 26XX Screen Device Driver 92071-16083
- %DD.20 264X Mini Cartridge Driver 92071-16084

Offline Downloadable Diagnostic

Offline downloadable diagnostics in various forms are available as part of the HP 24612A product (for A-Series systems) and the HP 23398B (A-Series) products.

Documentation

- Multiplexer Interface Installation and Reference Manual (This book)
- Driver Reference Manual for your operating system
- Performance Note for the HP 12040C Multiplexer (12040-90021)

IDENTIFICATION

MUX Interface

The MUX interface is identified by a ten-digit part number located near the HP logo.

PCA revisions are identified by a letter and a four-digit data code (e.g., A-2910). This designation is stamped below the part number. The letter identifies the revision of the etched trace pattern on the unloaded PCA. The four-digit date code refers to the electrical characteristics of the card with components mounted.

If the date code stamped on your MUX interface does not agree with the date code printed on the front page of this manual, there are differences between your interface and the interface described in this manual. These differences are described in manual supplements available through the nearest Hewlett-Packard Sales and Service Office. Offices are listed at the back of this manual.

Documentation

The manual supplied with the MUX card is identified by its name, part number, and print date. The part number and print date are printed on the title page. If the manual is revised, the publication date is changed. The Print History page (page iii) records the reprint dates.

MULTIPLEXER INTERFACE SPECIFICATIONS

The HP 12040C is a standard-size, A-Series I/O interface occupying one slot in the HP 1000 A-Series I/O backplane:

Physical Specifications

SIZE:

289 mm (11.38 inches) long
172 mm (6.75 inches) wide
1.6 mm (0.063 inch) thick

10.2 mm (0.4 inch) top-of-board clearance
5.1 mm (0.2 inch) beneath-board clearance

BACKPLANE INTERCONNECTS: Two 50-pin edge connectors which plug into two sockets (P1 and P2) mounted on the A-Series I/O backplane.

DEVICE INTERCONNECTS: One 80-pin edge connector on which a cable hood or connector may be placed for connection to any one or all of eight I/O devices.

Electrical Specifications

TRANSMISSION MODE: Bit serial, Asynchronous.

CAPACITY: Eight full-duplex (transmit and receive) communication channels with two 254-byte transmit buffers and two 254-byte receive buffers per channel.

PROGRAMMABLE FEATURES: Echo on or off; break key detection; record termination processing (CR, DC2, RS, control-D, end on count, or host-initiated termination); buffer overflow detection; baud rates from 50 to 19.2K; on-board editing (back space, line delete); selectable ENQ/ACK or XON/XOFF handshake compatibility; VCP mode capability; active modem support through HP 37214A Modem Card Cage.

INTERFACE LEVEL: Conforms to EIA Standards (RS-423-A/RS-232-C and CCITT V.24). Distance limited to 300 feet (91 meters).

CHARACTER LENGTH: Programmable character length at 5, 6, 7, or 8 bits per character with programmable (1, 1-1/2, or 2) stop bits.

DATA TRANSFER RATES: Two baud rate generators (BRG's) programmable from 50 to 19,200 baud. Each BRG can provide a single baud rate of 19.2K, 1800, 134.5, 110, or 50 baud; or it can provide multiple rates of 75 & 150, or 300 & 1200, or 2400, 4800, & 9600 baud simultaneously.

AGGREGATE THROUGHPUT CAPACITY: 76,800 bits per-second per interface (8 channels at 9600 bits per second). The aggregate throughput rate is attainable for short bursts. For continuous throughput, either the baud rate or the number of channels must be reduced to avoid data loss on input. There will be no data loss on output, but the full data rate may not be achieved.

ERROR DETECTION: Parity (even/odd/none), overrun, and framing error detection.

POWER REQUIREMENTS:

```
+ 5 VOLTS  @  2.5  AMPERES
+12 VOLTS  @  0.10 AMPERES
-12 VOLTS  @  0.05 AMPERES

Total Power Dissipation = 14.3 WATTS
```

Environmental Specifications

OPERATING TEMPERATURE RANGE: 0 TO 55 Degrees Celsius

Chapter 2
INSTALLATION

INTRODUCTION

This chapter contains information which is necessary to install the HP 12040C Multiplexer hardware. The following information is included:

- Calculation of Available Current vs Required Current
- Preparation Before Installation and Use
- Installation and Check-out of the Interface and Cable
- Reshipment for Repairs or Damage

CAUTION

SOME OF THE COMPONENTS USED IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

PREPARATION FOR USE

Available vs. Required Current

The HP 12040C MUX interface obtains its operating voltages from the host computer power supply. The MUX interface is designed to be inserted into the I/O card cage and backplane (rear of the computer) where it receives operating voltages and also becomes part of the I/O data and control bus structure. Since all items installed in the computer obtain their operating power from the computer power supply, a calculation should be performed to determine whether the MUX interface, when installed in your present system, will cause a current overload.

CAUTION

These calculations should be made before installing the MUX interface.

To do this, you must get and add all of the current requirements for each interface/product installed in the computer. The total current requirements should then be compared with the available current for each supplied voltage. The MUX interface power/current requirements are listed in Chapter 1.

If the additional multiplexer current overloads the host computer power supply, the MUX card should not be installed until alternative arrangements have been made to provide the required current.

Proper Firmware (EPROM) Installation

The HP 12040C product comes with a factory-installed firmware EPROM and the required jumpers. Ensure that the EPROM has not been damaged or loosened from its socket during shipping.

EPROM Jumper Configuration

Verify the correct EPROM jumper configuration. Figure 2-1 illustrates the location of the jumpers. Jumpers W4 and W7 should be installed.

CABLING

Connection to External Devices

The connection between the MUX card and external devices can be made in a variety of ways. The basic factors governing these connections are considered in the following paragraphs.

The HP 12040C MUX card follows the RS-423-A standard. This means that the cable connecting the MUX card to remote devices can be up to 300 feet (91 meters) long. That cable contains Send Data and Receive Data wire pairs for each of the eight multiplexed channels, as well as shield and power wires. The remote devices connected to the MUX card can be:

1. The RS-232-C panel. This panel provides RS-232-C connections for eight devices, typically terminals, printers, and hardwired full-duplex modems. Each cable connecting a device to the RS-232-C panel can be up to 50 feet (15 meters) long.

OR

2. The HP 37214A modem card cage. This card cage allows connection to RS-232-C devices (via terminal interface card), to modems (via modem interface card), and to telephone lines (via modem card). Up to seven devices can be connected through the modem card cage. The modem card cage is typically racked in the same cabinet as the host computer.

OR

3. Up to eight I/O devices, such as terminals and printers, that comply with the RS-423-A standard.

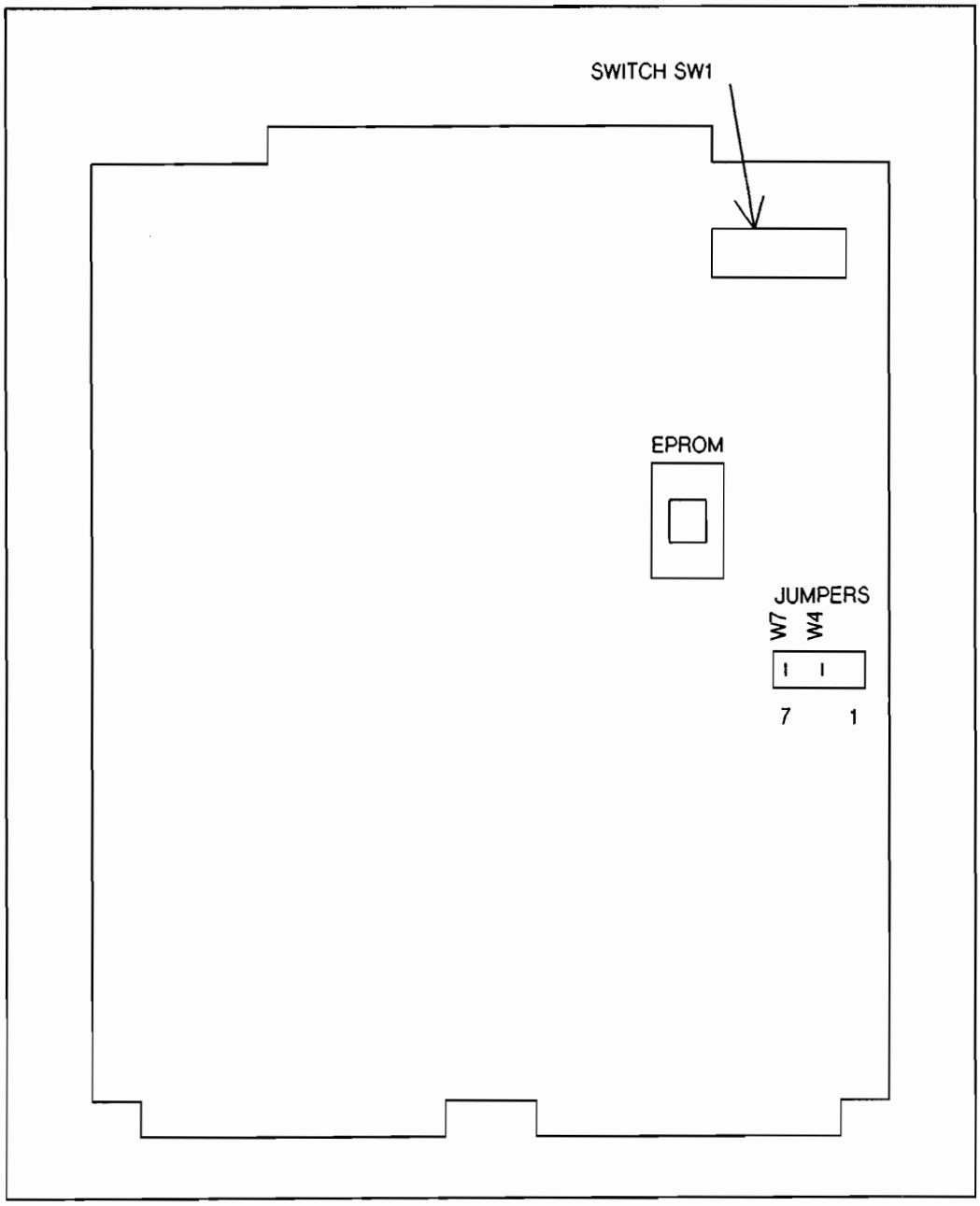


Figure 2-1. EPROM and Jumper Locations

The standard and optional equipment supplied with the HP 12040C is listed in Chapter 1.

Figure 2-2 shows typical cabling for the HP 12040C. (The terminals shown in the figure could actually be terminals, printers, or other appropriate devices. These devices will vary according to whether the connection is to an RS-232-C panel, to a modem card cage, or directly to the MUX card.)

Wiring diagrams for the cables mentioned above are contained in Section 4 of this manual.

Data Transmission Rate Wiring

The multiplexer interface uses two timers of a Z-80A CTC (Counter/Timer Circuit) to act as Baud Rate Generators (BRG0 and BRG1). Each port must be connected to either BRG0 or BRG1. This connection is made by wiring the MUX connector hood. (Details for this wiring are given in chapter 4 of this manual.) The standard HP 12040C comes wired from the factory with BRG0 connected to port 0 and BRG1 connected to ports 1 through 7. The 12040C Option 002 cable (HP 37214A interface) comes with the connector hood wired with BRG0 tied to port 0 and BRG1 tied to ports 1 through 7. This distribution can be modified to suit the application.

The host's software interface driver allows the user to programmatically set the rate of each BRG. Driver interaction also allows the user to select from a group of baud rates in certain ranges. The procedure for programming multiplexer data rates is discussed in the Driver Reference Manual for your particular system. The following data rates can be programmed: 19.2K, 9600, 4800, 2400, 1800, 1200, 300, 150, 134.5, 110, 75, and 50 baud.

For a number of baud rates (19.2K, 1800, 134.5, 110, or 50 baud), only one baud rate at a time is available to the ports connected to a given BRG. The remainder of the baud rates are available in groups:

Baud Rate Groups

Group 1	Group 2	Group 3
75	300	2400
150	1200	4800
		9600

If a baud rate from one of these groups is selected, any rate in that group can be supplied to any port connected to that BRG. Thus, up to five different baud rates can be supplied to the ports at one time.

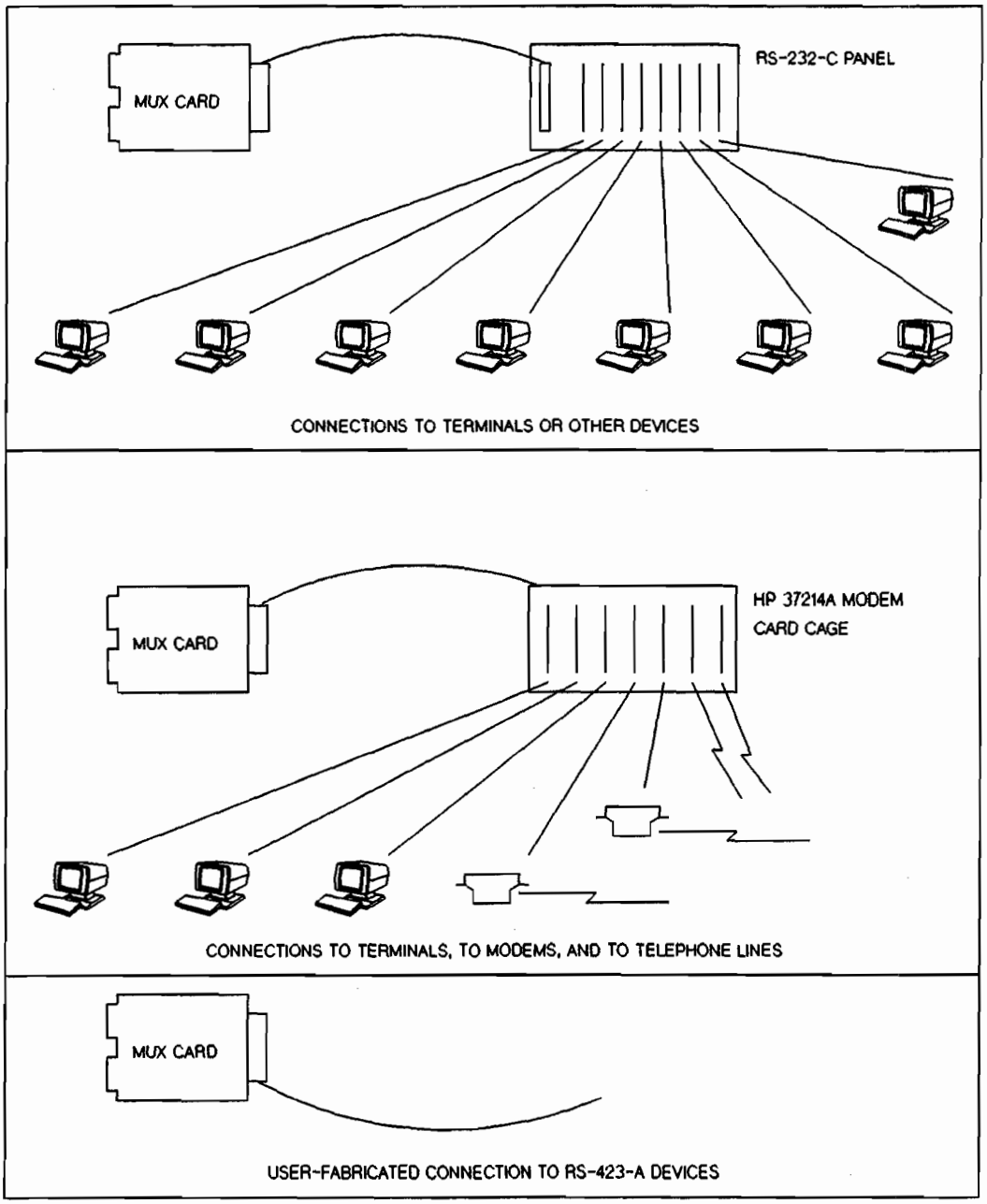


Figure 2-2. Connections to the HP 12040C MUX Card

On power-up, BRG0 and BRG1 are set to 9600 baud. However, many baud-rate combinations are possible. The following examples show just two of the many possible baud rate combinations. Example 1 would be useful for a configuration with one printer (1200 baud) and seven terminals (9600 baud). Example 2 would be useful for a configuration with printers (300 and 1200 baud), modems and line drivers (1200, 2400, and 4800 baud), and terminals (9600 baud).

	Example 1		Example 2	
Port NUMBER	Data BRG	Rate	Data BRG	Rate
Port 0	0	1200	0	300
Port 1	1	9600	0	1200
Port 2	1	9600	0	1200
Port 3	1	9600	1	2400
Port 4	1	9600	1	2400
Port 5	1	9600	1	4800
Port 6	1	9600	1	9600
Port 7	1	9600	1	9600

Switch Selectable Options

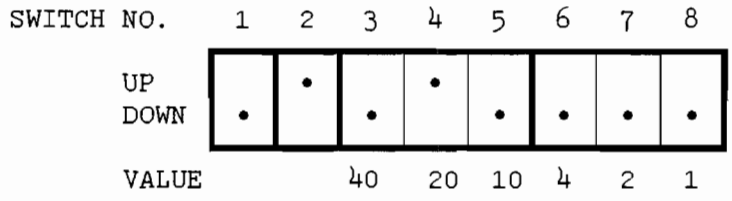
The MUX select code and VCP enabling are controlled by the settings of switch SW1. SW1 is an 8-segment DIP (Dual-Inline-Package) switch, located to the left of the frontplane edge connector (see figure 2-1). A switch in the UP position is OPEN and represents a logic one. A switch in the DOWN position is CLOSED and represents a logic zero. The meanings of the switches are explained in the next few paragraphs.

SW1S1 controls whether port 0 on the MUX interface is used as the virtual control panel (VCP) of an A-Series computer. If SW1S1 is DOWN, port zero is ENABLED as the VCP; if SW1S1 is UP, port 0 is DISABLED as the VCP. (Note that enabling the MUX for VCP is valid only on an A-Series computer.)

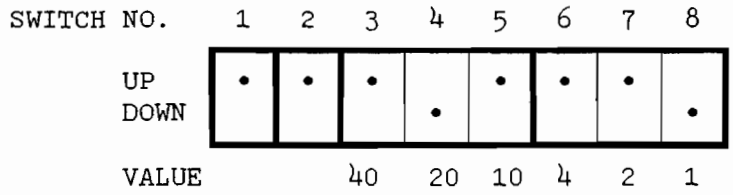
SW1S2 is not used and should be left in the UP (OPEN) position.

Switches SW1S3 through SW1S8 are used to identify the interface select code in octal. Switch 3 selects the most significant bit and switch 8 selects the least significant bit of the six bit select code. All interface cards in the system must have different select codes.

EXAMPLE NUMBER 1: The following switch settings enable VCP and set the select code to 20 (octal). Note that switch 2 is not used and is therefore set open (up).



EXAMPLE NUMBER 2: This switch configuration disables VCP and sets the select code to 56 (octal).



INSTALLATION

Installing the Interface PCA

Before continuing with the actual installation of the interface PCA, make sure that you have reviewed and completed the preparation tasks that have been previously outlined in this section, such as setting the select code switches, checking the location of the jumpers, etc.

CAUTION

Always turn off line power to the computer before installing or removing an interface card and associated cabling. Failure to do so may result in damage to the interface or the attached I/O device.

All cards must be inserted with the component side toward the TOP of an L-Series CPU cabinet, or the right side of an A-Series card cage. When installing the interface, carefully insert the card until it touches the I/O Backplane connectors, then firmly press the card into place.

Install the interface in the desired I/O slot of the computer card cage. Note the location of the card in the backplane; the interrupting and DMA priority of the interface is determined by its location in the card cage.

Installing the RS-232-C Panel

Install the RS-232-C panel as follows:

1. Mount the panel in the mounting bracket (part number 5001-5278) using the two screws provided.

2. Mount the bracket on the rear of the computer rack (the bracket can be mounted on other than the computer rack if a special cable is fabricated to reach from the PCA to the panel).

Installing the Cables

Connect the panel cable, part number 28658-63005, from the interface PCA to the 50-pin connector on the RS-232-C panel. (If a special cable was fabricated, mount this cable.) Connect cables from all peripherals to the RS-232-C panel.

After connecting the desired peripherals to the RS-232-C panel or user-fabricated cabling, power may be restored to the computer system.

MULTIPLEXER CHECK-OUT

Proper operation of the MUX interface and cabling can be assured by performing the verification procedures described in Chapter 5 of this manual.

RESHIPMENT

If any item of the HP 12040C Multiplexer Interface is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for reshipment. Include the part number of the item being shipped.

Pack the item in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

Chapter 3
THEORY OF OPERATION

INTRODUCTION

This chapter contains the following information:

- A description of the host computer I/O backplane interface.
- A brief description of the Z-80A CPU and support chips.
- Descriptions of the principal command and status words.
- A functional-level description of the interface operation.

HARDWARE DESCRIPTION

The HP 12040C Eight-Channel Multiplexer Interface can be described as having following functional areas:

- A-Series Computer I/O backplane interface (I/O master)
- Z-80A Microprocessor family subsystem (CPU, SIO, DMA and CTC)
- Read-Only Memory (ROM)
- Random-Access Memory (RAM)
- Communication line interface

A block diagram illustrating the major functional areas of the MUX interface is presented in Figure 3-1. For specific chip locations, refer to the schematics in Chapter 6.

HOST COMPUTER I/O BACKPLANE CIRCUITS

I/O Backplane Interface

The MUX interface communicates with the HP 1000 A-Series Computer through the I/O Master circuitry. The I/O Master provides the interface card with the capability of handling its own memory access (DMA) and decoding its own instructions from the centeral processing unit (CPU). This I/O Master, including the IOP (Input/Output Processor) chip, is located on the interface card and performs all functions (including instruction recognition and DMA control) necessary for interfacing with the A-Series backplane. For a detailed discussion of the I/O Master, refer to the HP 1000 A-Series Computer I/O Interfacing Guide, HP part number 02103-90005.

Timing

Counter U67 receives a 14.7456 MHz clock from the CPU, and in turn, provides the multiplexer with the following clocks: 7.373 MHz to the FPLA (Field Programmable Logic Array), 3.686 MHz to the Z-80 chips, 1.843 MHz to the DMA Pacer, and an overflow bit for the Reset logic.

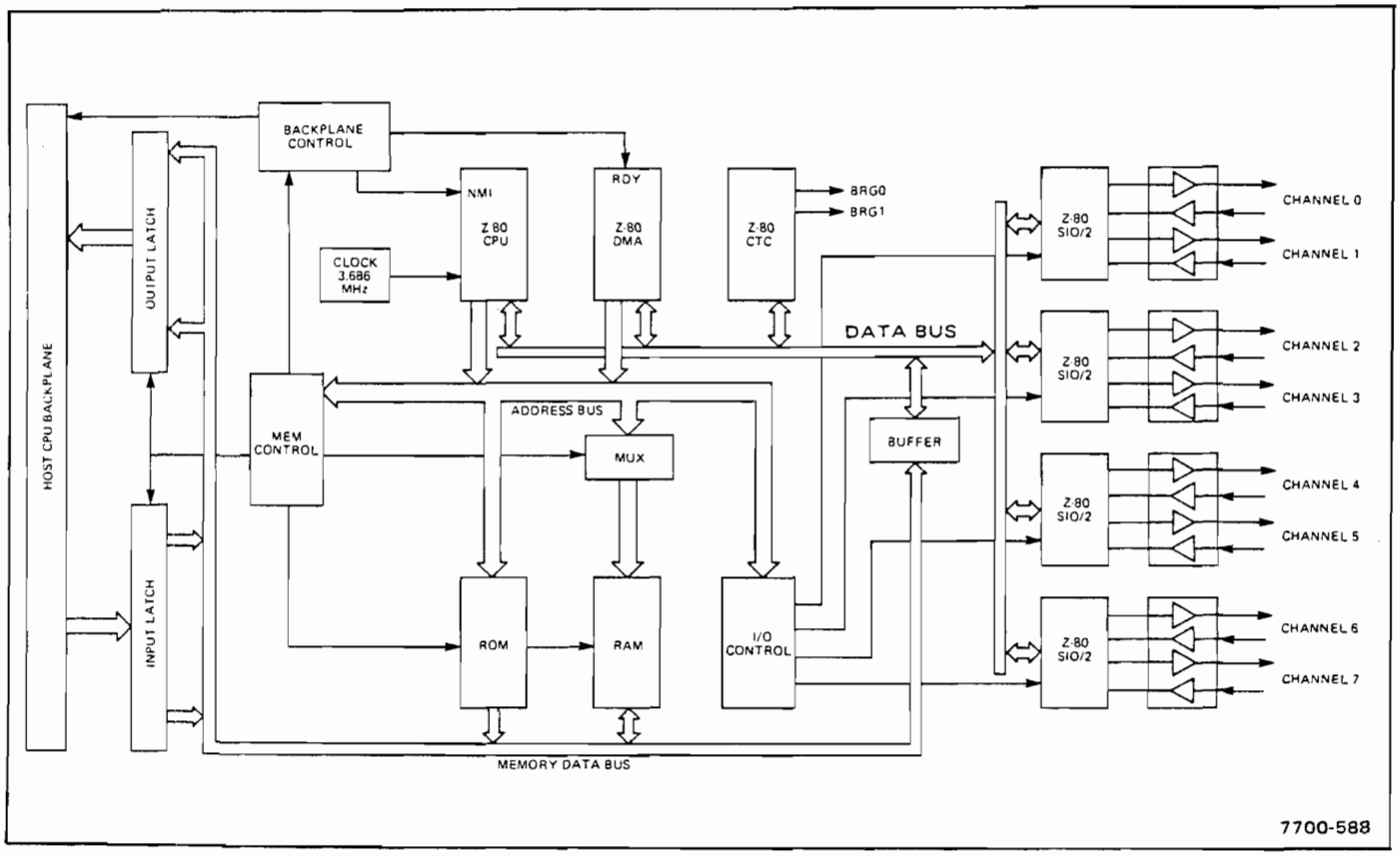


Figure 3-1. MUX Interface Functional Block Diagram

Multiplexer and Backplane Control Circuits

The primary function of the control circuitry is to generate and acknowledge interrupts and synchronize data transfers between the host and the interface.

Select Code

A six-bit select code for the interface is set by a DIP switch (SW1) located on the interface. This select code is used only as a means of addressing the card and bears no relation to the interrupt and DMA priority of the interface. Interrupt and DMA priority are determined solely by the physical location of the interface in the card cage. Setting the select code is described in Chapter 2.

THE Z-80 MICROPROCESSOR SUBSYTEM

This chapter contains a brief description of the Z80 subsystem. Additional information is available in technical manuals from either the Zilog Corporation or MOSTEK Corporation.

Central Processing Unit (CPU)

The heart of the interface is the Z-80A CPU (Central Processing Unit) which operates from a single 5 volt supply, uses a single-phase clock and has a typical instruction execution time of 1.0 microsecond. The Z-80A employs a data bus width of eight bits and an address bus width of 16 bits. All Z-80A CPU inputs and outputs are TTL compatible. The Z-80A CPU employs a register-based architecture that includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the MUX interface to function as a preprocessor to relieve the host computer of a majority of the protocol processing.

An important input function on the Z-80A as far as the MUX interface is concerned is the NMI (Non-Maskable Interrupt) input. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A. An NMI is the highest priority interrupt to the Z-80A and forces it to start fetching and executing instructions from a predetermined location in the firmware. The MUX interface software driver (IDM00) executed by the host uses this feature to inform the interface that it requires service.

Various support chips are used in conjunction with the Z-80A CPU to facilitate interface operation as an intelligent communication multiplexer interface. These chips are discussed in the paragraphs that follow.

Two-Channel Serial Input/Output (SIO/2)

Four Z-80A SIO/2 chips are used on the interface to provide eight serial data communications channels, see figure 3-1. Each SIO/2 chip contains two Universal Synchronous-Asynchronous Receiver Transmitters (USART). The major functions performed by the SIO/2 chips are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data. In addition, break, parity, overrun and framing error detection are also provided by the SIO/2 chip.

As shown in the illustration, the SIO/2 chips share the Z-80A data bus with other Z-80A devices. The data bus allows the Z-80A CPU to transfer data to and from the SIO/2 chips. In addition, the CPU can read status from the SIO/2 status registers and configure the SIO/2 chips for a particular operation by writing to their control registers.

The SIO/2 chip interrupts the Z-80A CPU on an interrupt-per-character basis when transferring data to and from the communication line. In the transmit mode, the SIO/2 interrupts the CPU for the next character to be transmitted after the preceding character has been sent. In the receive mode, the CPU is interrupted each time the SIO/2 converts serial data into an 8-bit parallel data character. Three 1-byte buffer registers are implemented on the SIO/2 chip to prevent the CPU from missing data characters when it responds to interrupts by the SIO/2 in the receive mode.

Direct Memory Access (DMA)

The interface uses a Z-80A DMA chip which is an LSI Direct Memory Access controller. The sole task of the DMA logic is to transfer data directly between the MUX interface memory and the host computer via the data latches of the backplane interface circuitry. By operating synchronously with the IOP chip, the interface takes advantage of the A-Series I/O structure to accomplish the DMA transfers between the Main CPU memory and the MUX RAM as efficiently as possible. The DMA logic accomplishes this task by creating signal sequences that enable data transfers to and from the

host. The Z-80A CPU and A-Series CPU are free to execute other code while the data transfer is taking place, thus increasing the throughput rate of the interface.

The DMA chip is capable of taking control of the data and address buses to accomplish its data transfer tasks. Since the Z-80A CPU and the DMA cannot take control of the buses at the same time, the CPU is locked out (from using either bus) during DMA data transfers. The DMA chip is prevented from taking control of the buses for extended periods of time by a counter called a DMA pacer so that the CPU has a chance to monitor all events taking place on the interface. In this manner, data is not lost on the interface while a DMA transfer is in progress.

Counter Timer Circuit (CTC)

The MUX interface uses one Z-80A Counter Timer Circuit which provides four independent counter/timers. Two of the counter/timers are used as serial baud rate generators (BRG0 and BRG1). Another is used to maximize the effective throughput of the interface by controlling the frequency of DMA cycle stealing (this is called a DMA pacer) and the fourth counter/timer is used as a system timer to control the processing of certain events within the Z-80A subsystem.

The CTC interfaces to the Z-80A data bus to allow the CPU to send configuration control words to the CTC and to read the status of four counter/timers when the need arises.

BRG0 and BRG1 provide baud rates to the eight ports. Each port must be connected to a single baud rate generator, but the grouping of ports to either baud rate generator is arbitrary. The procedure for programming BRG0/BRG1 is discussed in the Driver Reference Manual for your particular system. Through a command word issued by the host software driver to the interface, a selected BRG is initialized with a specified baud rate. Thus, you would expect that only one baud rate at a time is available to the ports connected to the same BRG. This is true for baud rates of 19.2K, 1800, 134.5, 110, or 50 baud.

However, an additional parameter of the command word may be used to select a prescaler within the SIO chip which acts upon the signal received from the BRG. The prescaler redefines the baud rate such that data rates in any one of the groups listed below can be simultaneously provided from one BRG:

SIO PRESCALER		GROUP 1	GROUP 2	GROUP 3
X16	=	75	300	2400
X32	=	150		4800
X64	=		1200	9600

BRG0 and BRG1 are routed to the eight SIO/2 devices through wire jumpers on the communications cable connector. The maximum number of different baud rates available at any one time is five, utilizing the three clocks in GROUP 3 and the two clocks from either GROUPs 1 or 2.

MEMORY

Eraseable Programmable Read-Only Memory (EPROM)

The MUX interface employs 8K bytes of EPROM on one chip. All of the Z-80A software required to implement the backplane control and interactive functions for eight serial data communications channels is contained in this EPROM and is referred to as firmware. The power fail recovery and initialization routines are also contained in EPROM.

A set of jumpers on the MUX interface allow the use of different EPROM devices. Refer to Chapter 2, Installation, for the proper EPROM jumper configuration. The HP 12040C product is shipped from the factory with the EPROM jumpers properly installed for the factory-installed EPROM.

Random-Access Memory (RAM)

The MUX interface employs 16K bytes of dynamic RAM. This memory is used for data buffers (two 254-byte buffers for transmit and two 254-byte buffers for receive per channel) and the storage of firmware variables. The appropriate refresh signals are provided to the dynamic RAM devices by a combination of the refresh capability of the Z-80A CPU and a Field Programmable Logic Array (FPLA), U127, on the MUX interface. The FPLA operates as a state machine and also invokes WAIT states during reads from PROM and interrupt cycles, among others.

Communication Line Circuitry

The communication line circuitry refers to the receivers and drivers on the MUX interface that transmit and receive data to and from a terminal or user device over the communication line. The MUX interface communication line circuitry is capable of supporting the EIA RS-232-C, CCITT V.24 and EIA RS-423-A serial I/O standards. For the purposes of this discussion, the various communications circuits are referred to by their RS-423-A names. A comparison of EIA RS-232-C, CCITT V.24 and EIA RS-423-A circuits and their respective signal connector pin assignments are given in Section Four of this manual.

Section Four of this manual discusses serial interface standards and their relationship to various cabling options for the HP 12040C.

Command and Status Words

In addition to data words, command and status words are also exchanged between the host computer and the MUX interface. These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the interface. Command words are issued by the host to the interface and status words are sent by the interface to the host.

A brief description of the principal command and status words will prove helpful in understanding the functional level description given later in this section.

COMMAND WORDS. Command words are initiated by the host driver. Some examples of command words are as follows:

SET KEY - Intializes certain parameters for a particular channel such as baud rate, parity, number of stop bits, and the number of bits per character.

RESET - Causes a branch to the power-up routine within the interface firmware.

ENABLE UNSOLICITED INPUTS - Enables the MUX interface to send status inputs to the host without the host asking for them. This command must be issued to enable the MUX interface to interrupt the host.

DISABLE UNSOLICITED INPUTS - Disables status inputs from the MUX interface so that the host can initiate a transfer.

ACKNOWLEDGE - Host acknowledges an unsolicited status input from the MUX interface and requests any further information regarding the status input.

CANCEL ALL - Cancel all active receive buffers on an individual channel.

REQUEST WRITE - The host wishes to send data to a particular channel and requires information concerning the availability of transmit buffer space.

WRITE - The host is ready to send data to an individual channel.

SET READ CONFIGURATION - The host sets the read configuration parameters such as echo, edit (backspace) and record terminators (CR, RS, DC2, control-D or character count).

SET CHARACTER COUNT - The host specifies that a line of text will be terminated on a predetermined character count as opposed to an end-of-text (EOT) character.

READ - The host is ready to receive data from an individual channel.

STATUS WORDS. Status words are generated by the MUX interface to inform the host of events that have occurred or are occurring on the interface or communications line. Examples of these status words are as follows:

BREAK RECEIVED - The break key has been pressed on this particular channel.

BUFFER AVAILABLE - A transmit buffer is available for transmitting data to the terminal.

TEXT AVAILABLE - The MUX interface has received a line of text from an individual channel.

The MUX interface can send status inputs to the host only after the host has enabled unsolicited inputs. The host can, of course, ask for status from the card. This constitutes a solicited status input.

Communications Functional-Level Description

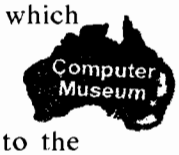
The description that follows typifies the transmit and receive operations of the MUX interface. The command and status words used in the description below were explained in the previous section and the various data paths and hardware groups referenced below are presented in the block diagram in figure 3-1.

Initially, the HP 1000 has been powered up and the communications line is not yet operational. The process of powering up the host resets the logic on the MUX interface.

Before either a transmit or a receive operation can take place between the host and the MUX interface, certain setup parameters for each channel are sent to the interface via a command word from the host. These parameters include baud rate, parity type, number of stop bits, number of bits per character and ENQ-ACK or XON/XOFF handshake select. Once these parameters are set for each operational channel, the transmit and receive operations may proceed.

Transactions initiated by the host driver begin with a DISABLE UNSOLICITED INPUTS command followed by a series of other commands which vary from task-to-task. This command sequence is terminated by an ENABLE UNSOLICITED INPUTS command. The MUX Interface initiates transactions by sending an unsolicited status input to the host. The host driver takes over at this point and sends an ACKNOWLEDGE and a series of commands. These transactions are terminated by the host sending an ENABLE UNSOLICITED INPUTS command.

The host sends a command to the MUX interface by writing data to the select code of the interface and executing an STC instruction. The STC instruction causes a Z-80A Non-Maskable Interrupt which then informs the interface to treat the data in its input latch as a command instead of data.



RECEIVE MODE. The steps involved in a "receive transfer" (i.e., a transfer from a terminal to the host computer) are as follows:

1. The host computer issues SET READ CONFIGURATION and, if required, SET CHARACTER COUNT commands to configure a particular channel for the request.

2. The host computer issues an ENABLE UNSOLICITED INPUTS command to the MUX interface.

3. Characters are transmitted one at a time from the terminal to the RAM buffer on the MUX interface via the SIO/2 chip which converts the serial data characters to parallel data for processing on the MUX interface and the host computer.

4. When the MUX interface has received an end-of-text character (or a predetermined number of characters) from the terminal, it informs the host of this event by writing a TEXT AVAILABLE status input message to the data latches and interrupting the host by setting the Flag flip-flop. The Host sends an ACK command and the MUX sends the control information and the data.

5. The host returns with a READ command and the line of text is transferred from the RAM buffer on the MUX interface to the output data latches via the DMA chip on the interface.

It should be noted that the Z-80A CPU is controlling all of the processing on the MUX interface by executing instructions that it fetches from EPROM. This allows the host computer, via the I/O Master, to communicate with eight separate devices in a multiplexed fashion.

TRANSMIT MODE. The steps involved in a "transmit transfer" (i.e., a transfer from the host computer to a terminal are as follows:

1. The host software driver issues a REQUEST WRITE command to the MUX interface to find out if buffer space is available for the transmission of data.

2. When a transmit buffer becomes available, the MUX interface sends a BUFFER AVAILABLE status word to the host.

3. The host sends a WRITE command to the MUX interface.

4. The text block is transferred from the host to a RAM buffer on the MUX interface allocated to this particular channel via the DMA chip on the interface. The interface firmware appends carriage-return/line-feed characters to the text (if enabled to do so).

5. The transmit buffer on the MUX interface is transferred to the terminal one character at a time after all previous data transmissions to that terminal have completed. The transfer of the text to the terminal involves the RAM and the SIO/2 chips on the interface. The SIO/2 chip requests each character by interrupting the Z-80A CPU. If enabled, ENQ/ACK handshake is performed every 80 characters.

Chapter 4
CABLING INFORMATION

INTRODUCTION

This chapter provides information to aid you in purchasing and fabricating cables for the HP 12040C Eight-Channel Multiplexer Interface. The following information is given in this chapter:

- A brief description of the RS-232-C and RS-423 serial interface standards.
- Cabling information for all MUX connections.
- Data transmission rate wiring.

SERIAL INTERFACE STANDARDS

The most widely used standard for interfacing data communications equipment to data terminal equipment is the RS-232-C standard issued in its original form by the Electronic Industries Association (EIA) in 1969. This standard defines a single-ended, bipolar (+/- 25 volts, maximum), unterminated circuit for serial data transmission rates of up to 20 kilobaud with a maximum line length of 15 meters (50 ft). Only one signal line is required per circuit. However, the simplicity of the RS-232-C interface has its drawbacks. The line length and bandwidth restrictions result from the fact that considerable crosstalk and radiated emissions are generated by this interface.

The EIA issued the RS-423 standard in 1976 to allow higher data signalling rates and longer line lengths than the RS-232-C standard. This interface standard is single-ended, bipolar (+/- 6 volts, maximum) and unterminated for backward compatibility with RS-232-C. Signalling rates vary from 3 kilobaud at a 1219 meter (4000 feet) line length to 300 kilobaud at 12 meters (40 feet). RS-423 differs from RS-232-C in that a balanced receiver is used which references the driver's ground, thus permitting a ground potential difference between the local environments in which the driver and the receiver reside. In addition, the Signal Ground, Send Common and Receive Common circuits of the RS-423 equipment are connected to the AB circuit of the RS-232-C equipment. The end result of these measures is a reduction in noise interference.

Satisfactory operation and backward compatibility of RS-232-C circuits with the RS-423 circuits is possible if certain electrical, functional, and mechanical provisions are made. These provisions include the following:

- The RS-423 receivers must withstand the maximum RS-232-C driver voltages of +/- 25 volts.
- The RS-423 driver waveshape must be compatible with the RS-232 risetime.
- The RS-423 load resistance should be equal to or greater than 3K ohms.
- All common returns should be connected together.
- Other differences between RS-232-C and RS-423 include:

  RS-232-C circuits that do not have equivalents in RS-423, and eight RS-423 circuits that do not have RS-232-C equivalents.

- RS-232-C devices typically use a 25-pin connector; RS-423 devices use a 37-pin connector.

Figure 4-1 illustrates the RS-423-to-RS-232-C conversion. The balanced receiver for each channel on the MUX interface is fed from a twisted pair containing a data transmission line, Receive Data (RD(A)), and a Receive Data common (RD(B)). The fact that the RD(A) line carries the actual data signal may be confusing, however the MUX interface design inverts this signal as it enters the interface for use with the Z-80A SIO subsystem. The non-differential signal drivers, Send Data (SDX) and a respective Signal Ground line (SGX) make up the transmit data twisted pair.

Since the MUX interface is designed to meet RS-423 standards, the aforementioned electrical and functional considerations are provided. The mechanical provisions such as connector compatibility and circuit wiring are your responsibility. The following paragraghs provide the information necessary to build or purchase custom cables (if need be) for proper MUX interface operation with either RS-232-C or RS-423 devices.

CABLING

Any one of the following three connections can be made to the HP 12040C MUX card:

1. Connection to one RS-232-C panel. Up to eight RS-232-C devices (terminals, printers, and hard-wired full duplex modems) can be connected to an RS-232-C panel.

2. Connection to one HP 37214 modem card cage. The modem card cage allows up to seven connections to terminals, to modems, or directly to telephone lines.

3. Direct connection to RS-423-A devices. Up to eight such devices (terminals, printers, modems, "black boxes", and so on) can be connected to a single HP 12040C MUX card.

These connections are described in the following paragraphs.

Connection to RS-232-C Panel

The standard HP 12040C product is designed for connection to user-supplied devices through the RS-232-C panel. The equipment supplied with the HP 12040C is listed in Section 1.

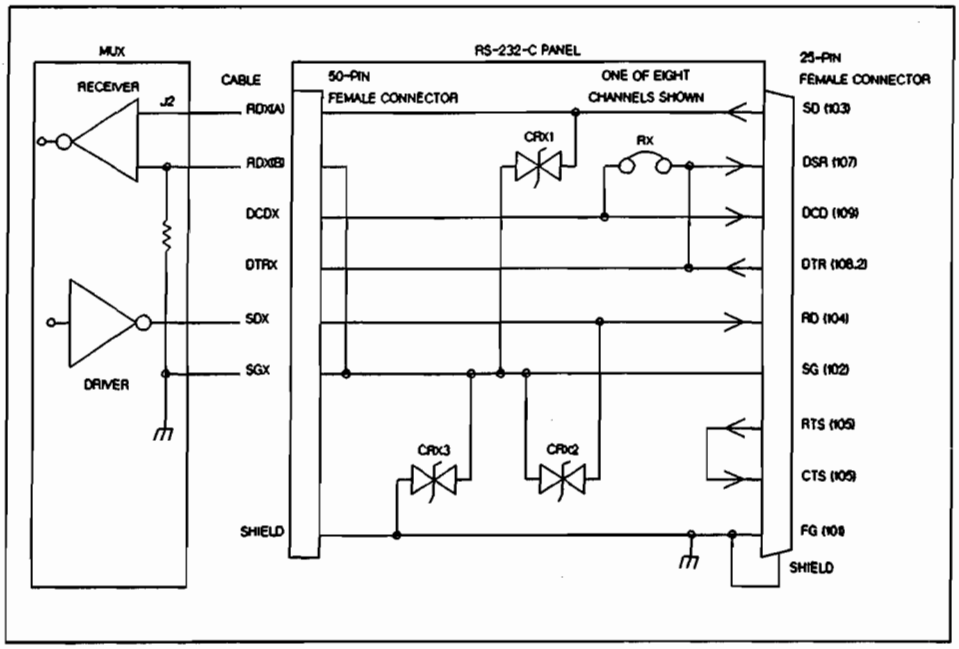


Figure 4-1. MUX Interface to RS-232-C Panel to Device Wiring

Connect the MUX card to the RS-232-C panel with the connecting cable (part number 28658-63005). (When you connect the hooded connector to the MUX card, make sure that the top of the connector (as indicated by right-side-up printing on the hood) goes to the top (component) side of the board. The connector will face the same way as all other connectors in the card cage.)

If the cable isn't long enough for your application, you can build an extension cable using the connector kit supplied. This extension cable goes between the 28658-63005 cable and the RS-232-C panel. The total cable length must not exceed 91 meters (300 feet).

The extension connector kit includes male and female connectors for the extension cable, as well as an insertion tool to aid in connecting the wires to the connector pins. The cable used for the extension is not supplied as part of the HP 12040C. You should use a shielded cable that contains 16 pairs of 24 AWG wire. The recommended cable is available from Hewlett-Packard as part number 8120-4039. Use a twisted pair for each Data/Dataground connection.

The male and female connectors of the extension cable are wired the same. For example, connect pin 1 of the male connector to pin 1 of the female connector, pin 3 to pin 3, pin 4 to pin 4, etc. (See table 6-3 in chapter 6 for pin connections.) Tie off unused pairs and cover them with a short length of heat-shrink tubing to prevent them from making contact with any of the other wires in the cable.

The RS-232-C panel is designed to convert the RS-423 standard, which originates at the MUX interface, to the RS-232-C standard, thus providing the backward compatibility needed for existing terminals and user I/O devices. Figure 4-1 illustrates the Panel-to-RS-232-C device connections. The Panel provides the necessary EIA RS-232-C Modem signal simulation (CA, CB, CC, CD, and CF) to be used if your terminals or devices require it. A device not requiring the extra protocol lines can operate sufficiently using the Transmitted Data (BA) and Received Data (BB) lines.

There are several ready-made cables available from Hewlett-Packard for connecting RS-232-C devices to the RS-232-C panel. Among these cables are:

Cable	Length	Remarks
13222N	5 m (17 ft)	Connects an HP 262x terminal to the RS-232-C panel.
13232A	4.5 m (15 ft)	Connects an HP 264x terminal to the RS-232-C panel.
30062B	7.6 m (25 ft)	Connects a hard-wired full duplex modem to the RS-232-C panel.
30062B, opt. 001	15.2 m (50 ft)	Longer version of 30062B.
30062C	7.6 m (25 ft)	Extension cable for any of the above cables.

If you need to make your own cables for connection to the RS-232-C panel, the wiring information in figure 4-2 will be useful. Figure 4-2 illustrates the RS-232-C Panel device connector pin assignments that are representative of each port, J0 through J7. Note that in keeping with EIA RS-232-C standards when referring to the terminal or I/O device, Received Data (BB) and Transmitted Data (BA) should be referenced with respect to the terminal or device. In other words the Transmitted Data (BA) at the device end is actually the Receive Data (RD-) at the MUX interface. By the same convention, Received Data (BB) at the device is actually Send Data (SD-) at the MUX interface. A standard 25-pin male connector (shown in figure 4-2) must be attached to the RS-232-C Panel end of the cable and your device compatible connector at the other. It is recommended that such a cable not exceed 15 meters (50 ft) in length by the RS-232-C standard. Figure 4-2 gives the pin-to-signal relationships for the 25-pin connector at the RS-232-C Panel end of the fabricated cable.

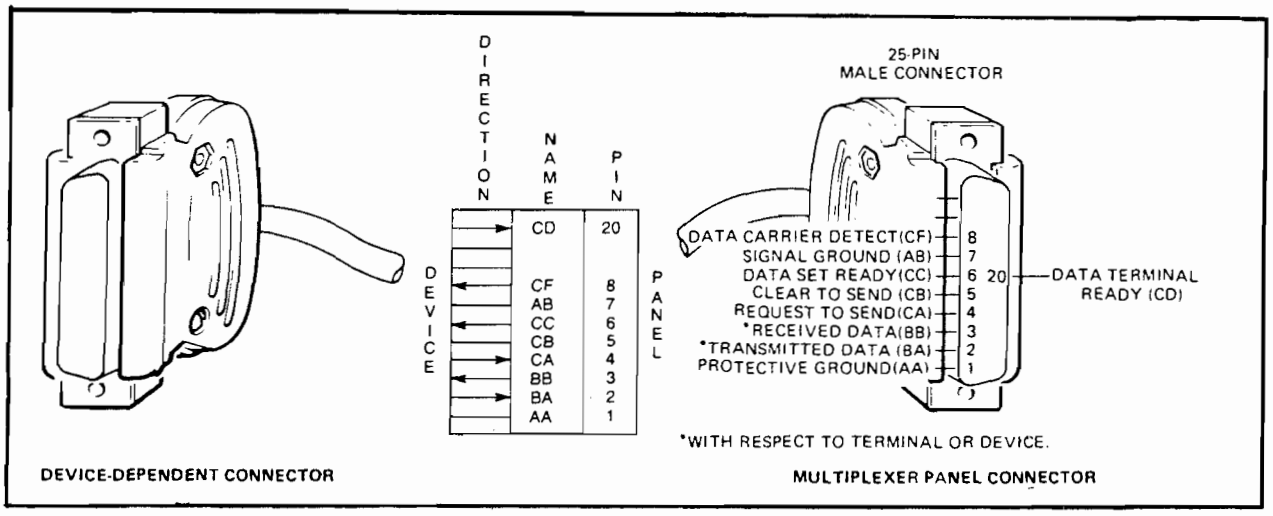


Figure 4-2. RS-232-C Panel to Device Wiring

Connection to Modem Card Cage

Option #002 of the HP 12040C is designed for connection to the HP 37214 modem card cage. The HP 12040C with option 002 has the parts listed in Chapter 1.

Since ports 1 through 7 are tied to the same baud rate generator, modems operating at 300 or 1200 baud on ports 1 through 6 will automatically configure port 7 to 1200 baud. This is convenient since the MUX firmware uses port 7 to communicate with the HP 37214A controller at 1200 baud. You may desire to further modify the jumper configuration depending on your particular application. See the paragraph *Data Transmission Rate Wiring* later in this section.

Connect the MUX card to the modem card cage using the 3-meter connecting cable. (When you connect the hooded connector to the MUX card, make sure that the upper side of the connector (as indicated by right-side-up printing on the hood) goes to the upper (component) side of the board. The connector will face the same way as all other connectors in the card cage.

Connection to RS-423-A Devices

Option #003 of the HP 12040C is appropriate for direct connection to RS-423-A devices. The HP 12040C with option 003 includes the parts listed in Chapter 1.

Two possible types of connections are suggested: a direct connection from your device to the MUX interface or a connection that would involve a central distribution panel of your own design. You might consider a panel that does not impose the RS-232-C restriction but would implement and pass the RS-423 circuit standards, which are originally observed on the interface, to your I/O devices.

The HP 12040C Multiplexer may be directly connected to terminals, printers, hardwired full-duplex modems or user-supplied termination panels, thereby removing the need for the RS-232-C Panel. The backward-compatible nature of the RS-423 drivers and receivers with RS-232-C devices makes this possible. The direct connection involves the fabrication of a cable not longer than 91 meters (300 ft) with the 80-pin card connector (supplied with the HP 12040C Option 003 product) at one end and up to eight device-dependent connectors or a termination panel at the other.

Figure 4-3 details the actual fabrication of the cable. Terminals require connection of the Send Data (SD-) signal for data reception, the Receive Data (RD-) signal for data transmission and a signal ground. The Send Data (SD-) and ground signals (SD+) are all that are needed to connect a line printer. Remember that these signal names are referenced with respect to the MUX and not the terminal, printer, or I/O device.

Use a shielded cable with 24 AWG wire, not more than 91 meters (300 ft) in length. The MUX interface connector is an eighty-pin hooded connector (supplied with 12040C Option 003). This connector contains a different pin numbering scheme than the MUX interface it connects to. The even-numbered (component) side of the MUX interface corresponds with the side labeled "B" of the connector. The odd-numbered (solder) side of the MUX interface corresponds with the side of the connector labeled "A".

The device connectors will depend upon the devices being interfaced. Hewlett-Packard terminals require a 30-pin hooded card connector (HP 264x series and 2675A), a 50-pin connector (HP 262x series), or a standard 25-pin connector (HP 2635A). Hewlett-Packard printers require a 25-pin connector (HP 2631A, 2635A and HP 7310A).

Figure 4-4 illustrates the fabrication of the hooded card connector end of the custom cable.

According to the RS-423 standard, the MUX interface Send Data common signals are simply ground connection pins on the edge connector. For instance, the channel 0 Send Data common (SD0+) signal is actually a ground pin on the MUX interface edge connector. This pin is numbered 18 on the interface and 9A on the connector. Note that there are two cases in which one ground pin serves as the Send Data common line for two channels. Pin 31B (62 on the MUX interface) is the Send Data common for channels 3 and 4; and pin 35B (70 on the MUX interface) is the Send Data common for channels 5 and 7.

In making the RS-423-to-RS-232-C conversion for your terminal or device, the two common lines, Send Data common and Receive Data common (the white wire in each of the twisted pairs), can be tied together at the terminal or device end.

Custom Panel

If the RS-423 (subset of RS-449) standards are followed you can design and construct an RS-423 distribution panel. The RS-423 panel would have to implement the use of twisted pair for both send and receive lines between the panel and the device as well as from the MUX interface to the panel. The common (white) wires for each function should not be tied together at the panel but instead passed through to the device, thus providing the needed differential operation between the host and the device. Good shielding and grounding practices should also be followed.

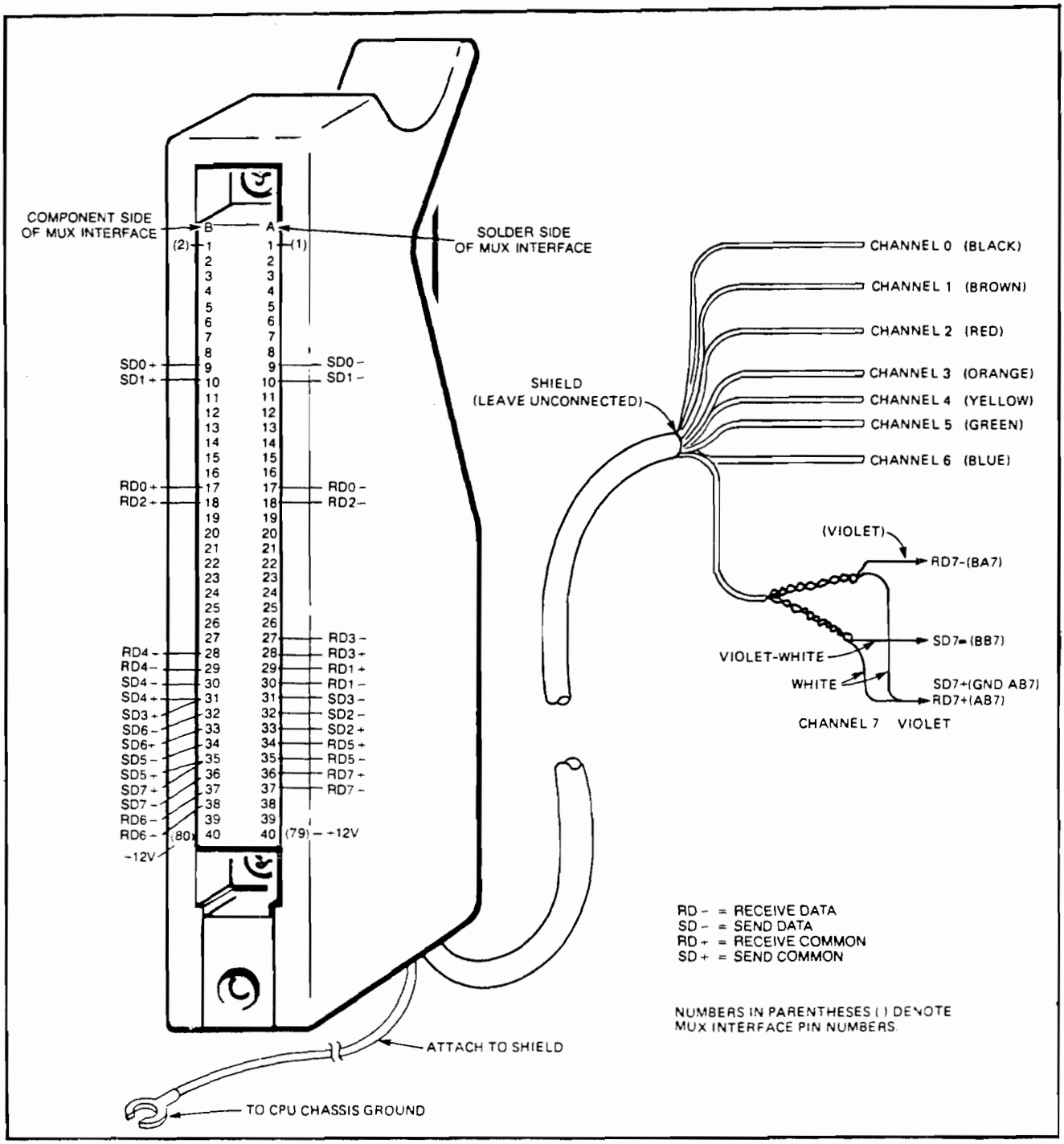


Figure 4-3. MUX Connector Wiring

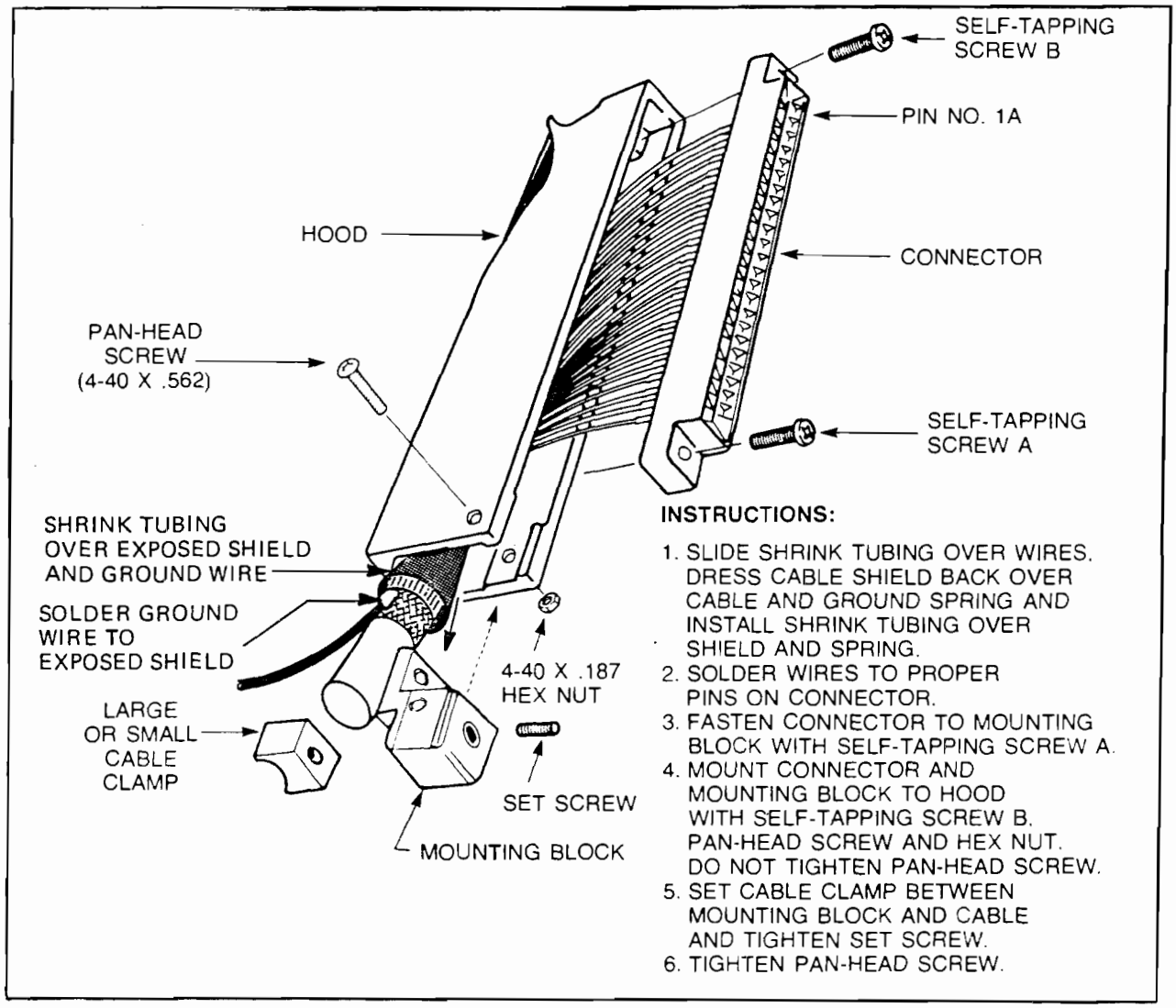
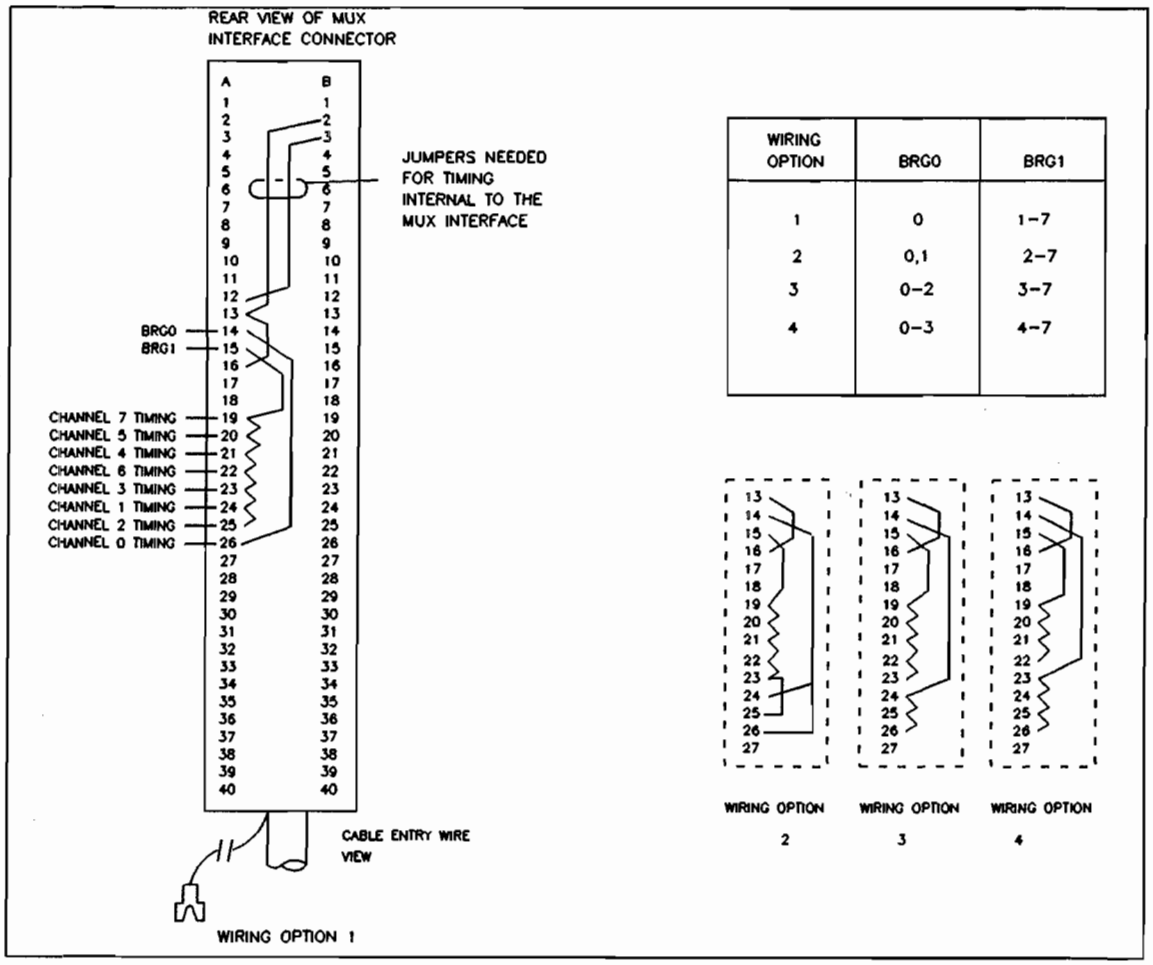


Figure 4-4. 80-Pin Card Connector

Data Transmission Rate Wiring

There are two hardware baud rate generators (BRGs) on the MUX card. Each MUX channel is connected to one (and only one) of the BRGs. These connections are hard-wired through the use of jumpers in the MUX card connector. You can rearrange the jumpers at any time (as long as the MUX card is not in use) to suit your needs. (See figure 4-5 for details.)

The host software interface driver allows you to programatically set the baud rate of each MUX channel. This, in turn, sets the baud rates of the BRGs. The combination of the software-selectable baud rate and the hard-wired distribution of the BRG outputs gives you great flexibility. By using the "grouped" baud rates (described in Chapter 2) you can distribute up to five different baud rates to the eight MUX channels.



WIRING OPTION	BRG0	BRG1
1	0	1–7
2	0,1	2–7
3	0–2	3–7
4	0–3	4–7

Figure 4-5. Data Transmision Rate Wiring

Chapter 5
MAINTENANCE

INTRODUCTION

This chapter provides maintenance information for the HP 12040C Eight Channel Asynchronous Multiplexer Interface. Included are preventive maintenance instructions and troubleshooting information.

CAUTION

SOME OF THE COMPONENTS IN THIS PRODUCT ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE HANDLING THE CARD.

PREVENTIVE MAINTENANCE

There is no preventive maintenance (PM) required for the HP 12040C Multiplexer Interface other than a routine inspection of the interface, cables, etc. This should be performed as part of the entire HP 1000 system PM. At that time, the interface and cables should be visually inspected for loose or broken components, or the presence of foreign objects. The following MUX Interface Tests/Diagnostics should only be performed when a failure is suspected in the MUX hardware.

TROUBLESHOOTING

Four methods exist to verify proper operation of the Multiplexer hardware interface:

- The HP 1000 A-Series self test
- The Echo Verification
- The Kernel Diagnostic
- The Off-line Functional Diagnostics

HP 1000 A-Series Self-Test

The on-board intelligence of the MUX interface makes problem isolation using the host A-Series self-test more complete. The Z-80 subsystem generates the flag functions required to indicate successful completion of the host self-test.

If the MUX interface is suspected, perform the following:

1. Verify placement of the EPROM jumpers; see figure 2-1.
2. Replace the EPROM (U115) and retest.
3. Replace the MUX interface and retest.

Echo Verification

After CPU power up, the MUX interface is initialized to ECHO characters. This initialized state allows a quick check of terminal communications to the MUX using the on board Z80A microprocessor subsystem. Typing characters and verifying that the ECHOed characters were those typed indicates that the Z-80A subsystem and the terminal are communicating. You may wish to type in several ASCII combinations as well as perform the EDIT features (line delete and backspace) available in this mode. This check may be performed on any terminal that meets the following conditions of the system's default configuration:

1. Connected to BRG0 or BRG1 set at 9600 baud
2. Transmits 8 bits per character
3. Has 1 stop bit per character
4. Does not check Parity
5. Transmits in Character Mode.

NOTE

If the terminal is configured for LOCAL mode it may appear to function in the ECHO mode; however, this does not test the MUX interface and supporting hardware. Verify the terminal is in REMOTE and not in BLOCK MODE.

If characters are not echoed back properly, a quick check of the following items may save troubleshooting time:

1. Are MUX interface and supporting hardware correctly installed?
2. Is the interface inserted all the way into the backplane of the host?

3. Are the cabling connections (BRG-to-ports and input/output data lines) wired correctly for the ports you are using?

4. Is there power supplied to the interface from the host CPU? 5. Did you intialize the MUX by cycling the host computer power?

6. Is the terminal correctly connected and configured?

7. Is the cable properly connected to the terminal?

8. Is the terminal set to the REMOTE mode, Character Mode, and the baud rate correctly set?

9. Is there a reason to suspect a failure in the terminal?

10. Does the terminal operate correctly in other applications including connection to an HP 1000 computer under RTE?

The MUX interface will remain in the initialized (uninitialized from an operating system point of view) after power-up until the driver software initialization commands are executed as a function of the RTE operating system. Thus the MUX hardware/firmware subsystem will not respond to operating software without first performing the proper control requests to the interface from the driver. Consult your system's Driver Reference Manual for further details regarding MUX interface initialization.

Kernel Diagnostic

Run the kernel diagnostic. Refer to the Kernel Diagnostic Operating Manual for your system.

Off-Line Functional Diagnostic

Run the interface diagnostic. Refer to the Diagnostic Operating Manual for the diagnostic product that you are using.

Chapter 6
SERVICE DIAGRAMS

INTRODUCTION

This chapter has the following tables and servicing diagrams:

- MUX interface backplane connections (P1 and P2)
- MUX interface I/O connections (connector J1)
- MUX interface card to RS-232-C panel cable connections
- RS-232-C panel 25-pin connections (connectors J0 through J7)
- Serial I/O circuits and equivalents
- MUX interface schematic diagrams
- RS-232-C panel schematic diagram

Table 6-1. MUX Interface Backplane Connections (P1 and P2)

P1-	SIGNAL NAME	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	SPARE 1	
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	
14	GND	
15	SPARE 2	
16	GND	
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
20	AB1	Address Bus Bit 1
21	AB2	Address Bus Bit 2
22	AB3	Address Bus Bit 3
23	AB4	Address Bus Bit 4
24	AB5	Address Bus Bit 5
25	AB6	Address Bus Bit 6
26	AB7	Address Bus Bit 7
27	AB8	Address Bus Bit 8
28	AB9	Address Bus Bit 9
29	AB10	Address Bus Bit 10
30	AB11	Address Bus Bit 11
31	AB12	Address Bus Bit 12
32	AB13	Address Bus Bit 13
33	AB14	Address Bus Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Data Bus Bit 1
37	DB2	Data Bus Bit 2
38	DB3	Data Bus Bit 3
39	DB4	Data Bus Bit 4
40	DB5	Data Bus Bit 5
41	DB6	Data Bus Bit 6
42	DB7	Data Bus Bit 7
43	DB8	Data Bus Bit 8
44	DB9	Data Bus Bit 9
45	DB10	Data Bus Bit 10
46	DB11	Data Bus Bit 11
47	DB12	Data Bus Bit 12
48	DB13	Data Bus Bit 13
49	DB14	Data Bus Bit 14
50	DB15	Data Bus Bit 15

P2-	SIGNAL NAME	SIGNAL DEFINITION
1	CPUTURN-	Processor Turn
2	GND	
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI-	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	GND	
16	SLAVE-	Slave Request
17	GND	
18	MRQ-	Memory Request
19	GND	
20	FCLK-	Fast Clock
21	GND	
22	CCLK-	Communications Clock
23	PINT-	Priority Interrupt
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	GND	
28	BUSY-	Memory Busy
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	
34	GND	
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12M	
40	−12M	
41	+12V	
42	+12V	
43	−12V	
44	−12V	
45	+5M	
46	+5M	
47	AC∅2	
48	AC∅2	
49	AC∅1	
50	AC∅1	

Table 6-2. MUX Interface I/O Connections (Connector J1)

LEGEND: > = OUTPUT FROM MUX INTERFACE
< = INPUT TO MUX INTERFACE
( ) = MUX INTERFACE CABLE CONNECTOR PIN NUMBER
EIA = DENOTES EIA RS-423 SIGNAL

* MUX Interface and cable connector pinouts both given.

* TTL is implied when no logic level is given.

MUX INTERFACE CIRCUIT SIDE				MUX INTERFACE COMPONENT SIDE			
PIN	LABEL	NOTE		PIN	LABEL	NOTE	
1 (1A)	+5V			2 (1B)	GND		
3 (2A)	+5V			4 (2B)	SCLK	1.843 MHz	>
5 (3A)	+5V			6 (3B)	FCLK	7.373 MHz	>
7 (4A)	+5V			8 (4B)	PNLIN	TTL	<
9 (5A)				10 (5B)	PNLIN	GND	
11 (6A)	PNLOUT	TTL	>	12 (6B)	PNLOUT	GND	
13 (7A)	CLK'	3.686MHz	>	14 (7B)	CLK'	GND	
15 (8A)	ENABL	LED DRIVER	>	16 (8B)	ENABL	GND	
17 (9A)	SD0-	EIA	>	18 (9B)	SD0+	GND	
19 (10A)	SD1-	EIA	>	20 (10B)	SD1+	GND	
21 (11A)				22 (11B)	GND	GND	
23 (12A)	TIMSTRB	TTL	<	24 (12B)	TIMSTRB	GND	
25 (13A)	CLK1	CTC1 IN	<	26 (13B)	CLK1	GND	
27 (14A)	BRG0	CTC0 OUT	>	28 (14B)	BRG0	GND	
29 (15A)	BRG1	CTC1 OUT	>	30 (15B)	BRG1	GND	
31 (16A)	CLK0	CTC0 IN	<	32 (16B)	CLK0	GND	
33 (17A)	RD0-	EIA	<	34 (17B)	RD0+	EIA	<
35 (18A)	RD2-	EIA	<	36 (18B)	RD2+	EIA	<
37 (19A)	T7	TTL	<	38 (19B)	T7	GND	
39 (20A)	T5	TTL	<	40 (20B)	T5	GND	
41 (21A)	T4	TTL	<	42 (21B)	T4	GND	
43 (22A)	T6	TTL	<	44 (22B)	T6	GND	
45 (23A)	T3	TTL	<	46 (23B)	T3	GND	
47 (24A)	T1	TTL	<	48 (24B)	T1	GND	
49 (25A)	T2	TTL	<	50 (25B)	T2	GND	
51 (26A)	T0	TTL	<	52 (26B)	T0	GND	
53 (27A)	RD3-	EIA	<	54 (27B)	GND	GND	
55 (28A)	RD3+	EIA	<	56 (28B)	RD4+	EIA	<
57 (29A)	RD1+	EIA	<	58 (29B)	RD4-	EIA	<
59 (30A)	RD1-	EIA	<	60 (30B)	SD4-	EIA	>
61 (31A)	SD3-	EIA	>	62 (31B)	SD3+,4+	GND	
63 (32A)	SD2-	EIA	>	64 (32B)	SD6-	EIA	>
65 (33A)	SD2+	GND		66 (33B)	SD6+	GND	

Table 6-2. MUX Interface I/O Connections (Connector J1) (Continued)

MUX INTERFACE CIRCUIT SIDE			MUX INTERFACE COMPONENT SIDE		
PIN	LABEL	NOTE	PIN	LABEL	NOTE
67 (34A)	RD5+	EIA <	68 (34B)	SD5-	EIA >
69 (35A)	RD5-	EIA <	70 (35B)	SD5+,7+	GND
71 (36A)	RD7+	EIA <	72 (36B)	SD7-	EIA >
73 (37A)	RD7-	EIA <	74 (37B)	RD6-	EIA <
75 (38A)			76 (38B)	RD6+	EIA <
77 (39A)	+12V		78 (39B)	BLANK	
79 (40A)	+12V		80 (40B)	-12V	

Table 6-3. MUX Interface to RS-232-C Cable Connections

CONNECTOR (J8) PIN NUMBER	SIGNAL MNEMONIC	SIGNAL FUNCTION
1	RD7(A)	Receive Data (A)
3	SD7	Send Data
4	RD6(A)	Receive Data (A)
6	SD6	Send Data
7	RD5(A)	Receive Data (A)
9	SD5	Send Data
10	RD4(A)	Receive Data (A)
12	SD4	Send Data
13	RD3(A)	Receive Data (A)
15	SD3	Send Data
16	RD2(A)	Receive Data (A)
18	SD2	Send Data
19	RD1(A)	Receive Data (A)
21	SD1	Send Data
22	RD0(A)	Receive Data (A)
24	SD0	Send Data
26	RD7(B)	Receive Data (B)
28	SG7	Signal Ground
29	RD6(B)	Receive Data (B)
31	SG6	Signal Ground
32	RD5(B)	Receive Data (B)
34	SG5	Signal Ground
35	RD4(B)	Receive Data (B)
37	SG4	Signal Ground
38	RD3(B)	Receive Data (B)
40	SG3	Signal Ground
41	RD2(B)	Receive Data (B)
43	SG2	Signal Ground
44	RD1(B)	Receive Data (B)
46	SG1	Signal Ground
47	RD0(B)	Receive Data (B)
49	SG0	Signal Ground

Table 6-4. RS-232-C Panel 25-Pin Connections (Connectors J0 through J7)

25-PIN CONNECTOR	SIGNAL MNEMONIC	SIGNAL FUNCTION
(Device ports J0-J7) PIN NUMBER	(with respect to Terminal or I/O Device)	
1	AA	PROTECTIVE GROUND
2	BA	TRANSMITTED DATA
3	BB	RECEIVED DATA
4	CA	REQUEST TO SEND
5	CB	CLEAR TO SEND
6	CC	DATA SET READY
7	AB	SIGNAL GROUND
8	CF	DATA CARRIER DETECT
9	NC	NO CONNECTION
10	NC	NO CONNECTION
11	NC	NO CONNECTION
12	NC	NO CONNECTION
13	NC	NO CONNECTION
14	NC	NO CONNECTION
15	NC	NO CONNECTION
16	NC	NO CONNECTION
17	NC	NO CONNECTION
18	NC	NO CONNECTION
19	NC	NO CONNECTION
20	CD	DATA TERMINAL READY
21	NC	NO CONNECTION
22	NC	NO CONNECTION
23	NC	NO CONNECTION
24	NC	NO CONNECTION
25	NC	NO CONNECTION

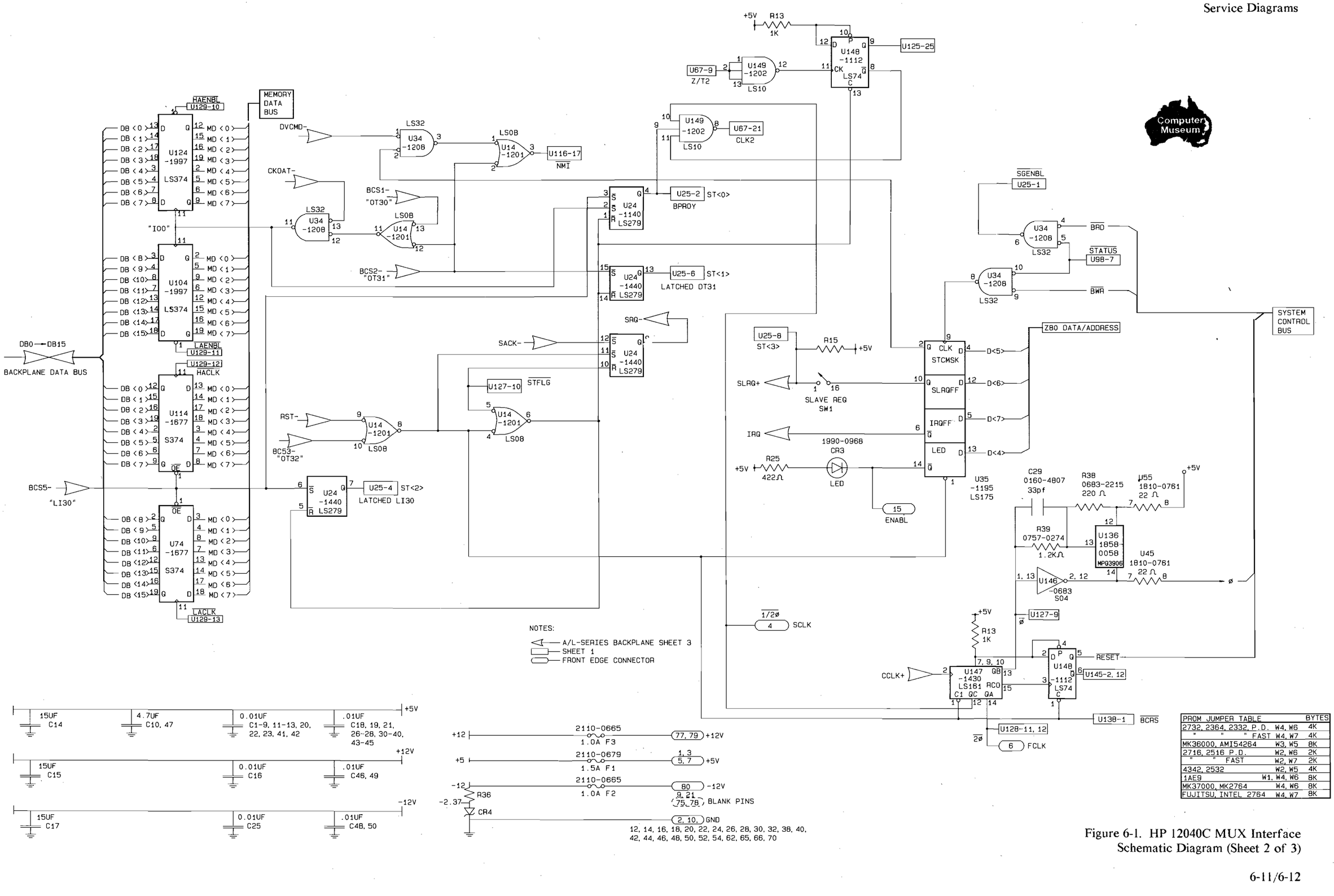
Table 6-5. Serial I/O Circuits

SIGNAL RS-232-C	CCITT V.24	FUNCTION	SIGNAL RS-449	FUNCTION	DIRECTION W/ RESPECT TO TERMINAL
AA	101	PROTECTIVE GROUND	--		
AB	102	SIGNAL GROUND	SG	SIGNAL GROUND	
--	---		SC	SEND COMMON	
--	---		RC	RECEIVE COMMON	
BA	103	TRANSMITTED DATA	*SD	SEND DATA	OUT
BB	104	RECEIVED DATA	*RD	RECEIVE DATA	IN
CA	105	REQUEST TO SEND	RS	REQUEST TO SEND	OUT
CB	106	CLEAR TO SEND	CS	CLEAR TO SEND	IN
CC	107	DATA SET READY	DM	DATA MODE	IN
CD	108.2	DATA TERMINAL READY	TR	TERMINAL READY	OUT
CF	109	CARRIER DETECT	RR	RECEIVER READY	IN

*SD (terminal) = RD(B) (MUX interface)
*RD (terminal) = RD(A) (MUX interface)

Z80 DATA / ADDRESS
SYSTEM CONTROL BUS
Z80 CONTROL BUS

Figure 6-1. HP 12040C MUX Interface Schematic Diagram (Sheet 1 of 3)



PROM JUMPER TABLE		BYTES
2732, 2364, 2332, P.D.	W4, W6	4K
" " " FAST	W4, W7	4K
MK36000, AMI54264	W3, W5	8K
2716, 2516 P.D.	W2, W6	2K
" " FAST	W2, W7	2K
4342, 2532	W2, W5	4K
1AE9	W1, W4, W6	8K
MK37000, MK2764	W4, W6	8K
FUJITSU, INTEL 2764	W4, W7	8K

Figure 6-1. HP 12040C MUX Interface Schematic Diagram (Sheet 2 of 3)

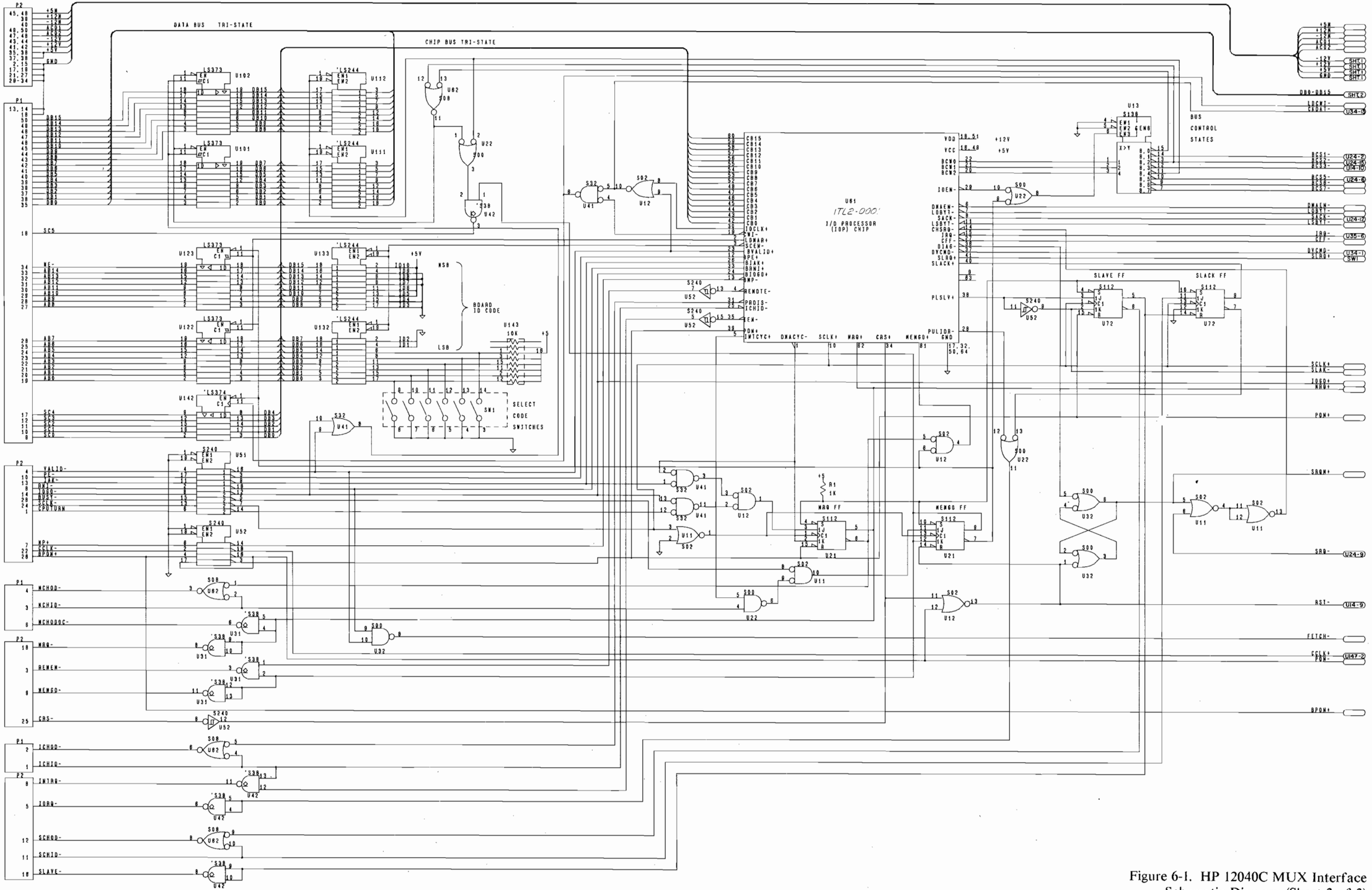


Figure 6-1. HP 12040C MUX Interface Schematic Diagram (Sheet 3 of 3)

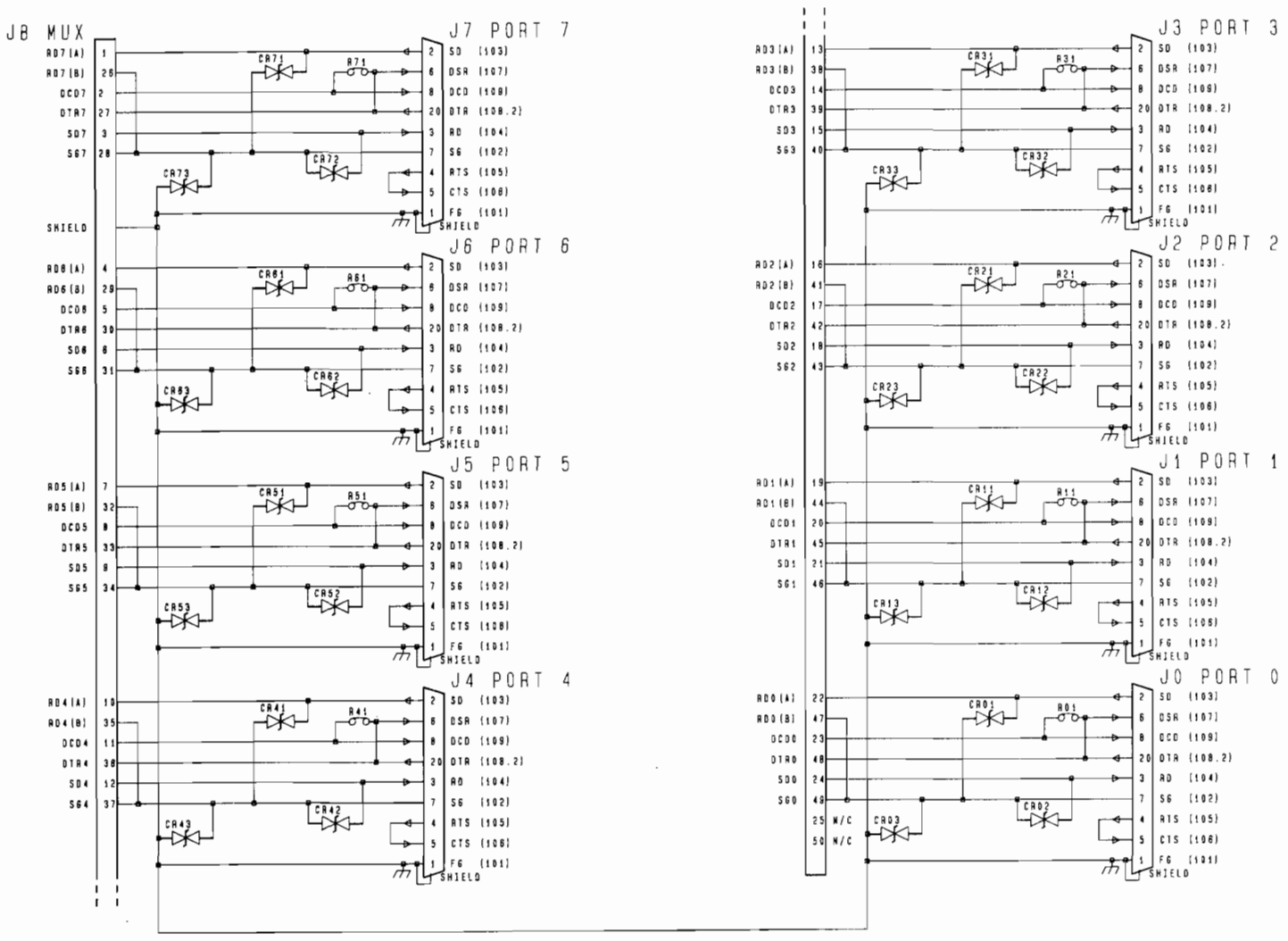


Figure 6-2. RS-232-C Panel Schematic Diagram

Chapter 7
REPLACEMENT PARTS

INTRODUCTION

This chapter has information that will help you to order replacement parts for the HP 12040C MUX Interface:

- How to order listed and non-listed parts for the MUX
- Replaceable Parts tables and information for the MUX
- Code List of Manufacturers for the replaceable parts

REPLACEABLE PARTS

Table 7-1 contains a list of the replaceable parts in alphanumeric order of the reference designations used on the MUX Interface. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY) of each part used in the interface.
5. Description of the part.
6. A five-digit code number that corresponds to the manufacturer of the part.
7. The manufacturer's part number.

ORDERING INFORMATION

To order replacement parts or to obtain information on the parts used in the MUX interface, address the order or inquiry to your local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed in the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity you require. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the MUX interface or part.
2. Description and function of the part.
3. Quantity required.

Table 7-1. HP 12040C Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12040-60014	1	1	PCA-A/L MUX	28480	12040-60014
C1	0160-6500	7	43	CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C2	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C3	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C4	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C5	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C6	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C7	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C8	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C9	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C10	0180-0100	3	2	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C11	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C12	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C13	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C14	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C15	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C16	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C17	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C18	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C19	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C20	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C21	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C22	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C23	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C25	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C26	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C27	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C28	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C29	0160-4807	3	1	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
C30	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C31	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C32	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C33	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C34	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C35	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C36	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C37	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C38	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C39	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C40	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C41	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C42	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C43	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C44	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C45	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C46	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C47	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C48	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C49	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C50	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
CR3	1990-0968	9	1	LED-LAMP LUM-INT=4MCD IF=15MA-MAX BVR=5V	28480	1990-0968
CR4	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
F1	2110-0679	6	1	FUSE 1.5A 125V NTD .28X.096	28480	2110-0679
F2	2110-0665	0	2	FUSE 1A 125V NTD .28X.096	28480	2110-0665
F3	2110-0665	0		FUSE 1A 125V NTD .28X.096	28480	2110-0665
R1	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R4	0811-3716	2	2	RESISTOR ZERO OHM	28480	0811-3716
R7	0811-3716	2		RESISTOR ZERO OHM	28480	0811-3716
R8	0698-3155	1	6	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R9	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R15	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R16	0757-0465	6	4	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R24	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R25	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R26	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F

Table 7-1. HP 12040C Replaceable Parts (continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
R27	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R28	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R29	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R30	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R36	0698-4590	0	1	RESISTOR 422 1% .25W F TC=0+-100	24546	C5-1/4-T0-422R-F
R38	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R39	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1211-F
SW1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U11	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U12	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U13	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U14	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U16	1820-2300	8	4	IC-Z80A SIO/2	28480	1820-2300
U17	1820-2594	2	4	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U18	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U21	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U22	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U24	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U25	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U27	1810-0760	9	2	NETWORK-RES 14-DIP 6.0K OHM X 13	28480	1810-0760
U28	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U31	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U32	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U34	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U35	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U36	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U37	1810-0760	9		NETWORK-RES 14-DIP 6.0K OHM X 13	28480	1810-0760
U38	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U41	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U42	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U44	1818-3214	0	2	IC TMS4416-15NL	28480	1818-3214
U45	1810-0761	0	2	NETWORK-RES 16-DIP 22.0 OHM X 15	28480	1810-0761
U47	1820-1858	9	2	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U48	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U49	1820-3778	6	4	IC DRVR TTL COMM EIA RS-432 DUAL	28480	1820-3778
U51	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U52	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U55	1810-0761	0		NETWORK-RES 16-DIP 22.0 OHM X 15	28480	1810-0761
U56	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U61	1TL2-0001	3	1	BICKS	28480	1TL2-0001
U62	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U64	1818-3214	0		IC TMS4416-15NL	28480	1818-3214
U65	1820-1077	4	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U66	1820-2300	8		IC-Z80A SIO/2	28480	1820-2300
U67	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
U69	1820-3778	6		IC DRVR TTL COMM EIA RS-432 DUAL	28480	1820-3778
U72	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U74	1820-1677	0	2	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U75	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U76	1820-2075	4	1	IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U77	1820-1987	5	1	IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT	01295	SN74LS299N
U78	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U79	1820-3778	6		IC DRVR TTL COMM EIA RS-432 DUAL	28480	1820-3778
U97	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
U98	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U99	1820-3778	6		IC DRVR TTL COMM EIA RS-432 DUAL	28480	1820-3778
U101	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U102	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U104	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U111	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U112	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U114	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U115	5180-7228	5	1	BURNIN 1818-3384	28480	5180-7228
U116	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U117	1820-1624	7	1	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U122	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U123	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N

Table 7-1. HP 12040C Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U124	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U125	1820-2299	4	1	IC-Z80A DMA	28480	1820-2299
U127	1820-2544	2	1	IC MISC TTL S	18324	82S100I PROGRAMMED
U128	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U129	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U132	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U133	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U135	1820-1470	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U136	1858-0058	8	1	TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	MPQ3906
U138	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U139	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U142	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U143	1810-0286	4	1	NETWORK-RES 16-DIP10.0K OHM X 15	01121	316A103
U145	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
U146	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U147	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U148	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U149	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
X61	1200-1011	2	1	SOCKET-IC 64-CONT SQUARE DIP-SLDR	28480	1200-1011
X115	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Table 7-2. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address		Zip Code
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS	TX	75222
02802	AMERICAN SAFETY RAZOR CO DIV PHILIP	STAUNTON	VA	24401
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

Appendix A
PRODUCT HISTORY

This is the history of the 12040 series multiplexer products:

NEW BOARD	EXCHANGE	FIRMWARE	COMMENTS
5061-3427	5061-4906	12040-80001	Product number 12040A
"	"	12040-80002	Powering down terminal locked it out, fixed. See SN 12040-01**.
"	"	5180-1970	The following changes were made to th firmware: - Receive buffer made round-robin. - EDIT charac, Back sp, Del line not echo if echo off, fixed. - Baud rate capability improved. - Character count reset, fixed. - CANCEL ALL reset parity flag, fixe - ENQ/ACK handshake increment, fixed - Modem capability, Xon-Xoff, added.
12040-60003	12040-69003	"	IOP chip changed. - See SN 12040-06** Firmware structured to the exchange board.
"	12040-69013	"	Firmware taken off the exchange board
"	"	5180-7227	The following changes were made to th firmware: - Set ENQ/ACK timer to 10 seconds. - Allows CPU to force Xon. - Port using parity didn't initalize properly if terminal power is off, fixed. - BREAK key on an odd parity terminal hangs port, fixed. - If last character of a receive buffer is KATAKANA port hangs, fixed. See SN 12040-9**.

Product History Continued:

NEW BOARD	EXCHANGE	FIRMWARE	COMMENTS
12040-60004	12040-69004	5180-7228	Product number 12040C: - BRG 0 & BRG 1 both programmed to 9600 bps on power-up (BRG 0 previously defaulted to 2400) - CCITT V.28-compatible, fail-safe line receivers added. - SYNAPSE, new 8-port panel & interface cable, replaced previous. - Backward compatible with 12040B

The 12040-60002 replaced the 12828-60002 as the cable to connect the card to the J-Box. See SN 12040-07**.

**HP Service Note number.

CABLES	PORT	BRG
12828-60002	0	0
	1-7	1
12040-60002	0-6	1
	7	0
28658-63005	0	0
	1-7	1

FIRMWARE	BAUD RATE	
	BRG 0	BRG 1
5180-1970	2400	9600
5180-7227	2400	9600
5180-7228	9600	9600

INDEX

A

B

C

D

E

F

G

H

I

K

M

O

P

R

S

T

V