HEWLETT PACKARD

REFERENCE MANUAL

HP 12008A
PROM STORAGE MODULE

Manual part no. 12008-90001

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Card Assembly: 12008-60001
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LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent update number on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a updated page. Within the manual, changes are marked with a vertical bar in the margin. When a update is incorporated in a reprinted manual, the update number and vertical bar in the margin is removed but the update number will remain on this List of Effective Pages page.

Pages	Update No.	Pages	Update No.
7-9/7-10	1		
7-13/7-14	1		

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

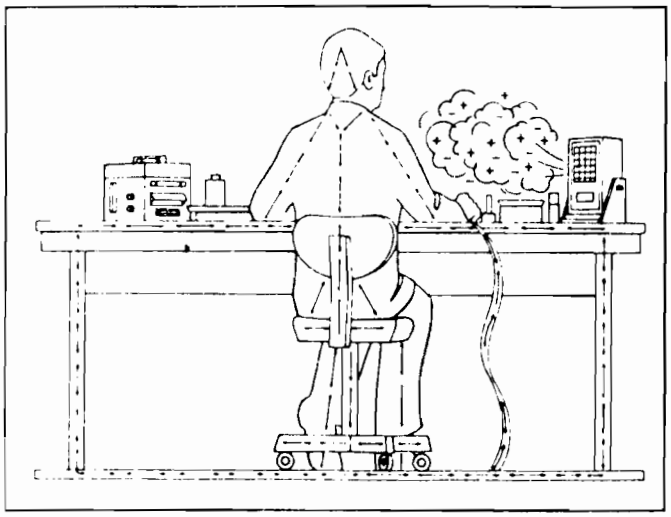
Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

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ILLUSTRATIONS

TABLES

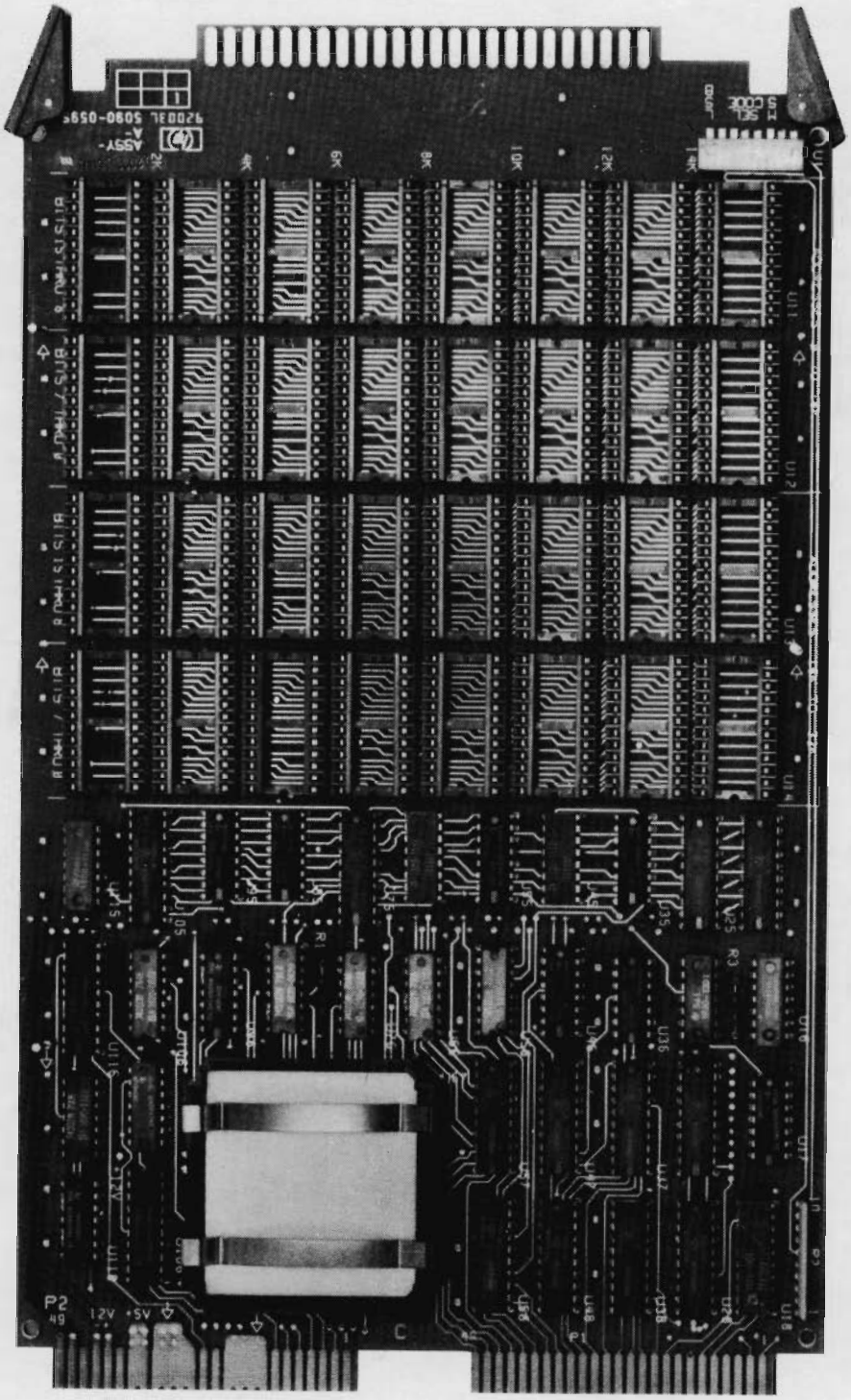

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Figure 1-1. PROM Storage Module HP 12008A

INTRODUCTION

SECTION I

1-1. INTRODUCTION

This manual provides general information, installation instructions, programming instructions, theory of operation, maintenance instructions, replaceable parts and service diagrams for the HP 12008A PROM Storage Module.

This section contains general information concerning the HP 12008A PROM Storage Module including a description and specifications.

1-2. DESCRIPTION

The HP 12008A (see Figure 1-1) provides an L-Series Computer with up to 64 kbytes of non-volatile storage for data or programs. Multiple programs may be stored on one PROM Storage Module and multiple PROM Storage Modules may be installed in the L-Series backplane. The stored program or data must be loaded into main memory before it can be executed by the computer.

The PROM's provide a rugged storage medium for use in environments too harse for flexible or hard discs or other mechanical storage devices. Also, for minimal storage requirements, the PROM Storage Module is more compact and less costly than disc storage.

The PROM Storage Module plugs into a single slot in the L-Series backplane (see Figure 1-2) and is assigned a single select code. The PROM Storage Module consists of an I/O Master (an I/O Processor Chip and its associated logic circuits), an address counter circuit, and 32 24-pin IC sockets. The PROMs are not supplied with the card. The PROM's used with the card must be Intel 2716A PROM's or equivalents. To the L-Series computer, this card is an I/O card and is under its software control at all times.

The PROM Storage Module has the capability of handling its own Direct Memory Access (DMA) and of decoding its own instructions from the processor. These features are performed by th I/O Master located on the PROM Storage Module. The I/O Master is composed of the I/O Processor (IOP) Chip and its associated logic circuitry and performs all of the functions necessary (instruction recognition and DMA control) for interfacing with the L-Series backplane. Figure 1-3 shows the PROM Storage Module in a typical L-Series system environment.

1-3. EQUIPMENT SUPPLIED

The HP 12008A product consists of the following items (see Figure 1-1):

a. PROM Storage Module, part no. 12008-60001.

b. PROM Storage Module Reference Manual, part no. 12008-90001 (not shown).

1-4. IDENTIFICATION

Five digits and a letter are used to identify standard HP products used with HP computers. The five digits identify the product and the letter indicates the revision level of the product.

The circuit card is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a date code and, possibly, a revision letter, i.e., A-1926A. This information is placed below the part number of the card. The first letter identifies the version of the etched circuit on the card. The date code (four digits following the letter) identifies the electrical characteristics of the assembled card. The letter following the date code will be present only if the card has been revised. Thus, the complete part number on the PROM Storage Module could be as follows:

12008-60001
A-1926A

If the date code stamped on the PROM Storage Module is not listed with the date code on the title page of this manual, then there are differences between that card and the card described in this manual. The differences are described in manual supplements available at the nearest HP Sales and Service Office (listed in the back of this manual).

1-5. REFERENCE MANUAL

The manual supplied with the product is identified by its name and part number. The part number, 12008-90001, is printed on the title page. If the manual is revised, the publication date is changed Print History will reflect the revision date, and the List of Effective Pages will show the pages involved.

1-6. SPECIFICATIONS

Table 1-1 lists the specifications of the HP 12008A PROM Storage Module.

Table 1-1. Specifications

ELECTRICAL CHARACTERISTICS

PROM Chips: Must be Intel 2716A or pin compatible equivalent

PROM Memory Size: 64k bytes in 4k byte blocks

Transfer Rate: Random Instruction Mix: 2.0M bytes under DMA control
†Worst Case Instruction Mix: 1.8M bytes under DMA control

Transfer Size (maximum): 64k byte block under DMA control
(maximum): 2 byte block

Compatible with all features of the HP 1000 L-Series I/O System

Operating Temperature: 0 to +55 Degrees Celsius

Power Requirements: This card requires the following amounts of power from the computer's power supply at 25 degrees Celsius:

Voltage	Current	Power Dissipated
+5Vdc	2.0A	10.5W
+12Vdc	50mA	0.6W
	Total Power	11.6W

PHYSICAL CHARACTERISTICS

Card Dimensions:
Length: 28.91cm (11.380 in.)
Width: 17.15cm (6.750 in.)

†Worst Case Instruction Mix: A JMP* (a Jump instruction who's target address is it's own address).

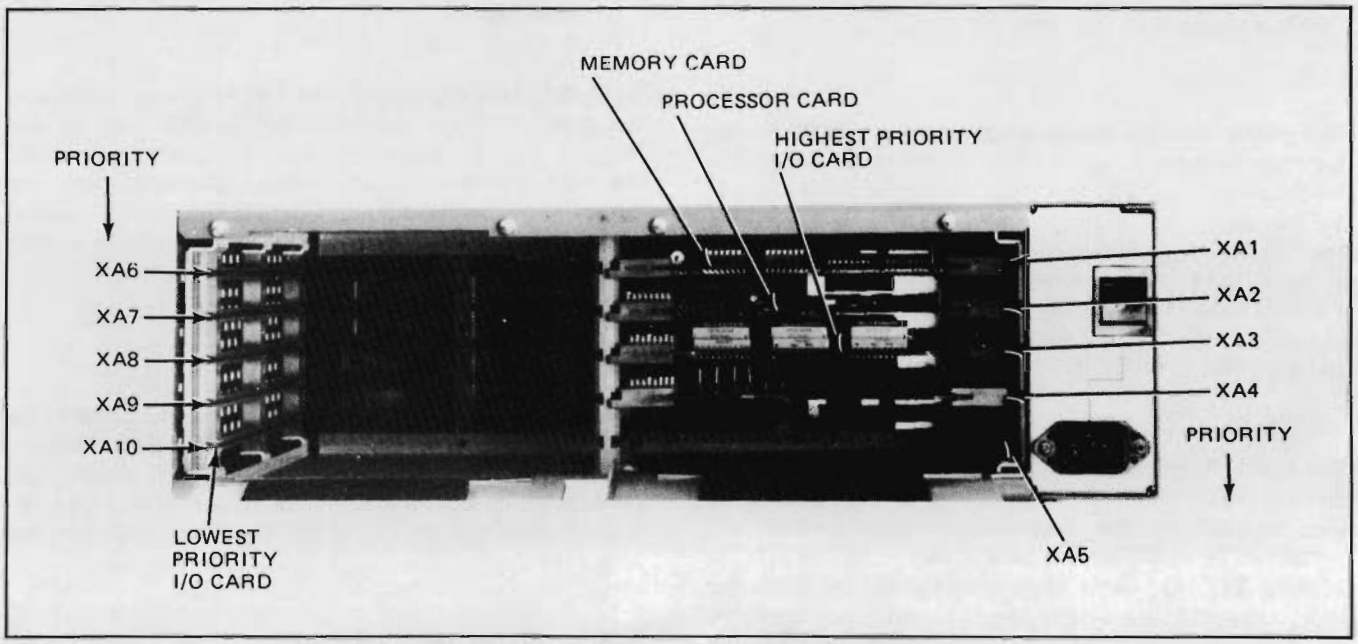

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Figure 1-2. Typical L-Series Card Cage Layout

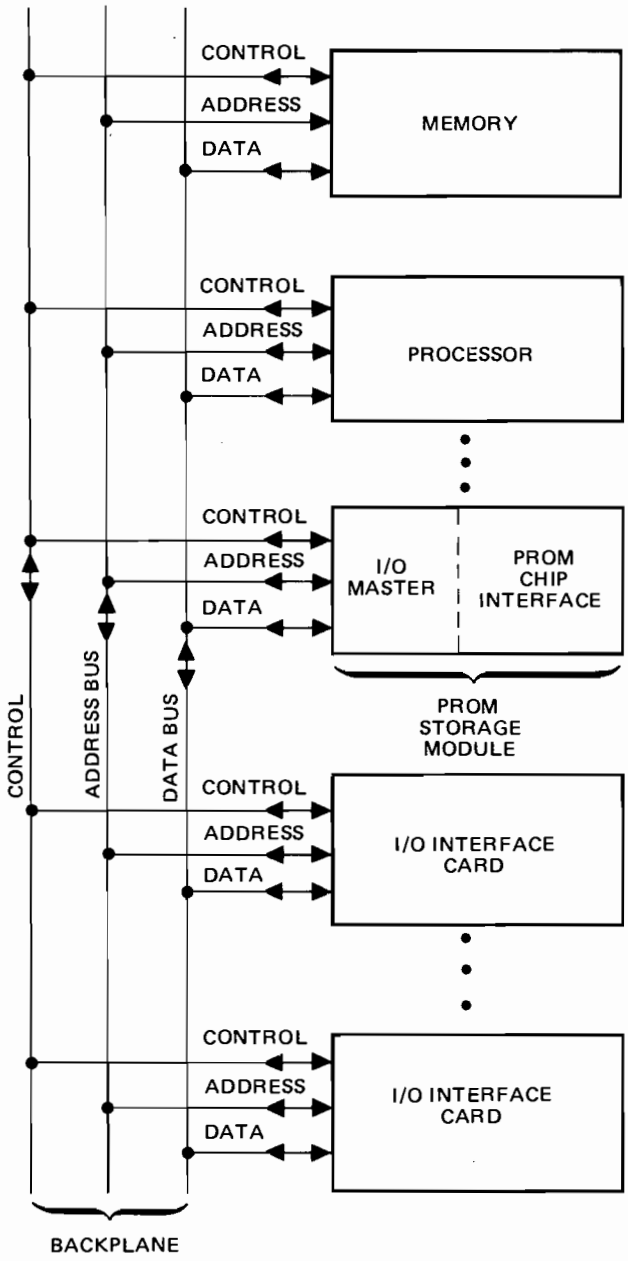

Figure 1-3. PROM Storage Module in a Typical L-Series System Environment

INSTALLATION

SECTION II

2-1. INTRODUCTION

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12008A PROM Storage Module.

2-2. UNPACKING AND INSPECTION

CAUTION

Use antistatic handling procedures when handling the printed circuit assemblies.

If the PROM Storage Module is ordered with a computer, the card is installed in the computer at the factory. When this is the case, it is necessary only to check the operation of the card after the computer is installed. Checkout instructions are furnished in paragraph 2-10. If the PROM Storage Module is ordered separately, inspect the carton containing the product before opening it. If there is evidence of damage, if water stains are visible, or if the box rattles, request that the carrier's agent be present when the box is opened.

Inspect each portion of the product as the parts are unpacked. Look for such damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the product is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest HP Sales and Service Office. The Sales and Service Office will arrange for repairs or replacement of the damaged parts without waiting for settlement of claims against the carrier. The HP Sales and Service Offices are listed in the back of this manual.

After inspecting all parts and components, refer to paragraph 1-3 to insure that the product is complete. Also, check the part numbers listed in paragraph 1-4 against the part numbers on the components. If the product is incomplete, or if an incorrect component has been supplied, notify the nearest HP Sales and Service Office.

2-3. PREPARATION FOR INSTALLATION

2-4. COMPUTATION OF POWER REQUIREMENTS

The PROM Storage Module obtains its operating power from the L-Series computer through the backplane. Before installing the card, it is necessary to determine whether the additional current drain will overload the power supply. If the card was installed at the factory, the required calculations have been made and it has been determined that an overload will not occur. The current and voltage requirements for the PROM Storage Module are listed in Table 1-1.

2-5. INTERFACE REQUIREMENTS

2-6. BACKPLANE TO PROM STORAGE MODULE

All interaction between the PROM Storage Module, the processor card, and the memory card occur on the backplane. Connections from the backplane to the PROM Storage Module are listed in Tables 2-1 and 2-2.

2-7. PROM CHIP PROGRAMMING

The PROM Storage Module is supplied without the PROM chips. The PROM chips may be purchased from several vendors, but must be Intel 2716A or equivalent. Most vendors can program the PROM chips. The PROM chips must consume less than 150 milliwatts when not selected.

The PROM chips will have to be programmed in various formats according to the usage. Refer to the L-Series Computer Reference Manual, part no. 02103-90007 or the appropriate driver manual.

The PROM chip addresses are shown in Figure 2-1. The PROM chips may be placed at any location on the card. The starting address of the program is decided by the location of the first pair of PROM chips. The PROM chip's pin out is shown in Figure 2-2.

2-8. SELECT CODE SELECTION

The location of the dip switch (U1) is shown in Figure 2-1. Switches U1S3 through U1S8 determine the select code for the PROM Storage Module. An open switch represents a logic 1 and a closed switch represents a logic 0. U1S3 represents the Most Significant Bit (MSB) and U1S8 represents the Least Significant Bit (LSB), see Figure 2-3.

2-9. INSTALLATION

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS. Wear safety glasses when removing or installing the retaining clips on the SOS chip sockets.

Table 2-1. Backplane Connections, Connector P1

P1-	SIGNAL NAME	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	SPARE 1	
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	
14	GND	
15	SPARE 2	
16	GND	
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
20	AB1	Address Bus Bit 1
21	AB2	Address Bus Bit 2
22	AB3	Address Bus Bit 3
23	AB4	Address Bus Bit 4
24	AB5	Address Bus Bit 5
25	AB6	Address Bus Bit 6
26	AB7	Address Bus Bit 7
27	AB8	Address Bus Bit 8
28	AB9	Address Bus Bit 9
29	AB10	Address Bus Bit 10
30	AB11	Address Bus Bit 11
31	AB12	Address Bus Bit 12
32	AB13	Address Bus Bit 13
33	AB14	Address Bus Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Data Bus Bit 1
37	DB2	Data Bus Bit 2
38	DB3	Data Bus Bit 3
39	DB4	Data Bus Bit 4
40	DB5	Data Bus Bit 5
41	DB6	Data Bus Bit 6
42	DB7	Data Bus Bit 7
43	DB8	Data Bus Bit 8
44	DB9	Data Bus Bit 9
45	DB10	Data Bus Bit 10
46	DB11	Data Bus Bit 11
47	DB12	Data Bus Bit 12
48	DB13	Data Bus Bit 13
49	DB14	Data Bus Bit 14
50	DB15	Data Bus Bit 15

Table 2-2. Backplane Connections, Connector P2

P2-	SIGNAL NAME	SIGNAL DEFINITION
1	CPUTURN-	Processor Turn
2	GND	
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI-	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	GND	
16	SLAVE-	Slave Request
17	GND	
18	MRQ-	Memory Request
19	GND	
20	FCLK-	Fast Clock
21	GND	
22	CCLK-	Communications Clock
23	PINT-	Priority Interrupt
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	GND	
28	BUSY-	Memory Busy
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	
34	GND	
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12M	
40	−12M	
41	+12V	
42	+12V	
43	−12V	
44	−12V	
45	+5M	
46	+5M	
47	ACϕ2	
48	ACϕ2	
49	ACϕ1	
50	ACϕ1	

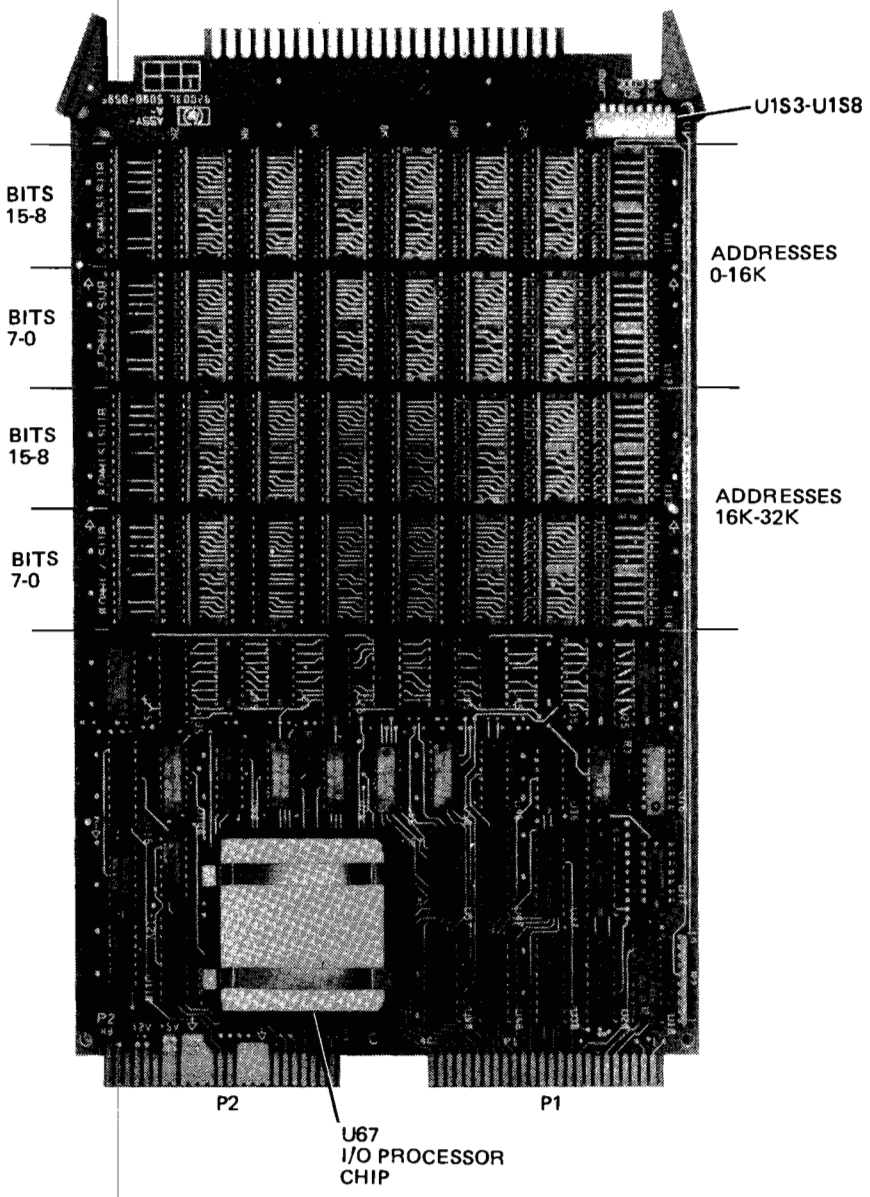

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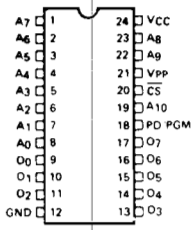
Figure 2-1. HP 12008-60001 PROM Storage Module

PIN CONFIGURATION



PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

Figure 2-2. PROM Chip Pinout

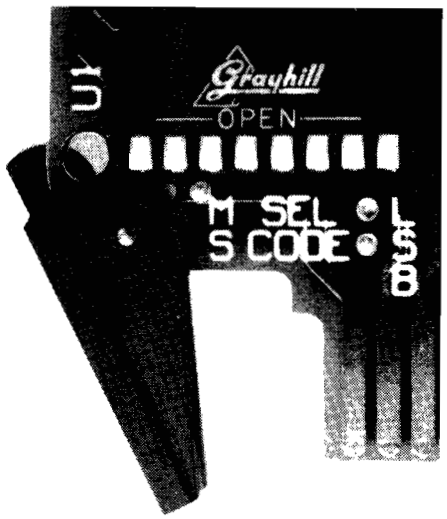


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Figure 2-3. Select Code Switches U1S3-U1S8

CAUTION

STATIC SENSITIVE DEVICES. Use antistatic handling procedures while removing or installing the chips.

After ensuring that the computer's power supply can handle the added load, perform the following steps:

a. Load PROM chips into sockets.

b. Set the select code for the PROM Storage Module with switches U1S3 through U1S8 (see paragraph 2-8).

c. Turn off the power to the computer. Insert the PROM Storage Module into the desired slot in the backplane. Make sure that the components on the card are on the same side as the other interface cards in the backplane. When installing the card, use care not to damage the card or any adjacent cards. Press the card firmly into place.

2-10. CHECKOUT

To verify operation of the PROM Storage Module, see Section V, paragraph 5-6, steps 1, 2, and 3 of this manual.

2-11. RESHIPMENT

If an item of the product or the product is to be returned to the nearest Hewlett-Packard Sales and Service Office for repair, attach a tag to the item identifying the owner and indicating the service to be performed.

CAUTION

STATIC SENSITIVE DEVICES. Use antistatic handling procedures while installing or removing the chips.

Use antistatic handling procedures when handling the printed circuit assemblies.

Remove the PROM chips and the I/O Processor (IOP) Chip (U67) before returning the PROM Storage Module. These chips will have to be used on the replacement card (see Section V, paragraph 5-3 for removal and installation procedures).

Pack the item in the original factory packing material, if available. It the original material is not available, an equivalent type of commercial packaging material should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack the item.

PROGRAMMING

SECTION III

3-1. INTRODUCTION

This section provides assembly-language programming procedures for the PROM Storage Module. For information on assembly-language programming, refer to the HP 1000 L-Series Reference Manual, part number 02103-90007.

This card has the capability to handle its own Direct Memory Access (DMA) and to decode its own instructions from the processor.

3-2. USE OF THE GLOBAL REGISTER

The PROM Storage Module is comprised of two sections: an I/O Master Section and a PROM Interface Section. The I/O Master Section performs all of the I/O processing functions for the computer. These functions include I/O instruction recognition and execution, and direct memory accessing (DMA). The I/O Master consists of the I/O Processor (IOP) Chip and its associated logic circuitry. The Global Register (GR) is located in the I/O Processor Chip and is a six-bit register that contains a select code. See Figure 3-1 for a block diagram of the I/O Processor Chip (U67).

All global registers on all interface cards are controlled by the Processor, thus all global registers contain the same select code. The global register may be loaded with an OTA 2 or OTB 2 I/O instruction, enabled with a CLF 2 I/O instruction, and disabled with an STF 2 I/O instruction. When the global register is enabled, any I/O instruction that is executed by the Processor automatically applies to the card whose select code is in the global register. For the PROM Storage Module for example, if the global register contains the PROM Storage Module's select code, the current I/O instruction is decoded and executed by the PROM Storage Module. Using the global register to store the select code frees the six least significant bits of the I/O instructions. These bits do not need to store the select code of the I/O card to receive the I/O instruction. Thus, these six bits can be used to address a register on the I/O interface cards.

Data may be transferred from the PROM Storage Module with or without the global register enabled.

3-3. I/O INSTRUCTION SET

The I/O Master executes the following twelve I/O instructions:

CLC	Clear Control
CLF	Clear Flag
LIA	Load Into A
LIB	Load Into B
MIA	Merge Into A
MIB	Merge Into B
OTA	Output A
OTB	Output B
SFC	Skip if Flag Clear
SFS	Skip if Flag Set
STF	Set Flag
STC	Set Control

The six-bit global register allows a maximum of 64 (decimal) select codes. The I/O Master, however, executes only a portion of these. Select codes 00 through 17 (octal) are reserved for the Processor, leaving 20 through 77 (octal) available for the I/O system.

3-4. INSTRUCTION USAGE SUMMARY

Table 3-1 lists all ot the instructions recognized by the IOP Chip by their select code. There are three conditions relevant to the instruction's execution. These conditions are as follows:

a. Is the global register (GR) enabled?

b. Do the contents of the GR equal the I/O Processor Chip's select code, (GR=SC)?

c. Do the lower six bits of the instruction equal the I/O Processor Chip's select code, (IR=SC)?

The summary indicates which conditions must be met for instruction execution by listing in each column: Y for yes, N for no, and X for don't care.

3-5. OUTPUT CONTROL WORDS

Four control words can be received by the PROM Storage Module. These control words are loaded into four registers. Three of these registers (registers 21, 22, and 23) are located in the IOP Chip and are used only in the DMA mode. These registers are described in paragraph 3-11 through 3-13.

One of the control words is used in any mode (DMA or non-DMA) and is the only control word necessary when DMA is not used. This control word is loaded into register 31 (U35, U45, U55, and U65) on the PROM Storage Module and is sent to the card using an OT* 31 only when the global register is enabled.

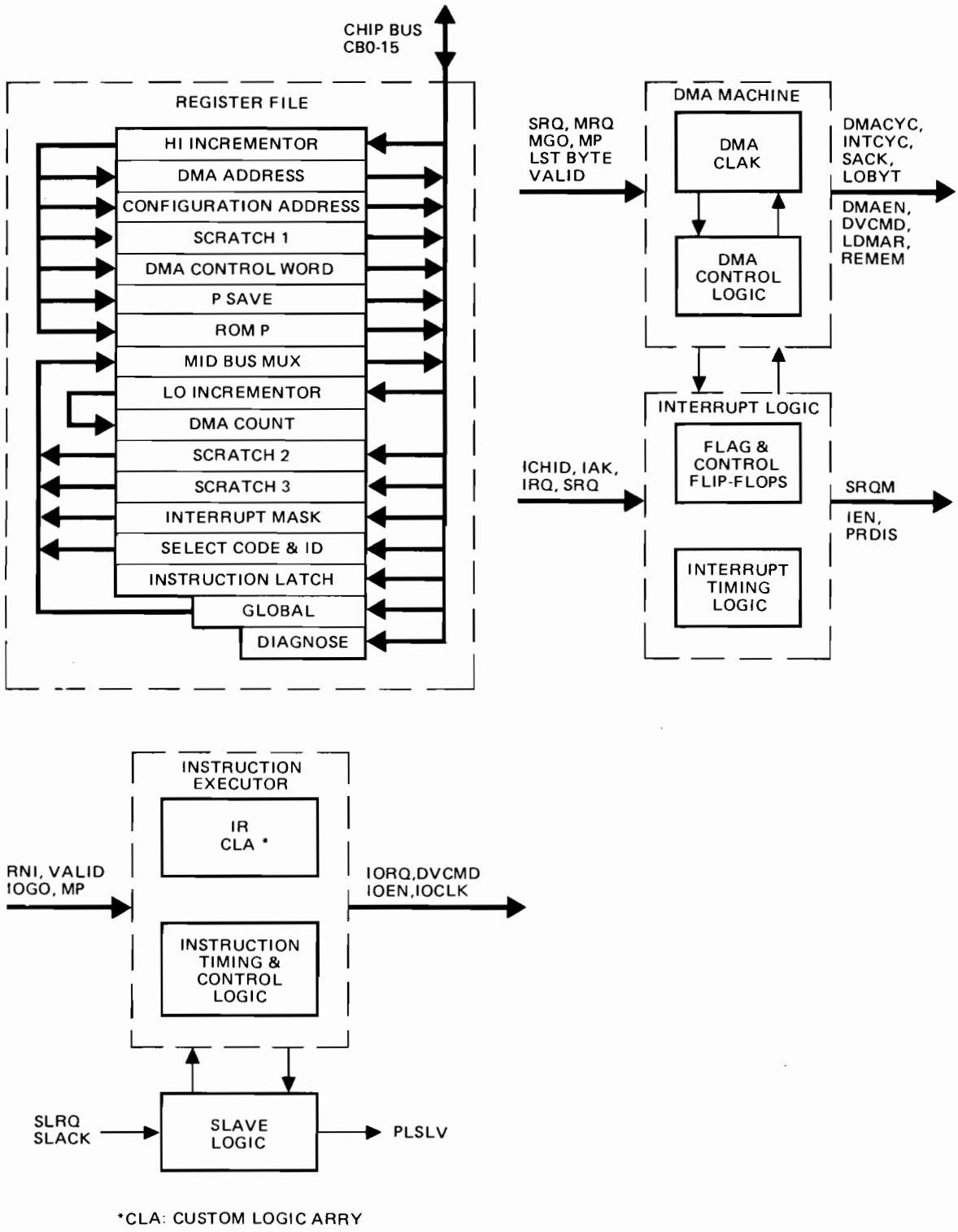


Figure 3-1. IOP (U67) Chip Block Diagram

3-6. CONTROL WORD REGISTER 31

The control word (Register 31) is used for both DMA and programmed I/O (non-DMA) transfers. The control word provides the PROM Storage Module with the 15-bit address that the PROM Storage Module will use to fetch the data word. The control word can be transferred to the PROM Storage Module using an OTA 31B with Register 31 containing the select code of the PROM Storage Module, or as the second word of the four word DMA configuration (quadruplet), see Figure 3-2.

CONTROL WORD REGISTER 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PROM ADDRESS														

Diagnostic Bit

3-7. INPUT STATUS WORD, REGISTER 31

A status word is available from the PROM Storage Module and it provides the address from the PROM Storage Module's Address Register (U35,45,55, and 65). The 15-bit address (RA0-RA14) is accompanied by an address error bit (RA15). If this bit is set, it indicates that the address has rolled over or that the address provided is larger than 32k words. This error bit will either cause an interrupt if the interrupt system is enabled, or will set the flag if the interrupt system is off. The error bit in the status word is cleared by the transmission of an address into the control register with bit 15 cleared.

INPUT STATUS WORD, REGISTER 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS ERROR BIT	PROM ADDRESS														

When the PROM Storage Module's Address Word Bit 15 is set, the PROM Storage Module's Address Bus is connected directly to the card's Data bus and therefore, is connected to the backplane's DATA BUS. The data retrieved from the card's Data Register will be the contents of the Address Register. The following sample diagnostic is provided:

```
                PROGRAM                    REMARKS

START LDA   PROM I/O
      OTA   02,C                     Enable the GR
      CLA
      INA
      RAR                            Set the Diagnostic Bit
      OTA   31B                      Read
NEXT  STC   PROM I/O                   and
      LIB   PROM I/O                     compare
      CPA   B                              returned
      RSS                                    data.
      JMP   ERROR
      INA
      CPA   LAST ADDRESS
      RSS
      JMP   NEXT
      HLT
      TEST  COMPLETE
```

3-8. DIRECT MEMORY ACCESS (DMA) FUNCTION

The PROM Storage Module is capable of transferring data directly into memory. All control logic and registers necessary to supervise the memory transfers are contained in the IOP Chip. Appropriate signals are available to signal when to enable the PROM's data onto the computer's Data Bus and when to initiate the next transfer. In addition, signals to the IOP Chip indicate when a data transfer is needed and when an interrupt-requesting condition has occurred.

Any given card has a maximum DMA rate at which it is capable of running. In order to achieve this maximum rate however, there can be no other requests on the backplane. Typically, there are other transactions on the backplane which degrade the maximum possible DMA rate. When the processor decides to fetch an instruction at the same time as an interface card is preparing for DMA, that DMA cycle can be held off for 908 ns. If an interface card is in the highest priority slot, it can be held off by the processor, or, in addition by a lower priority card doing DMA for a worst case of 454 ns per transfer. All DMA rate specifications given in Table 1-1 assume the card in question is plugged into the highest priority slot. When plugged into a lower priority slot, DMA rates can not be guaranteed when the additive rates of the higher priority cards are capable of consuming the total backplane bandwidth (2.72 Mbytes). Typically, however, even in a busy system, the backplane is only fully congested for very short periods of time, so that even the lowest priority I/O cards transfer at rates very close to their nominal specifications.

3-9. DMA CONTROL AND STATUS WORDS

Software DMA set-up and control involves six different control and status words, each of which is associated with a different register. Four of these registers (Registers 20-23) are located in the IOP Chip and the other two registers (Registers 30 and 31) are located on the circuit card. The six registers numbers and functions are as follows:

DMA Register Number 20, DMA Self-Configuration Register, In or Out

DMA Register Number 21, DMA Control Register, In or Out

DMA Register Number 22, DMA Address Register, In or Out

DMA Register Number 23, Word/Byte Count Register, In or Out

DMA Register Number 30, Data Register, In

DMA Register Number 31, Control Register, In or Out

Table 3-1. IOP Chip Instructions By Select Code

INSTRUCTION	FUNCTION	GR ON	GR=SC	IR=SC	NOTES
LI* 0	Read interrupt mask	X	Y	X	
MI* 0	Merge interrupt mask	X	Y	X	
OT* 0	Write interrupt mask	X	X	X	
CLF 2	Enable GR	X	X	X	
STF 2	Disable GR	X	X	X	
LI* 2 [,C]	Read GR	X	Y	X	1, 9
MI* 2 [,C]	Merge GR	X	Y	X	1, 9
OT* 2 [,C]	Write GR	X	X	X	
STC 2 [,C]	Enable Slave logic	X	X	X	1, 2
[,C]	Enable GR				
CLC 3	"BREAK" to front panel	X	X	X	2
HLT XX	"BREAK" to front panel	X	X	X	2
LI* 3	Read P SAVE	X	X	X	2
MI* 3	Merge P SAVE	X	X	X	2
OT* 3	Write P SAVE	X	X	X	2
LI* 3,C	Read ROM P	X	X	X	2
MI* 3,C	Merge ROM P	X	X	X	2
OT* 3,C	Write ROM P	X	X	X	2
SFC 20	Skip if FLG 20 clear	Y	Y	X	3
SFS 20	Skip if FLG 20 set	Y	Y	X	
CLF 20	Clear FLG 20 and FLG 21	Y	Y	X	
STF 20	Set FLG 20	Y	Y	X	
STC 20 [,C]	Enable DMA self configuration	Y	Y	X	
CLC 20 [,C]	Disable DMA self configuration	Y	Y	X	
LI* 20 [,C]	Read DMA configuration address	Y	Y	X	
MI* 20 [,C]	Merge DMA configuration address	Y	Y	X	
OT* 20 [,C]	Write DMA configuration address	Y	Y	X	
[,C]	Clear FLG 20 and FLG 21				
SFC 21	Skip if FLG 21 clear	Y	Y	X	4
SFS 21	Skip if FLG 21 set	Y	Y	X	
CLF 21	Clear FLG 21	Y	Y	X	
STF 21	Set FLG 21	Y	Y	X	
STC 21 [,C]	Enable DMA transfers	Y	Y	X	
CLC 21 [,C]	Disable DMA transfers	Y	Y	X	
LI* 21 [,C]	Read DMA Control word	Y	Y	X	
MI* 21 [,C]	Merge DMA Control word	Y	Y	X	
OT* 21 [,C]	Write DMA Control word	Y	Y	X	
[,C]	Clear FLG 21				
SFC 22	Skip if FLG 22 clear	Y	Y	X	5
SFS 22	Skip if FLG 22 set	Y	Y	X	
CLF 22	Clear FLG 22	Y	Y	X	
STF 22	Set FLG 22	Y	Y	X	
CLC 22 [,C]	Force DMA reconfiguration	Y	Y	X	
LI* 22 [,C]	Read DMA address	Y	Y	X	
MI* 22 [,C]	Merge DMA address	Y	Y	X	
OT* 22 [,C]	Write DMA address	Y	Y	X	
[,C]	Clear FLG 22				
SFC 23	Skip if FLG 20, FLG 21, AND FLG 22 ALL Clear	Y	Y	X	6
SFS 23	Skip if FLG 20 OR FLG 21 OR FLG 22 Set (inclusive OR)	Y	Y	X	
CLF 23	Clear FLG 20, FLG 21, and FLG 22	Y	Y	X	
CLC 23 [,C]	Terminate DMA operation	Y	Y	X	
LI* 23 [,C]	Read DMA Count	Y	Y	X	
MI* 23 [,C]	Merge DMA Count	Y	Y	X	
OT* 23 [,C]	Write DMA Count	Y	Y	X	
[,C]	Clear FLG 20, FLG 21, and FLG 22				

Table 3-1. IOP Chip Instructions By Select Code (Continued)

INSTRUCTION	FUNCTION	GR ON	GR =SC	IR =SC	NOTES
SFC 24	Skip if DMA disabled (DMAEN — asserted)	Y	Y	X	
SFS 24	Skip if DMA enabled (DMAEN — not asserted)	Y	Y	X	
LI* 24	Read Scratch 1	Y	Y	X	
MI* 24	Merge Scratch 1	Y	Y	X	
OT* 24	Write Scratch 1	Y	Y	X	
LI* 25	Read Scratch 2	Y	Y	X	
MI* 25	Merge Scratch 2	Y	Y	X	
OT* 25	Write Scratch 2				
LI* 26	Read Scratch 3	Y	Y	X	
MI* 26	Merge Scratch 3	Y	Y	X	
OT* 26	Write Scratch 3	Y	Y	X	
SFC 30	Skip if FLG 30 clear	Y	Y	X	7
SFS 30	Skip if FLG 30 set	Y	Y	X	
CLF 30	Clear FLG 30	Y	Y	X	
STF 30	Set FLG 30	Y	Y	X	
STC 30 [,C]	Set CNTRL 30 and issue DVCMD	Y	Y	X	
CLC 30 [,C]	Clear CNTRL 30	Y	Y	X	
LI* 30 [,C]	Read device data	Y	Y	X	
MI* 30 [,C]	Merge device data	Y	Y	X	
OT* 30 [,C]	Write device data	Y	Y	X	
[,C]	Clear FLG 30				
LI* 31	Read interface control word	Y	Y	X	
MI* 31	Merge interface control word	Y	Y	X	
OT* 31	Write interface control word	Y	Y	X	
LI* 32	Read interface status	Y	Y	X	8
MI* 32	Merge interface status	Y	Y	X	
OT* 32	Reset interface status	Y	Y	X	9
SFC SC	Skip if FLG 30 clear	N	X	Y	7
SFS SC	Skip if FLG 30 set	N	X	Y	
CLF SC	Clear FLG 30	N	X	Y	
STF SC	Set FLG 30	N	X	Y	
STC SC [,C]	Set CNTRL 30 and issue DVCMD	N	X	Y	8
CLC SC [,C]	Clear CNTRL 30	N	X	Y	
LI* SC [,C]	Read device data	N	X	Y	10
MI* SC [,C]	Merge device data	N	X	Y	10
OT* SC [,C]	Write device data	N	X	Y	
[,C]	Clear FLG 30				

SC = Interface select code

Notes:

1. The [,C] is always executed even if the primary instruction is not.
2. The SLAVE logic must be enabled; i.e., SLRQ LOW at power up.
3. FLG 20 is set by DMA upon completion of self configured DMA block transfer which is not to be followed by another self configuration.
4. FLG 21 is set by DMA upon completion of any block transfer which is not to be followed by a self configuration.
5. FLG 22 is set by DMA if a parity error occurs during a DMA read.
6. FLG 23 is the logical OR of flags 20 through 22.
7. FLG 30 and CNTRL 30 are controlled by the Flag and Control flip-flops located in the IOP chip.
8. The IOP chip indicates only that the select code is in the range 32 to 77, it is up to the user to decode any specific select code.
9. Serial I/O cards, by convention, use this instruction as a card reset.
10. When the IOP chip is in diagnose mode, these instructions fetch the following:

    Diagnose mode 1 — the interface's select code and ID word.
    Diagnose mode 2 — the global register and IOP chip status bits.

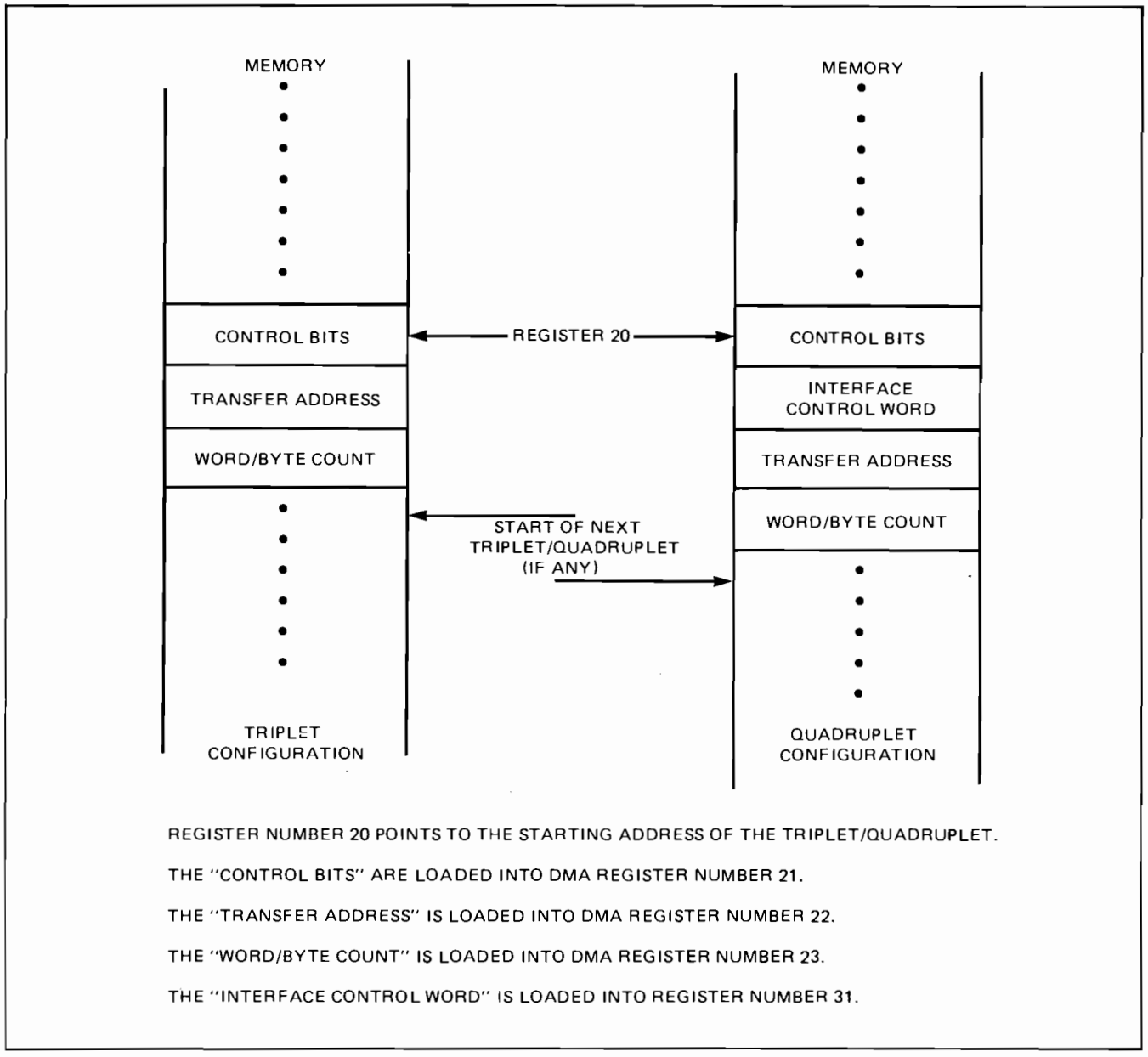


Figure 3-2. DMA Self-Configuration Formats

3-10. DMA SELF-CONFIGURATION, REGISTER 20

The DMA self-configuration register contains the address of the DMA triplets or quadruplets. A DMA triplet (see Figure 3-2) is of the form: control bits, transfer address, and word/byte count. The triplet words are the words to be used in registers 21,22, and 23, respectively. A DMA quadruplet (see Figure 3-2) is of the form: control bits, interface control, transfer address, and word/byte count. These words are to be put into registers 21, 31, 22, and 23, respecitvely.

3-11. DMA CONTROL WORD 1, REGISTER 21

The bit definitions for the DMA control word 1 are as follows:

DMA CONTROL WORD 1, REGISTER 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	DV CMD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	RESERVED						

Bits 0-6: Reserved

Bit 7: IN

1= Indicates that the direction of the data transfer is from the PROM Storage Module to memory.

0= not used

Bit 8: AUTO

AUTO has different meanings depending on whether bit 7 (IN) is set.

1= Last input transfer will be followed by a DVCMD pulse.

0= The last DVCMD pulse will be suppressed.

Bit 9: FOUR

1= Indicates that there are four words to be fetched for the current DMA configuration. Loads Register 31 as part of a DMA quad.

0= Indicates that there are three DMA control words to be fetched for the current DMA configuration. Register 31 must be loaded separately prior to triplet.

Bit 10: REM Remote Memory

1= All memory requests will be accomplished by the REMEM (Remote Memory) signal, that disables standard memory and enables remote memory.

0= Remote memory not enabled.

Bit 11: CINT Completion Interrupts

1= Inhibits DMA transfer completion interrupts.

0= Completion interrupt is to be requested by DMA logic when word/byte count rolls over (goes from −1 to 0).

Bit 12: RES Residue

1= If set, and if DMA is enabled to self-configure, i.e., a STC 20 has been executed, DMA will write its word/byte count residue into the location from which it read the word/byte count.

0= Word/byte count is not written.

Bit 13: BYTE

1= Indicates that the DMA transfer is to be conducted in byte mode, i.e., each data transfer is counted as one byte. Byte mode transfers are packed, two bytes per word, with the left byte (bits 15-9 of the data word) being transferred first.

0= Each data transfer will be a full 16-bit word.

Bit 14: DVCMD Device Command

1= DMA control logic will issue a Device Command (DVCMD) signal immediately following each data transfer from the interface logic.

0= Device Command is not issued.

Bit 15: CONT Control

1= If set and an STC 20 has been executed, then at the end of a DMA transfer the IOP Chip will fetch the next set of DMA control words and reconfigure itself to start a new transfer.

0= DMA will stop at the end of the current transfer.

3-12. DMA ADDRESS, REGISTER 22

DMA control word 2 is the 15-bit (bits 0-14) address of the next memory location to be accessed by DMA. The most significant bit (bit 15) cannot be controlled by OTA 22 or OTB 22 and will be the complement of control word 1, bit 7 (IN) when fetched by an LIA 22.

3-13. DMA WORD/BYTE COUNT, REGISTER 23

The word/byte count register, register 23, is a 16-bit register whose value is the two's complement of the number of data elements to transfer. A data element may be either a word or a byte, as indicated by bit 13 (BYTE) of the DMA control word, contained in register number 21.

The end of a data transfer is indicated by the transition of the word/byte count register's value from −1 to 0. Rollover from 177777 octal to 000000 occurs at this same time. This allows up to 65,536 data elements to be transferred at any one time. The memory size (32,768 words maximum) limits a word transfer to a length of 32,768 words or 65,536 bytes. The hardware does not detect this, however, so it is up to the programmer not to exceed this limit.

3-14. DMA TRANSFER OPERATION

A DMA transfer is started by configuring the DMA control register, DMA address register, word/byte count register, and the output control word register, and then issuing a STC instruction to register 21 (DMA Control Register).

3-15. DMA INPUT TRANSFER

A DMA input transfer is defined as being from the PROM Storage Module to memory. The transfer must be in Word mode. To start the transfer, a Device Command (DVCMD) signal and a memory access signal are generated immediately. The memory request goes directly to the backplane where memory access priority is determined by

the location of the requesting card with respect to the processor card (the closer the card is to the processor, the higher the card's priority). When the memory access request is granted, the data is transferred, the DMA word/byte count, and DMA address registers are incremented, and the DMA control logic is ready to accept another data transfer request.

3-16. DMA OUTPUT TRANSFER

The DMA output transfer function is not used on the PROM Storage Module.

3-17. DMA TRANSFER TERMINATION

A DMA data transfer continues as described in paragraph 3-15 until a terminating condition is detected. The terminating conditions are as follows:

a. Word count transition from −1 to 0. (Rollover from 177777 octal to 000000 occurs.) This indicates that all the data elements that were to be transferred have been transferred.

b. Detection of a Control Reset (CRS) signal. This signal is generated by the processor card during its power-up sequencing, or by execution of a CLC 0 instruction.

c. Parity error indication from memory.

3-18. DMA SELF-CONFIGURATION FEATURE

Available in the IOP Chip is circuitry that enables the DMA registers (discussed in the preceding paragraphs) to be loaded directly from sequential memory locations. Upon completion of each successive DMA operation, the contents of register 20 are used as a pointer to the location in memory containing the next set of values to be loaded into registers 21, 22, and 23. As each register is loaded, the contents of register 20 are incremented, leaving register 20 pointing to the values to be used for the next transfer.

3-19. DMA SELF-CONFIGURATION INITIALIZATION

The DMA self-configuration feature is initialized by setting the value of register 20 to the memory address of the first word of a list of DMA triplets or quadruplets. A triplet is of the form: control bits, transfer address, and word/byte count. The triplet words are the words to be used in registers 21, 22, and 23, respectively. A quadruplet is of the form: control bits, card control word, transfer address, and word/byte count. The quadruplet words are to be loaded into registers 21, 31, 22, and 23, respectively. Bit 8 of the control word is used with both a triplet or quadruplet. Figure 3-2 illustrates the formats of both the triplets and quadruplets.

Once the DMA self-configuration feature is initialized by setting the value of register 20 equal to the memory address of the first word of a list of DMA triplets or quadruplets, an STC to register 20 starts the feature. This STC instruction to register 20 has the effect of simultaneously setting the control on registers 20 and 21 to achieve an initial state for full execution.

3-20. DMA SELF-CONFIGURATION OPERATION

After receiving the STC instruction from register 20, the self-configuration control logic fetches the word addressed by the contents of register 20 and loads this word into register 21. Assume bit 7 of this word is set, signifying a quadruplet. The contents of register 20 are incremented during the memory access. The new value of register 20 is used as the address of the next memory read. This next word is loaded into the control register on the PROM Storage Module by means of a virtual OTA 31 generated by the IOP Chip. Register 20 then is incremented for the next read and this new data is loaded into register 22. Register 20 is again incremented. The new value of register 20 is used to address the fourth word of the current quadruplet. This fourth word is loaded into register 23. The value of register 20 is again incremented, pointing to the beginning of the next triplet/quadruplet. The DMA operation just loaded is then started as soon as the interface is ready (see paragraph 3-15). When the DMA operation terminates (see paragraph 3-18), if bit 11 of register 21 is clear, an interrupt request is generated. If the DMA operation terminated due to either an end-of-transfer indication from the interface or a word/byte count transition from −1 to 0, and bit 12 of register 21 is set, the DMA self-configuration logic writes the word-count residue into the location formerly occupied by the current DMA operation's word/byte count. Operation of the self-configuration feature is continued, as previoulsy noted, for the next triplet/quadruplet.

3-21. DMA SELF-CONFIGURATION TERMINATION

The operation of the DMA self-configuration feature continues as described in paragraph 3-20 until one of the following events occurs:

a. A CLC instruction to register 20 is executed. This serves to inhibit the self-configuration logic from advancing its pointer to the next triplet, while still allowing the current DMA to continue. An STC instruction to register 20 allows the self-configuration feature to continue.

b. A CLC instruction to register 21 is executed. This stops the current DMA operation at its present state of operation.

c. A CLC instruction to register 22 is executed. This aborts the current DMA operation and causes the

self-configuration logic to advance to the next triplet/quadruplet. No interrupt is generated by the aborted transfer.

d. A CLC instruction to register 23 is executed. This stops the operation of the self-configuration logic and aborts the transfer in progress.

e. The first word of a triplet is read with the CONT bit (DMA Control Word 1) clear, indicating that there are no more DMA triplets. This sets the flag on register 20, which generates an interrupt request if the control flip-flop of register 20 is set.

3-22. PROGRAMMING EXAMPLES

The PROM Storage Module requires a control word and a start command to provide the computer's memory with data word. The control word provides the PROM Storage Module with the 15 bit address that the PROM Storage Module will use to fetch the data word. The control word can be transferred to the PROM Storage Module using an OTA 31B instruction with the global register containing the select code of the PROM Storage Module, or as the second word of the four word DMA quadruplet configuration. The start command initiates the PROM card's read and is generated by sending a set control command to the PROM Storage Module, either by an STC instruction or by DMA. The result of the read is available immediately under program control so that flag tests are not required. Blocks of data can be transferred without retransferring the control word. The PROM Storage Module's address is automatically incremented at the beginning of each successive transfer. Two sample programs are shown in Table 3-2 using both the DMA and non-DMA operations.

3-23. DETAILED PROGRAMMING EXAMPLE

For this example the PROM Storage Module is considered to have two programs burned into it. One program starts at address 0 octal and continues through 231 octal and the other starts at 232 octal and continues through 177777 octal. These programs are to be executed sequentially and are to be loaded using DMA. The PROM Storage Module is assigned select code 22 and the memory system has 64k bytes of available memory. The sample program is listed in Table 3-3.

3-24. WORD FORMAT SUMMARY

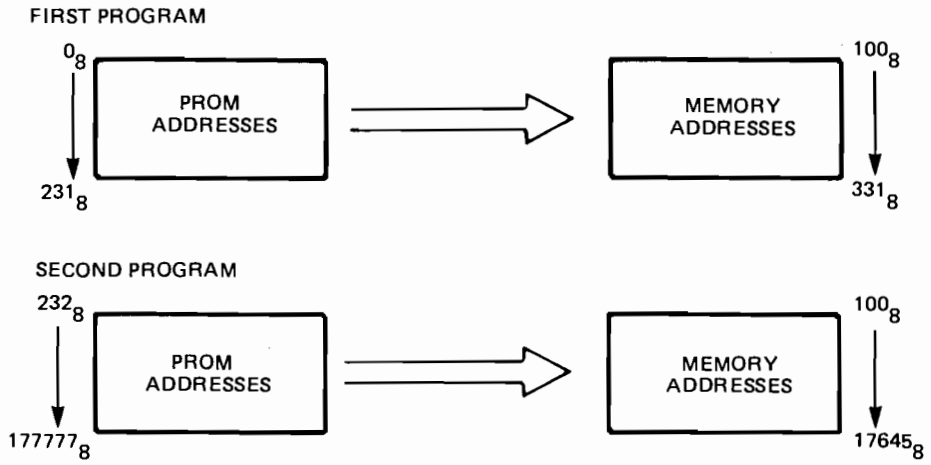
Figure 3-3 contains a reference guide to all control and data word formats for the PROM Storage Module.

Table 3-2. Sample DMA and Non-DMA Operations

```
DMA

LDA PRMSC   GET PROM SELECT CODE
OTA 2,C     SET GR AND ENABLE
LDA DMACW   GET DMA CONTROL WORD
OTA 21B     PASS IT TO PROM CARD
LDA DMAAD   DO THE SAME FOR ADDRS
OTA 22B
LDA DMACN   AND FOR TRANSFER COUNT
OTA 23B
LDA PRMAD   GET ADDRESS ON PROM CARD
OTA 31B     PASS IT TO PROM CARD
STC 21B,C   START TRANSFER
  .
  .
  .
```

```
PROGRAM CONTROL (NON-DMA)

LDA PRMSC   GET PROM SELECT CODE
OTA 2,C     SET GR AND ENABLE
LDB PRGAD   GET PROGRAM STARTING ADDRESS
LDA PRGAD   GET PROM CARD ADDRESS
OTA 31B     PASS ADDRESS TO PROM CARD
STC 30B,C   TRANSFER ONE WORD#
LIA 30B     GET DATA FROM PROM CARD
STA B,I     PUT DATA IN MEMORY
INB         MOVE TO NEXT ADDRESS IN MEMORY
CPB PRGLA   IS THIS THE LAST ADDRESS?
RSS
JMP *-6     NO DO NEXT WORD
  .
  .
  .

 # ALSO INCREMENTS ADDRESS ON PROM CARD
```

Table 3-3. Detailed Programming Example




```
ASMB,AL
        ORG 20B
PROM    OCT 22          SELECT CODE OF PROM CARD
GLOB    EQU 2B          SELECT CODE OF GLOBAL REG
DMA1    OCT 52200       DMA CONTROL WORD 1
DMA2    OCT 100         DMA CONTROL WORD 2
DMA3A   OCT 177546      DMA WORD COUNT A
DMA3B   OCT 160232      DMA WORD COUNT B
DMA4A   OCT 0           PROM CONTROL WORD A
DMA4B   OCT 232         PROM CONTROL WORD B
START   LDA PROM
        OTA GLOB,C      SET UP THE GLOBAL REG
        LDA DMA1
        OTA 21B         SET UP DMA
RELOD   LDA DMA2
        OTA 22B           TO LOAD
        LDA DMA3A
        OTA 23B             THE FIRST
        LDA DMA4A
        OTA 31B                PROGRAM
        STC 21B,C       START DMA
        SFS 21B         WAIT FOR DMA
        JMP *-1           TO COMPLETE
        JSB 100B        EXECUTE THE LOADED PROGRAM
        LDA DMA2
        OTA 22
        LDA DMA3B
        OTA 23B         SET UP DMA TO
        LDA DMA4B
        OTA 31B           LOAD THE SECOND PROGRAM
        STC 21B,C       START DMA
        SFS 21B         WAIT FOR DMA
        JMP *-1           TO COMPLETE
        JSB 100B        EXECUTE THE SECOND PROGRAM
        JMP RELOD
      END
```

CONTROL WORD REGISTER 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PROM ADDRESS														

Diagnostic Bit

INPUT STATUS WORD, REGISTER 31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDRESS ERROR BIT	PROM ADDRESS														

DMA SELF-CONFIGURATION, REGISTER 20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POINTER TO DMA TRIPLET/QUADRUPLET															

DMA CONTROL WORD 1, REGISTER 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	DV* CMD	BYTE*	RES	CINT	REM	FOUR	AUTO*	IN	RESERVED						

* Bit 14 must be a 1 and Bits 8 and 13 must be 0.

DMA ADDRESS, REGISTER 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA ADDRESS														

DMA WORD/BYTE COUNT, REGISTER 23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA WORD/BYTE COUNT															

DMA WORD MODE DATA, REGISTER 30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB ←															→ LSB

Figure 3-3. Word Format Reference Summary

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION

This section provides information on the theory of operation of the PROM Storage Module, first at the block level (overview) and then at the functional level. The theory will cover individual components only when they serve a unique purpose.

In order to achieve a complete understanding of the PROM Storage Module, a copy of the HP 1000 L-Series Interfacing Guide, part number 02103-90005 should be available.

4-2. GENERAL DESCRIPTION

The HP 12008A PROM Storage Module provides the L-Series Computer with the capability of transferring up to 64k bytes of data into main memory. The data can not be executed directly from the PROM Storage Module but must first be loaded into main memory and then executed.

Figure 4-1 shows the card in a typical L-Series system. As shown in the figure, the card can be installed in any I/O slot below the processor card (highest priority I/O slot).

The PROM Storage Module is a computer input device that is capable of storing up to 64k bytes of data or programs in PROMs. The minimum segment of data is 4k bytes which requires two PROM packages. The PROM packages are addressed by a 15-bit control word and consecutive locations may be read by simply passing the PROM Storage Module a Device Command (DVCMD) between reads. A DVCMD signal is generated upon execution of a STC 30 instruction, or during DMA, it is generated between data transfers if the STC bit of the first DMA control word is set. The PROM Storage Module access time is fast enough that flag testing is not necessary between reads.

As noted in Section I, the card contains an I/O Master Section and a PROM Interface Section. The I/O Master Section gives the card the capability of handling its own Direct Memory Access (DMA) and of decoding its own instructions from the processor. The I/O Master Section is composed of the I/O Processor Chip (U67) and its associated logic circuitry and performs all of the functions necessary for interfacing with the L-Series backplane. The PROM Interface Section is composed of the 32 PROM packages, the Address Counter/Register, and the associated control logic circuits.

A six-bit select code for the card is set by the DIP switches (U1S3-U1S8) located on the card. This select code is used only as a means of addressing the card and bears no relation to or interrupt the DMA priority of the card. The interrupt and DMA priorities are determined solely by the physical location of the card from the processor card in the card cage. The card slots are marked from XA1 (highest priority) to XA10 or XA16 (lowest priority). The number depends on the size of the backplane.

4-3. THEORY OF OPERATION OVERVIEW

The simplified block diagram shown in Figure 4-2 illustrates the basic operation of the PROM Storage Module in an L-Series system.

The main flow of data is from the PROM Storage Module into the main memory via the computer's backplane. Status and address commands flow from the processor card via the computer's backplane into the PROM Storage Module. The status and address data is put into main memory so that it can be examined.

The computer's processor card issues a 16-bit control word to the PROM Storage Module. It is stored in the 16-bit Control Register/Counter when the Control Logic produces a LDCNT- signal. The Address Register/Counter puts the 11 bits (RA0-RA10) onto the Buffered Address Bus which are then applied to the address inputs of the PROM chips. The Address Bits (RA11-RA14) are applied to the Chip Select Logic to produce the eight Upper Select Bits (US0-US7) and the eight Lower Select Bits (LS0-LS7) that are used to select the 16-bits of data from the 16 lower or 16 upper PROM chips. The Buffered Address Bus is also applied to the Address Buffer. When RA15 is set, the Address Buffer outputs the 16-bits of address into the Data Buffer. When the Control Logic is issued a status instruction, the Data Buffer puts the 16 bits of address onto the Data Bus and into the main memory via the backplane. The 16-bit output of the PROM chips (RO0-RO15) is applied to the Data Buffer directly and not through the Address Buffer. When the Control Logic receives a load data command, it enables the Data Buffer to put the 16-bit data word onto the Data Bus and into main memory via the backplane.

4-4. FUNCTIONAL THEORY OF OPERATION

It is necessary to refer to the Overall Functional Block Diagram (Figure 7-2) and the three Schematic Logic Diagrams (Figure 7-4) that are to be found in Section VII when reading this section of the manual. It may be necessary to refer to the HP 1000 L-Series Interfacing Guide, part number 02103-90005 to achieve a full understanding of

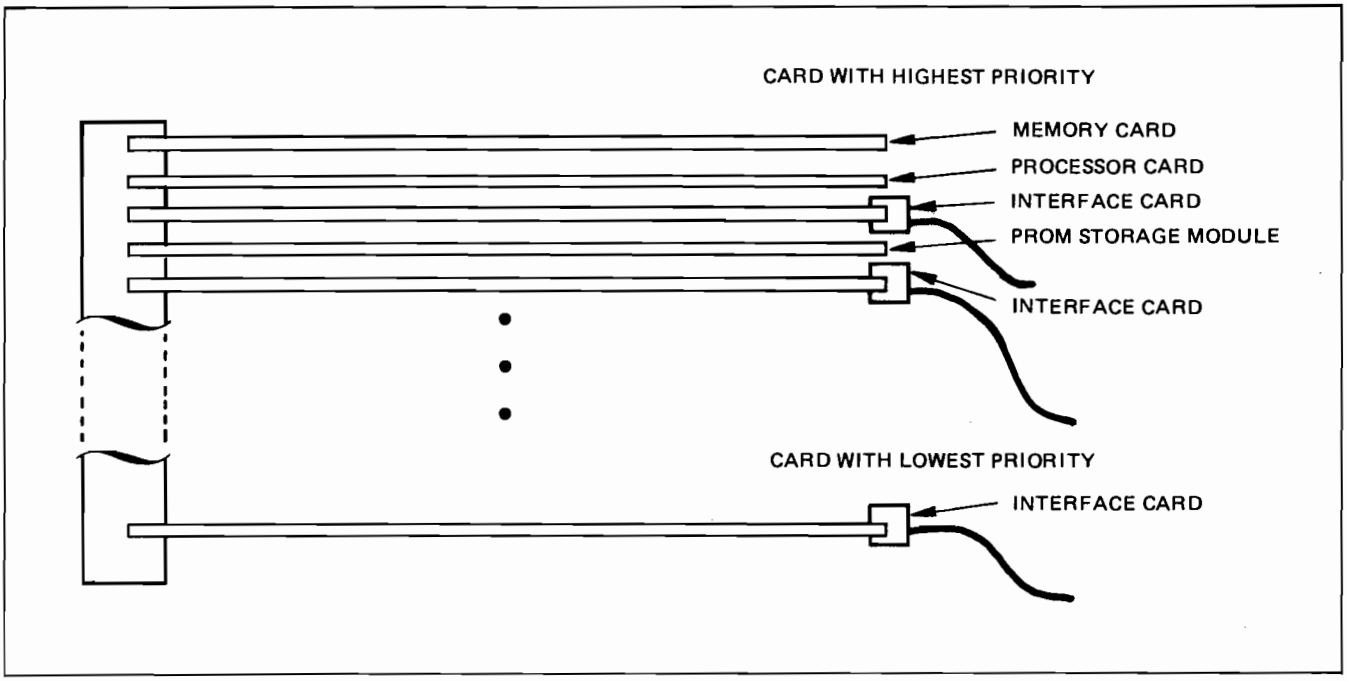
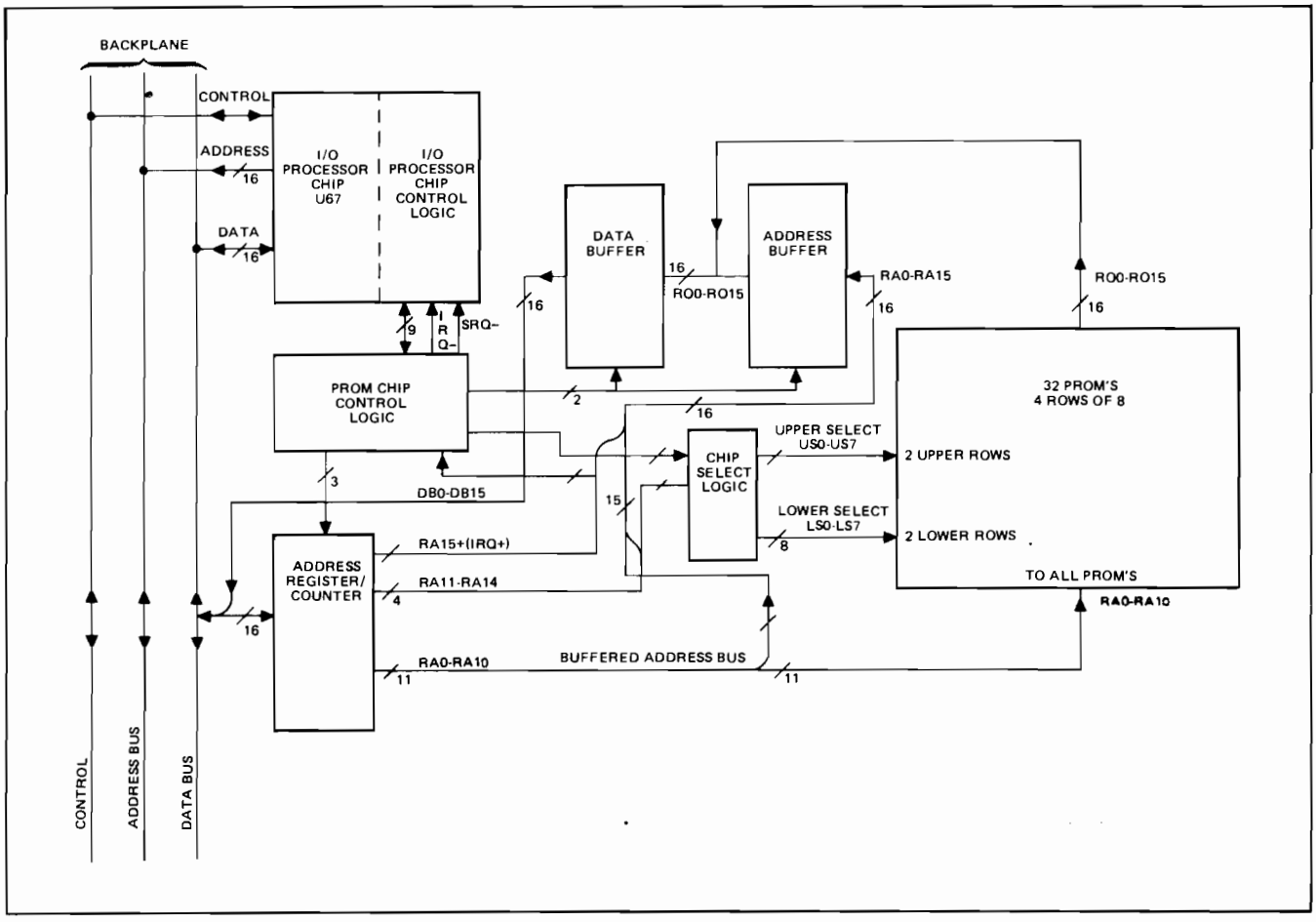


Figure 4-1. Typical L-Series System



7700-486

Figure 4-2. Simplified Block Diagram of the PROM Storage Module

the theory of operation for this card. Integrated circuit base diagrams and function tables are provided in Figure 7-1 for the I/O Processor Chip and all IC's that are used on this card.

To simplify locating components on the three schematics, the following scheme is used. There are 10 numbers across the top and bottom borders of the schematics, going from 10 to 19, 20 to 29, and 30 to 39. The first number indicates the sheet number,i.e., 1, 2, or 3, and the second number is the vertical column. A set of five alphabetical letters,i.e., A-E, on the left and right borders of the schematics are used to form 50 easy to locate areas on the schematics. To make the coordinates easy to find in the text, they are set off in brackets []. For example, [23B,C] would be found on the second sheet, column number 3, and horizontal rows B and C. The Handshake Flip-Flop circuit is to be found at this location. In some cases, the coordinates may consist of multiple numbers and only one letter,i.e., [25,26D], or they may be multiple letters and multiple letters,i.e., [32-38B-E]. These are the coordinates for the location of the 32 PROM chips.

The PROM Storage Module performs three main functions, they are as follows:

a. Data Mode Transfer, paragraph 4-6

b. Status Transfers, paragraphs 4-7 and 4-8

c. Diagnostic Mode Transfer, paragraph 4-9

4-5. DATA MODE TRANSFER

4-6. INPUT DATA TRANSFER

The computer passes the PROM Storage Module's address of the desired data to the PROM Storage Module's Address Register/Counter, U35, U45, U55, and U65, four 74LS193's [21B-D], by an OTA 31 instruction in the Programmed Mode with the global register enabled or by the card control word in the quadruplet DMA configuration. The 16-bit control word is stored in the 16-bit Address Register/Counter when the Load Count Gate, U17 [23D], a 74LS32, produces a LDCNT- signal (U17 pin 3) from the signals BCS2- (STCNTRL-) and CKDAT-. The LDCNT- signal also clears the Handshake F-F U16 [23B], a 74LS74, thus preventing U17 pin 8 from producing a INCCNT- (Increase Count) signal that would increment the Address Register/Counter.

The address Register/Counter provides 11 bits (RA0-RA10) of address onto the Buffered Address Bus and four bits (RA11-RA14) to the Chip Select Decoder, U85 and U95 [31A,B], two 74S138's. When bit RA14 is set, it selects the lower 16 PROM chips and when it is cleared, it selects the upper 16 PROM chips. The 11 bits (RA0-RA10) on the Buffered Address Bus are applied directly to each PROM chip. The Upper and Lower Select Bits (US0-US7 and LS0-LS7) each select one set of two PROM chips. That is, the Lower Select Bit 0 (LS0) enables PROM chips U83 and U84 [32,33C-D], producing two eight-bit bytes that are applied to the Address Buffer, U15 and U105 [26,27B-D], two 74LS244's.

To read the data in the Address Buffer, it is necessary to send the PROM Storage Module a Device Command (DVCMD-). The DVCMD- signal and the SCLK+ signal are combined and produce at U17 pin 6 a signal that sets the SRQ F-F [23B]. The SRQ- signal from U16 pin 8 signals the I/O Master that data is ready to be transferred to the main memory. The I/O Master produces a BCS5- (LDDATA-) signal that is a result of an LIA from the Data Register or a DMA transfer. The data can be re-read by repeating the LIA instruction. The BCS5- signal applied to U26 pin 8 [23C], a 74LS08, enables the Data Buffer, U25 and U75 [25B-D], two 74LS244's, to put the 16-bit data word (DB0-DB15) onto the Data Bus. A new data word can be selected by reloading the Address Register/Counter and then reading the data from the Data Buffer. The next sequential address can be read by issuing a DVCMD- signal. The DVCMD- signal causes U17 pin 8 [23B], a 74LS32, to produce an INCCNT- (Increase Count) signal that is applied to the Address Register/Counter and increments the address by one count each time the DVCMD- signal is issued after the first read is initiated.

The Address Register/Counter is cleared on power-up by the PON- signal being applied to the CLR input (pin 14). The Handshake F-F U16 [23B] is cleared on power-down by the PON+ signal and is held in the clear state until PON+ goes positive after power-up.

When the DVCMD- and the SCLK+ signals cause the SRQ F-F to assert the SRQ- (Service Request) signal from U16 pin 8, it initiates a data transfer. The I/O Master asserts an SACK- (SRQ Acknowledge) signal and it remains asserted until the SRQ- signal is cleared. The SACK- signal causes the CLR input (U16 pin 13) to go low and clear the SRQ flip-flop, setting SRQ- high.

4-7. STATUS TRANSFERS

The PROM Storage Module has two status modes: A Status Word Mode, and an Interrupt Response Mode.

4-8. STATUS WORD MODE

In the Status Word Mode, the 15 bits of address (RA0-RA14) and one bit (RA15) that indicates the status of the Interrupt Request F-F part of U65 [31B], (the D section of a four bit counter). U65 pin 7 is the flip-flop's output. The Interrupt F-F is set when the Address Register/Counter exceeds 77777 (octal) bytes. The Interrupt F-F is cleared by loading a valid address into the Address Register/Counter. The Address Register/Counter's output is loaded into the Address Buffer (U15 and U105) when BCS6- (LDCNTRL-) is asserted causing U26 pins 6 and 8 [23C] to go low. These two outputs allow the 16 address bits (RA0-RA15) to be loaded onto the Data Bus via U15, U25, U75, and U105. The Interrupt F-F asserts IAK- until it is cleared by a valid address being loaded into the Address Register/Counter.

4-9. INTERRUPT RESPONSE MODE

When RA15+ is set, the Chip Select Decoder, U85 and U95 [31A,B], is disabled by the RDAR- signal and the contents of the Address and Data Buffers, (U15, U25, U75, and U105), are driven onto the Data Bus.

4-10. TIMING CONSIDERATIONS

The only area of critical timing is the delay caused by the PROM chips under a DMA transfer. The DVCMD- signal increments the 74LS193 counters (U35, U45, U55, and U65) and generates the SRQ- to the I/O Master, indicating that data is ready.

The minimum latency for service of the SRQ- signal is 900 ns after the trailing edge of the DVCMD- signal (refer to Figure 4-3). The Address Register/Counter has a maximum delay (count to Q) of 47 ns past the trailing edge of the DVCMD- signal, plus 450 ns of delay (address to data) within the PROM chips, making the data ready for enabling onto the Data Bus in 497 ns. Therefore, there is a wide safety margin in the timing.

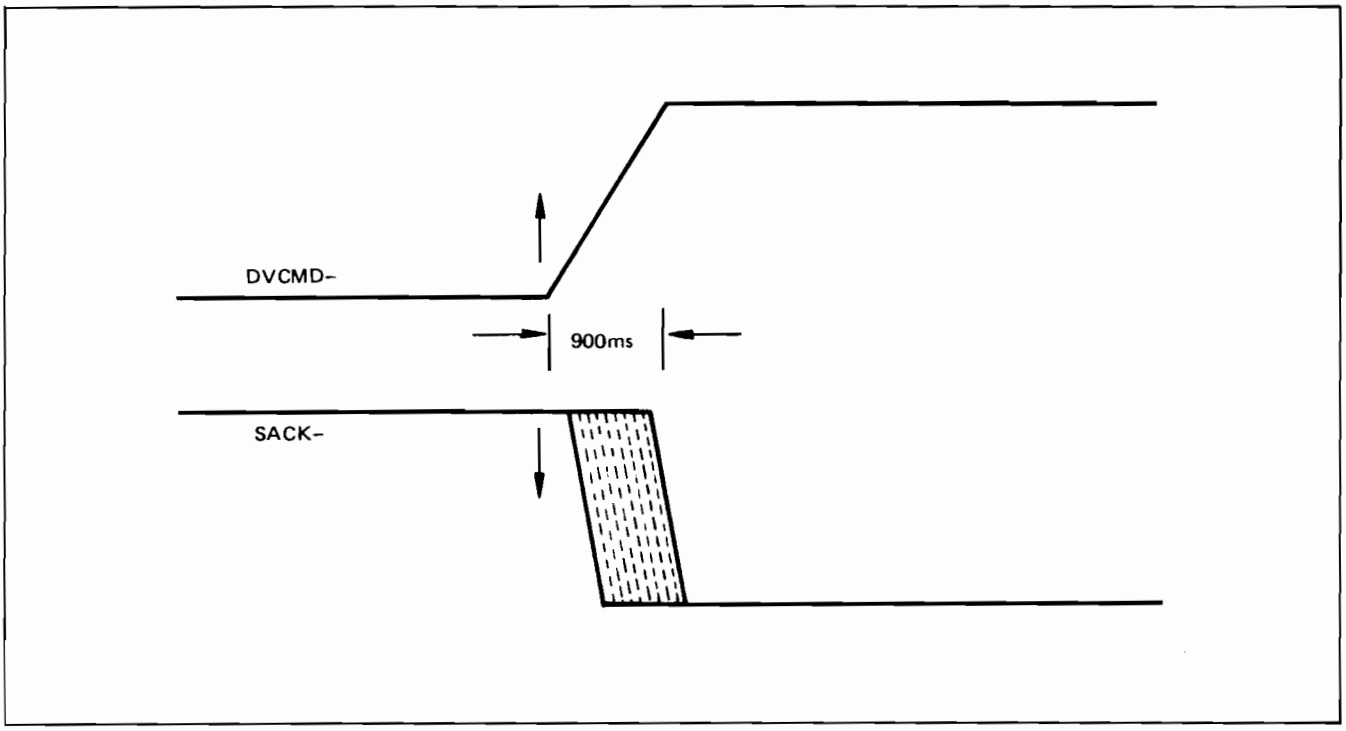


Figure 4-3. DVCMD- and SACK- Latency Timing

MAINTENANCE

SECTION V

5-1. INTRODUCTION

This section provides maintenance information for the HP 12008A PROM Storage Module. Included are preventive maintenance instructions and troubleshooting information.

5-2. PREVENTIVE MAINTENANCE

Preventive maintenance for the PROM Storage Module is performed at the same intervals as for the computer system.

CAUTION

STATIC SENSITIVE DEVICE. Use antistatic handling procedures when handling the printed circuit assemblies.

Preventive maintenance consists of inspecting the card for burned or broken components, or the presence of foreign material. After any damage has been repaired, run the system self-test. (Refer to the HP 1000 L-Series Installation and Service Manual, part no. 02145- 90003.) If it is determined that the card is malfunctioning, perform the troubleshooting procedures listed in paragraph 5-6.

5-3. REMOVAL AND INSTALLATION PROCEDURES FOR THE I/O PROCESSOR CHIP (U67)

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS. Wear safety glasses when removing or installing the retaining clips on the SOS chip sockets.

CAUTION

STATIC SENSITIVE DEVICE
Use antistatic handling procedures while removing or installing the SOS chips.

5-4. REMOVING THE SOS CHIP FROM ITS SOCKET

The chip is removed from the socket in the following manner:

1. With the card removed from the computer, place the card on a flat surface.
2. While pressing down on one of the retaining clips with a thumb, insert the flat blade of a screwdriver or similar instrument between the retaining clip and the side of the socket (B).
3. Twist the bottom portion of the blade away from the socket to free the retaining clip (A) from the bottom edge of the socket (refer to Figure 5-1).
4. When the retaining clip (A) is free, lift it up and over the chip.
5. Remove the second retaining clip by following steps 2 through 4.
6. Carefully tip the card on edge and remove the chip. Observe all the antistatic handling precautions while handling the chip.
7. Do not put retaining clips back on an empty socket as it will distort the socket's contacts.

5-5. INSTALLING THE SOS CHIP IN ITS SOCKET

The chip is installed in the socket in the following manner:

1. Observe all the antistatic handling precautions while handling the chip.
2. Place the card on a flat surface with the component side up.
3. Locate both retaining clips.
4. Place the chip in the socket, locating the two flat corners (C) of the socket facing the two flat corners of the chip. The trace side of the SOS chip package must be on the bottom side when the chip is placed in the socket.
5. Place the retaining clips in the two places provided for them in the side of the socket.

6. Press down with a thumb on the retaining clip (A) and press the retaining clip over the edge of the socket until it snaps under bottom edge of the socket (B).

7. Install the second retaining clip in the same manner, following steps 5 and 6.

5-6. TROUBLESHOOTING

To troubleshoot the PROM Storage Module , perform the following steps:

1. Run the computer self-test. Refer to the HP 1000 L-Series Computer Installation and Service Manual, part no. 02103-90003; or the HP 1000 L-Series Computer System Installation and Service Manual, part no. 02145-90003.

2. Run the kernel diagnostic. Refer to the Kernel Diagnostic Operating Manual, part no. 24397-90002.

3. Run the PROM Storage Module diagnostic. Refer to the PROM Storage Module Diagnostic Operating Manual, part no. 24397-90008.

4. If the card is defective, contact the nearest Hewlett-Packard Sales and Service Office for information on repair or replacement of the interface. The Sales and Service Offices are listed in the back of this manual.

5. Further isolation to a defective component may be performed, if necessary, using an oscilloscope or logic analyzer. Refer to Section VII, Figure 7-1 for integrated circuit pin connections and logic functions, to Figure 7-2 for a functional block diagram, to Figure 7-3 for a component location diagram, and to Figure 7-4 for the schematic logic diagram. Refer to Section VI, Table 6-3 for replaceable parts information.

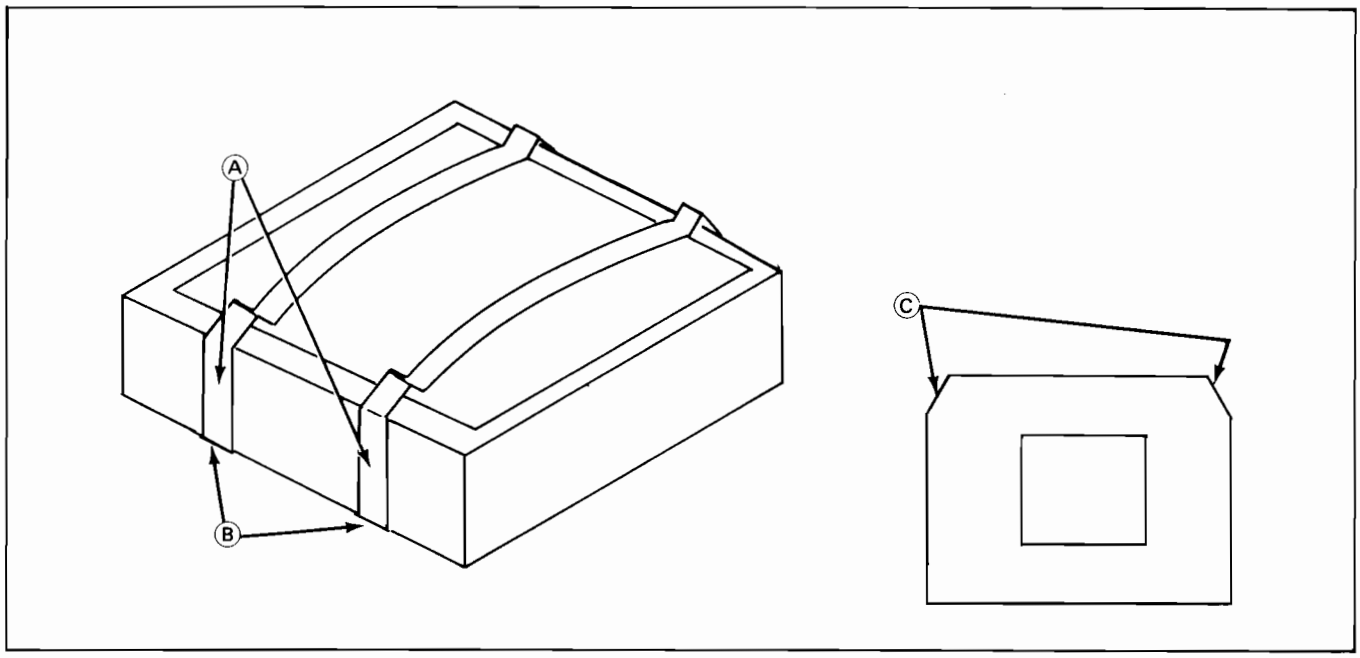


Figure 5-1. IOP Chip Socket With Retaining Clips

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section contains information for ordering replaceable parts for the HP 12008 PROM Storage Module. Table 6-1 is a list of exchange board part numbers, Table 6-2 lists the meanings of the reference designations and abbreviations used in the table of replaceable parts, Table 6-3 is the list of replaceable parts, and Table 6-4 contains the names and addresses of manufacturers of the parts.

6-2. REPLACEABLE PARTS

Table 6-3 contains the list of parts in reference designation order. The following information is listed for each part:

a. Reference designation of the part. Refer to Table 6-2 for an explanation of the abbreviations used in the "Reference Designation" column.

b. The Hewlett-Packard part number.

c. Part number check digit (CD).

d. Total quantity (QTY).

e. Description of the part.

f. A five-digit manufacturer's code number of a typical manufacturer of the part.

g. The manufacturer's part number.

6-3. ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (a list of Sales and Service Offices is given in the back of this manual).

To order a part listed in the replaceable parts list, give the Hewlett-Packard part number with the check digit, and indicate the quantity required. The check digit will ensure accurate and timely processing of the order.

To order a part that is not listed in the replaceable parts list, specify the following information:

a. Identification of the product containing the part (refer to Section I, paragraph 1-5).

b. Description and function of the part.

c. Quantity required.

Table 6-1. Exchange Board Part Numbers

Exchange Card Without IOP Chip (U67)	New Card With IOP Chip
12008-69001	12008-60001

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly
B	= motor, synchro
BT	= battery
C	= capacitor
CB	= circuit breaker
CR	= diode
DL	= delay line
DS	= indicator
E	= Misc electrical parts
F	= fuse
FL	= filter
J	= receptacle connector
K	= relay
L	= inductor
M	= meter
P	= plug connector
Q	= semiconductor device other than diode or integrated circuit
R	= resistor
RT	= thermistor
S	= switch
T	= transformer
TB	= terminal board
TP	= test point
U	= integrated circuit, non-repairable assembly
V	= vacuum tube, photocell, etc.
VR	= voltage regulator
W	= jumper wire
X	= socket
Y	= crystal
Z	= tuned cavity, network

ABBREVIATIONS

A	= amperes
ac	= alternating current
Ag	= silver
Al	= aluminum
ar	= as required
adj	= adjust
assy	= assembly
b	= base
bp	= bandpass
bpi	= bits per inch
blk	= black
blu	= blue
brn	= brown
brs	= brass
Btu	= British thermal unit
Be Cu	= beryllium copper
cpi	= characters per inch
coll	= collector
cw	= clockwise
ccw	= counterclockwise
cer	= ceramic
com	= common
crt	= cathode-ray tube
CTL	= complementary-transistor logic
cath	= cathode
Cd pl	= cadmium plate
comp	= composition
conn	= connector
compl	= complete
dc	= direct current
dr	= drive
DTL	= diode-transistor logic
depc	= deposited carbon
dpdt	= double-pole, double-throw
dpst	= double-pole, single-throw
em	= emitter
ECL	= emitter-coupled logic
ext	= external
encap	= encapsulated
elctlt	= electrolytic
F	= farads
FF	= flip-flop
flh	= flat head
flm	= film
fxd	= fixed
filh	= fillister head
G	= giga (10^9)
Ge	= germanium
gl	= glass
gnd	= ground(ed)
gra	= gray
grn	= green
H	= henries
Hg	= mercury
hr	= hour(s)
Hz	= hertz
hdw	= hardware
hex	= hexagon, hexagonal
ID	= inside diameter
IF	= intermediate frequency
in.	= inch, inches
I/O	= input/output
int	= internal
incl	= include(s)
insul	= insulation, insulated
impgrg	= impregnated
incand	= incandescent
ips	= inches per second
k	= kilo (10^3), kilohm
lp	= low pass
m	= milli (10^{-3})
M	= mega (10^6), megohm
My	= Mylar
mfr	= manufacturer
mom	= momentary
mtg	= mounting
misc	= miscellaneous
met. ox.	= metal oxide
mintr	= miniature
n	= nano (10^{-9})
nc	= normally closed or no connection
Ne	= neon
no.	= number
n.o.	= normally open
np	= nickel plated
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NSR	= not separately replaceable
NRFR	= not recommended for field replacement
OD	= outside diameter
OBD	= order by description
orn	= orange
ovh	= oval head
oxd	= oxide
p	= pico (10^{-12})
PC	= printed circuit
PCA	= printed-circuit assembly
PWB	= printed-wiring board
phh	= phillips head
pk	= peak
p-p	= peak-to-peak
pt	= point
prv	= peak inverse voltage
PNP	= positive-negative-positive
pwv	= peak working voltage
porc	= porcelain
posn	= position(s)
pozi	= pozidrive
rf	= radio frequency
rdh	= round head
rms	= root-mean-square
rwv	= reverse working voltage
rect	= rectifier
r/min	= revolutions per minute
RTL	= resistor-transistor logic
s	= second
SB, TT	= slow blow
Se	= selenium
Si	= silicon
scr	= silicon controlled rectifier
sst	= stainless steel
stl	= steel
spcl	= special
spdt	= single-pole, double-throw
spst	= single-pole, single-throw
Ta	= tantalum
td	= time delay
Ti	= titanium
tgl	= toggle
thd	= thread
tol	= tolerance
TTL	= transistor transistor logic
U(μ)	= micro (10^{-6})
V	= volt(s)
var	= variable
vio	= violet
Vdcw	= direct current working volts
W	= watts
ww	= wirewound
wht	= white
WIV	= working inverse voltage
yel	= yellow

Table 6-4. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12008A	1		PROM STORAGE MODULE	28480	12008A
	12008-60001	6	1	ASSEMBLY-PROM STORAGE MODULE	28480	12008-60001
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
U1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U15	1820-2024	3	8	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U16	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U17	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U18	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U25	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U26	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U27	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U35	1820-1194	6	4	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U45	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U46	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U65	1820-1194	6		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS193N
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U67	1AC5-6001	7	1	I/O PROCESSOR (IOP) CHIP	28480	1AC5-6001
U75	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U76	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U85	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U95	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U105	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U115	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
				MISCELLANEOUS PARTS		
	0403-0289	3	2	EXTR-PC 8D RED POLYC .063-8D-THKNS	28480	0403-0289
	1200-0541	1	32	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
	1200-0845C	0	2	RET SPRING CLIP	28480	1200-0845C
	1200-0848C	3	1	SOCKET-64-PIN	28480	1200-0848C
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Table 6-4. Manufacturer's Code List

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS
01121	Allen-Bradley Co.	Milwaukee, WI 53204
01295	Texas Instr Inc. Semiconductor CMPNT Div	Dallas, TX 75222
07263	Fairchild Semiconductor Div.	Mt. View, CA 94042
24546	Corning Glass Works (Bradford)	Bradford, PA 16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA 94304

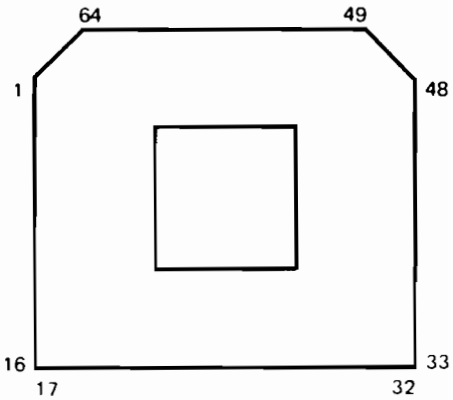
SERVICE DIAGRAMS

SECTION VII

7-1. INTRODUCTION

This section contains the service diagrams for the PROM Storage Module. Base diagrams of the integrated circuits used on this card are shown in Figure 7-1. A component location diagram is shown in Figure 7-3. The following is a list of diagrams to be found in this section.

IAF5-6001
U67



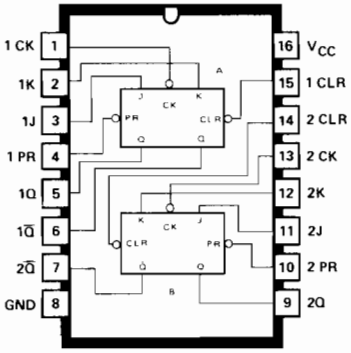
1AF5-6001 I/O PROCESSOR (IOP) CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DMACYC-	17	GND	33	BRNI+	49	VCC
2	LDMAR+	18	VDD	34	CRS +	50	GND
3	SCEN-	19	CW1 -	35	IEN -	51	VDD
4	REMOTE-	20	BCW2 +	36	DIAG -	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD -	53	CB8 +
6	DMAEN -	22	BCW0 +	38	PLSLV+	54	CB9 +
7	LOBYT -	23	BVALID+	39	PON +	55	CB10 +
8	SACK -	24	BIOGO+	40	SLACK +	56	CB11 +
9	NC	25	ICHID-	41	SLRQ+	57	CB12 +
10	SCLK +	26	BIAK+	42	CB0 +	58	CB13 +
11	LSBYT -	27	CFF-	43	CB1 +	59	CB14 +
12	BPE+	28	PULIOR-	44	CB2 +	60	CB15 +
13	BMP-	29	IOEN -	45	CB3 +	61	MEMGO+
14	CHSRQ-	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ -	31	PRDIS -	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 1 of 4)

1820-0629
U56,86
Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear

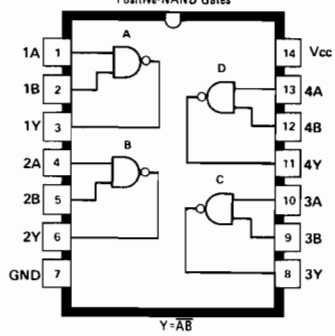


FUNCTION TABLE

INPUTS					OUTPUTS	
PRESENT	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

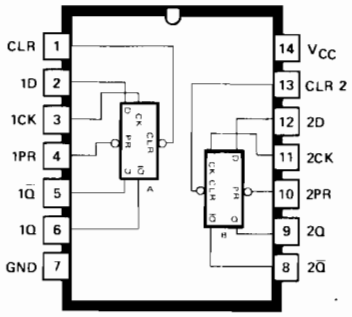
*Non-stable condition exists only while both preset and clear inputs are low.

1820-0681
U76,106
Quadruple 2-Input Positive-NAND Gates



$Y=\overline{AB}$

1820-1112
U16
Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

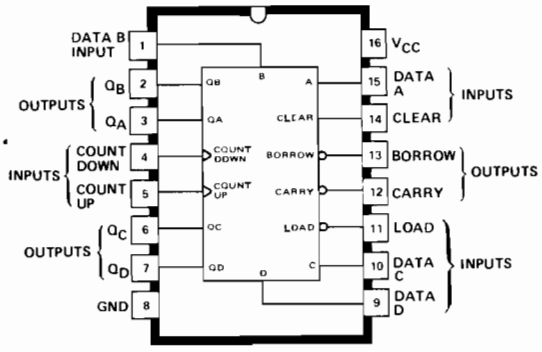


FUNCTION TABLE

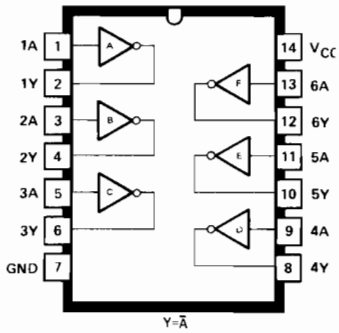
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

*Non-stable condition exists only while both preset and clear inputs are low.

1820-1194
U35,45,55,65
Synchronous Up/Down Dual Clock Counters



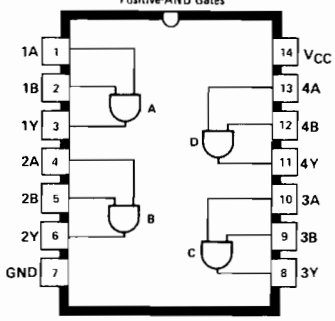
1820-1199
U115
Hex Inverters



$Y=\bar{A}$

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 2 of 4)

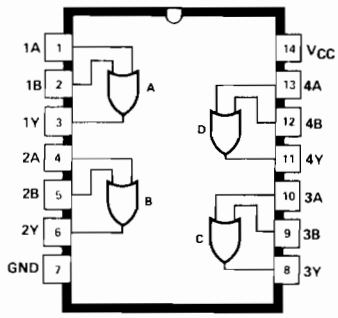
1820-1201
U26
Quadruple 2-Input
Positive-AND Gates



Y=AB

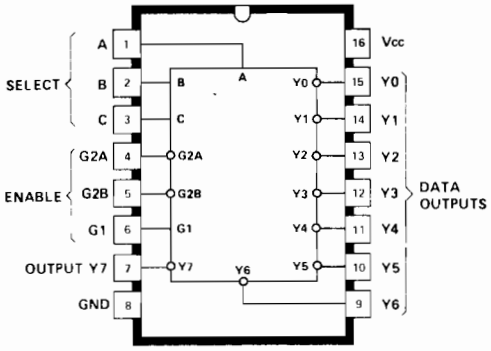
1820-1208 **1820-1449**
U17 U107

Quadruple 2-Input
Positve-OR Gates



Y = A + B

1820-1240
U46,85,95
3 To 8 Line Decoders/Multipilexers

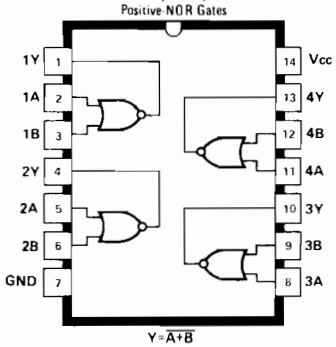


FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

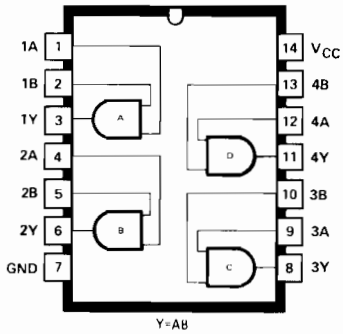
*G2 = G2A + G2B
H = high level
L = low level
X = irrelevant

1820-1322
U66,117
Quadruple 2-Input
Positive-NOR Gates



$Y=\overline{A+B}$

1820-1367
U36
Quadruple 2-Input
Positive-AND Gates

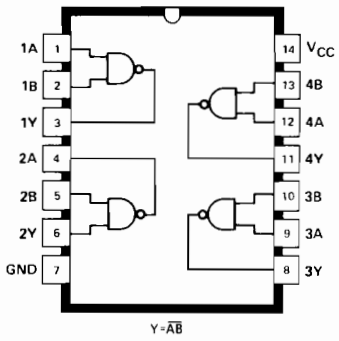


Y=AB

1820-1449
U107
(See 1820-1208)

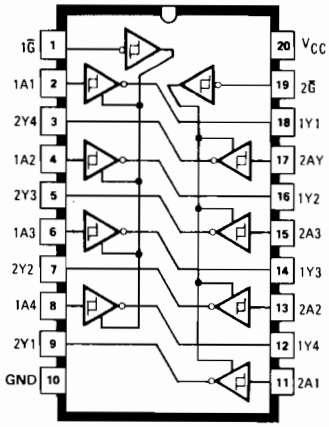
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 3 of 4)

1820-1451
U96,118
Quadruple 2-Input
Positive-NAND Buffers
With Open-Collector Outputs

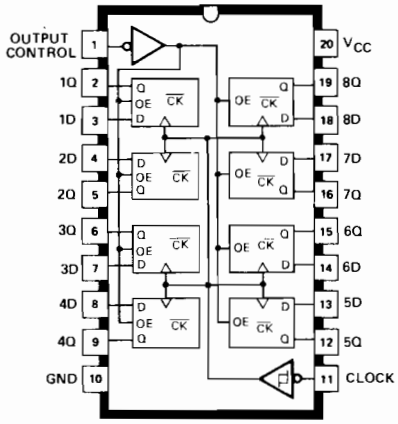


$Y = \overline{AB}$

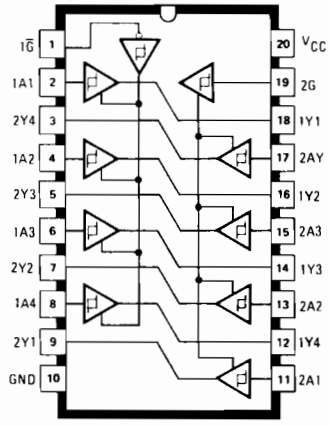
1820-1633
U108,116
Octal Buffers/Line Drivers/Line Receivers
Inverted 3-State Outputs



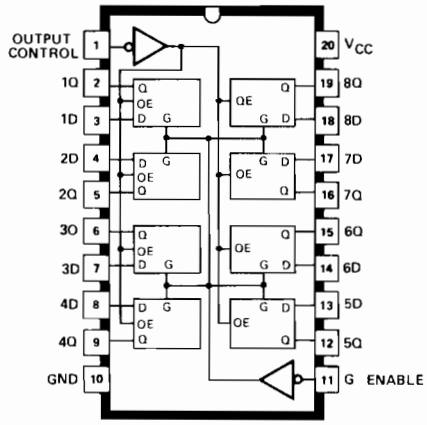
1820-1997
U18
Octal D-Type Flip-Flops
Common Output Control
Common Clock



1820-2024
U15,25,27,28,47,48,75,105
Octal Buffers/Line Drivers/Line Receivers
Non-inverted 3-State Outputs



1820-2102
U37,38,57,58
Octal D-Type Latches
3-State Outputs
Common Output Control
Common Enable



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 4 of 4)

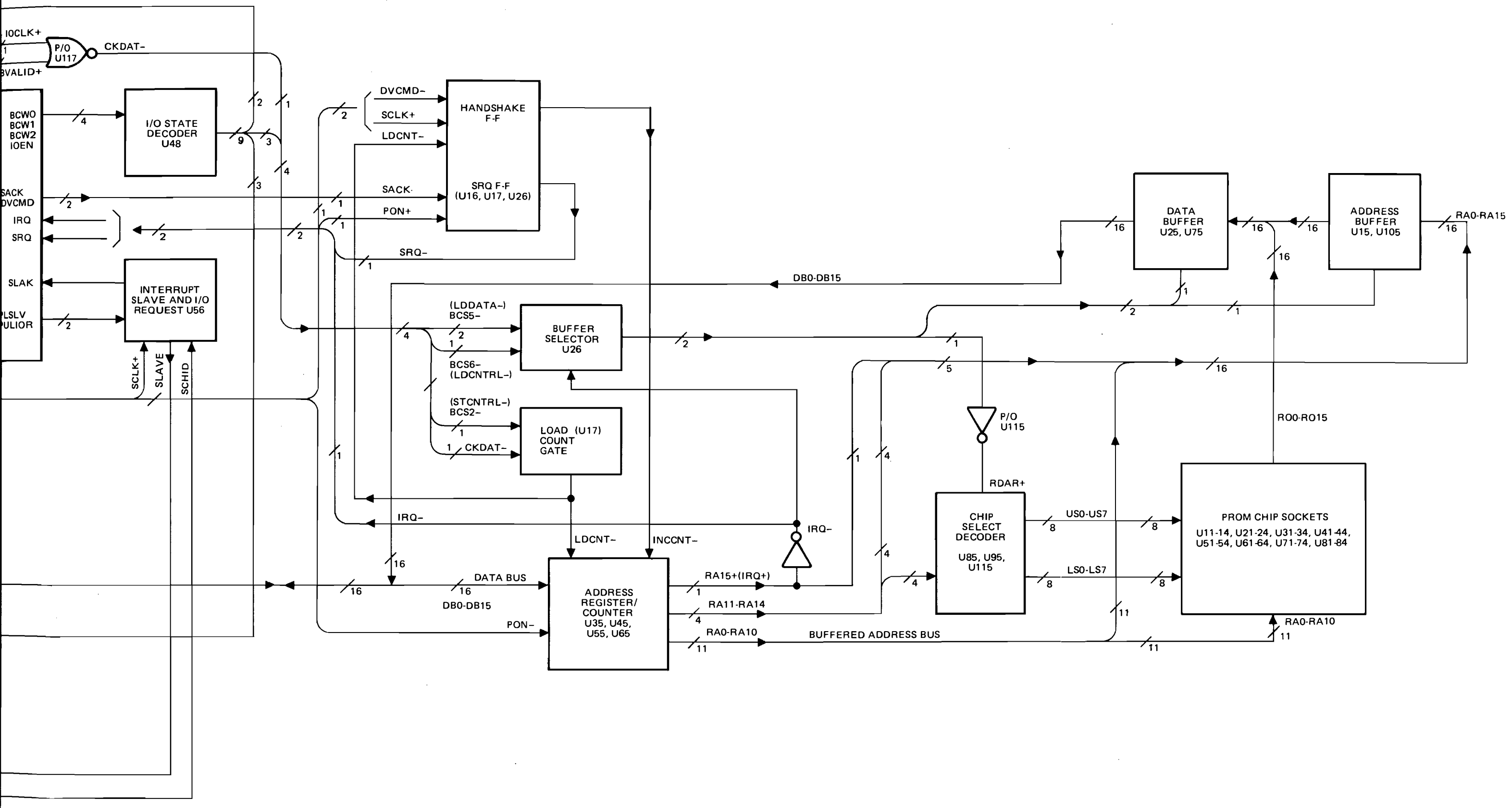
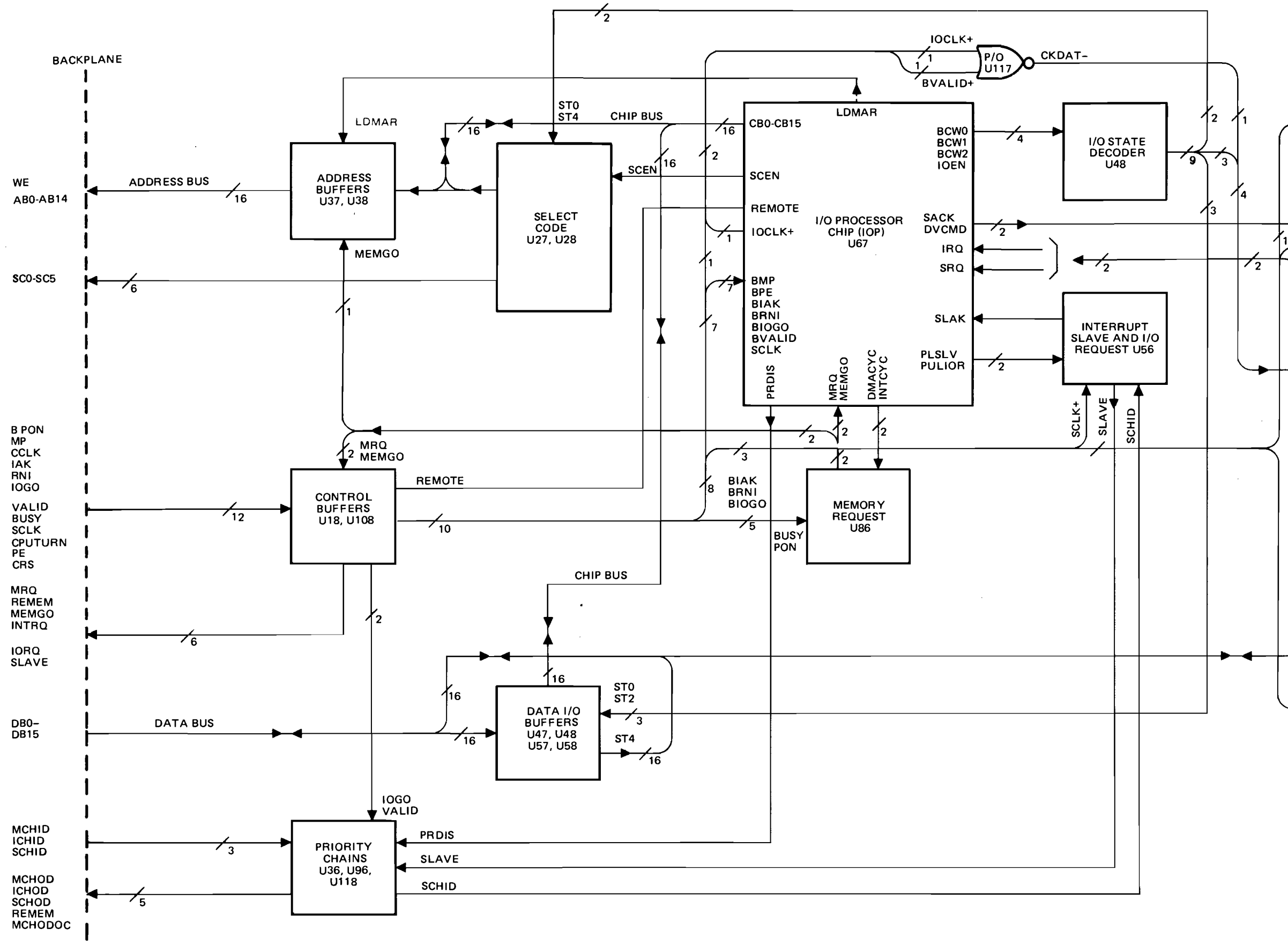


Figure 7-2. PROM Storage Module Functional Block Diagram


BACKPLANE
LDMAR
ADDRESS BUFFERS U37, U38
WE
AB0-AB14
ADDRESS BUS
16
SC0-SC5
6
MEMGO
1
SELECT CODE U27, U28
ST0
ST4
CHIP BUS
16
SCEN
16
2
IOCLK+
1
1
P/O U117
CKDAT-
BVALID+
LDMAR
CB0-CB15
SCEN
REMOTE
IOCLK+
1
1
7
7
BMP
BPE
BIAK
BRNI
BIOGO
BVALID
SCLK
I/O PROCESSOR CHIP (IOP) U67
BCW0
BCW1
BCW2
IOEN
4
I/O STATE DECODER U48
9
SACK
DVCMD
IRQ
SRQ
2
2
2
SLAK
PLSLV
PULIOR
2
INTERRUPT SLAVE AND I/O REQUEST U56
PRDIS
MRQ
MEMGO
DMACYC
INTCYC
2
2
2
SCLK+
SLAVE
SCHID
B PON
MP
CCLK
IAK
RNI
IOGO
VALID
BUSY
SCLK
CPUTURN
PE
CRS
MRQ
REMEM
MEMGO
INTRQ
IORQ
SLAVE
2
MRQ
MEMGO
12
CONTROL BUFFERS U18, U108
REMOTE
10
6
2
3
8
BIAK
BRNI
BIOGO
5
BUSY
PON
MEMORY REQUEST U86
2
CHIP BUS
16
16
ST0
ST2
3
ST4
16
DATA I/O BUFFERS U47, U48 U57, U58
DB0-
DB15
DATA BUS
16
IOGO
VALID
MCHID
ICHID
SCHID
3
PRIORITY CHAINS U36, U96, U118
PRDIS
SLAVE
SCHID
MCHOD
ICHOD
SCHOD
REMEM
MCHODOC
5

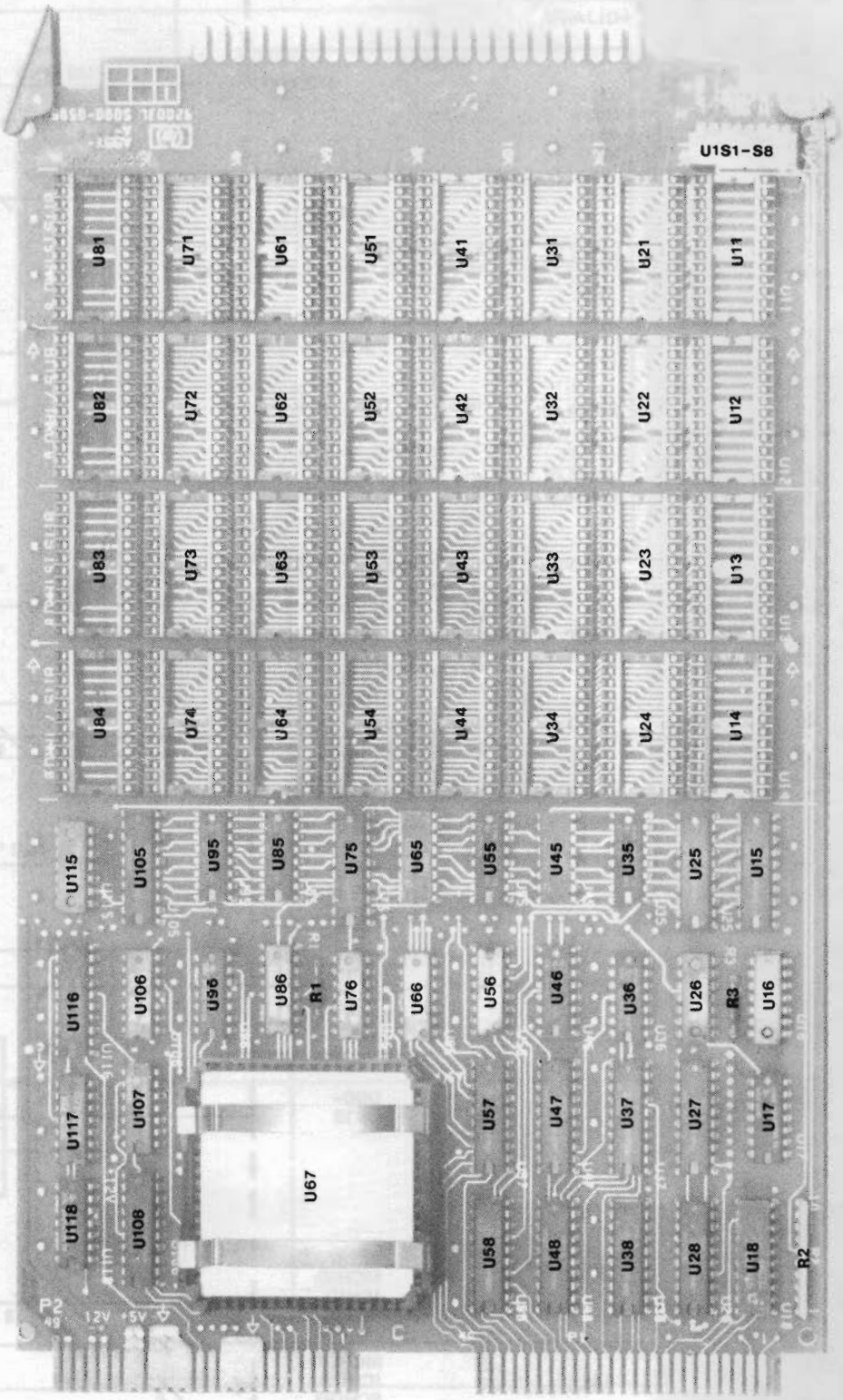


Figure 7-3. HP 12008-60001 PROM Storage Module Component Location Diagram

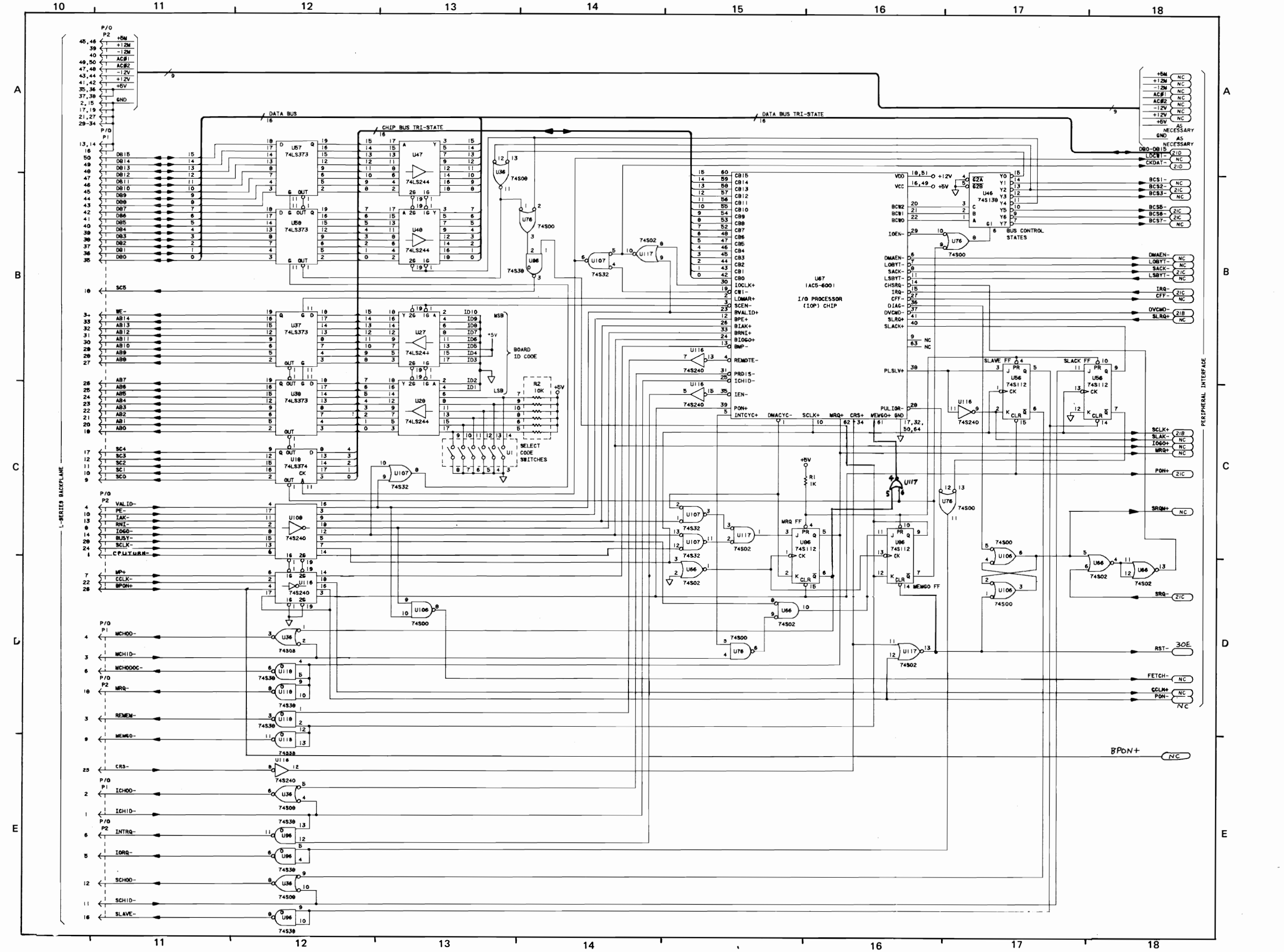


Figure 7-4. HP 12008-60001 PROM Storage Module Schematic Logic Diagram (Sheet 1 of 3)

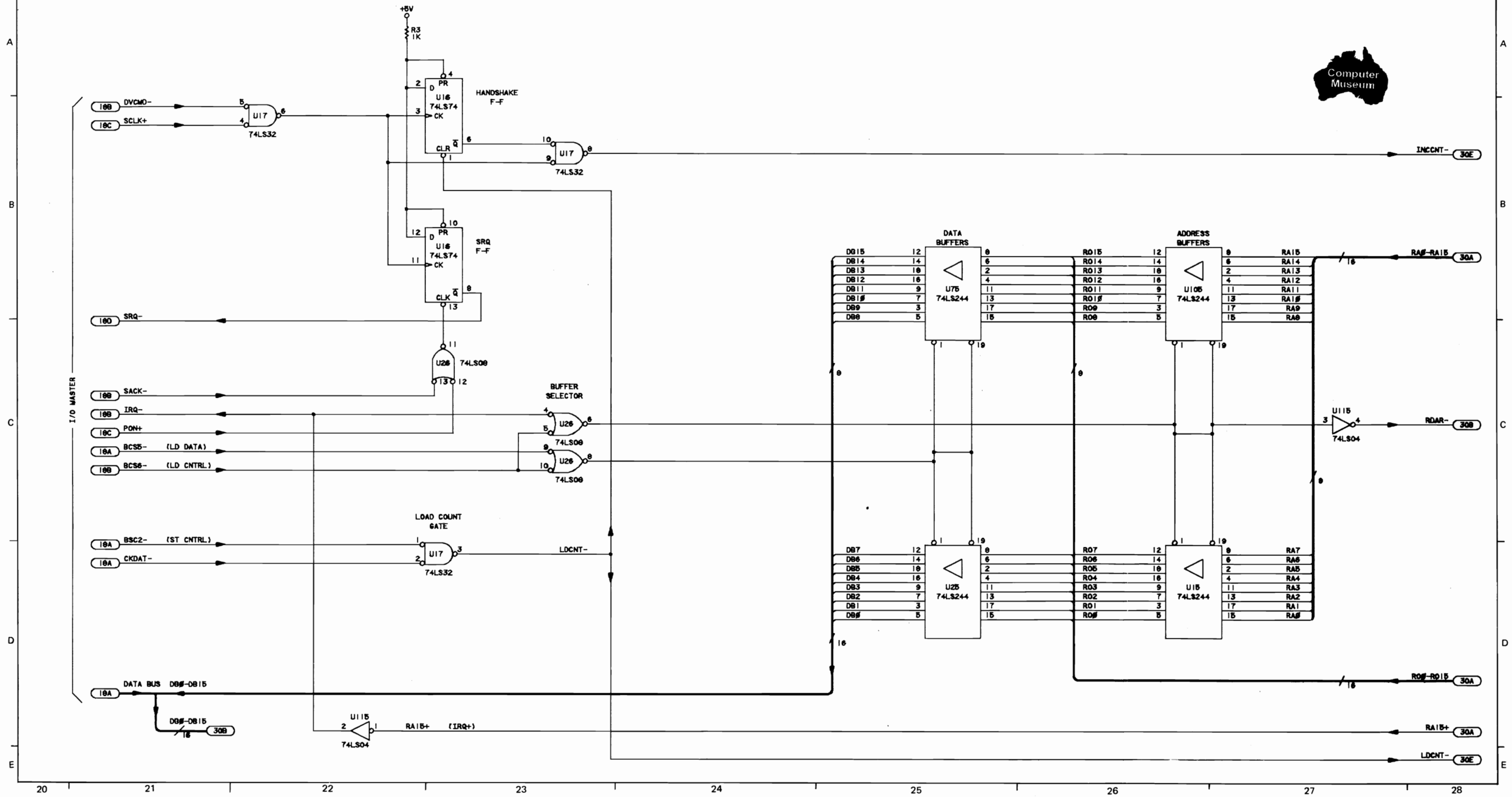


Figure 7-4. HP 12008-60001 PROM Storage Module
Schematic Logic Diagram (Sheet 2 of 3)

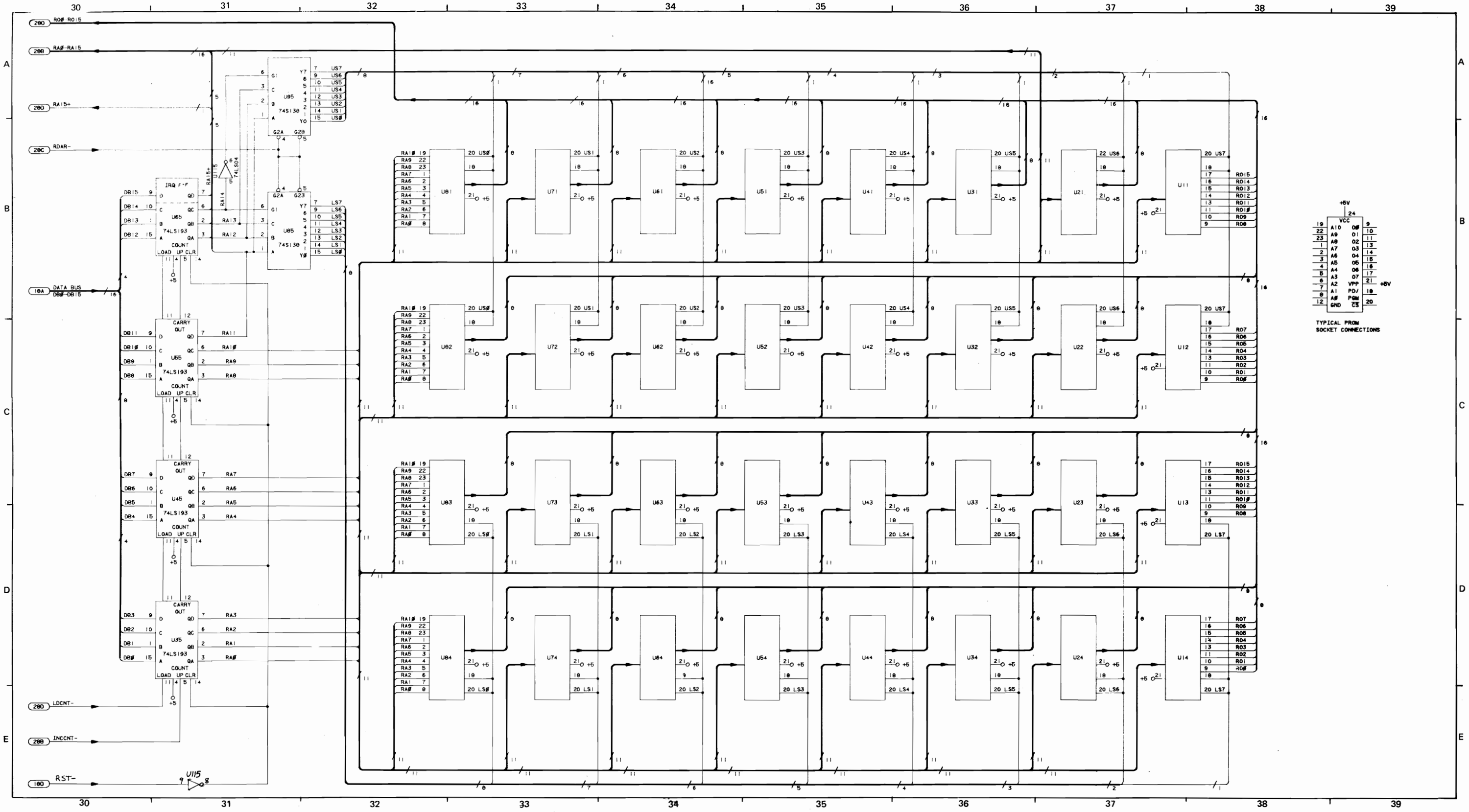


Figure 7-4. HP 12008-60001 PROM Storage Module Schematic Logic Diagram (Sheet 3 of 3)

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