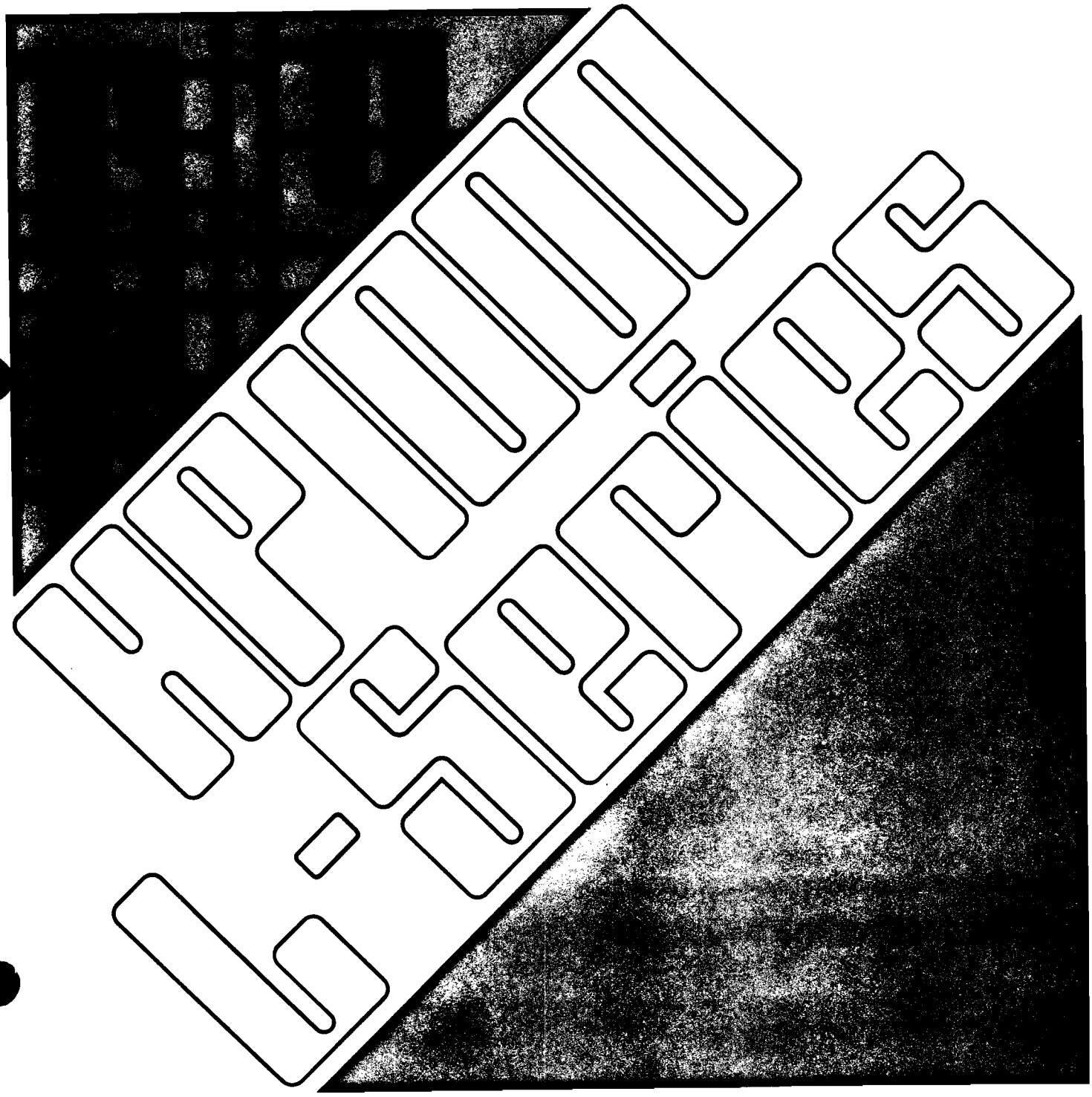
HEWLETT PACKARD

HP 12005A Asynchronous Serial Interface

Reference Manual



HEWLETT PACKARD

REFERENCE MANUAL

HP 12005A ASYNCHRONOUS SERIAL INTERFACE

Manual Part No. 12005-90001

Printed in U.S.A. January 1980

Card Assembly: 12005-60001
Date Code: A-2001, B-2001

HEWLETT-PACKARD COMPANY
Data Systems Division
11000 Wolfe Road
Cupertino. California 95014

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MANUAL UPDATE

MANUAL IDENTIFICATION

Title: HP 12005A Asynchronous Serial Interface Reference Manual
Part Number: 12005-90001

Edition: First Edition

Edition or Reprint Date: Jan 1980

UPDATE IDENTIFICATION

Update Number: 1 June 1980

This Packet also Includes: 2 May 1981

THE PURPOSE OF THIS MANUAL UPDATE
is to provide new information for your manual to bring it up to date. This is important because it ensures that your manual accurately documents the current version of the software.

THIS UPDATE CONSISTS OF
this cover sheet, a printing history page or a revised "List of Effective Pages," all replacement pages, and write-in instructions (if any). Replacement pages are identified by the update number at the bottom of the page. A vertical line (change bar) in the outside margin indicates new or changed text material. The change bar is not used for typographical or editorial changes that do not affect the text.

TO UPDATE YOUR MANUAL
identify the latest Update (if any) already contained in your manual by referring to the Printing History Page or List of Effective Pages (page ii). Incorporate only the Updates from this packet not already included in your manual. Following the instructions on the back of this page, replace existing pages with the Update pages and insert new pages as indicated. If any page is changed in two or more Updates, such as the Printing History Page which is furnished new for each Update, only the latest page will be included in the Update package. Destroy all replaced pages. If "write-in" instructions are included they are listed on the back of this page.

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Data Systems Division
11000 Wolfe Road
Cupertino, California 95014

TECHNICAL MANUAL UPDATE

(12005-90001)

UPDATE NO.	DESCRIPTION
1	**Page 1-1. Under Sections 1-8 entitled options add:** **Option 004: 48 pin connector kit** **Option 005: Cable 12005-60005, used for 2645A.** **Insert page 7-19.** **Page vii. Under Tables add:** **Interface cable wire list for 12005 Page 7-19** **Page 2-6. Under Section 2-15 entitled Baud Rate Selection add:** **The external clock (x16) setting (U21S1-U21S4 all closed) is not supported with prefabricated HP supplied cables.** **Title Page/ii and iii/iv. Remove and replace with new pages.**

UPDATE NO	DESCRIPTION
2	This manual update does not apply to 12005A with Date Code earlier than 2104. Replace every where: Card Assembly 12005-60001 by Card Assembly 12005-60007 Date Code is : A-2104 Page 2-6 Delete Note : Switches U21 S7 and S8 are not used Page 2-6 P.2-18C Add : U21 S7 Must be open (up) U21 S8 Must be closed (down)

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PRINTING HISTORY

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First Edition . . . . . Jan 1980

Update 1 . . . . . June 1980

LIST OF EFFECTIVE PAGES

The List of Effective Pages gives the most recent update number on which the technical material on any given page was altered. If a page is simply re-arranged due to a technical change on a previous page, it is not listed as a updated page. Within the manual, changes are marked with a vertical bar in the margin. When a update is incorporated in a reprinted manual, the update number and vertical bar in the margin is removed but the update number will remain on this List of Effective Pages page.

Pages	Update No.	Pages	Update No.
Title	1		
ii	1		
iii/iv	1		
1-1	1		
2-6	1		
7-19	1		

Table 7-1. Interface cable wire list for 12005.

(PCA) J1-	SIGNAL NAME	SIGNAL DEFINITION	WIRE COLOR (NOTE 1)	RS-232C	RS-449	SIGNAL SOURCE	12005-60002 J2	12005-60003 J2	12005-60004 J2	12005-60005 J2
A	GND									
1	GND									
B	*IC(A)	Incoming Call (A)	BLU	CE	IC	Dev			22	
2	*RS(B)	Request to Send (B)		CA	RS	Intfc				
C	RIC	Used by diagnostics only								
3	*RS(A)	Request to Send (A)		CA	RS	Intfc				
D	TTYI	Teleprinter Input								
4	TTYI	Teleprinter Input								
E	**RS(U)	Request to Send (U)	RED	CA	†	Intfc	44	5	4	E,J (ORN)
5	DRST	Reset line used by diagnostics only								
F	*IC(B)	Incoming Call (B)		CE	IC	Dev			Δ	
6	RDM	Used by diagnostics only								
H	RCS	Used by diagnostics only								
7	EXTCLK	Clock from External Device(if any)(16X)								
J	+5V	+5 to terminal								
8	ECHOM	Used by diagnostics only								
K	SPC2	Used by diagnostics only								
9	*SD(B)	Send Date (B)		BA	SD	Intfc				
L	RRR	Used by diagnostics only								
10	*SD(A)	Send Data (A)		BA	SD	Intfc				
M	TR	Terminal Ready	GRN	CD	TR	Intfc		8	20	
11	SBS	Stop Bit Select								
N	TTY+12	+12 to teleprinter	GRN			Intfc	46			
12	TTY+12	+12 to teleprinter								
P	RDRCNTL	Reader Control (GND)								
13	RDRCNTL	Reader Control (GND)								
R	TTY-12	-12 to teleprinter								
14	TTY-12	-12 to teleprinter								
S	*RD(B)	Receive Data (B)	WHT	BB	RD	Dev	12	2	3	B (BRN)
15	*SRD(A)	Secondary Receive Data (A)	WHT-BRN	SBB	SRD	Dev			16	
T	TTYO	Output to teleprinter								
16	TTYO	Output to teleprinter								
U	*RD(A)	Receive Data (A)		BB	RD	Dev	Δ	Δ	Δ	Δ
17	*SRD(B)	Secondary Receive Data (B)		SBB	SRD	Dev			Δ	
V	*RR(A)	Receiver Ready (A)	WHT-BLK	CF	RR	Dev			8	
18	*RR(B)	Receiver Ready (B)		CF	RR	Dev			Δ	
W	**SD(U)	Send Data (U)	BRN	BA	†	Intfc		3	2	C (RED)
19	MSB-	Most significant bit of baud rate select								
X	*CS(A)	Clear to Send (A)	YEL	CB	CS	Dev		4	5	
20	NMSB-	Next to most significant bit of baud rate select								
Y	*CS(B)	Clear to Send (B)		CB	CS	Dev		Δ	Δ	
21	NLSB+	Next to least significant bit of baud rate select								
Z	*DM(A)	Data Mode (A)	GRA	CC	DM	Dev			6	
22	LSB+	Least significant bit of baud rate select								
AA	*DM(B)	Data Mode (B)		CC	DM	Dev			Δ	
23	SSD	Secondary Send Data		SBA	SSD	Intfc				
BB	GND		BLK				Δ	Δ	Δ	Δ
24	GND		BLK				Δ	Δ	Δ	Δ

NOTE: 1. Wire colors do not apply for 12005-60005.

* Indicates differential driver or receiver used on this signal.

** Indicates single-ended driver used on this signal.

† RS-449 recommends the use of differential drivers.

Δ These pins are connected within the PCA cable hood for the specific cable.

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First Edition ..... Jan 1980

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SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

CONTENTS

CONTENTS (Continued)

ILLUSTRATIONS

TABLES

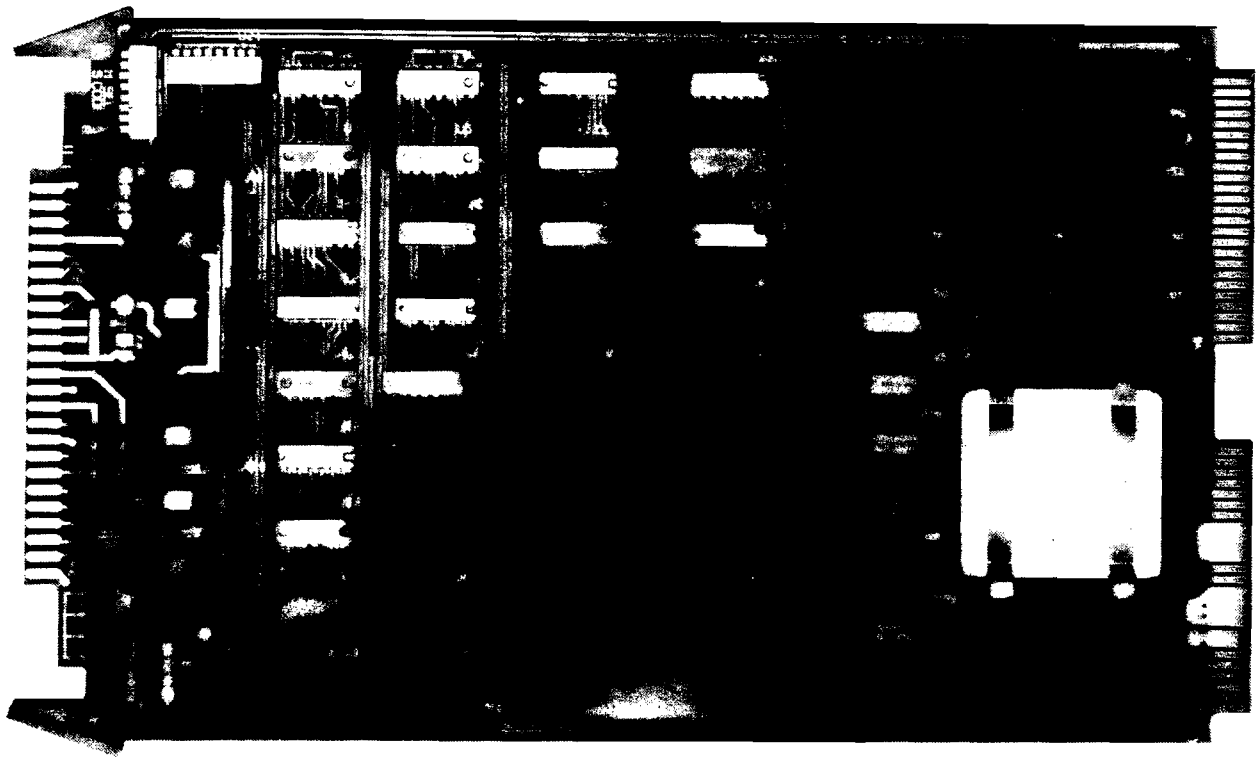

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Figure 1-1. HP 12005A Asynchronous Serial Interface

INTRODUCTION

1-1. INTRODUCTION

This manual provides general information, installation, programming instructions, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 12005A Asynchronous Serial Interface.

1-2. DESCRIPTION

1-3. GENERAL

The HP 12005A Asynchronous Serial Interface provides an asynchronous serial communications link between the HP 1000 L-Series Computer and an RS-449 or RS-232 compatible terminal. The asynchronous serial interface, hereafter called the interface, plugs into a single slot in the L-Series backplane (see figure 1-2) and is assigned a single select code.

The interface has the capability of handling its own memory accesses (Direct Memory Access (DMA)), of decoding its own instructions from the central processor unit (CPU), and of forcing the CPU into slave mode processing. These features are performed by an input/output (I/O) master containing an I/O processor (IOP) integrated circuit (chip) and associated logic. This I/O master, (including the IOP chip) is located on the interface and performs all functions (including instruction recognition and DMA control) necessary for interfacing with the L-Series backplane. Figure 1-3 is a simplified block diagram of the asynchronous serial interface and figure 1-4 shows the interface in a typical L-Series system environment.

1-4. PHYSICAL DESCRIPTION

The HP 12005A Asynchronous Serial Interface is a single circuit card as shown in figure 1-1. Two 50-finger edge connectors connect the interface to the backplane, and one 48-finger edge connector connects the interface, via a cable, to its peripheral device (terminal). The cable is not furnished with the interface. See paragraph 1-8 for a list of available cable options.

NOTE

In this manual, the word "terminal" refers to a cathode ray tube or other type of terminal, or a teleprinter.

1-5. IDENTIFICATION

1-6. PRODUCT. Five digits and a letter (12005A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product; the letter indicates the revision level of the product.

1-7. CIRCUIT CARD. The interface circuit card is further identified by a part number marked on the card. In addition, a letter and a date code consisting of four digits (e.g., A-1926) are placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the interface card could be as follows:

12005-60001
A-1926

If the date code stamped on the interface does not agree with the date code on the title page of this manual, there are differences between your interface and the interface described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

1-8. OPTIONS. Three cable options are available for the HP 12005A Asynchronous Serial Interface, as follows:

Option 001:	Cable 12005-60002, used for HP 2621 terminals.
Option 002:	Cable 12005-60003, used for RS-232 terminals connected directly to the interface.
Option 003:	Cable 12005-60004, used for RS-232 terminals connected to the interface through a modem.

1-9. REFERENCE MANUAL. The manual supplied with the interface is identified by its name and part number. The part number, 12005-90001, is printed on the title page. The publication date also is printed on the title page. If the manual is revised, the publication date is changed.

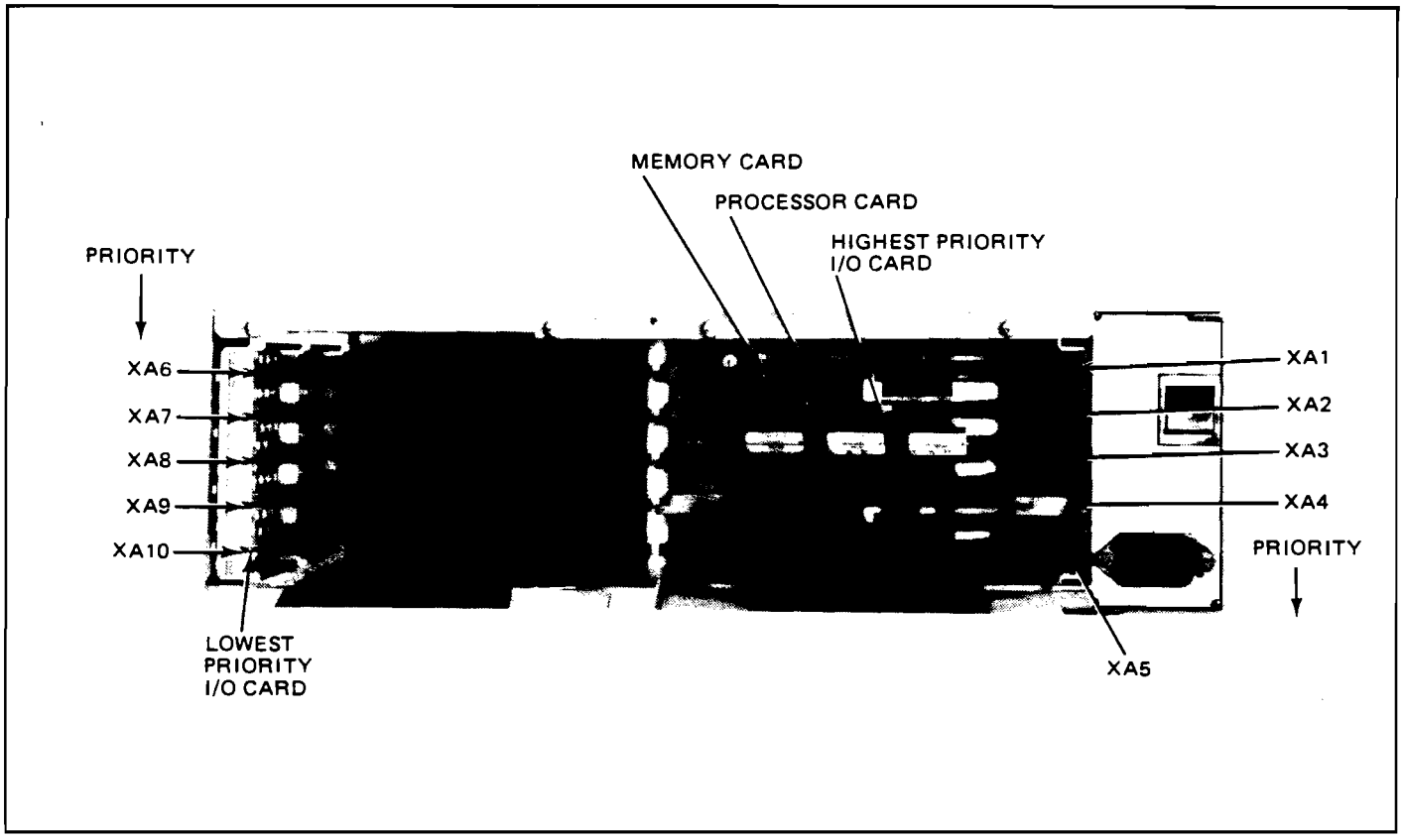

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Figure 1-2. Typical L-Series Card Cage Layout

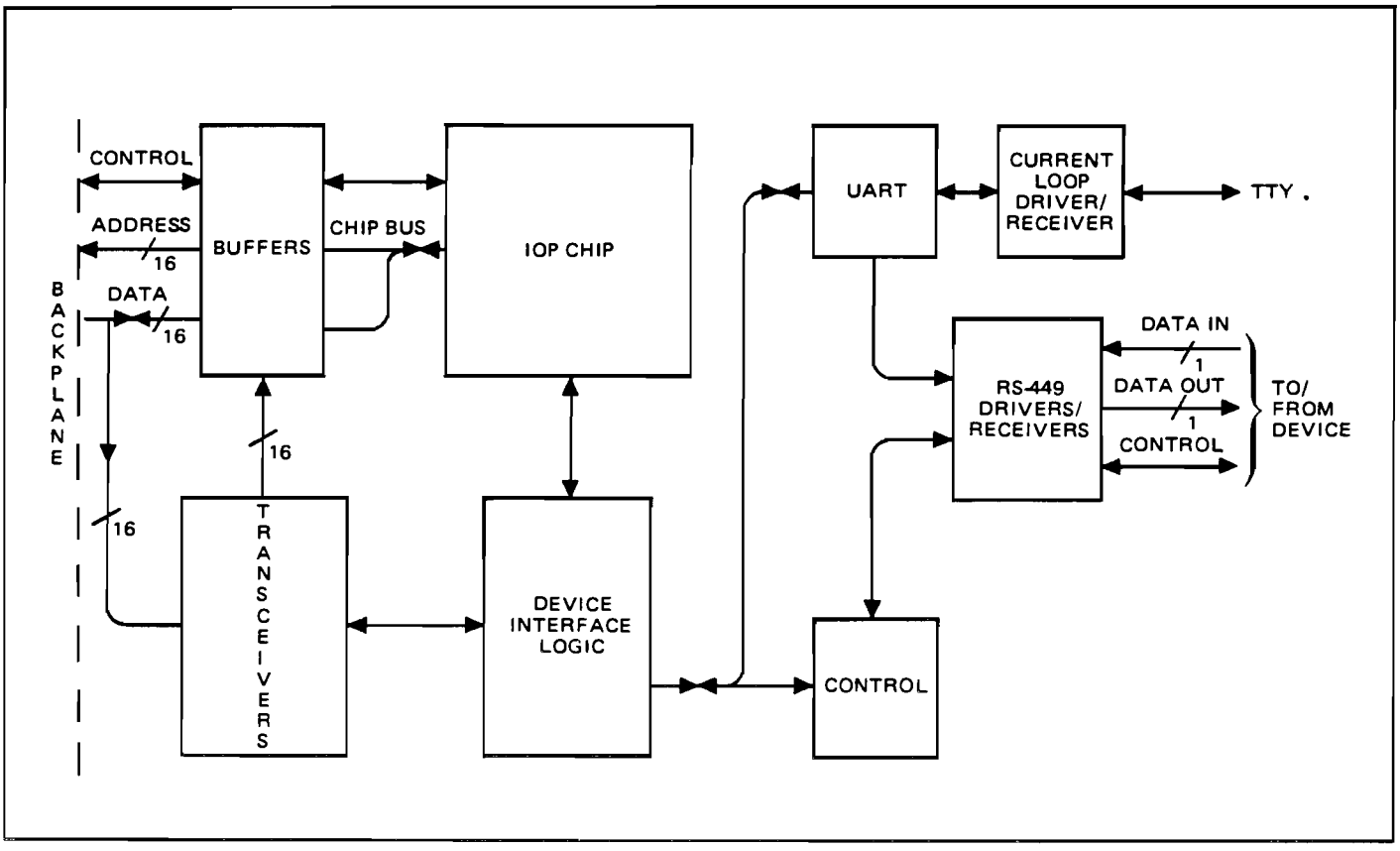

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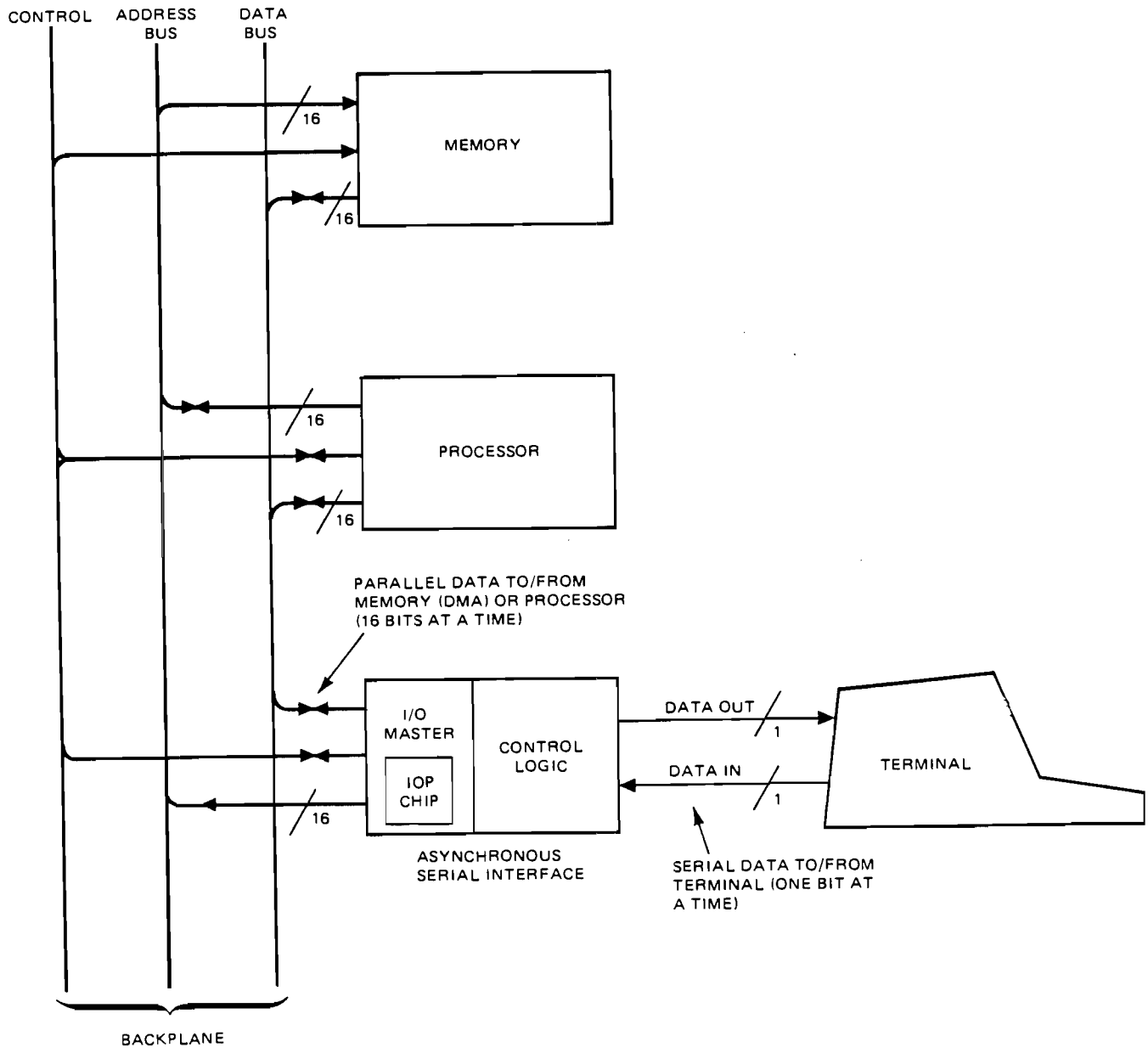
Figure 1-3. Asynchronous Serial Interface Simplified Block Diagram



7700-471

Figure 1-4. Asynchronous Serial Interface in Typical System Environment

1-10. SPECIFICATIONS

Table 1-1 lists the specifications of the HP 12005A Asynchronous Serial Interface. In the table and throughout this manual the word "character" signifies a 7-bit ASCII (American Standard Code for Information Interchange) character with start and stop bits and an optional parity bit; or an 8-bit binary character with start and stop bits. Thus, a character as handled by the interface can consist of from 9 to 11 bits.

In the case of data sent to a terminal, each character results in the display of a letter of the alphabet, a digit, or a symbol; or the character causes actuation of such mechanical functions as carriage return or bell stroke. When a character is sent to the cartridge tape unit of a terminal, the eight data bits are written on the tape.

When data is received from a terminal keyboard, a character is supplied to the interface each time a key is pressed. If a character is furnished by a cartridge tape unit of a terminal, eight data bits are supplied to the interface.

Table 1-1. Specifications

OUTPUT CHARACTERS	In an output operation, 7-bit (ASCII) or 8-bit (binary) characters are transferred in parallel from the central processor to the interface. There, one start bit and one or two stop bits, and an optional parity bit, are added, and the resulting bits are transferred in serial to a terminal.
INPUT CHARACTERS	In an input operation, 9-bit to 11-bit characters are transferred serially from the terminal to the interface. There, a start bit, optional parity bit, and one or two stop bits are discarded. The resulting 8-bit character is transferred in parallel to the central processor A or B register, or directly into memory.
DATA TRANSFER RATE:	
Using Internal Clock Pulse:	Data transfer rate is 50, 75, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 7200, or 9600 baud, depending on the settings of switches U21 S1 through U21 S4.
Using External Clock Pulse:	Depends on the terminal. Maximum is 56,000 baud.
PHYSICAL CHARACTERISTICS	
Size:	17.15 by 28.91 centimeters (6.75 by 11.38 inches)
Backplane Interconnects:	Two 50-finger edge connectors which plug into two sockets (P1 and P2) mounted on the backplane.
Device Interconnects:	One 48-finger edge connector on which a cable hood (J1) may be connected.

POWER REQUIREMENTS:

Voltage	Current	Power Dissipation
+5	1.6A	8.3W
+12	143mA	1.8W
−12	107.5mA	1.4W
	Total Power Dissipation	11.5W

OPERATING TEMPERATURE RANGE

0 to 55 °C

INSTALLATION

2-1. INTRODUCTION

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12005A Asynchronous Serial Interface.

CAUTION

STATIC SENSITIVE DEVICE. Use anti-static procedures when handling the interface.

2-2. UNPACKING AND INSPECTION

If ordered with a computer, the interface is installed at the factory. When this is the case, it is necessary only to check the operation of the terminal and the interface after the computer and the terminal are installed. Checkout instructions are furnished in paragraph 2-19. If the interface is ordered separately, inspect the carton containing the interface before opening it. If there is evidence of damage, if water stains are visible, or if the box rattles, request that the carrier's agent be present when the box is opened.

Inspect the interface for such damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest Hewlett-Packard Sales and Service Office. The Sales and Service Office will arrange for repair or replacement of damaged parts without waiting for settlement of claims against the carrier. (HP Sales and Service Offices are listed at the back of this manual.)

After inspecting all components, check the part numbers listed in paragraph 1-5 against the part number on the interface. If an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

2-3. PREPARATION FOR INSTALLATION

2-4. COMPUTATION OF CURRENT REQUIREMENTS

The interface obtains its operating voltages from the computer power supply through the backplane. Before installing the interface, it is necessary to determine whether the added current will overload the power supply. (If the interface was installed at the factory, the required calculations have been made, and it has been determined that an overload will not occur.) The current requirements of the interface are listed in Section I, table 1-1.

2-5. INTERFACE REQUIREMENTS

2-6. BACKPLANE TO HP 12005A ASYNCHRONOUS SERIAL INTERFACE

All interface between the HP 12005A Asynchronous Serial Interface, central processor, and main memory occur on the backplane. Connections from the backplane to the 12005A are listed in table 2-1 (connector P1) and table 2-2 (connector P2).

2-7. HP 12005A ASYNCHRONOUS SERIAL INTERFACE TO TERMINAL

Several options are offered for the serial communication between the 12005A and the terminal or modem to which it is connected. The 20 mA current loop driver and receiver provide a minimal teleprinter interface. The RS-449 drivers and receivers provide an interface to most Electronics Industries Association (EIA) standard devices. The 12005A may be connected directly to a terminal, or it can be connected through a Bell 103, 202, or similar modem.

2-8. RS-449 INTERFACE

The EIA has defined a number of standards for interfaces between data communications and data terminals equipment. Currently, RS-232 is the most widely used of these standards. Standards RS-422 and RS-423 have been developed to offer enhanced operation of serial data communications. These new standards allow faster baud rates over longer cables. The basic difference between RS-422 and RS-423 is that RS-422 drivers and receivers are balanced, or differential, so that they offer the highest noise immunity, the highest data signalling rates, and the highest permissible cable lengths. RS-423 drivers and receivers, on the other hand, are single-ended, so that they offer better downward compatibility to RS-232 equipment.

RS-449 is a new standard which is basically a mix of RS-422 and RS-423 specifications. For interchange circuits where higher data signalling rates are used, such as the timing and data circuits and control circuits, RS-449

Table 2-1. Backplane Connections, Connector P1

P1-	SIGNAL NAME	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	SPARE 1	
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	
14	GND	
15	SPARE 2	
16	GND	
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
20	AB1	Address Bus Bit 1
21	AB2	Address Bus Bit 2
22	AB3	Address Bus Bit 3
23	AB4	Address Bus Bit 4
24	AB5	Address Bus Bit 5
25	AB6	Address Bus Bit 6
26	AB7	Address Bus Bit 7
27	AB8	Address Bus Bit 8
28	AB9	Address Bus Bit 9
29	AB10	Address Bus Bit 10
30	AB11	Address Bus Bit 11
31	AB12	Address Bus Bit 12
32	AB13	Address Bus Bit 13
33	AB14	Address Bus Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Data Bus Bit 1
37	DB2	Data Bus Bit 2
38	DB3	Data Bus Bit 3
39	DB4	Data Bus Bit 4
40	DB5	Data Bus Bit 5
41	DB6	Data Bus Bit 6
42	DB7	Data Bus Bit 7
43	DB8	Data Bus Bit 8
44	DB9	Data Bus Bit 9
45	DB10	Data Bus Bit 10
46	DB11	Data Bus Bit 11
47	DB12	Data Bus Bit 12
48	DB13	Data Bus Bit 13
49	DB14	Data Bus Bit 14
50	DB15	Data Bus Bit 15

Table 2-2. Backplane Connections, Connector P2

P2-	SIGNAL NAME	SIGNAL DEFINITION
1	CPUTURN-	Processor Turn
2	GND	
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI-	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	GND	
16	SLAVE-	Slave Request
17	GND	
18	MRQ-	Memory Request
19	GND	
20	FCLK-	Fast Clock
21	GND	
22	CCLK-	Communications Clock
23	PINT-	Priority Interrupt
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	GND	
28	BUSY-	Memory Busy
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	
34	GND	
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12M	
40	−12M	
41	+12V	
42	+12V	
43	−12V	
44	−12V	
45	+5M	
46	+5M	
47	AC∅2	
48	AC∅2	
49	AC∅1	
50	AC∅1	

recommends that the balanced drivers be used. For the remaining circuits, unbalanced equipment may be used. Table 2-3 lists EIA standards for RS-232, RS-422, RS-423, and RS-449.

An RS-449 interface is implemented on the 12005A using the scheme shown in table 2-4. Only differential receivers are used. Both differential and single-ended drivers are used, however, and some are driven in parallel. When connecting to single-ended drivers, one of the receiver inputs is grounded. This implementation of RS-449 offers complete compatibility with RS-232 and offers many of the enhancements of RS-422 and RS-423 interfaces.

NOTE

Although the lines shown in table 2-4 are named according to the RS-449 standards, this does not restrict their usage to this specification. All lines are software controllable and may be assigned arbitrary meanings according to the needs of a specific application.

The four output lines and six input lines shown in table 2-4 are a subset of RS-449 and are sufficient for most all asynchronous modem and terminal applications. Those

Table 2-3. Electronics Industries Association Standards

TYPE DRIVER/ RECEIVER	RS-232C	RS-422	RS-423	RS-449
	SINGLE-ENDED	DIFFERENTIAL	SINGLE-ENDED	BOTH
Maximum Cable Length	15.24 meters (50 feet)	12.19 meters (40 feet) @ 10M baud. 1219 meters (4000 feet) @ 100K baud.	12.19 meters (40 feet) @ 100K baud. 1219 meters (4000 feet) @ 1K baud.	60.96 meters (200 feet) @ 2M baud.
Maximum Data Rate	20K baud	10M baud @ 12.19 meters (40 feet)	100K baud @ 12.19 meters (40 feet)	2M baud

Table 2-4. RS-449/RS-232 Equivalency

DIRECTION WITH RESPECT TO HP 12005A	NAME	RS-449	NAME	RS-232C
			AA	Protective Ground
	SG	Signal Ground	AB	Signal Ground
	SC	Send Common		
	RC	Receive Common		
OUT	RS*	Request to Send	CA	Request to Send
IN	CS*	Clear to Send	CB	Clear to Send
IN	DM*	Data Mode	CC	Data Set Ready
OUT	TR	Terminal Ready	CD	Data Terminal Ready
IN	IC*	Incoming Call	CE	Ring Indicator
IN	RR*	Receiver Ready	CF	Received Line Signal Detector
OUT	SD*	Send Data	BA	Transmitted Data
IN	RD*	Receive Data	BB	Received Data
OUT	SSD	Secondary Send Data	SBA	Secondary Transmitted Data
IN	SRD*	Secondary Receive Data	SBB	Secondary Received Data

* Indicates differential driver or receiver used on this signal.

lines containing an asterisk in table 2-4 indicate a circuit which optionally uses RS-422 or balanced electrical characteristics. See figure 2-1 for an illustration of how this option is implemented. When the interface is cabled directly to a terminal, most of the control lines listed in table 2-4 will not be used. When the interface is connected to a modem, however, the output control lines will be software programmed and the input lines can be continuously monitored for status change.

2-9. TELEPRINTER INTERFACE

The HP 12005A Asynchronous Serial Interface has a 20 mA current loop interface which is designed to run at 110 baud.

A 20 mA current loop driver is used when interfacing to a teleprinter, and left open otherwise. A 20 mA current loop receiver is used to receive data from a teleprinter, and when left open is pulled down to a logic zero.

2-10. CONNECTOR J1 PIN CONNECTIONS

See table 2-5 for pin connections to connector J1. Connector J1 is used to connect a cable from the interface to a terminal or modem.

The seven signals which are brought out to the connector for diagnostic purposes only are marked as such. These signals are used with the diagnostic test hood (see the HP 12005A Asynchronous Serial Interface Diagnostic Operating Manual, part no. 24397-90005) to set baud rates and for testing the 12005A.

2-11. HARDWIRED OPTIONS

The only hardwired option on the 12005A is the wiring of the RS-449 receivers for balanced or unbalanced signals. All HP 12005A cable options are wired for unbalanced signals; therefore, one input to the differential receiver is grounded in the cable hood. In order to interface to a balanced driver (RS-422 specification), refer to the connections shown in table 2-4. The cable hood may be disassembled as shown in figure 2-2. Check the wiring of all the receivers and remove or add jumpers to ground as necessary.

2-12. SWITCH SELECTABLE OPTIONS

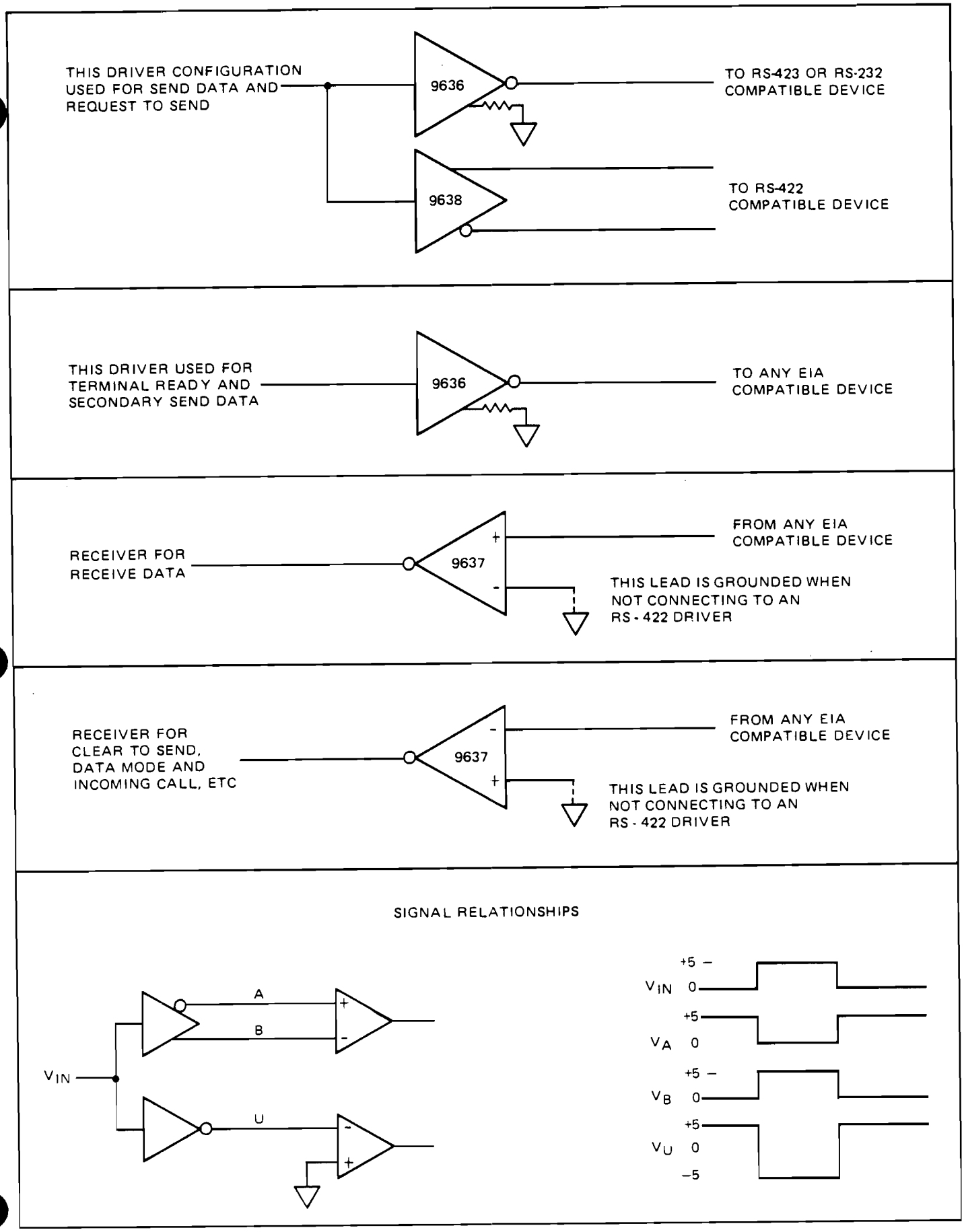
The switch selectable options are the select code (6 bits), the baud rate (4 bits), parity sense (1 bit), number of stop bits (1 bit), and Virtual Control Panel (VCP) interface enable (1 bit). The switches are mounted in two dual in-line packages (U1 and U21) located close to the cable connector on the interface (see figure 1-1 for the locations of the switches). Each set of switches, U1 and U21, are numbered from S1 to S8. Each switch is closed when in the down position, and is open in the up position.

Table 2-5. Interface-to-Terminal (Connector J1) Pin Connections

J1-	SIGNAL NAME	SIGNAL DEFINITION
A	GND	
1	GND	
B	IC (A)	Incoming Call (A)
2	RS (B)	Request to Send (B)
C	RIC	Used by diagnostics only
3	RS (A)	Request to Send (A)
D	TTYI	Teleprinter Input
4	TTYI	Teleprinter Input
E	RS (U)	Request to Send (U)
5	DRST	Reset line used by diagnostics only
F	IC (B)	Incoming Call (B)
6	RDM	Used by diagnostics only
H	RCS	Used by diagnostics only
7	EXTCLK	Clock from External Device (if any) (16X)
J	+5V	+5 to terminal
8	ECHOM	Used by diagnostics only
K	SC2	Used by Diagnostics only
9	SD (B)	Send Data (B)
L	RRR	Used by diagnostics only
10	SD (A)	Send Data (A)
M	TR	Terminal Ready
11	SBS	Stop Bit Select
N	TTY+12	+12 to teleprinter
12	TTY+12	+12 to teleprinter
P	RDR CNTL	Reader Control (Gnd)
13	RDR CNTL	Reader Control (Gnd)
R	TTY−12	−12 to teleprinter
14	TTY−12	−12 to teleprinter
S	RD (B)	Receive Data (B)
15	SRD (A)	Secondary Receive Data (A)
T	TTYO	Output to teleprinter
16	TTYO	Output to teleprinter
U	RD (A)	Receive Data (A)
17	SRD (B)	Secondary Receive Data (B)
V	RR (A)	Receiver Ready (A)
18	RR (B)	Receiver Ready (B)
W	SD (U)	Send Data (U)
19	MSB-	Most significant bit of baud rate select
X	CS (A)	Clear to Send (A)
20	NMSB-	Next to most significant bit of baud rate select
Y	CS (B)	Clear to Send (B)
21	NLSB+	Next to least significant bit of baud rate select
Z	DM (A)	Data Mode (A)
22	LSB+	Least significant bit of baud rate select
AA	DM (B)	Data Mode (B)
23	SSD	Secondary Send Data
BB	GND	
24	GND	

2-13. VIRTUAL CONTROL PANEL (VCP) INTERFACE SELECTION

Switch U1 S1 is used to select the 12005A to operate as an interface to a terminal which is functioning as a Virtual Control Panel (VCP). Note that the select code of the



7700-463

Figure 2-1. RS-449 Interface

12005A must be set to 20 (octal) when it is to function as the Virtual Control Panel interface.

U1 S1 closed (down): The 12005A has been selected to operate as interface to the Virtual Control Panel. A BREAK character will cause the 12005A to enter this mode.

U1 S1 open (up): The 12005A will not operate as a VCP interface. A BREAK character will cause a flag (Flag 30) to set.

NOTE

Switch U1 S2 is not used.

2-14. SELECT CODE SELECTION

Switches U1 S3 through U1 S8 determine the select code for the interface. Note that the select code of the 12005A must be set to 20 (octal) when it is to function as the Virtual Control Panel interface. Switch S3 selects the most significant bit and S8 selects the least significant bit of the six-bit select code.

Open (up) switch: Logic one.

Closed (down) switch: Logic zero.

2-15. BAUD RATE SELECTION

The baud rate for the 12005A can be set from 50 to 9600 baud using switches U21 S1 through U21 S4. An open (up) switch produces a logic 1, a closed (down) switch produces a logic zero. Table 2-6 shows the switch settings for the various baud rates.

2-16. STOP BIT SELECTION

Switch U21 S5 selects either one or two stop bits.

U21 S5 open: Two stop bits.

U21 S5 closed: One stop bit.

2-17. PARITY SENSE SELECTION

Switch U21 S6 selects even or odd parity.

U21 S6 open: Even parity.

U21 S6 closed: Odd parity.

NOTE

Switches U21 S7 and S8 are not used.

Table 2-6. Baud Rate Selection

S1	S2	S3	S4	BAUD RATE
0	0	0	0	External Clock (x16)
0	0	0	1	50
1	0	0	0	75
1	0	0	1	110
0	1	0	0	134.5
0	1	0	1	150
1	1	0	0	300
1	1	0	1	600
0	0	1	0	900
0	0	1	1	1200
1	0	1	0	1800
1	0	1	1	2400
0	1	1	0	3600
0	1	1	1	4800
1	1	1	0	7200
1	1	1	1	9600

An open (up) switch produces a logic 1.

A closed (down) switch produces a logic 0.

2-18. INSTALLATION

After insuring that the computer power supply can handle the added load, perform the following:

a. Select the baud rate by setting switches U21 S1 through U21 S4 as shown in table 2-6.

b. Set switch U1 S1 open or closed depending on whether the 12005A has been selected to operate as interface to a Virtual Control Panel. (See paragraph 2-13.)

c. Set switch U21 S6 open or closed to determine even or odd parity (open equals even parity, closed equals odd parity. See paragraph 2-17.).

d. Set the select code for the interface with switches U1 S3 through U1 S8 (see paragraph 2-14).

e. Install the computer system and the I/O device to be connected to the interface (if these have not already been installed).

f. Turn off power at the computer and the I/O device. Install the interface in the desired I/O slot in the computer card cage. Note that the interrupting and DMA priority of an I/O interface card depends on its location in the card cage. The card slots are numbered from XA1 (highest priority), in sequence down to the

lowest priority slot, XA10 or XA16, depending on the size of the backplane.

Components on the card must be on the same side of the card as for other cards in the I/O slots. When installing the card, use care not to damage components or traces on the card or on adjacent cards. Press the card firmly into place.

g. Connect the appropriate cable from the terminal (or a modem if one is to be used) to the 12005A interface.

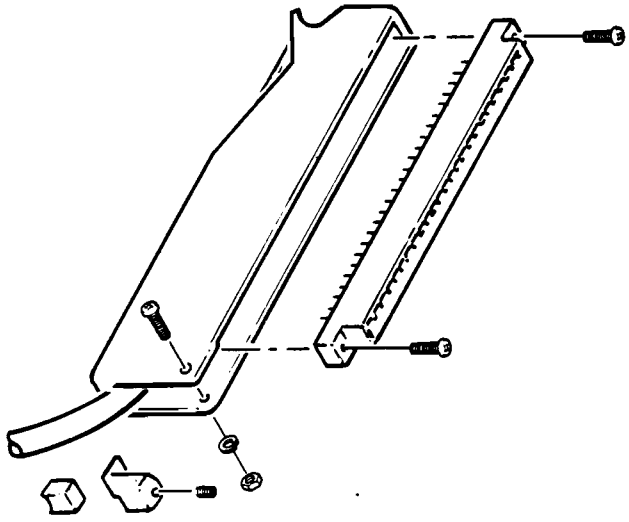
2-19. CHECKOUT

To verify operation of the interface, perform the diagnostic test for the interface. Operating procedures for the diagnostic tests are described in the HP 12005A Asynchronous Serial Interface Diagnostic Operating Manual, part no. 24397-90005.

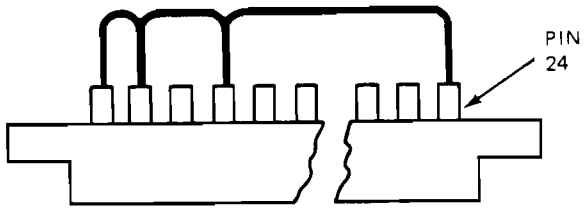
2-20. RESHIPMENT

If the interface is to be shipped to Hewlett-Packard for repair, attach a tag identifying the owner and indicating the service to be performed. Include the part number of the interface.

Pack the interface in the original factory packing material. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack the item.



DISASSEMBLY AND ASSEMBLY



48-PIN CONNECTOR

1. DISASSEMBLE CABLE CONNECTOR AS SHOWN IN TOP SECTION OF THIS FIGURE.
2. ALL PINS TO BE GROUNDED SHOULD BE JUMPERED TO 24 AND 88.

7700-462

Figure 2-2. Cable Hood Jumper Instructions

3-1. INTRODUCTION

This section provides assembly-language programming procedures for the HP 12005A Asynchronous Serial Interface and its associated terminal. For information on assembly-language programming, refer to the HP 1000 L-Series Reference Manual, part no. 02103-90007.

Although it has many capabilities such as byte packing, handling its own Direct Memory Access (DMA), decoding its own instructions from the central processor unit (CPU), and handling variable-length records, the 12005A offers the advantage of simplicity, from a software standpoint, in that it can be driven using only one control word.

3-2. USE OF THE GLOBAL REGISTER

Every I/O interface card (serial interface, parallel interface, etc.) in the HP 1000 L-Series Computer System contains a global register. The global register is located in the IOP chip and is a six-bit register which contains a select code. See figure 3-1 for a block diagram of the IOP chip.

All global registers on all interface cards are controlled by the CPU, thus all global registers contain the same select code. (It is useful, therefore, to think of all the global registers as being one "global" register.) The global register may be loaded with an OTA 2 or OTB 2 instruction, enabled with a CLF 2 instruction and disabled with an STF 2 instruction. When the global register is enabled, any instruction which is executed by the CPU automatically applies to the card whose select code is in the global register. For example, if the global register is enabled and contains the 12005A's select code, the current I/O instruction is decoded and executed by the interface. Using the global register to store select code frees the six least significant bits of I/O instructions (these bits do not need to store the select code of the I/O device which is to receive the I/O instruction). Thus, these six bits can be used to address a register on I/O interface cards. On the asynchronous serial interface, there are three such registers: one for data, one for control, and one for status, in addition to registers which are internal to the IOP chip.

Data may be transferred to and from the asynchronous serial interface with or without the global register being enabled. In order to access the interface's control and status registers, however, the global register must be used.

3-3. I/O INSTRUCTION SET

The I/O master executes twelve I/O instructions as follows:

CLC	Clear Control
CLF	Clear Flag
LIA	Load Into A
LIB	Load Into B
MIA	Merge Into A
MIB	Merge Into B
OTA	Output A
OTB	Output B
SFC	Skip if Flag Clear
SFS	Skip if Flag Set
STF	Set Flag
STC	Set Control

The six-bit global register allows a maximum of 64 (decimal) select codes. The I/O master, however, executes only a portion of this maximum. Select codes 00 through 17 (octal) are reserved for the central processor, leaving 20 through 77 (octal) available for the I/O system.

3-4. INSTRUCTION USAGE SUMMARY

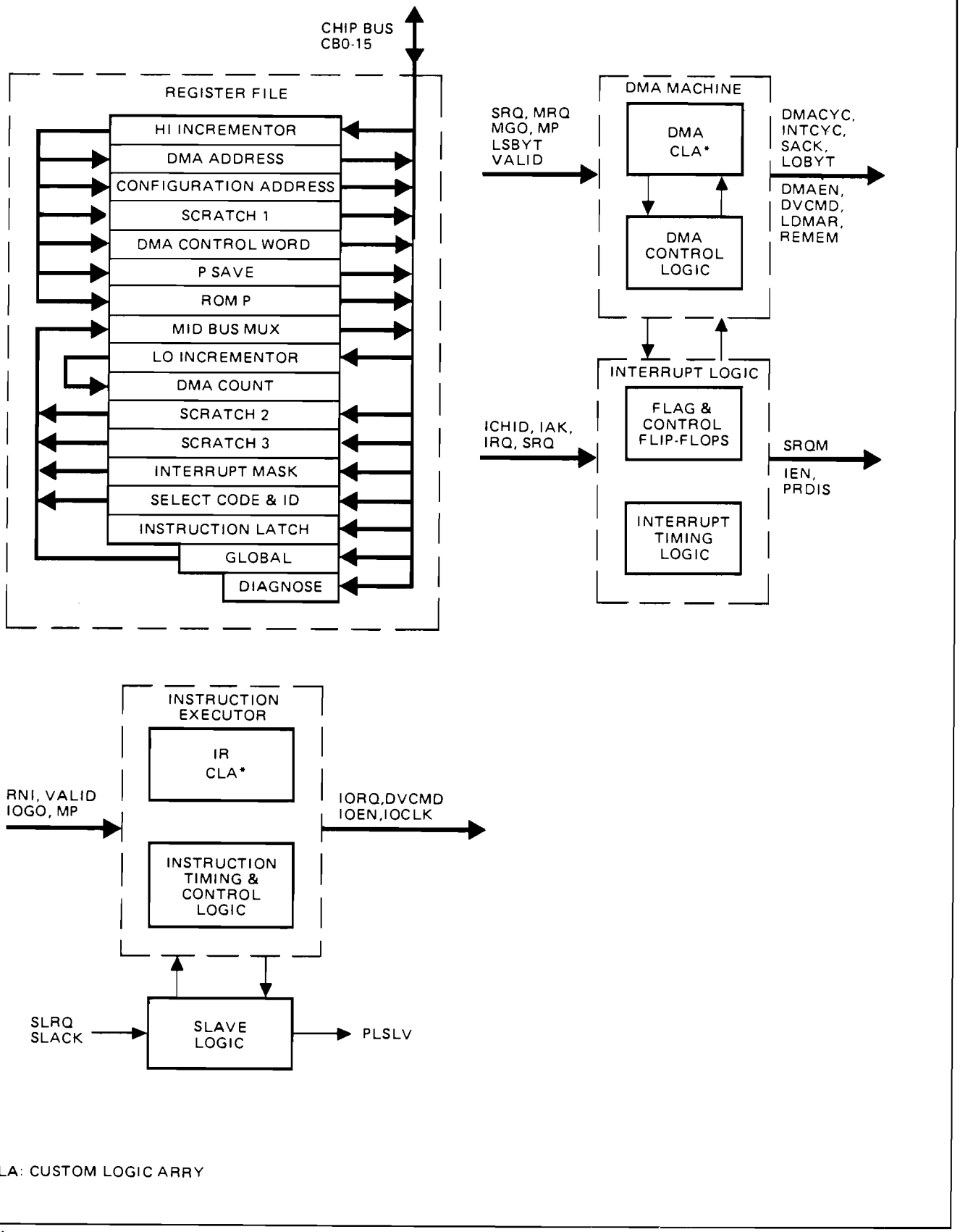
Table 3-1 lists all the instructions recognized by the IOP chip by their select code. There are three conditions relevant to the instruction execution. These conditions are as follows:

a. Is the global register (GR) enabled?

b. Do the contents of the GR equal the IOP chip's select code, (GR = SC)?

c. Do the lower six bits of the instruction register equal the IOP chip's select code, (IR = SC)?

The summary indicates which conditions must be met for instruction execution by listing Y for yes, N for no, and X for don't care in each column.



7700-464

Figure 3-1. I/O Chip Block Diagram

Table 3-1. IOP Chip Instructions By Select Code

INSTRUCTION	FUNCTION	GR ON	GR=SC	IR=SC	NOTES
LI* 0	Read interrupt mask	X	Y	X	
MI* 0	Merge interrupt mask	X	Y	X	
OT* 0	Write interrupt mask	X	X	X	
CLF 2	Enable GR	X	X	X	
STF 2	Disable GR	X	X	X	
LI* 2 [,C]	Read GR	X	Y	X	1, 9
MI* 2 [,C]	Merge GR	X	Y	X	1, 9
OT* 2 [,C]	Write GR	X	X	X	
STC 2 [,C]	Enable Slave logic	X	X	X	1, 2
[,C]	Enable GR				
CLC 3	"BREAK" to front panel	X	X	X	2
HLT XX	"BREAK" to front panel	X	X	X	2
LI* 3	Read P SAVE	X	X	X	2
MI* 3	Merge P SAVE	X	X	X	2
OT* 3	Write P SAVE	X	X	X	2
LI* 3,C	Read ROM P	X	X	X	2
MI* 3,C	Merge ROM P	X	X	X	2
OT* 3,C	Write ROM P	X	X	X	2
SFC 20	Skip if FLG 20 clear	Y	Y	X	3
SFS 20	Skip if FLG 20 set	Y	Y	X	
CLF 20	Clear FLG 20 and FLG 21	Y	Y	X	
STF 20	Set FLG 20	Y	Y	X	
STC 20 [,C]	Enable DMA self configuration	Y	Y	X	
CLC 20 [,C]	Disable DMA self configuration	Y	Y	X	
LI* 20 [,C]	Read DMA configuration address	Y	Y	X	
MI* 20 [,C]	Merge DMA configuration address	Y	Y	X	
OT* 20 [,C]	Write DMA configuration address	Y	Y	X	
[,C]	Clear FLG 20 and FLG 21				
SFC 21	Skip if FLG 21 clear	Y	Y	X	4
SFS 21	Skip if FLG 21 set	Y	Y	X	
CLF 21	Clear FLG 21	Y	Y	X	
STF 21	Set FLG 21	Y	Y	X	
STC 21 [,C]	Enable DMA transfers	Y	Y	X	
CLC 21 [,C]	Disable DMA transfers	Y	Y	X	
LI* 21 [,C]	Read DMA Control word	Y	Y	X	
MI* 21 [,C]	Merge DMA Control word	Y	Y	X	
OT* 21 [,C]	Write DMA Control word	Y	Y	X	
[,C]	Clear FLG 21				
SFC 22	Skip if FLG 22 clear	Y	Y	X	5
SFS 22	Skip if FLG 22 set	Y	Y	X	
CLF 22	Clear FLG 22	Y	Y	X	
STF 22	Set FLG 22	Y	Y	X	
CLC 22 [,C]	Force DMA reconfiguration	Y	Y	X	
LI* 22 [,C]	Read DMA address	Y	Y	X	
MI* 22 [,C]	Merge DMA address	Y	Y	X	
OT* 22 [,C]	Write DMA address	Y	Y	X	
[,C]	Clear FLG 22				
SFC 23	Skip if FLG 20, FLG 21, AND FLG 22 ALL Clear	Y	Y	X	6
SFS 23	Skip if FLG 20 OR FLG 21 OR FLG 22 Set (inclusive OR)	Y	Y	X	
CLF 23	Clear FLG 20, FLG 21, and FLG 22	Y	Y	X	
CLC 23 [,C]	Terminate DMA operation	Y	Y	X	
LI* 23 [,C]	Read DMA Count	Y	Y	X	
MI* 23 [,C]	Merge DMA Count	Y	Y	X	
OT* 23 [,C]	Write DMA Count	Y	Y	X	
[,C]	Clear FLG 20, FLG 21, and FLG 22				

Table 3-1. IOP Chip Instructions By Select Code (Continued)

INSTRUCTION	FUNCTION	GR ON	GR =SC	IR =SC	NOTES
SFC 24	Skip if DMA disabled (DMAEN — asserted)	Y	Y	X	
SFS 24	Skip if DMA enabled (DMAEN — not asserted)	Y	Y	X	
LI* 24	Read Scratch 1	Y	Y	X	
MI* 24	Merge Scratch 1	Y	Y	X	
OT* 24	Write Scratch 1	Y	Y	X	
LI* 25	Read Scratch 2	Y	Y	X	
MI* 25	Merge Scratch 2	Y	Y	X	
OT* 25	Write Scratch 2				
LI* 26	Read Scratch 3	Y	Y	X	
MI* 26	Merge Scratch 3	Y	Y	X	
OT* 26	Write Scratch 3	Y	Y	X	
SFC 30	Skip if FLG 30 clear	Y	Y	X	7
SFS 30	Skip if FLG 30 set	Y	Y	X	
CLF 30	Clear FLG 30	Y	Y	X	
STF 30	Set FLG 30	Y	Y	X	
STC 30 [,C]	Set CNTRL 30 and issue DVCMD	Y	Y	X	
CLC 30 [,C]	Clear CNTRL 30	Y	Y	X	
LI* 30 [,C]	Read device data	Y	Y	X	
MI* 30 [,C]	Merge device data	Y	Y	X	
OT* 30 [,C]	Write device data	Y	Y	X	
[,C]	Clear FLG 30				
LI* 31	Read interface control word	Y	Y	X	
MI* 31	Merge interface control word	Y	Y	X	
OT* 31	Write interface control word	Y	Y	X	
LI* 32	Read interface status	Y	Y	X	8
MI* 32	Merge interface status	Y	Y	X	
OT* 32	Reset interface status	Y	Y	X	9
SFC SC	Skip if FLG 30 clear	N	X	Y	7
SFS SC	Skip if FLG 30 set	N	X	Y	
CLF SC	Clear FLG 30	N	X	Y	
STF SC	Set FLG 30	N	X	Y	
STC SC [,C]	Set CNTRL 30 and issue DVCMD	N	X	Y	8
CLC SC [,C]	Clear CNTRL 30	N	X	Y	
LI* SC [,C]	Read device data	N	X	Y	10
MI* SC [,C]	Merge device data	N	X	Y	10
OT* SC [,C]	Write device data	N	X	Y	
[,C]	Clear FLG 30				

SC = Interface select code

Notes:

1. The [,C] is always executed even if the primary instruction is not.
2. The SLAVE logic must be enabled: i.e., SLRQ LOW at power up.
3. FLG 20 is set by DMA upon completion of self configured DMA block transfer which is not to be followed by another self configuration.
4. FLG 21 is set by DMA upon completion of any block transfer which is not to be followed by a self configuration.
5. FLG 22 is set by DMA if a parity error occurs during a DMA read.
6. FLG 23 is the logical OR of flags 20 through 22.
7. FLG 30 and CNTRL 30 are controlled by the Flag and Control flip-flops located in the IOP chip.
8. The IOP chip indicates only that the select code is in the range 32 to 77, it is up to the user to decode any specific select code.
9. Serial I/O cards, by convention, use this instruction as a card reset.
10. When the IOP chip is in diagnose mode, these instructions fetch the following:

    Diagnose mode 1 — the interface's select code and ID word.
    Diagnose mode 2 — the global register and IOP chip status bits.

3-5. OUTPUT CONTROL WORD

There are four output control words which may be sent to the interface. Three of these are used only in the DMA mode and are described in paragraphs 3-9 through 3-11. One output control word is used in any mode (DMA or non-DMA) and is the only control word necessary when DMA is not used. This control word may be sent to the interface using an OTA 31 or OTB 31 only when the global register is enabled.

In the following example, the interface is configured for transmit mode (transmit mode signifies a transfer from the computer to the terminal), and then some data is transferred.

```
LDA select code        Load and enable the global
                       register
OTA 2,C

LDA control word       Send control word to interface
OTA 31

LDA data
OTA 30                 Transfer data to terminal
STC 30,C
```

The foregoing instructions load the 12005A's select code into the A-register, send this select code to all global registers on all interface cards, and enable the global registers. A control word is then sent to the card whose select code is contained in the global registers (the 12005A interface in this case). Next, some data is loaded into the A-register, then output to the interface, and, finally, the data is transferred from the interface to the terminal and the flag bit on the interface is cleared.

The definitions of the bits in the output control word are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC1	SC2	PEE	FEE	ECHO	RCV	XMIT	CHLN	MIEN	REF RR	REF IC	REF CS	REF DM	SSD	RS	TR

Bit 0: TR Terminal Ready

1 = OFF
0 = ON

Bit 1: RS Request to Send

1 = OFF
0 = ON

Bit 2: SSD Secondary Send Data

1 = MARK
0 = SPACE

NOTE

The following four bits set up reference status to which the corresponding terminal status input lines are compared. If any of the status lines differs from the reference and MIEN (bit 7) is set, the flag (Flag 30) will be set.

Bit 3: REFDM Reference Data Mode

1 = DM OFF
0 = DM ON

Bit 4: REFCS Reference Clear to Send

1 = CS OFF
0 = CS ON

Bit 5: REFIC Reference Incoming Call

1 = IC OFF
0 = IC ON

Bit 6: REFRR Reference Receiver Ready

1 = RR OFF
0 = RR ON

Bit 7: MIEN Modem Interrupts Enable

1 = Set the flag if any of the four incoming modem control states changes from its reference programmed above

0 = Disable modem interrupts

Bit 8: CHLN Character Length Select

1 = Eight data bits

0 = Seven data bits (as in ASCII code)

Bit 9: XMIT

1 = Enable 12005A transmitter and associated logic

0 = Disable 12005A transmitter

NOTE

The effect of bit 9 is that a "1" enables the 12005A transmitter (when it is ready to transmit) to set the flag in the case of programmed I/O, or to initiate a memory read cycle in the case of DMA.

Bit 10: RCV

1 = Enable the 12005A receiver and associated logic

0 = Disable the 12005A receiver

NOTE

The effect of bit 10 is that a "1" will enable the receiver to set the flag or, in the case of DMA, to initiate a write into memory whenever the 12005A receives data.

Bit 11: ECHO

1 = Enable ECHO

0 = Disable ECHO

NOTE

When ECHO is enabled, the received data gets sent back (is "echoed") to the terminal via the Transmitted Data Line. This is true even when the interface is in transmit mode (see bit 9). Normally, you will want to turn ECHO off every time you place the interface in transmit mode.

Bit 12: FEE Framing and Overrun Error Interrupt Enable

1 = Enable
0 = Disable

(See note following bit 13 description)

Bit 13: PEE Parity Error Interrupt Enable

1 = Enable parity generation and set flag if a parity error is detected

0 = Disable parity generation and checking

NOTE

If any of the framing, overrun, or parity error detections are left enabled while the 12005A receiver is disabled, an interrupt condition could still occur if erroneous data were received. For example, during a transmission, if a key were hit at a terminal and that character had an error, an interrupt which is irrelevant to the data transmission would occur.

Normally, therefore, you will want to set bits 12 and and 13 to "0" every time you place the interface in transmit mode with the intent of operating in half- duplex mode only. Also note that it is advisable to do a card reset (see paragraph 3-29) before setting either of these bits to "1." This will clear any residual error flags which may have been set by data transfers.

Bits 15 and 14: SC1 and SC2 Special Character Select 1 and 2

SC1	SC2	
0	0	Disable special character recognition feature.
0	1	Enable Type 1 special character recognition feature.
1	0	Enable Type 2 special character recognition feature.
1	1	Enable Type 3 special character recognition feature.

See paragraph 3-32 for definitions of special characters.

3-6. INPUT STATUS WORD

It is often necessary to interrogate a terminal (or interface card) as to its status, in order to obtain such information as the cause of an interrupt or the state of a control circuit. Sixteen bits of information are available in a software accessible status word. This status word may be fetched using an LIA 32 or LIB 32 with the global register enabled. The leftmost bit (bit 15) is a valid data indicator if set; if clear, some type of interrupt condition such as, for example, a parity error occurred in the most recent byte input transfer. This leftmost bit can be tested using an SSA or SSB.

The definitions of the bits in the status word are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL DAT	BRK	PE	FE	OE	SRD	RR	EPE	LST BYT	MS CH	IC	CS	DM	RC DT	TRE	DR

Bit 0: DR Data Received

1 = Data has been received from device.

0 = No new data has been received since last STC.

Bit 1: TRE Transmitter Register Empty

1 = Transmitter has transferred data and is ready for new data.

0 = Transmitter is busy.

Bit 2: RCDT Received Data

This bit indicates the dynamic state of the Received Data line.

1 = Mark or logic one.

0 = Space or logic zero.

Bit 3: DM Data Mode

1 = OFF
0 = ON

Bit 4: CS Clear to Send

1 = OFF
0 = ON

Bit 5: IC Incoming Call

1 = OFF
0 = ON

Bit 6: MSCH Modem Line Status Change

1 = MIEN not set, or all modem input lines are equal to their reference status.

0 = MIEN is set and at least one of the four modem input lines differs from its reference state (see output control word, paragraph 3-3).

Bit 7: LSBYT Special Character Detect

1 = Special character not detected.

0 = The most recently received character was determined to be special.

Bit 8: EPE Even Parity

1 = The Universal Asynchronous Receiver Transmitter (UART) is set for even parity.

0 = The UART is set for odd parity.

Bit 9: RR Receiver Ready

1 = OFF
0 = ON

Bit 10: SRD Secondary Received Data

This bit indicates the dynamic state of the Secondary Received Data Line.

1 = Mark or logic one.

0 = Space or logic zero.

Bit 11: OE Overrun Error

1 = An overrun error was detected.

0 = No overrun error was detected.

Bit 12: FE Framing Error

1 = A framing error was detected.

0 = No framing error was detected.

Bit 13: PE Parity Error

1 = A parity error was detected.

0 = No parity error was detected.

Bit 14: BRK BREAK Character

1 = A BREAK character was detected on received data line.

0 = No BREAK has been detected.

Bit 15: VALDAT Valid Data

1 = Received data is valid.

0 = An interrupt condition occurred during the input of data.

3-7. DIRECT MEMORY ACCESS (DMA) OPERATION

The interface is capable of transferring data directly to or from memory (direct memory access). All control logic and registers necessary to supervise the memory transaction are contained in the IOP chip. Appropriate signals are available to the interface logic to signal when to enable its data onto the system data bus, when to receive data from the system data bus, and when to initiate the next interface operation. In addition, signals to the IOP chip indicate when a data transfer is needed and when an interrupt-requesting condition has occurred.

3-8. DMA CONTROL WORDS

Software DMA set up and control involves four different control words, each of which is associated with a different register. The four registers are control and status registers located in the IOP chip. Their numbers and functions are listed below:

Register Number 20, DMA Self-Configuration Register

Register Number 21, DMA Control Register

Register Number 22, DMA Address Register

Register Number 23, Word/Byte Count Register

3-9. DMA CONTROL REGISTER

The DMA control register, register number 21, is a 16-bit read/write register. The definitions of its bits (DMA Word 1) are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	STC	BYTE	RES IDU	CINT	RE MEM	FOUR	AUTO	IN							

Bits 0 through 4: Reserved.

Bits 5 and 6: Not used.

Bit 7: IN Transfer In

1 = Indicates that the direction of the data transfers is from the interface, to memory.

0 = Indicates that the direction of the data transfers is from memory, to the interface.

Bit 8: AUTO Automatic

1 = DMA control logic automatically performs the first data transfer once DMA is configured to output. On input transfers, AUTO will cause an additional DVCMD signal to be generated following the last Service Request (SRQ) signal.

0 = Once a DMA output is configured, the DMA control logic waits for the interface to initiate a service request (generate an SRQ signal) before performing the first transfer.

NOTE

Operation of the interface requires that bit 8 be set for all DMA output transfers. For input transfers, the state of this bit is optional. If set on input, it has the effect of clearing the last Data Received flag (see input status word, bit 0).

Bit 9: FOUR Fetch Four DMA Control Words

1 = Indicates that there are four DMA control words to be fetched for the current DMA configuration.

0 = Indicates that there are three DMA control words to be fetched for the current DMA configuration.

Bit 10: REMEM Remote Memory

1 = All memory requests will be accompanied by the REMEM bit, which disables standard memory and enables remote memory.

0 = Remote memory is not enabled.

Bit 11: CINT DMA Completion Interrupts

1 = Inhibits DMA transfer completion interrupts.

0 = An interrupt will be requested by the DMA logic when the word/byte count goes from −1 to 0.

Bit 12: RESIDU Residue

1 = If set, and DMA is enabled to self-configure (an STC 20 has been executed), DMA will write its word/byte count into the location from which it read the word/byte count.

0 = Word/byte count is not written.

Bit 13: BYTE Byte or Word Transfer

1 = DMA transfer is to be conducted in byte mode; that is, each data transfer is to be counted as one byte. Byte mode transfers are packed, two bytes per word, with the left byte (bits 15-8 of the data word) being transferred first.

0 = DMA transfer is a full word containing only one byte of information.

Bit 14: STC Set Control

1 = The DMA control logic will issue a Device Command (DVCMD) signal immediately following each data transfer (after each word in word mode (see bit 13), after each byte in byte mode).

0 = No Device Command signal is issued.

NOTE

Operation of the interface requires that bit 14 always be set.

Bit 15: CONT Continue

1 = If set (and an STC 20 has been executed), then at the end of a DMA block transfer, the interface will fetch the next set of DMA control words and reconfigure itself to start a new transfer.

0 = DMA will stop at the end of the current block transfer.

3-10. DMA ADDRESS REGISTER

The DMA address register, register number 22, is a 16-bit register. Its value represents the address of the first memory location to be read from or stored into when the DMA operation is initiated. The most significant bit, bit 15, is not used by the DMA control logic.

3-11. WORD/BYTE COUNT REGISTER

The word/byte count register, register number 23, is a 16-bit register whose value is the two's complement of the number of data elements to transfer. A data element may be either words or bytes, as indicated by bit 13 of the DMA control word (contained in register number 21).

The end of a data transfer is indicated by the transition of the word/byte count register's value from −1 to 0. (Rollover from octal 177777 to 000000 occurs.) This allows up to 65,536 data elements to be transferred at any one time. The memory size (32,768 words maximum) limits a word transfer to a length of 32,768. The hardware does not detect this, however, so detection is left to the programmer.

3-12. DMA TRANSFER OPERATION

A DMA transfer is started by configuring the three DMA registers (DMA control, register 21; DMA address, register 22; and word/byte count, register 23) and the output control word (described in paragraph 3-3), and then issuing an STC intruction to register number 21 (DMA control register).

3-13. DMA INPUT TRANSFER. For an input transfer, the DMA control logic waits until the Universal Asynchronous Receiver Transmitter (UART) signals that it is ready with the first data transfer. If the transfer is in word mode, a Device Command (DVCMD) signal and a memory access are generated immediately. If the transfer is in byte mode, the DMA control logic merely responds to the interface with DVCMD and changes the sense of its byte indicator line (which indicates to the interface which of the two bytes/word is involved in the transfer). When the second byte transfer is requested, the memory write request is generated. The memory request goes directly to the backplane where memory access priority is determined by the location of the requesting card in the backplane. When the memory access request is granted, the data is transferred, the DMA word/byte count and DMA address registers are incremented, and the DMA control logic is ready to accept another data transfer request from the interface logic.

3-14. DMA OUTPUT TRANSFER. A DMA output transfer is defined as being from memory to the interface card. For an output transfer, a memory access request is generated immediately. As soon as the data is available from memory, it is passed to the interface. The data is followed by a Device Command (DVCMD) signal. In byte

mode, the byte indicator signal is changed and another DVCMD is generated when the UART indicates that it is ready to accept more data.

3-15. DMA TRANSFER TERMINATION. A DMA data transfer continues as described in paragraphs 3-13 and 3-14 above until a terminating condition is detected. The terminating conditions are:

a. Word count transition from -1 to 0. (Rollover from octal 177777 to 000000 occurs.) This indicates that all the data elements that were requested to be transferred have been transferred.

b. End-of-transmission indication by the interface logic upon recognition of a special character (see paragraph 3-31). This terminates the DMA transfer even though the word count to be transferred may not have been reached.

c. Parity error indication from memory during the read requested by the DMA control logic.

d. Detection of a Control Reset (CRS) signal. This signal is generated by the central processor during its power-up sequencing, or by execution of a CLC 0 instruction.

Note that the 12005A can effectively suspend a DMA transfer operation by not requesting any further transfers. The interface will do this when a break character is received, or when any other type of interrupt condition is detected.

3-16. DMA SELF-CONFIGURATION FEATURE

Also available in the IOP chip is circuitry that enables the three DMA registers (discussed in the preceding paragraphs) to be loaded directly from sequential memory locations. Upon completion of each successive DMA operation, the contents of register 20 are used as a pointer to the location in memory containing the next set of values to be loaded into registers 21, 22, and 23. As each register is loaded, the contents of register 20 are incremented, leaving register 20 pointing to the values to be used for the next transfer.

3-17. DMA SELF-CONFIGURATION INITIALIZATION. The DMA self-configuration feature is initialized by setting the value of register 20 to the memory address of the first word of a list of DMA triplets or quadruplets. A triplet is of the form control bits, transfer address, and word byte counts. The triplet words are the words to be used in registers 21, 22, and 23, respectively. A quadruplet is of the form control bits, interface control, transfer address, word byte count. Bit 8 of the control word determines whether a triplet or quadruplet is used. See figure 3-2 for the formats of triplets and quadruplets.

Once the DMA self-configuration feature is initialized by setting the value of register 20 equal to the memory address of the first word of a list of DMA triplets or quadruplets, an STC to register 20 starts the feature. This STC to register 20 has the effect of simultaneously setting the control on registers 20 and 21 (to achieve an initial state for full execution).

3-18. DMA SELF-CONFIGURATION OPERATION. After receiving the STC in register 20, the self-configuration control logic fetches the word addressed by the contents of register 20 and loads this word into register 21. Assume bit 7 of this word is set, signifying a quadruplet. The contents of register 20 are incremented during the memory access. The new value of register 20 is used as the address of the next memory read. This next word is loaded into the control register on the interface by means of a virtual OTA 31 generated by the IOP chip. Register 20 then is incremented for the next read and this new data is loaded into register 22. Register 20 is again incremented. The new value of register 20 is used to address the fourth word of the current quadruplet. This fourth word is loaded into register 23. The value of register 20 is again incremented, pointing to the beginning of the next triplet/quadruplet.

The DMA operation just loaded is then started as soon as the interface is ready (see paragraph 3-12). When the DMA operation terminates (see paragraph 3-15), if bit 11 of register 21 is clear, an interrupt request is generated. If the DMA operation terminated due to either an end-of-transfer indication from the interface or a word/byte count transition from -1 to 0, then the DMA self-configuration logic writes the word-count residue into the location formerly occupied by the current DMA operation's word/byte count. Operation of the self-configuration feature is continued, as noted above, for the next triplet/quadruplet.

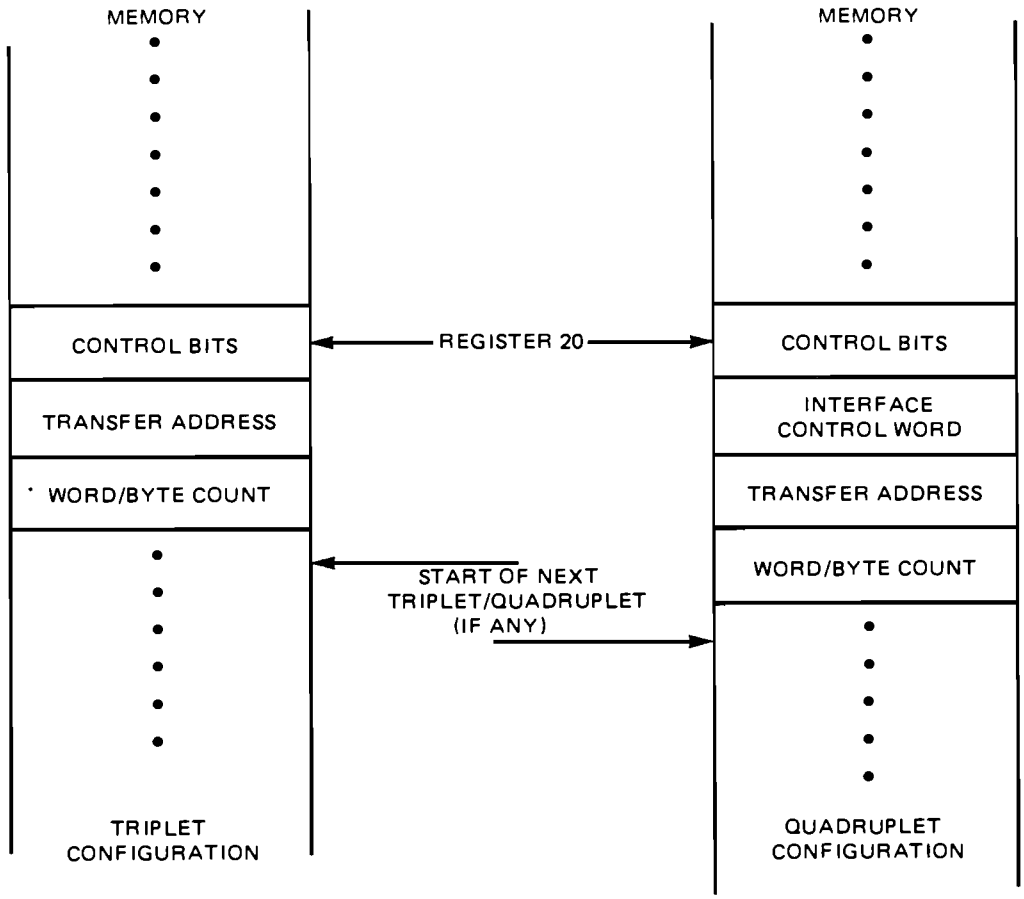
3-19. DMA SELF-CONFIGURATION TERMINATION. The operation of the DMA self-configuration feature continues as described in the preceding paragraphs until one of the following events occurs:

a. A CLC to register number 20 is executed. This serves to inhibit the self-configuration logic from advancing its pointer to the next triplet/quadruplet, while still allowing the current DMA to continue. An STC to register number 20 allows the self-configuration feature to continue.

b. A CLC to register 21 is executed. This stops the current DMA operation at its present state of operation.

c. A CLC to register number 22 is executed. This aborts the current DMA operation and causes the self-configuration logic to advance to the next triplet/quadruplet. No interrupt is generated by the aborted transfer.

d. A CLC to register number 23 is executed. This stops the operation of the self-configuration logic and aborts the transfer in progress.



REGISTER NUMBER 20 POINTS TO THE STARTING ADDRESS OF THE TRIPLET/QUADRUPLET.

THE "CONTROL BITS" ARE LOADED INTO DMA REGISTER NUMBER 21.

THE "TRANSFER ADDRESS" IS LOADED INTO DMA REGISTER NUMBER 22.

THE "WORD/BYTE COUNT" IS LOADED INTO DMA REGISTER NUMBER 23.

THE "INTERFACE CONTROL WORD" IS LOADED INTO REGISTER NUMBER 31.

Figure 3-2. DMA Self-Configuration Feature

e. The first word of a triplet is read with the CONT bit clear, indicating that there are no further DMA triplets. This sets the flag on register number 20, which generates an interrupt request if the control flip-flop of register number 20 is set.

3-20. FORMAT SUMMARY

The following paragraphs contain a reference guide to all control and data word formats for the interface.

3-21. CONTROL WORD OUTPUT (REGISTER NUMBER 31)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC1	SC2	PEE	FEE	ECHO	RCV	XMIT	CHLN	MIEN	REF RR	REF IC	REF CS	REF DM	SSD	RS	TR

3-22. STATUS WORD INPUT (REGISTER NUMBER 32)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VAL DAT	BRK	PE	FE	OE	SRD	RR	EPE	LST BYT	MSCH	IC	CS	DM	RCDT	TRE	DR

3-23. DMA REGISTER NUMBER 20 (IN OR OUT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POINTER TO DMA TRIPLET/QUADRUPLET															

3-24. DMA REGISTER NUMBER 21 (IN OR OUT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONT	STC	BYTE	RES IDU	CINT	RE MEM	FOUR	AUTO	IN	NOT USED						

3-25. DMA REGISTER NUMBER 22 (IN OR OUT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA ADDRESS															

3-26. DMA REGISTER NUMBER 23 (IN OR OUT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA WORD/BYTE COUNT															

3-27. DMA BYTE MODE DATA (IN OR OUT) (REGISTER NUMBER 30)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRST BYTE OF DATA TRANSFERRED								SECOND BYTE OF DATA TRANSFERRED							

3-28. DMA WORD MODE DATA OR NON-DMA DATA (IN OR OUT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED								DATA							

3-29. SAMPLE PROGRAMMED I/O ROUTINE

The following is an example of a full-duplex mode programmed I/O driver. Assume that the global register has already been loaded and enabled.

```
I.O     NOP
        OTA CSR       •OUTPUT CONTROL WORD
        OTB DR        •OUTPUT DATA WORD
        STC DR,C      •TRANSFER DATA IN OR OUT
        SFS DR        •WAIT FOR TRANSFER COMPLETE
        JMP•-1
        LIA DR        •GET DATA INPUT
        LIB SR
        SSB           •CHECK FOR ERRORS
        JMP I.?,I     •RETURN
        JSB ERROR

ERROR   NOP
        LIA CSR       •FETCH STATUS
                .
                .
                .
                      •IDENTIFY ERROR AND DEAL WITH IT
                .
                .
                .

RCV     LDA CWR       •CONTROL WORD FOR RECEIVE MODE IS LOADED
                       INTO A
        JSB I.O
                .
                .
                .     PROCESS DATA
                .
                .
                .

XMIT    LDA CWX       •CONTROL WORD FOR TRANSMIT MODE IS LOADED
                       INTO A
        LDB           •DATA BYTE IS LOADED INTO B
        JSB I.O
                .
                .
                .
                .
                .
```

3-30. HP 12005A ASYNCHRONOUS SERIAL INTERFACE INITIALIZATION

The 12005A responds to three different types of resets. There are two system resets, one of which occurs on power up and the other on execution of a CLC 0. When either of these events occurs, a reset signal is generated throughout the entire computer system, forcing every card into a known state. In many cases it may be desirable to reset the 12005A without performing a system reset. The third type of reset, which is an OTA 32 with the global register enabled, accomplishes this. (The A register should have bit 0 clear before performing this operation.)

Table 3-2 lists all the initialization functions performed on the interface and when they are done (on power up (PON), or on execution of CLC 0 or OTA 32).

Table 3-2. Initialization Functions

FUNCTION	WHEN ACCOMPLISHED		
	PON	CLC 0	OTA 32
Special character feature off	X	X	X
Parity, Framing, Overrun, Interrupts Disabled	X	X	X
Echo feature off	X	X	X
Transmit mode off	X	X	X
Receive mode off	X	X	X
Seven bit character bit selected	X	X	X
Modem interrupts disabled	X	X	
All RS-449 output control lines ON	X	X	
Parity Generation and checking disabled	X	X	X
Break Character flag cleared	X	X	X
Baud rate set to agree with select lines	X		
PE, FE, OE flags cleared	X	X	X
Data Received (DR) flag cleared	X	X	X
Abortion of any transmission in progress	X	X	X
Diagnose Mode OFF	X	X	

3-31. VIRTUAL CONTROL PANEL

The Virtual Control Panel is an interactive program that replaces a conventional hardware front panel. Because the L-series does not have a front panel, provision has been made so that an I/O interface card may be selected as the interface to a Virtual Control Panel (VCP). See Section II, paragraph 2-16, for instructions on selecting the 12005A to be the VCP interface.

A terminal being used as the VCP provides control and access to the CPU in a manner similar to a hardware front panel. It enables the operator to access the various registers (A, B, P, etc.), examine or change memory, or control execution of a program. The VCP program is located in a Read-Only Memory (ROM) located on the central processor card.

Only one card in the L-Series computer system can be selected as the VCP interface at any given time. The VCP mode can be entered in any one of three ways:

a. After power up, the boot loading program is directed to the VCP ROM program in lieu of a boot routine.

b. When the VCP interface receives a BREAK character from the terminal, this will not cause an interrupt, instead, the Virtual Control Panel routine will be entered.

c. Certain software instructions cause the VCP routine to be entered as follows:

1. An STC 3 or HALT instruction causes the interface card to simulate a BREAK The STC instruction does not cause a Memory Protect violation, thus maintaining the system when the VCP program is entered.

2. A CLC 3 instruction causes a simulated break after four instructions are executed. The CLC 3 instruction is used by the VCP program to allow the operator to single step through instructions.

For more information on the operation of the Virtual Control Panel, see the Asynchronous Serial Interface Diagnostic Operating Manual, part no. 24397-90005.

When the 12005A is used as the Virtual Control Panel interface, its select code must be set to 20 (octal).

3-32. SPECIAL CHARACTER RECOGNITION FEATURE

The 12005A has the hardware capability of monitoring the incoming serial data stream for any one of a set of special characters. A special character can be any 7- or 8-bit pattern designated as such. Special character recognition is accomplished with the use of a 256 by 4 ROM. There are three types of special characters as shown in table 3-3. Each special character type comprises a set of characters

Special characters in each of the sets have been chosen because they have traditionally been used as End of Transmission (EOT) markers.

An EOT marker is an important feature for DMA input operations. If the interface is configured for an n-word DMA input transfer, and less than n words are received, an EOT is necessary so that the interface does not hang up, waiting for non-existent data.

When the special character recognition logic on the 12005A recognizes a special character (and the special character recognition feature of that particular type has been enabled in the Output Control Word, see paragraph 3-3), the I/O chip is informed that the last byte of the transfer was received and the DMA completion interrupt occurs.

Table 3-3. Special Character Sets

TYPE 1	TYPE 2	TYPE 3
Carriage Return (%15)		
Back Space (%10)		
Rubout (DEL) (%177)	Record Separator (RS) (%36)	Carriage Return (%15)
CNTL D (EOT) (%4)		
DC2 (%22)		
NOTE. % signifies octal.		

3-33. SUMMARY OF I/O INSTRUCTION USAGE

3-34. OTA/OTB

Without the global register enabled, an OTA/OTB to the select code of the 12005A will transfer data to the terminal. In order to transfer control information to the 12005A, the global register must be set up and enabled. An OTA/OTB to select code 2 loads the global register. Under global register control (the global register is enabled), the register addresses are defined as follows:

OTA/OTB 2	Controls diagnostic mode of the interface (see Section V).
OTA/OTB 20	Transfers self-configurating DMA starting address to the interface.
OTA/OTB 21	Transfers DMA control word (see paragraph 3-8) to the interface.
OTA/OTB 22	Transfers DMA starting address to the interface.
OTA/OTB 23	Transfers DMA word or byte count to the interface.
OTA/OTB 30	Transmits one byte of data to terminal.
OTA/OTB 31	Transfers control word (see paragraph 3-3) to the interface.
OTA/OTB 32	Card Reset (LSB of A is clear).
OTA/OTB 32	Card Reset (LSB of A is set). The 12005A is reset and placed in diagnose mode (see paragraph 4-18).

3-35. LIA/LIB

Without the global register enabled, an LIA/LIB to the select code of the 12005A will input data from the terminal. In order to fetch status information, or to read back any of the control registers, the global register must be set up and enabled. Under global register control, the register addresses are defined as follows:

LIA/LIB 20	Reads next address to be used by DMA self-configuration feature. It is advisable to perform a CLC 20 before reading this register in order to insure its accuracy.
LIA/LIB 21	Reads the DMA control word (see paragraph 3-8) from the interface.
LIA LIB 22	Reads the next DMA address. It is advisable to perform a CLC 21 before reading this register in order to insure its accuracy.
LIA/LIB 23	Reads the remaining word or byte count. Again, it is advisable to perform a CLC 21 first.
LIA/LIB 30	Inputs a byte of data from the terminal.
LIA/LIB 31	Reads the interface control word (see paragraph 3-5).
LIA/LIB 32	Reads the status word (see paragraph 3-6).

3-36. STC

Without the global register enabled, an STC to the select code of the interface serves to set the Control flip-flop, thereby enabling interrupts. A Device Command (DVCMD) signal is also generated. Under global register control, an STC has various meanings defined as follows:

STC 20	Enables the DMA self-configuration feature. An STC with the Clear Flag bit set starts the transfer (see paragraph 3-16).
STC 21	Enables a normal DMA transfer. With the Clear Flag bit set, STC 21 also starts the transfer (see paragraph 3-12).
STC 30-77	Sets the Control flip-flop, enabling non-DMA interrupts, and generates a Device Command (DVCMD) signal.

3-37. CLC

Without the global register enabled, a CLC to the select code of the 12005A has the same effect as a CLC 30-77 as defined below. A CLC 3 (select code 3) will invoke the Virtual Control Panel which only affects the 12005A if it is set to operate in this mode (see paragraph 3-31). A CLC 0 generates a system reset signal. Under global register control, a CLC has various meanings defined as follows:

CLC 20	Suspends the operation of the DMA self-configuration logic. Does not suspend current DMA operation.
CLC 21	Suspends the operation of the current DMA transfer.
CLC 22	Aborts the current DMA transfer. If self-configuration feature is enabled, proceed to next transfer in the self-configuration list.
CLC 23	Aborts the DMA self-configuration feature and any transfer in progress.
CLC 30-77	Resets the Command flip-flop, disabling interrupts.

3-38. STF

Without the global register enabled, an STF to the select code of the 12005A sets the Flag flip-flop. An STF 2 disables global register operation. Under global register control, an STF has various meanings defined as follows:

STF 20	Sets the DMA self-configuration Flag flip-flop.
STF 21	Sets the DMA Flag flip-flop.
STF 30-77	Sets the Flag flip-flop.

3-39. CLF

Without the global register enabled, a CLF to the select code of the interface clears the Flag flip-flop. A CLF 2, or any instruction to select code 2 with the Clear Flag bit set, enables global register operation.

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION

The HP 12005A Asynchronous Serial Interface provides asynchronous serial communications between the central processor and an RS-449 compatible terminal or modem. In this section, the word "terminal" refers to the peripheral device being controlled by the interface, the terms "data in" and "received data" refer to data from the terminal to the processor or memory, and the terms "data out" and "transmitted data" refer to data from the processor or memory to the terminal.

As noted in Section I, the interface contains an I/O master which provides the interface with the capability of handling its own memory accesses (direct memory access (DMA)), of decoding its own instructions, and of forcing the central processor into slave-mode processing. Figure 4-1 shows the interface in a typical HP 1000 L-Series system. As shown, the interface can be installed in any I/O slot (an I/O slot is any slot below the processor card in the backplane), and then connected by a cable to a terminal or modem.

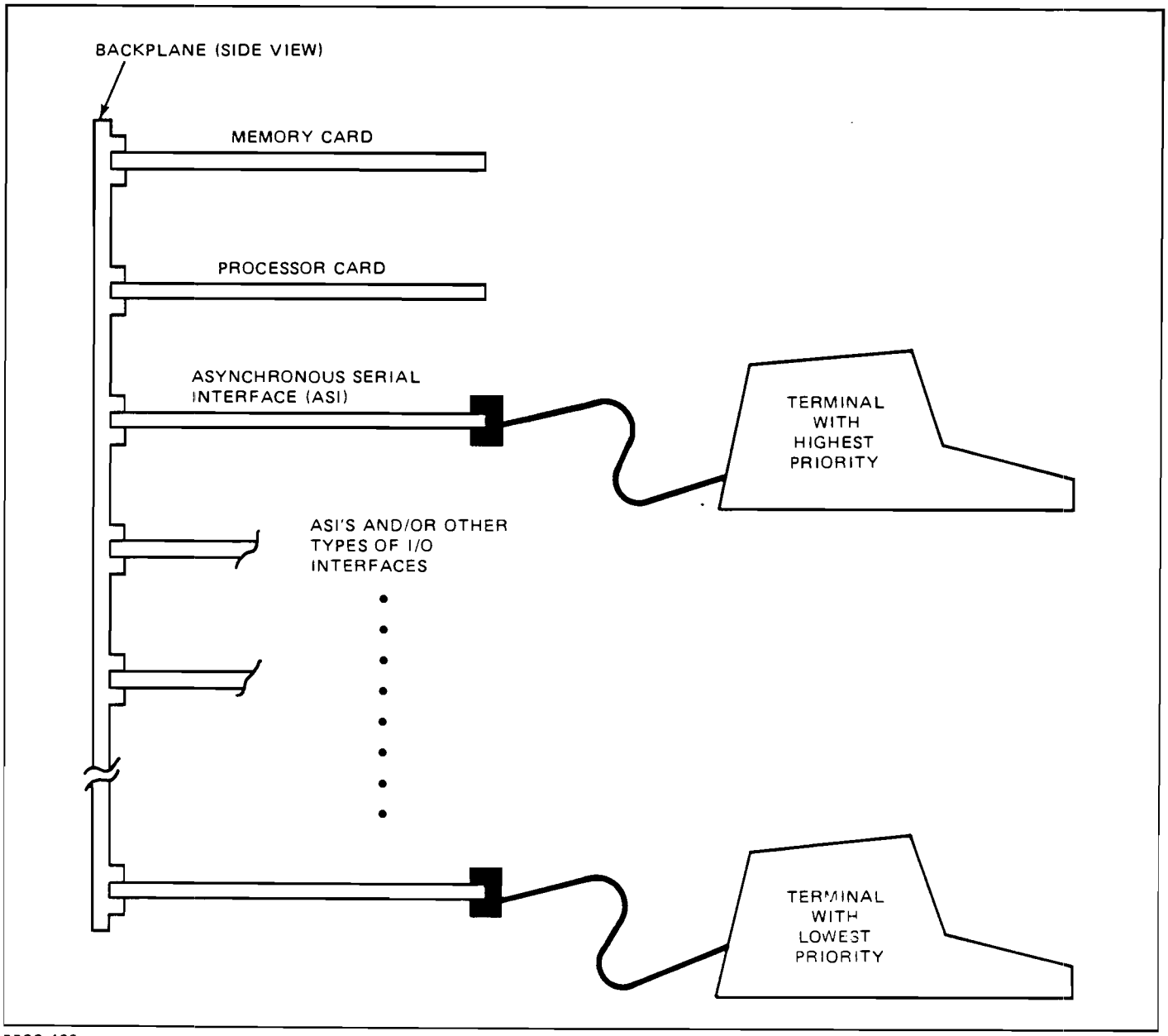


Figure 4-1. Asynchronous Serial Interface in Typical L-Series System

A six-bit select code for the interface is set by a dual in-line package switch (U1) located on the interface. This select code is used only as a means of addressing the card (and the terminal to which it is connected) and bears no relation to the interrupt and DMA priority of the interface. Interrupt and DMA priority are determined solely by the physical location of the interface in the card cage. The card slots are marked XA1 (highest priority), in sequence down to the lowest priority slot, XA10 or XA16, depending on the size of the backplane.

4-2. ASYNCHRONOUS SERIAL COMMUNICATION FORMAT

The term "asynchronous serial communications" means that characters are transferred serially between the interface and the terminal, each character is framed by start and stop bits and an optional parity bit, and the characters do not recur at predictable intervals.

The format of asynchronous serial communications is shown in figure 4-2. A "mark" condition is a logic one and a "space" condition is a logic zero. When no character is being transferred, the line is in the mark condition; a transition to the space condition indicates that a character is about to be transferred. One bit time later, the least significant bit of the character is driven onto the bus. After seven bits (ASCII) or eight bits (binary) are transferred, an optional parity bit is transferred. The line then returns to the mark state (signifying a stop bit) for at least one bit time period to indicate end of transfer.

The interface drives and receives its data from the backplane in parallel from a 16-line data bus. When the interface receives 16 bits of data from the backplane (containing either one or two bytes of information), it must then convert these bits to the format shown in figure 4-2 so that they can be sent in serial form to the terminal.

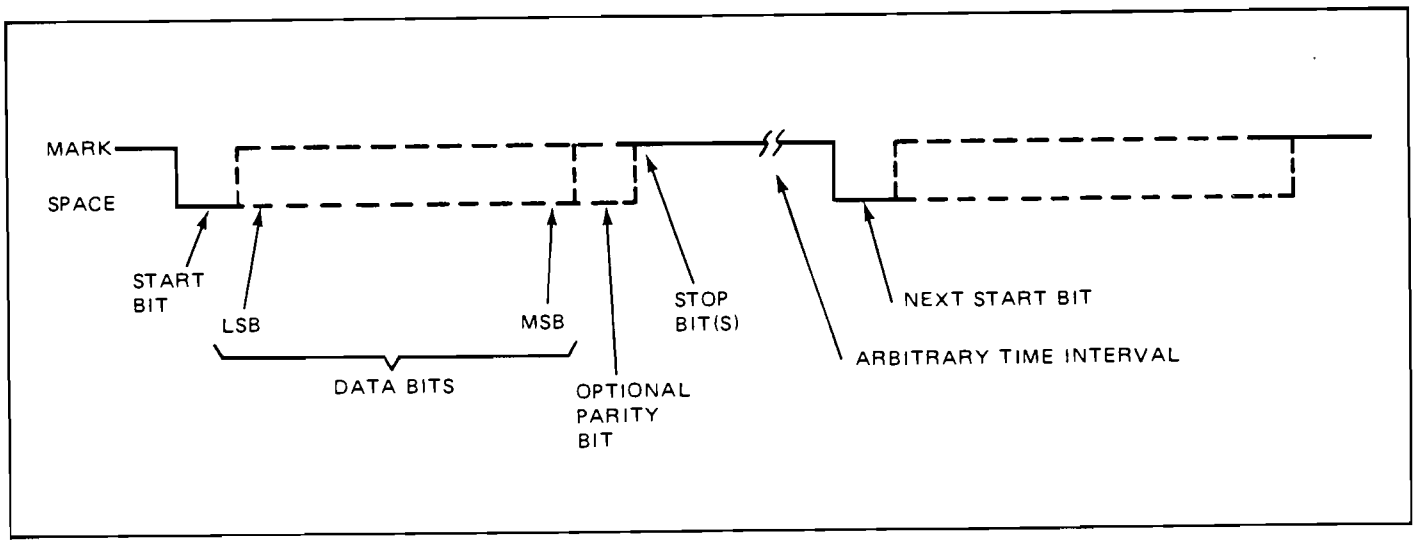
4-3. BASIC OPERATION OF THE ASYNCHRONOUS SERIAL INTERFACE

The simplified diagram shown in Section I, figure 1-3 illustrates the basic operation of the asynchronous serial interface.

The I/O master, consisting of the IOP chip and other support logic, performs all interaction between the backplane and the interface. This includes decoding and executing I/O instructions and direct memory access (DMA) operations.

The Universal Asynchronous Receiver/Transmitter (UART) performs the parallel-to-serial and serial-to-parallel data conversions. The UART also generates a start bit, one or more stop bits, and an optional parity bit when sending data to the terminal; and checks for start, stop, and parity bits on the data line coming from the terminal. Also, for data from the terminal, the UART generates a framing error if the correct stop bits are absent, and an overrun error if characters are being received from the terminal faster than the processor can receive them (so fast that they overwrite each other).

The data path directly into memory (DMA) also is shown in figure 4-3. The IOP chip contains a DMA controller and can drive the address bus; thus, transfers not involving the processor are possible. The ability of the interface to handle its own DMA significantly reduces the processing requirements of the central processor.



7700-468

Figure 4-2. Asynchronous Serial Communications Format

4-4. TRANSMIT MODE

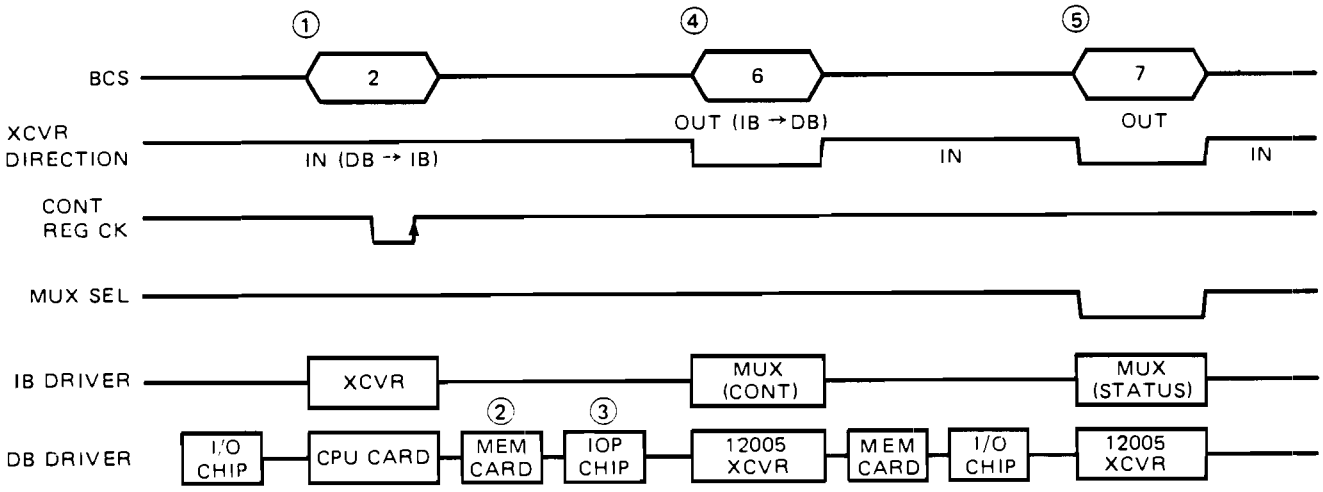
Transmit mode is defined as the transfer of data from the central processor (or, in the case of DMA, from memory) to the terminal. In transmit mode, the interface receives 16 bits of parallel data, containing one or two bytes, from the backplane data bus. The interface converts this parallel data to serial data, adds start and stop bits and an optional parity bit, and transfers the data one bit at a time (serially) to the terminal. Once set for transmit mode by a software control word (see Section III), the interface can accept any number of data transmissions without being reset.

As an example, assume that the interface is configured for transmission of programmed I/O (as opposed to DMA). The CPU fetches an OTA instruction, and the IOP chip, recognizing its select code and the instruction, performs the I/O handshake which signals the processor to drive the A register onto the data bus. The interface clocks this data into its output buffer registers. Next, there must be an STC instruction in order for the control logic on the interface to write the data into the UART. The UART adds start and parity bits, and the data is shifted out serially to the terminal.

Once the UART has finished transmitting the last stop bit, it signals to the I/O master that it is finished. The I/O master then sets its flag, as an indication that it is ready for more data. If the interface were configured for DMA, it would not set the flag; instead, the I/O master would request a memory cycle so that more data could be fetched from memory. The flag, in the case of DMA, would not get set until either there was some interrupt-causing condition such as a BREAK character, or until the DMA transfer was complete.

4-5. RECEIVE MODE

Receive mode is defined as the transfer of data from the terminal to the CPU (or, in the case of DMA, to memory). The serial data from the terminal is received by the UART, where the parity and framing are checked and the data is converted to parallel. Additional logic on the interface performs such functions as echoing the characters back to the terminal (if the echo feature was enabled in the control word). When the UART has received a character, the interface logic loads this character into the interface's input buffer. If the interface is programmed for normal I/O, an interrupt is then generated (flag is set), so that the CPU will be instructed to perform an LIA or LIB in order to fetch the data. If the interface is programmed for DMA, the I/O master logic will request a memory cycle, so that the received character can be written to memory.



1. ONCE AN OTA 31 HAS BEEN DECODED, THE IOP CHIP ASSERTS BCS2. THE PROCESSOR CARD IS DRIVING THE A REGISTER ONTO THE DATA BUS. THIS DATA IS BUFFERED INTO THE INTERFACE'S TRANSCEIVERS AND THE CONTROL REGISTER.
2. THIS IS AN INSTRUCTION FETCH OF THE LIA 31. MEMORY DRIVES THIS INSTRUCTION ONTO THE DATA BUS.
3. THE IOP CHIP DECODES THE INSTRUCTION AND DRIVES ITS CONTROL WORD ONTO THE DATA BUS.
4. THE IOP CHIP ASSERTS BCS6 WHICH CAUSES THE CONTROL/STATUS MULTIPLEXER TO DRIVE THE CONTROL WORD ONTO THE INTERNAL BUS. THE INTERFACE TRANSCEIVERS BUFFER THE CONTROL WORD ONTO THE DATA BUS.
5. THE IOP CHIP ASSERTS BCS7. THIS CAUSES THE CONTROL/STATUS MULTIPLEXER TO SELECT STATUS, AND THE BUSES ARE DRIVEN AS DESCRIBED ABOVE.

7700-467

Figure 4-3. Instructions OTA 31, LIA 31, LIA 32 Timing Diagram

4-6. FULL-DUPLEX OPERATION

The interface is capable of full-duplex operation, which means that receive and transmit modes are not mutually exclusive and that both the receiver and transmitter can be enabled at the same time.

When operating in full-duplex mode, the programmer must write the driver so that the status word (see Section III, paragraph 3-5) is fetched from the interface between every transfer. This is necessary in order to ascertain whether the flag was set because the transmitter was ready for new data, or because the receiver had received some new data.

Full-duplex operation is only possible when performing programmed I/O. Because the IOP chip contains only one DMA channel, the interface effectively operates in half-duplex mode when DMA is operating.

4-7. FUNCTIONAL THEORY OF OPERATION

The following paragraphs contain functional theory of operation for the interface. A detailed functional block diagram is shown in Section VII, figure 7-2. Reference also should be made, as necessary, to the schematic logic diagram contained in figure 7-4.

4-8. PRINCIPAL DATA PATHS

A set of bus transceivers (U55, U65) is used to buffer the system data bus (DB0 - DB15) onto the interface's internal bus (IB0 - IB15). Receiving the internal bus (IB) are a 16-bit data output register (U85, U95), and a 16-bit control register (U74, U75). Driving the IB are a 16-bit data input register (U84, U94) and a tri-state selector (U54, U64, U93, U103) which multiplexes 16 status bits with the 16-bit control register (U74, U75, mentioned above). The control register is therefore a readable/writeable register.

A timing diagram for the execution of instructions OTA 31, LIA 31, LIA 32 is shown in figure 4-3. All data bus (DB) and IB bus management is controlled by the IOP chip (U67) and a state decoder (U46). While executing I/O instructions or running DMA, the IOP chip controls the buses by asserting any one of several control signals (BCS1 - BCS7) which indicate when to latch or drive the bus. For example, BCS5 drives the data register onto the data bus, and is asserted whenever an LIA with the interface's select code is executed during programmed I/O, or whenever the interface is performing a write to memory during DMA input. When BCS5 is asserted, the interface's data input register (U84, U94) is enabled onto the IB, and the bus transceivers drive the IB onto the system DB.

4-9. TRANSMITTED DATA PATH. Next to the IOP chip, the most functionally complex chip on the interface is the UART. The UART's transmitter section converts parallel data to serial data, and adds a start bit, one or more stop bits, and an optional parity bit.

A timing diagram for transmitted data is shown in figure 4-4. An 8-bit data register located in the UART is loaded from the lower byte of the data output register (U85, U95) during programmed I/O. During DMA, the 8-bit data register is loaded alternately from the upper byte and then the lower byte of the data output register. In either case, LOBYT-, a signal generated by the IOP chip, points to the byte of data to be transmitted next. This byte is loaded into the UART's transmitter register after the UART indicates that it is ready for data by asserting TRE (Transmitter Register Empty). In the UART, the data is converted to serial form, and then sent to three types of line drivers connected in parallel. The three types of line drivers are as follows:

a. The 20 mA current loop driver (Q1), used mainly for teleprinters.

b. The RS-423 driver (U81), which is downward compatible to RS-232.

c. The RS-422 driver (U31) for higher speed and noise immunity applications.

4-10. RECEIVED DATA PATH. A timing diagram for received data is shown in figure 4-5. The UART's receiver section converts serial data to parallel data, and checks the parity and framing (start and stop) bits.

Data is received into one of two serial ports, as follows:

a. The 20 mA current loop receiver (U82).

b. An EIA-standard differential line receiver (U51).

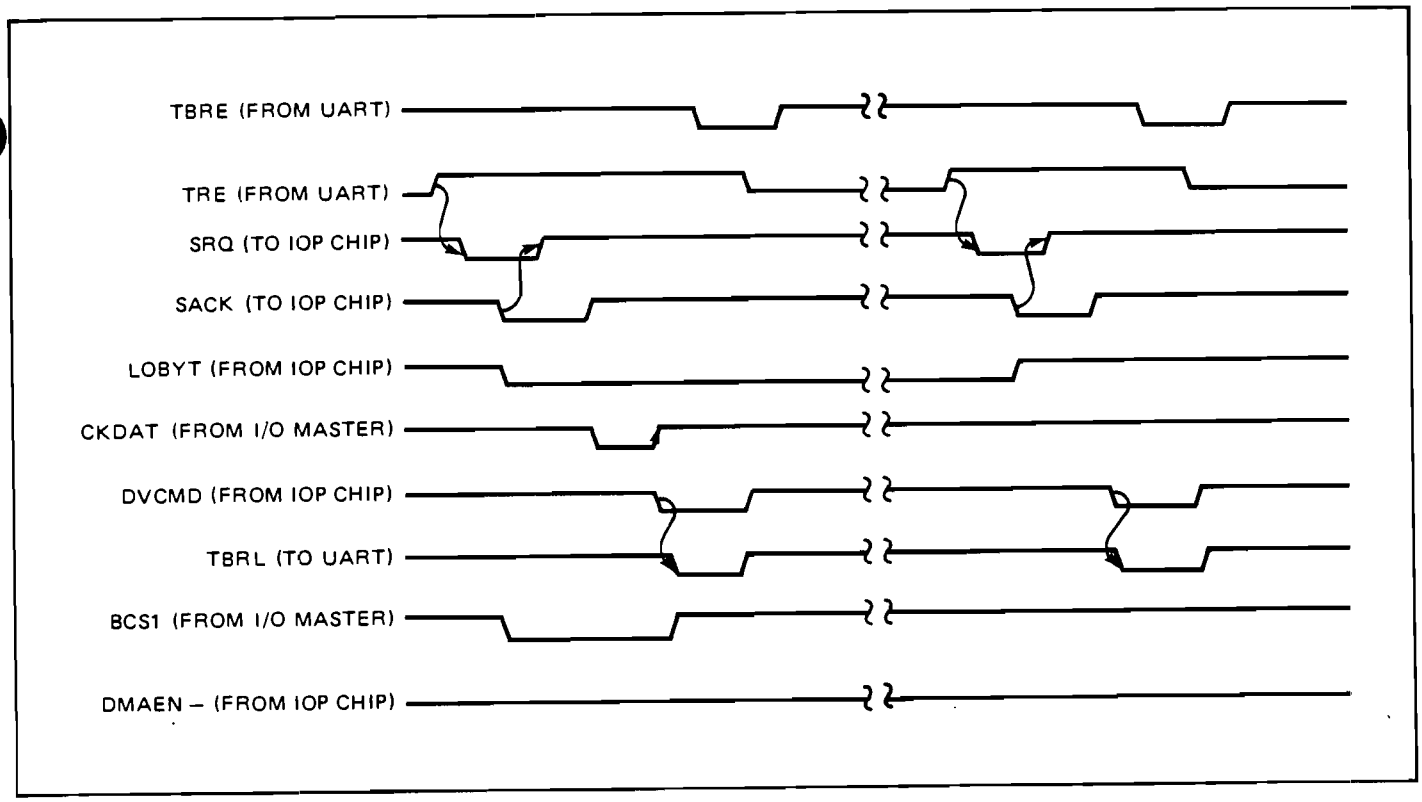
The serial data line becomes a TTL logic level on the interface and is sent to three places:

a. It is looped back (echoed) to the data transmitter drivers if the ECHO bit is set in the control word.

b. It is sent to the break detect logic (U24, U42).

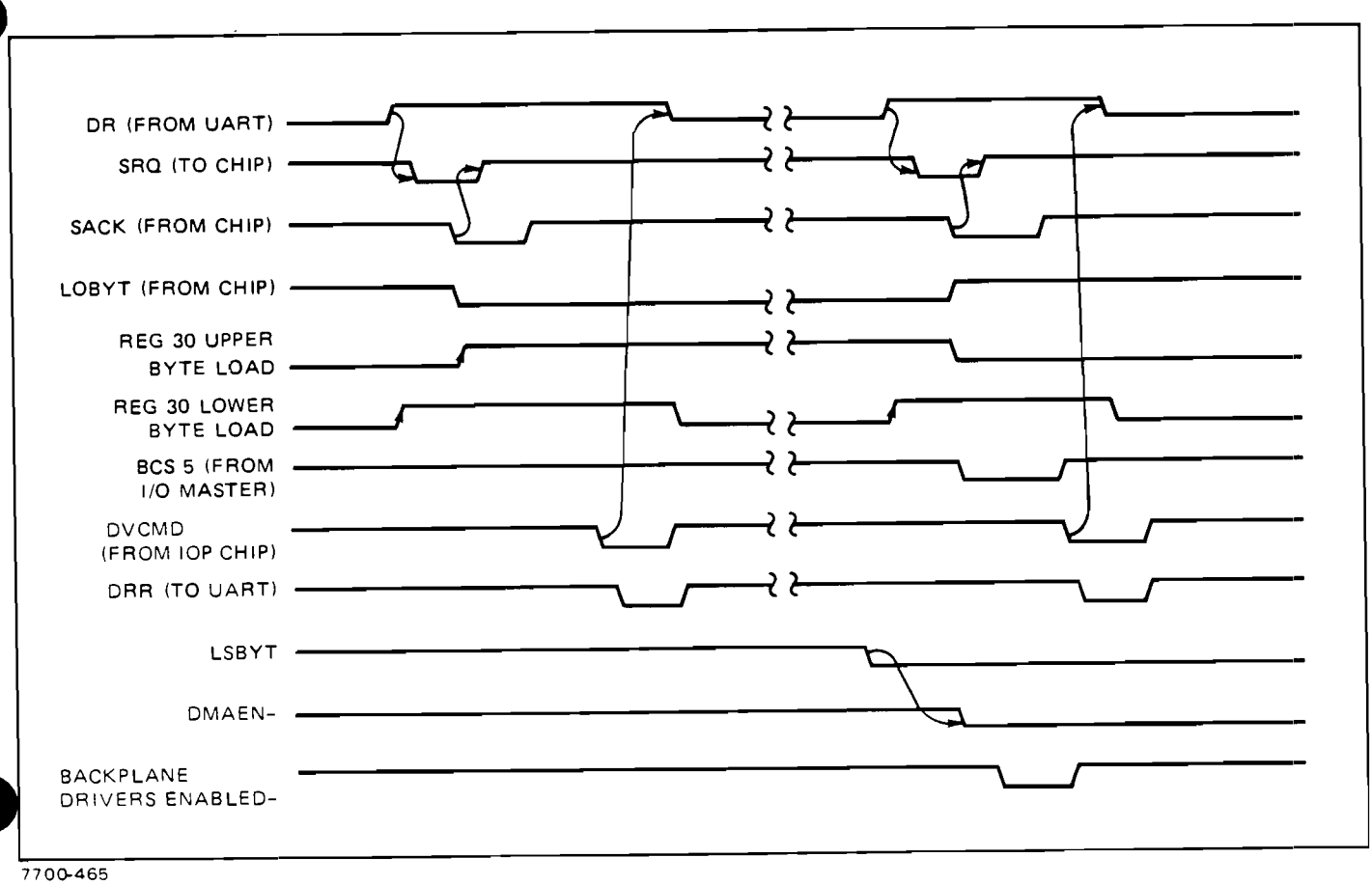
c. It is sent to the receiver section of the UART, where it is converted to parallel form.

As soon as the UART converts the received data to parallel form, it asserts DR (Data Received), which loads the data into the interface's data input register (U84, U94). If the IOP chip has been programmed to perform byte packing, the signal LOBYT will steer the data into the upper or lower byte of the data input register as necessary. If byte packing has not been programmed, LOBYT will stay low, indicating that only the lower byte of the 16-bit data word is to be valid. Once the data is in the data input register, it is driven onto the backplane data bus (DB) when BCS5 is asserted by the I/O state decoder (U46).



7700-466

Figure 4-4. Transmitted Data Timing Diagram



7700-465

Figure 4-5. Received Data Timing Diagram

4-11. SERVICE REQUEST LOGIC

All data transfers on the interface make use of a handshake with the IOP chip. This handshake consists of the signals SRQ, SACK, and DVCMD. The interface asserts SRQ to request service from the IOP chip. The IOP chip acknowledges this request by asserting SACK. When the actual data transfer is complete, the chip asserts DVCMD. These signals are explained in detail in the following paragraphs.

First, consider the case of an input transfer. The interface is configured to input which implies that RCV = 1. When the UART receives a byte, it asserts DR, which clocks on the Receive flip-flop (U53). DR also clocks the data into the lower byte of the data input buffer (U84). If a BREAK character is not pending, the setting of the Receive flip-flop causes the assertion of SRQ. SACK is then returned by the IOP chip, clearing the Receive flip-flop. As soon as an LIA 30 is executed, or, in the case of DMA, as soon as a memory write cycle has been granted, BCS5 is asserted by the I/O state decoder (U46), and the interface drives its data onto the backplane data bus. Once this is complete, the IOP chip asserts DVCMD to signal that the transfer is complete. DVCMD is ANDed with RCV (U52) to produce DRR, a signal to the UART which resets the DR flag. DR goes low until the next byte of data is received, at which time the sequence described above recurs.

If the interface is configured to output, then XMIT = 1. The data to be output is first loaded into the interface's output buffers during BCS1. As far as the processor and memory are concerned, the transfer is complete. The IOP chip asserts DVCMD. DVCMD is ANDed with XMIT (U52) and the resulting signal is TBRL, an input to the UART which loads data into the UART's transmitter buffer register. The data is then transmitted to the terminal. Once transmission is complete, the UART asserts TRE (Transmitter Register Empty). TRE clocks on the XMIT flip-flop (U53), which generates SRQ to indicate to the IOP chip that the UART is ready for more data. The IOP chip responds with SACK which clears the XMIT flip-flop. As soon as an OTA 30 is executed, or, in the case of DMA, a memory cycle is granted, data is written to the interface and the sequence described above begins again.

4-12. INTERRUPT REQUEST LOGIC

The IOP chip sets the Flag 30 flip-flop (when the Flag 30 and Control 30 flip-flops (located in the IOP chip) are set and if interrupts are not masked, the IOP chip requests an interrupt) whenever the interface asserts IRQ (Interrupt Request). Any one of five conditions can cause the assertion of IRQ:

a. A modem interrupt occurs (this is a special case and is explained in paragraph 4-15).

b. Framing Error.

c. Overrun Error.

d. Parity Error.

e. Break.

The last four of the above conditions are ANDed with their enabling signals using an AND-OR-INVERT gate (U54). The output of the gate generates IRQ whenever a BREAK character is not pending.

As mentioned in the preceding paragraph, each error condition must be individually enabled to cause an interrupt. Framing error and overrun error are enabled by the FEE (Framing and Overrun Error Enable) bit in the control word. Parity error is enabled by the PEE (Parity Error Enable) bit in the control word. The BREAK interrupt is enabled when the Virtual Control Panel switch (U1, S1) is open. That is, if the interface is not configured for Virtual Control Panel interface, then BREAK will always generate IRQ.

The assertion of IRQ, besides setting Flag 30 (on the IOP chip), also has the function of suspending operation of the interface by turning off the XMIT and RCV flip-flops. This prevents any SRQ's from being generated, thus no more data transfers can occur. This shut down feature is useful in that all software accessible parameters such as DMA byte count or program loop counters will be valid indicators of how much good data was transferred and where an error occurred.

4-13. SPECIAL CHARACTER RECOGNITION

The incoming data stream is monitored by the interface for any characters programmed as special. This is accomplished with the use of a 256 by 4 ROM (U83). As each character is assembled into the 8-bit receiver register in the UART, it is applied to the eight address bits of the ROM. If the data bit at that location is set, the character has been marked as being special. This is indicated to the IOP chip by asserting LSBYT (Last Byte), and is provided as a bit in the status word. (There are three sets of special characters, see Section III, table 3-3.) The three sets correspond to D1, D2, and D3 outputs of the ROM (all low true). Two bits (SC1 and SC2) in the control word are capable of turning off the special character recognition feature or enabling one out of the three sets. The two special character select bits in the control word go to the select inputs of a multiplexer (U73) so that one out of the three data bits may be selected. If the special character recognition feature is disabled, LSBYT is held off (high, LSBYT is low true).

4-14. BREAK CHARACTER DETECT

The interface monitors the incoming serial data stream for BREAK characters. A BREAK character is recognized when the line remains in a spacing condition for ten bit times. The computer system is not informed by the interface that a BREAK character was received, however, until the line returns to a marking condition.

The UART clock is 16 times the incoming data bit rate, so if the line is in a spacing condition for 160 clocks, a

BREAK character has been received. An 8-bit binary counter (U42) is used with the data line wired to the clear input. Whenever the data line goes low (spaces), the counter counts, but will clear whenever the data line goes high. If a count of 160 is reached, a flip-flop (U24) is jam set. This is done by ANDing two counter outputs (128 + 32 = 160). When both these counter outputs go high, the Break flip-flop is set. The flip-flop's Q output is ANDed with the received data line to generate the signal BRK. This BRK signal is available as a bit in the status word.

The assertion of BRK causes different actions depending on the position of the Virtual Control Panel switch (U1, S1). If the switch is open, the assertion of BRK will suspend any DMA in progress and will set Flag 30 in the IOP chip. If the switch is closed, the assertion of BRK will generate SLRQ (Slave Request), an input to the IOP chip which causes the chip to invoke slave mode, thereby forcing the processor to operate out of the Virtual Control Panel program.

When the received data line has remained in a spacing condition for 128 clocks (8 bit times), but BRK is not yet asserted, PEND is asserted to indicate that a BREAK character is pending. While PEND is asserted, all interrupt requests and service requests to the IOP chip are held off until it is determined whether or not a real BREAK was received. Because a BREAK character may cause the Parity Error flag to get set or other side effects to occur, PEND serves the purpose of not alerting software until the real cause of an interrupt is determined.

The 12005A also has the capability of asserting SLRQ in response to an externally generated signal. This signal is input to the interface via a test point labeled VCP and located near the front plane of the card. There are several applications for this feature, but it is principally intended for use by the HP 1610A (Logic Analyzer) Interface as a powerful debugging tool. In this application, the user configures the 1610A to search for a certain pattern. Upon encountering this breakpoint, a signal is generated to the 12005A, which in turn halts the CPU by entering the Virtual Control Panel mode.

4-15. MODEM LINE STATUS CHANGE DETECT

There are six modem input lines to the interface. All six bits are available in the status word. Two of these lines, Receive Data (RD) and Secondary Receive Data (SRD), are data lines. The primary received data line (RD) goes to the UART as described in paragraph 4-10. The secondary received data line (SRD) goes straight to the status word, thus this secondary received serial data is only software accessible and must be read with appropriate time-outs. The remaining four lines, Clear to Send (CS), Incoming Call (IC), Data Mode (DM), and Receiver Ready (RR), are control lines and go to the control status multiplexer (U54, U64, U93, U103).

The interface can be configured so that an interrupt is generated when any of the four control lines change state. Exclusive NOR gates (U72) are used to compare each of these control lines with a reference state programmed into the control word. The outputs of these four exclusive NOR gates are wire ORed together, so that if any compare fails, and MIEN (Modem Interrupt Enable) in the control word is set, MSCH (Modem Status Change) will be asserted. This generates an IRQ to the IOP chip which sets the flag. MSCH also is available as a bit in the status word.

4-16. BAUD RATE GENERATION

The interface is a full-duplex card in that the receiver and transmitter are capable of operating independently and simultaneously. The receiver and transmitter clocks are wired together, however, so that both sections must operate at the same baud rate. The interface baud rate is selected by switches (U21, S1 through S4). These four lines all have pull-up resistors connected to them, so that when the switches are open and the diagnostic test hood is in place, the baud rate can be altered programmatically.

Fifteen different baud rates may be selected by changing the four switches; or an external clock (EXTCLK) may be selected. See table 4-1 for a description of the external clock. Two diodes clamp the external clock below +5 volts and above ground so that it can be input to a TTL inverter (U82) and then to the baud rate generator (U92). This constitutes a programmable divider, which outputs a divisor of CCLK or passes EXTCLK through, depending on the states of the four lines. An LS14 inverter is placed on the output of this device due to its low drive capabilities. The output of the LS14 inverter goes to the UART and the break detect logic.

4-17. CARD RESET PULSE GENERATOR

The interface is reset (see Section III, paragraph 3-29) on power up, or upon execution of a CLC 0 (system reset) or OTA 32 (card reset). These reset pulses can be as short as 227 nsec. This is insufficient, however, for the UART which requires a 400 nsec reset pulse. The reset pulse is extended to the required length by the Set Reset (SR) flip-flop (U45) and a 4-bit counter (U25). The flip-flop is set when any of the three reset conditions occurs. The setting of the SR flip-flop causes the counter to start counting. When four cycles of SCLK have been counted, a counter output goes high which resets the SR flip-flop, generating the trailing edge of the card reset pulse.

4-18. DIAGNOSTIC MULTIPLEXER

A diagnostic multiplexer (U63) provides the capability of testing several features of the interface when in diagnose mode. The diagnostic multiplexer has the additional function of keeping the transmitted data line in a marking condition, so that no data may be sent to the terminal while testing of the interface is in progress.

Diagnose mode is entered upon execution of an OTA OTB 32 with the least significant bit of A set to 1. This sets the

Diagnose Mode flip-flop (U24). This flip-flop may be cleared by executing a CLC0, or by executing an OTA/OTB 32 with A/B = 0.

The primary function of the diagnostic multiplexer is data loop back. The serial data out line is fed back into the serial data input line when in diagnose mode.

The principal data paths on the interface may then be checked as follows:

```
LDA interface select code     Load and enable global register
OTA 2,C

LDA 1                         Initialize interface and enable
OTA 32                        diagnose mode

LDA 3400                      Set up for full duplex, eight
OTA 31                        data bits

LDB 252B                      Output data test pattern
OTB 30
STC 30,C

SFS 30                        Wait for data to loop back
JMP *-1

LIA 30                        Check for equality
CMA 1
```

In addition to the above tests, special character recognition may be tested by outputting characters as above, and then reading status once the flag is set. If a character is special, bit 7 of the status word (LSBYT) should be zero.

Note that because hardware byte packing capabilities exist only under DMA control, the upper eight bytes of the data path may only be checked by setting up DMA. A one-byte transfer in byte mode output, then reconfiguring to a one-byte input transfer in byte mode will accomplish the desired result because the upper byte is always transferred first.

The diagnostic multiplexer also enables testing of the break detect logic. This is done by connecting the SSD line (control word bit 2) into the break detect logic when in diagnose mode. When this bit is programmed low, held low for 160 clocks, and then programmed high, a BREAK interrupt should occur. If the interface is selected as the Virtual Control Panel interface, then instead of generating an interrupt, control will be transferred to the Virtual Control Panel program.

Finally, the diagnostic multiplexer allows the parity sense switch to be overwritten by Terminal Ready (TR, control word bit 0) when in diagnose mode. This procedure tests the parity logic.

4-19. INTERFACE-TO-TERMINAL SIGNAL DEFINITIONS

Table 4-1 contains interface-to-terminal signal definitions. Information for each signal includes: the signal mnemonic, its full name, where it originates, where it goes to, and what its function is.

Table 4-1. Interface-to-Terminal Signal Definitions

MNEMONIC:	CS(A), CS(B)
FULL NAME:	Clear to Send A and B (high true)
DRIVEN BY:	Modem
RECEIVED BY:	Control/status multiplexer and modem line status change detect logic.
FUNCTION:	Informs the interface that the modem is clear to send data.

MNEMONIC:	DM(A), DM(B)
FULL NAME:	Data Mode A and B (high true)
DRIVEN BY:	Modem
RECEIVED BY:	Control/status multiplexer and modem line status change detect logic.
FUNCTION:	Informs the interface that the modem is in the data mode.

MNEMONIC:	EXTCLK
FULL NAME:	External Clock (high true)
DRIVEN BY:	Terminal
RECEIVED BY:	Baud rate generator logic
FUNCTION:	Used to control baud rate of interface when U21 S1-S4 are closed. EXTCLK has a frequency of 16 times the baud rate. Maximum baud rate when External Clock is used is 56,000 baud.

MNEMONIC:	IC(A), IC(B)
FULL NAME:	Incoming Call A and B (high true)
DRIVEN BY:	Modem
RECEIVED BY:	Control/status multiplexer and modem line status change detect logic.
FUNCTION:	Informs the interface that the modem is going to send data.

Table 4-1. Interface-to-Terminal Signal Definitions (Continued)

MNEMONIC:	LSB
FULL NAME:	Least Significant Bit (of baud rate select) (high true)
DRIVEN BY:	Set by switch U21 unless diagnostic test hood is in place.
RECEIVED BY:	Baud rate generator logic
FUNCTION:	One of four bits used to select baud rate of interface.

MNEMONIC:	MSB
FULL NAME:	Most Significant Bit (of baud rate select) (high true)
DRIVEN BY:	Set by switch U21 unless diagnostic test hood is in place.
RECEIVED BY:	Baud rate generator logic
FUNCTION:	One of four bits used to select baud rate of interface.

MNEMONIC:	NLSB
FULL NAME:	Next to Least Significant Bit (of baud rate select) (high true)
DRIVEN BY:	Set by switch U21 unless diagnostic test hood is in place.
RECEIVED BY:	Baud rate generator logic
FUNCTION:	One of four bits used to select baud rate of interface.

MNEMONIC:	NMSB
FULL NAME:	Next to Most Significant Bit (of baud rate select) (high true)
DRIVEN BY:	Set by switch U21 unless diagnostic test hood is in place.
RECEIVED BY:	Baud rate generator logic
FUNCTION:	One of four bits used to select baud rate of interface.

MNEMONIC:	RD(A), RD(B)
FULL NAME:	Receive Data A and B
DRIVEN BY:	Terminal
RECEIVED BY:	Echo logic and UART
FUNCTION:	Incoming serial data from terminal.

MNEMONIC:	RR(A), RR(B)
FULL NAME:	Receiver Ready A and B (high true)
DRIVEN BY:	Modem
RECEIVED BY:	Control/status multiplexer and modem line status change detect logic.
FUNCTION:	Informs the interface that the modem is ready for a data transfer.

MNEMONIC:	RS(A), RS(B), RS(U)
FULL NAME:	Request to Send A, B, and U (high true)
DRIVEN BY:	Control register
RECEIVED BY:	Terminal
FUNCTION:	RS(A) and RS(B) are sent differential (balanced) to the terminal to request a transfer of data; RS(U) is an unbalanced signal which performs the same function.

MNEMONIC:	SBS
FULL NAME:	Stop Bit Select (high true)
DRIVEN BY:	Set by switch U21 unless diagnostic test hood is in place.
RECEIVED BY:	UART
FUNCTION:	Informs the interface to add one or two stop bits to the data to be transmitted to the terminal. If SBS = 1, two stop bits are added; if SBS = 0, one stop bit is added.

MNEMONIC:	SD(A), SD(B), SD(U)
FULL NAME:	Send Data A, B, and U (high true)
DRIVEN BY:	UART
RECEIVED BY:	Terminal
FUNCTION:	SD(A) and SD(B) are differential (balanced) data sent to the terminal; SD(U) is single-ended data sent to the terminal.

MNEMONIC:	SRD(A), SRD(B)
FULL NAME:	Secondary Receive Data A and B (high true)
DRIVEN BY:	Modem
RECEIVED BY:	Control/status multiplexer
FUNCTION:	Data from a modem

Table 4-1. Interface-to-Terminal Signal Definitions (Continued)

MNEMONIC:	SSD
FULL NAME:	Secondary Send Data
DRIVEN BY:	Control Register
RECEIVED BY:	Modem
FUNCTION:	Data to a modem.

MNEMONIC:	TR
FULL NAME:	Terminal Ready (high true)
DRIVEN BY:	Control/status multiplexer
RECEIVED BY:	Modem or terminal
FUNCTION	Informs the modem to get ready for a data transfer.

MNEMONIC:	TTYI
FULL NAME:	Teleprinter Input (high true)
DRIVEN BY:	Teleprinter
RECEIVED BY:	20 mA current loop receiver and UART
FUNCTION:	Input data from a teleprinter.

MNEMONIC:	TTYO
FULL NAME:	Teleprinter Output
DRIVEN BY:	UART and 20 mA current loop driver
RECEIVED BY:	Teleprinter
FUNCTION:	Output data to a teleprinter.

5-1. INTRODUCTION

This section provides maintenance information for the HP 12005A Asynchronous Serial Interface. Included are preventive maintenance instructions and troubleshooting information.

CAUTION

STATIC SENSITIVE DEVICE. Use anti-static procedures when handling the interface.

5-2. PREVENTIVE MAINTENANCE

Preventive maintenance for the interface is performed at the same intervals as for the computer as a whole.

Preventive maintenance consists of inspecting the interface for burned or broken components, or the presence of foreign material. The cable and connector which connect the interface to the terminal should also be checked for damaged insulation, bent or broken pins, etc. After any damage has been repaired, run the system self-test. (Refer to the HP 1000 L-Series Installation and Service Manual, part no. 02145-90003.) If it is determined that the interface is malfunctioning, perform the troubleshooting procedures listed in paragraph 5-6.

5-3. REMOVAL AND INSTALLATION PROCEDURES FOR THE IOP CHIP

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS Wear safety glasses when removing or installing the retaining clips on the IOP chip.

CAUTION

STATIC SENSITIVE DEVICE Use anti-static handling procedures when removing or installing the IOP chip.

5-4. REMOVING THE IOP CHIP

The chip is removed from its socket as follows:

a. Remove the card from the computer and place it on a flat surface.

b. While pressing down on one of the retaining clips with a thumb, insert the flat blade of a screwdriver or similar instrument between the retaining clip and the side of the socket.

c. Twist the bottom portion of the blade away from the socket to free the retaining clip (A) from the bottom edge of the socket (see figure 5-1).

d. When the retaining clip (A) is free, lift it up and over the chip.

e. Remove the second retaining clip by following steps b through d.

f. Carefully tip the card on edge and remove the chip. Observe the anti-static handling precautions when handling the chip.

5-5. INSTALLING THE IOP CHIP

The chip is installed in its socket as follows:

a. Observe the anti-static handling precautions when handling the chip.

b. Place the card on a flat surface with the component side up.

c. Remove both retaining clips from the socket, if they are in place (see figure 5-1).

d. Place the chip in the socket, locating the two flat corners (B) of the socket facing the two flat corners of the chip. The trace trace side of the chip package must be on the bottom when the chip is placed in the socket.

e. Place the retaining clips in the two places provided for them in the side of the socket.

f. Press down with a thumb on the retaining clip (A) and press the retaining clip over the edge of the socket until it snaps under bottom edge of the socket (B).

g. Install the second retaining clip, following steps c through f.

5-6. TROUBLESHOOTING

To troubleshoot the interface, perform the following steps:

1. Run the computer self-test. Refer to the HP 1000 L-Series Computer Installation and Service Manual, part no. 02103-90003, or the HP 1000 L-Series Computer System Installation and Service Manual, part no. 02145-90003.

2. Run the kernel diagnostic. Refer to the Kernel Diagnostic Operating Manual, part no. 24397-90002.

3. Run the interface diagnostic. Refer to the Asynchronous Serial Interface Diagnostic Operating Manual, part no. 24397-90005.

4. If the interface is defective, contact the nearest Hewlett-Packard Sales and Service Office for information on repair or replacement of the interface. (Sales and Service Offices are listed at the back of this manual.)

5. If desired, however, further isolation to a defective component may be performed using an oscilloscope. Refer to Section VII, figure 7-1, for integrated circuit pin connections and characteristics, to figure 7-3 for interface part locations, and to figure 7-4 for a schematic logic diagram. Refer to Section VI, table 6-3, for replaceable parts information.

Refer to Section II, table 2-1, for backplane connections to connector P1, table 2-2 for backplane connections to connector P2, and table 2-5 for interface-to-terminal (connector J1) pin connections.

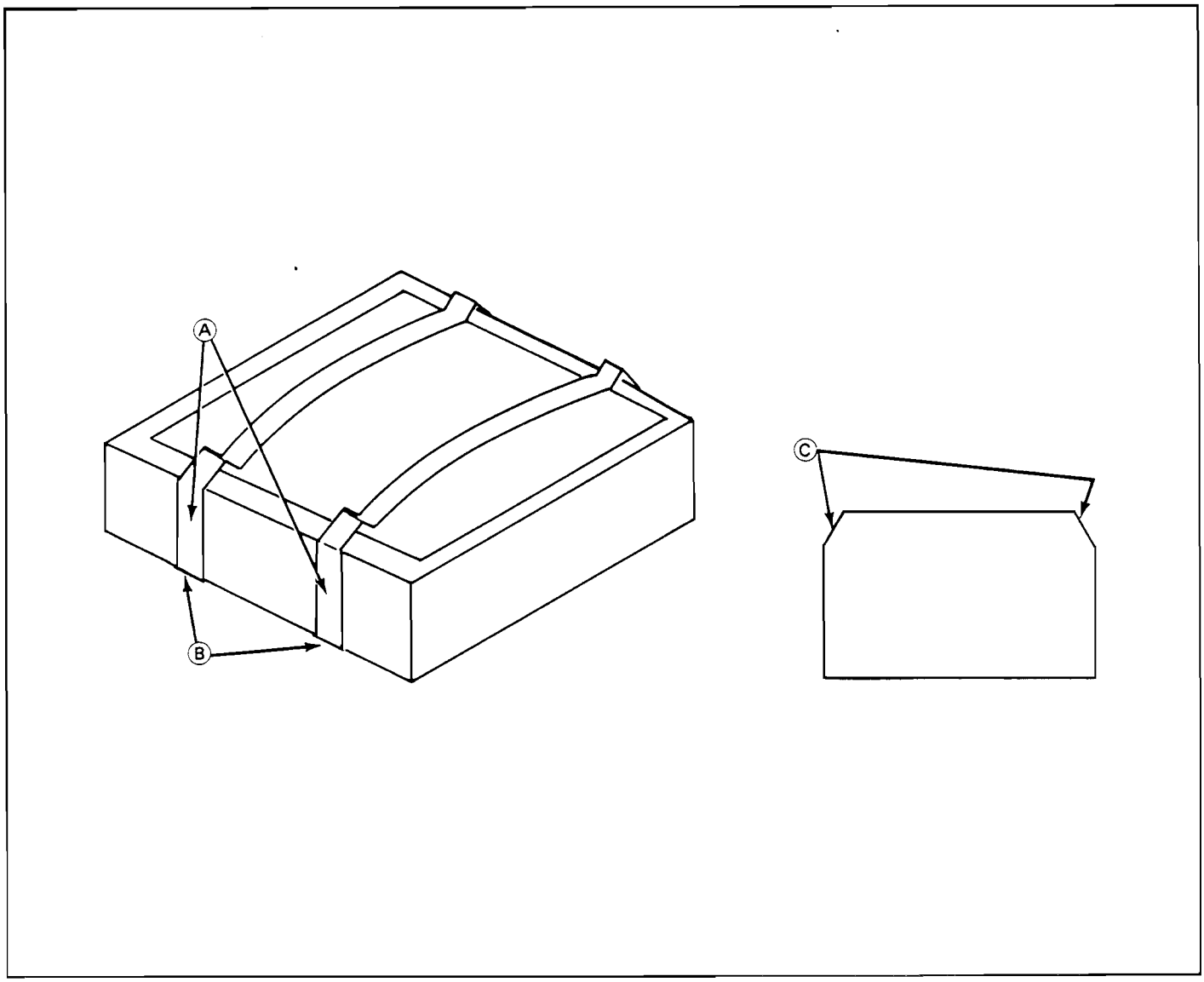


Figure 5-1. IOP Chip Socket with Chip and Retaining Clips in Place

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section contains information for ordering replaceable parts for the HP 12005A Asynchronous Serial Interface. Table 6-1 lists the meanings of the reference designations and abbreviations used in the table of replaceable parts, table 6-2 is a list of part numbers for replaceable circuit boards, table 6-3 is the list of replaceable parts, and table 6-4 contains names and addresses of manufacturers of the parts.

6-2. REPLACEABLE PARTS

Table 6-3 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

a. Reference designation of the part. Refer to table 6-2 for an explanation of the abbreviations used in the "REFERENCE DESIGNATION" column.

b. The Hewlett-Packard part number.

c. Part number check digit (CD).

d. Total quantity (QTY).

e. Description of the part.

f. A five-digit manufacturer's code number of a typical manufacturer of the part.

g. The manufacturer's part number.

6-3. ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

a. Identification of the board containing the part (refer to Section I, paragraph 1-5).

b. Description and function of the part.

c. Quantity required.

Table 6-1. Commonly-Used Prefixes for Component Parts

PREFIX	COMPONENT/PART/MATERIAL
0121-	Capacitors, Variable (mechanical)
0122-	Capacitors, Voltage Variable (semiconductor)
0140-	Capacitors, Fixed
0150-	Capacitors, Fixed Non-Electrolytic
0160-	Capacitors, Fixed
0180-	Capacitors, Fixed Electrolytic
0330-	Insulting Materials
0340-	Insulators, Formed
0370-	Knobs, Control
0380-	Spacers and Standoffs
0410-	Crystals
0470-	Adhesives
0490-	Relays
0510-	Fasteners
0674- thru 0778-	Resistors, Fixed (non wire wound)
0811- thru 0831-	Resistors (wire wound)
1200-	Sockets for components
1205-	Heat Sinks
1250-	Connectors (RF and related parts)
1251-	Connectors (non RF and replated parts)
1410-	Bearings and Bushings
1420-	Batteries
1810-	Resistor, Network, 10-pin
1820-	Monolithic Digital Integrated Circuits
1826-	Monolithic Linear Integrated Circuits
1853-	Transistors, Silicon PNP
1854-	Transistors, Silcon NPN
1855-	Field-Effect-Transistors
1900- thru 1912-	Diodes
1920- thru 1952-	Vacuum Tubes
1990-	Semiconductor Photosensitive and Light-Emitting Diodes
3100- thru 3106-	Switches
8120-	Cables
9100-	Transformers, Coils, Chokes, Industors, and Filters

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or integrated circuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= jumper wire
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
Ag	= silver			phh	= phillips head
Al	= aluminum	H	= henries	pk	= peak
ar	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	prv	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
b	= base	hex	= hexagon, hexagonal	pwv	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rms	= root-mean-square
Be Cu	= beryllium copper	insul	= insulation, insulated	rwv	= reverse working voltage
		impgrg	= impregnated	rect	= rectifier
cpi	= characters per inch	incand	= incandescent	r/min	= revolutions per minute
coll	= collector	ips	= inches per second	RTL	= resistor-transistor logic
cw	= clockwise				
ccw	= counterclockwise	k	= kilo (10^3), kilohm	s	= second
cer	= ceramic			SB, TT	= slow blow
com	= common	lp	= low pass	Se	= selenium
crt	= cathode-ray tube			Si	= silicon
CTL	= complementary-transistor logic	m	= milli (10^{-3})	scr	= silicon controlled rectifier
		M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
Cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous		
		met. ox.	= metal oxide	Ta	= tantalum
dc	= direct current	mintr	= miniature	td	= time delay
dr	= drive			Ti	= titanium
DTL	= diode-transistor logic	n	= nano (10^{-9})	tgl	= toggle
depc	= deposited carbon	nc	= normally closed or no connection	thd	= thread
dpdt	= double-pole, double-throw			tol	= tolerance
dpst	= double-pole, single-throw	Ne	= neon	TTL	= transistor transistor logic
		no.	= number		
em	= emitter	n.o.	= normally open	U(μ)	= micro (10^{-6})
ECL	= emitter-coupled logic	np	= nickel plated		
ext	= external	NPN	= negative-positive-negative	V	= volt(s)
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	var	= variable
elctlt	= electrolytic			vio	= violet
		NSR	= not separately replaceable	Vdcw	= direct current working volts
F	= farads	NRFR	= not recommended for field replacement		
FF	= flip-flop			W	= watts
flh	= flat head	OD	= outside diameter	ww	= wirewound
flm	= film	OBD	= order by description	wht	= white
fxd	= fixed	orn	= orange	WIV	= working inverse voltage
filh	= fillister head	ovh	= oval head		
		oxd	= oxide	yel	= yellow
G	= giga (10^9)				
Ge	= germanium	p	= pico (10^{-12})		
gl	= glass	PC	= printed circuit		
gnd	= ground(ed)				

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12005-60001	3	1	ASSEMBLY, PC ASYNCH SERIAL	28480	12005-60001
C1	0160-0127	2	3	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
C2	0180-0228	6	1	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X9015B2
C3	0160-0127	2		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
C4	0160-0127	2		CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
C5	0160-4806	8	1	CAPACITOR-FXD 470 PF +-5% 100VDC CER	28480	0160-4806
C6	0160-4814	2	1	CAPACITOR-FXD 150 PF +-5% 100VDC CER	28480	0160-4814
CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR3	1902-0064	1	1	DIODE-ZNR 7.5V 5% DO-7 PD=.4W TC=+.05%	28480	1902-0064
L1	9100-1620	5	2	COIL-MLD 15UH 10% Q=65 .155DX.375LG-NOM	28480	9100-1620
L2	9100-1620	5		COIL-MLD 15UH 10% Q=65 .155DX.375LG-NOM	28480	9100-1620
Q1	1853-0281	4	.	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
R1	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	2	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A103
R3	0698-3400	9	2	RESISTOR 147 1% .5W F TC=0+-100	28480	0698-3400
R4	0757-0820	1	1	RESISTOR 1.10K 1% .125W F TC=0+-100	24546	C4-1/8-1101-F
R5	0757-0449	6	5	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R6	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R7	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R8	0698-3400	9		RESISTOR 147 1% .5W F TC=0+-100	28480	0698-3400
R9	1810-0275	1	1	NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A102
R10	1810-0280	8		NETWORK-RES 10-PIN-SIP .1-PIN-SPCG	01121	210A103
R11	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R13	0683-1045	3	1	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R14	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
U1	3101-2243	6	2	SWITCH, DIP 8-ROCKER	28480	3101-2243
U18	1820-1997	7	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
U21	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U21	3101-2243	6		SWITCH, DIP 8-ROCKER	28480	3101-2243
U22	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U23	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U24	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U25	1820-1989	7	2	IC CNTR TTL LS 8IN DUAL 4-BIT	07263	74LS393PC
U27	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U31	1820-2199	3	1	IC DRVR TTL S LINE DRVR DUAL	07263	9638TC
U32	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U33	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U34	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U35	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	6	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U41	1820-2117	5	2	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U42	1820-1989	7		IC CNTR TTL LS 8IN DUAL 4-BIT	07263	74LS393PC
U43	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U44	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
U45	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U46	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U51	1820-2198	2	3	IC RCVR TTL S LINE RCVR DUAL	07263	9637TC
U52	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U53	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
U54	1820-1438	1	4	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U55	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U62	1820-1205	0	1	IC GATE TTL LS AND QUAD 4-INP	01295	SN74LS21N
U63	1820-1470	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U64	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U65	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U67	1AC5-6001	7	1	I/O PROCESSOR (IOP) CHIP	28480	1AC5-6001
U71	1820-2198	2		IC RCVR TTL S LINE RCVR DUAL	07263	9637TC
U72	1820-1297	0	1	IC GATE TTL LS EXCL-NOR QUAD 2-INP	01295	SN74LS266N
U73	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U74	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U75	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U76	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U81	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U82	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U83	1816-0782	7	1	IC, ROM	18324	N82S129F
U84	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U85	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U91	1820-2198	2		IC RCVR TTL S LINE RCVR DUAL	07263	9637TC
U92	1820-1348	2	1	IC GEN PMOS	27014	MM5307N
U93	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U94	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	SN74LS374PC
U95	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U102	1820-1285	6	1	IC GATE TTL LS AND-OR-INV 4-INP	01295	SN74LS54N
U103	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U105	1820-2204	1	1	IC UART CMOS	32293	IM6402-1IPL
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74800N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U11A	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
	0360-1682	0	4	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0845C	0	2	RET SPRING CLIP	28480	1200-0845C
	1200-0848C	3	1	SOCKET-64-PIN	28480	1200-0848C
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. Manufacturer's Code List

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
01121	Allen-Bradley Co	Milwaukee, WI 53204	27014	Nat'l. Semiconductor Corp	Santa Clara, CA 95051
01295	Texas Instr Inc Semiconductor CMPNT Div	Dallas, TX 75222	28480	Hewlett-Packard Co Corporate Hq	Palo Alto, CA 94304
04713	Motorola Semiconductor Prods	Phoenix, AZ 85062	32293	Intersil Inc	Cupertino, CA 95014
07263	Fairchild Semiconductor Div	Mt. View, CA 94042	34335	Advanced Micro Devices Inc	Sunnyvale, CA 94086
18324	Signetics Corp	Sunnyvale, CA 94086	56289	Sprague Electric Co	North Adams, MA 01247
24546	Corning Glass Works (Bradford)	Bradford, PA 16701			

SERVICING DIAGRAMS

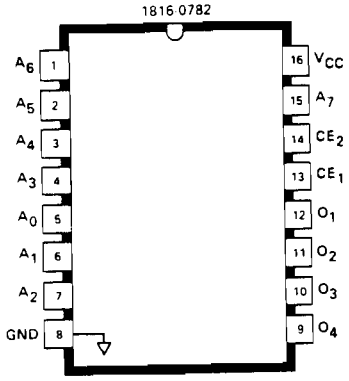
SECTION VII

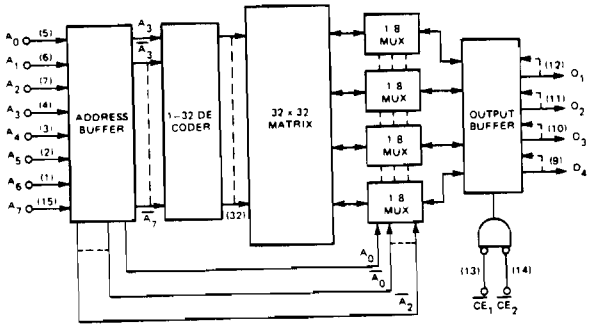
7-1. INTRODUCTION

This section contains servicing diagrams for the HP 12005A Asynchronous Serial Interface.

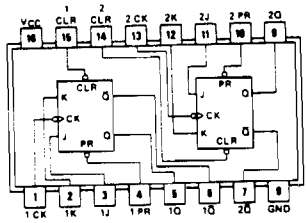
The content of this section is as follows:

1816-0782



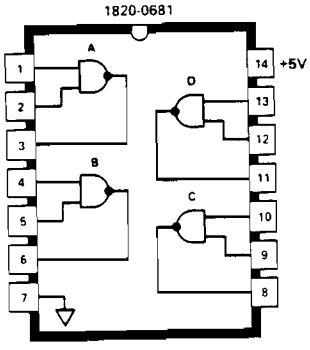


1820-0629



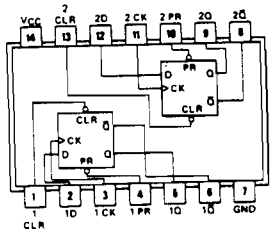
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

1820-0681



$Y = \overline{AB}$

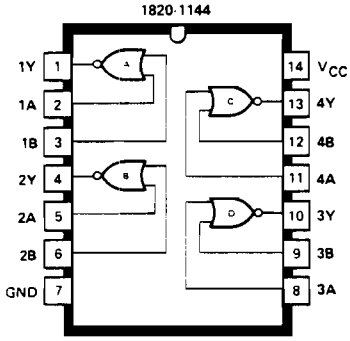
1820-1112



INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 1 of 11)

1820-1144



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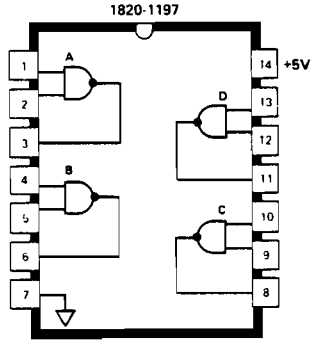
1820-1197



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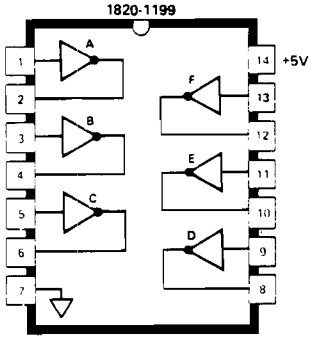
1820-1199



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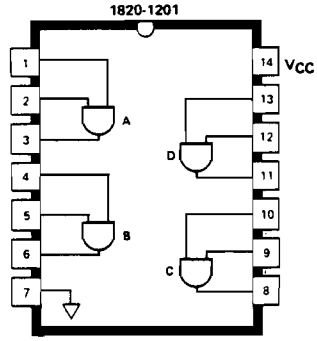
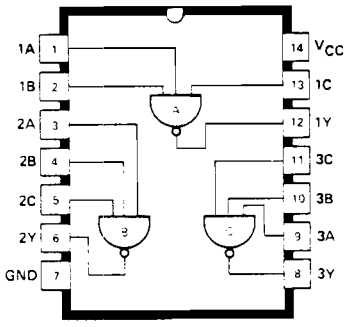
1820-1201



Y=AB

1820-1203

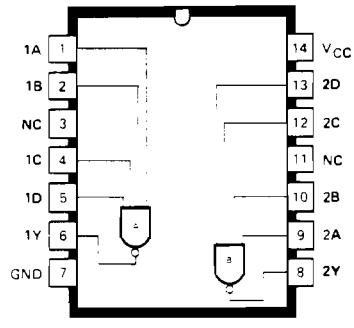


Y=ABC

1820-1205

Type: TTL Compatible

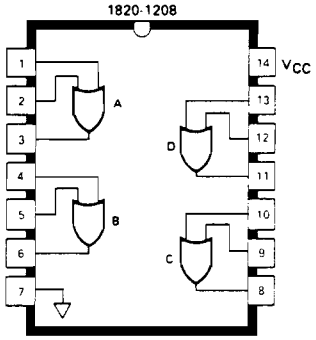
Description: Dual 4-Input AND Gates.



Y=ABCD

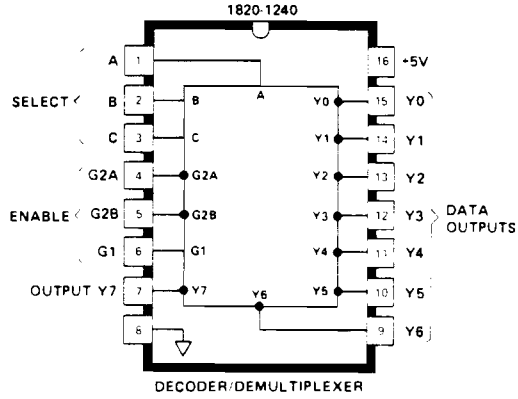
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 2 of 11)

1820-1208



Y=A•B

1820-1240



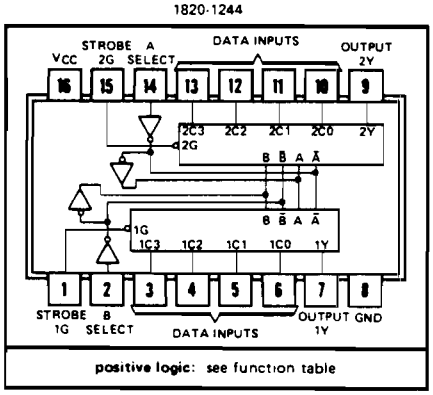
DECODER/DEMULTIPLEXER

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

1820-1244



positive logic: see function table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant

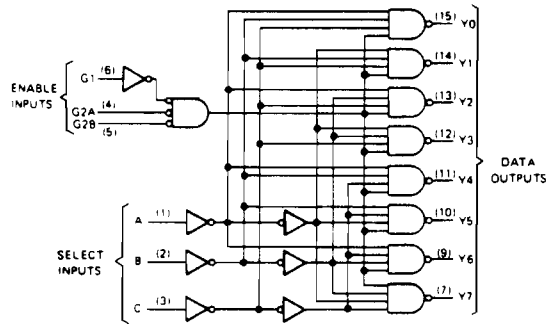
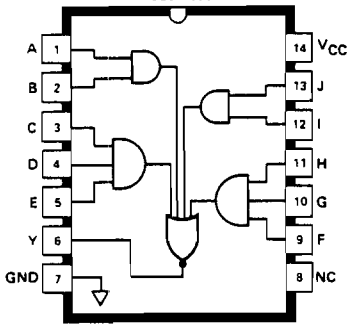


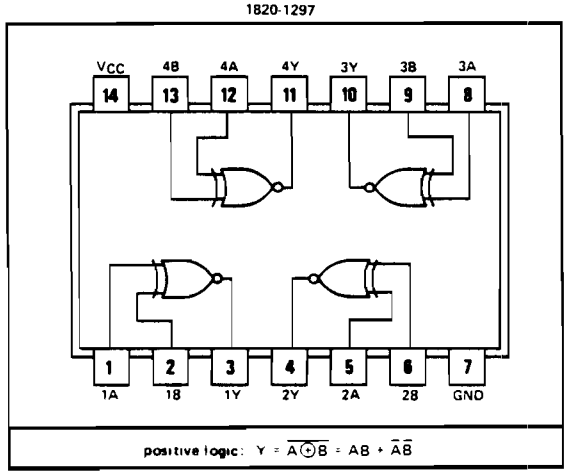
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 3 of 11)

1820-1285



$Y=\overline{AB+CDE+FGH+IJ}$

1820-1297



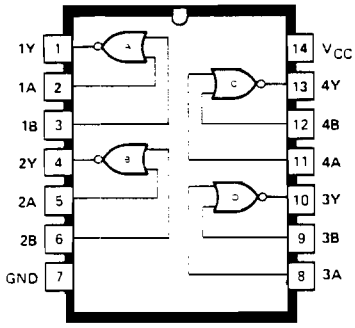
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

1820-1322

Type: TTL Compatible

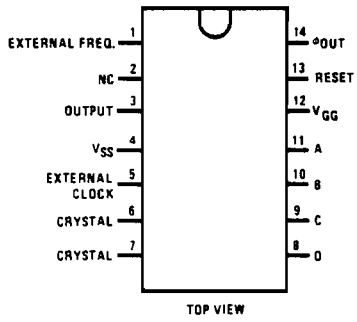
Description: Quad 2-Input NOR Gates.



$Y=\overline{A+B}$

1820-1348

Dual-In-Line Package



TOP VIEW

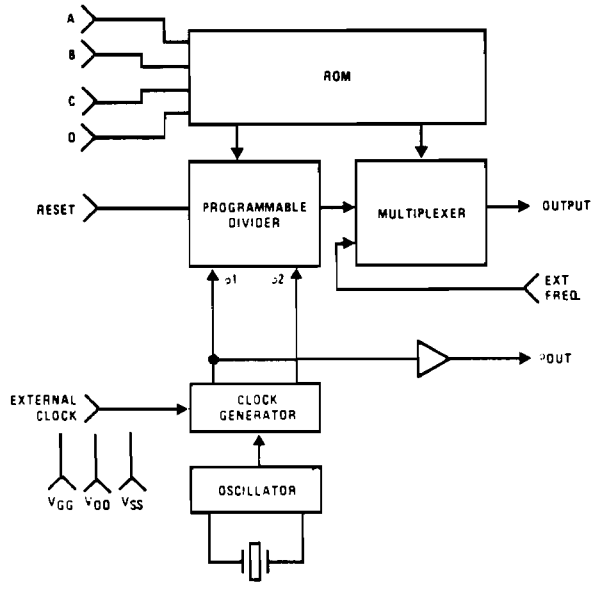
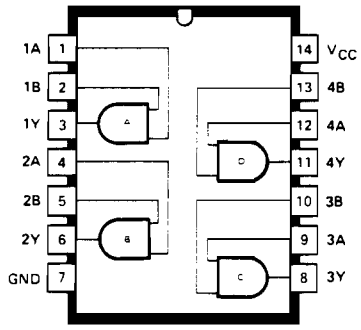


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 4 of 11)

1820-1367

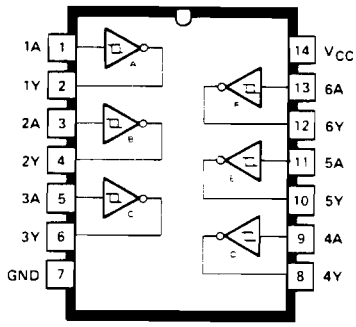
Description Quad 2-Input AND Gates.



Y=AB

1820-1416

Description Hex Inverters

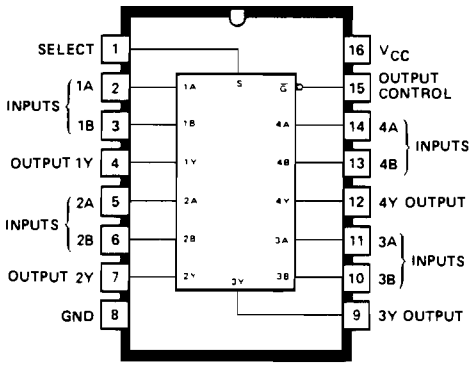


$Y=\overline{A}$

1820-1438

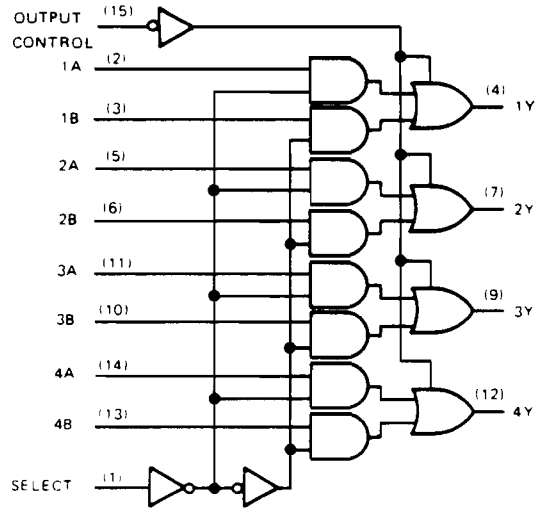
Type TTL Compatible

Description Quad, 2-line-to-1-line, Data Selectors/Multiplexers.



INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off).



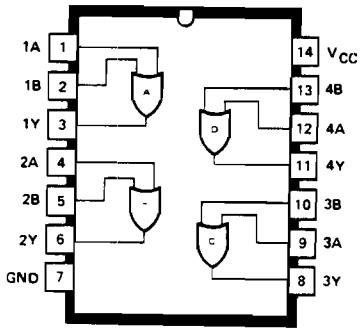
schematics of inputs and outputs

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 5 of 11)

1820-1449

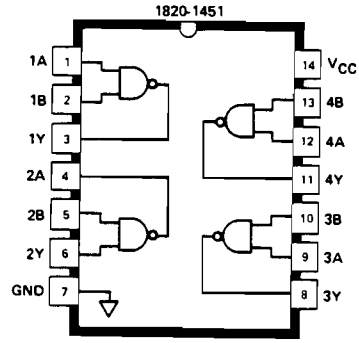
Type: TTL Compatible

Description: Dual input, positive OR Gates



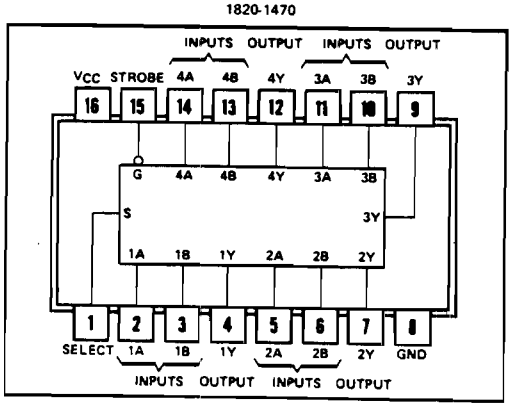
Y=A+B

1820-1451



$Y=\overline{AB}$

1820-1470



INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

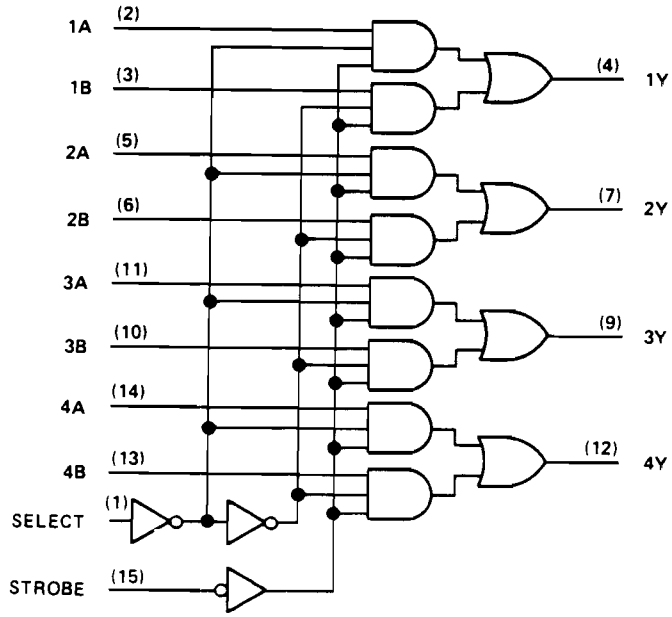
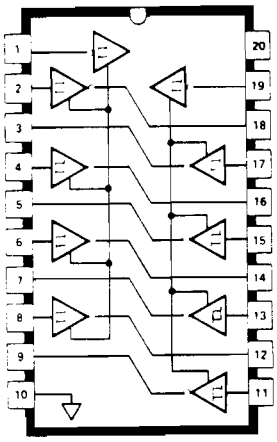
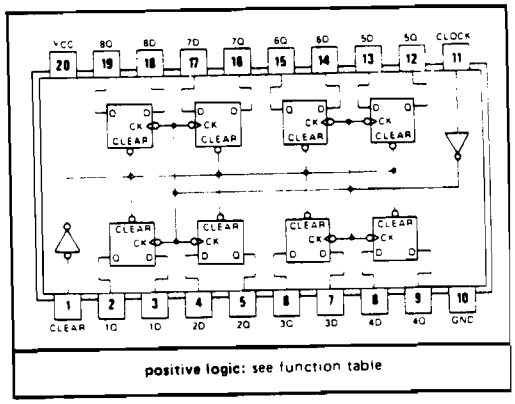


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 6 of 11)

1820-1633

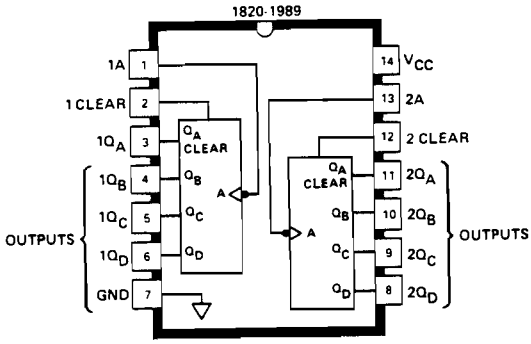


1820-1730



INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

1820-1989



COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

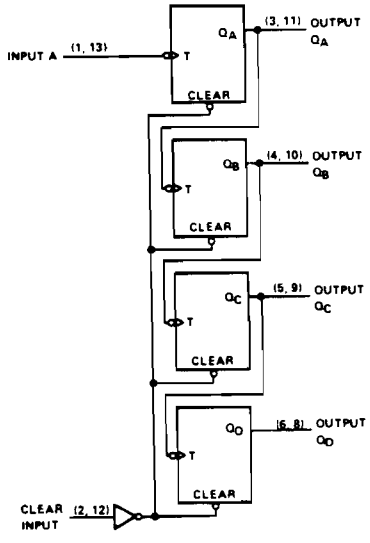
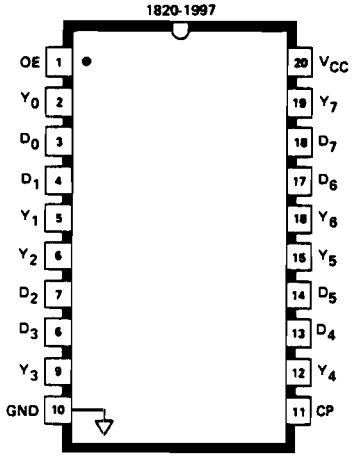
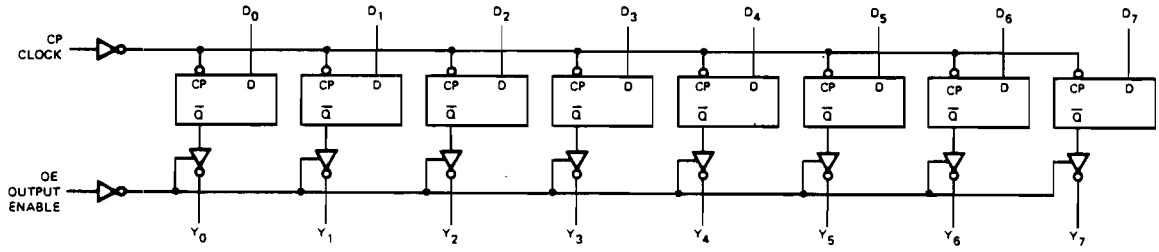


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 7 of 11)

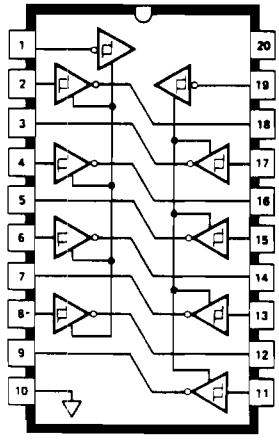
1820-1997



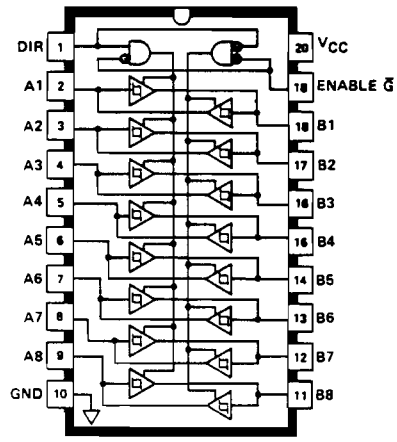
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z



1820-2024



1820-2075

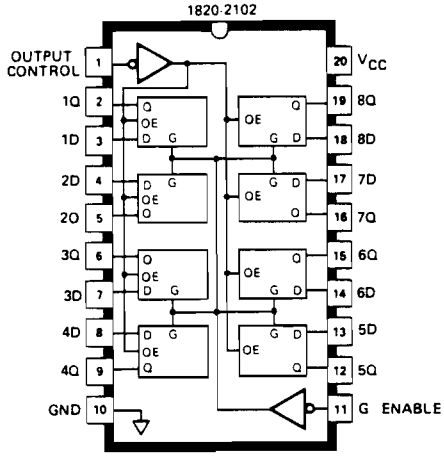


ENABLE $\bar{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

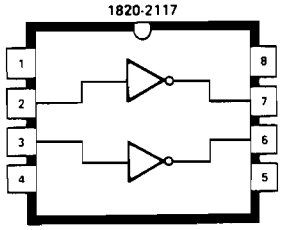
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 8 of 11)

1820-2102

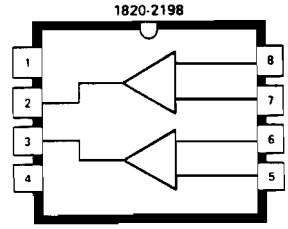


OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

1820-2117



1820-2198



1820-2199

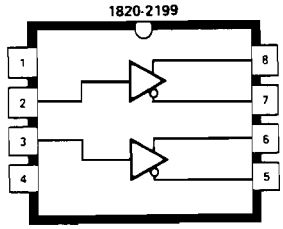
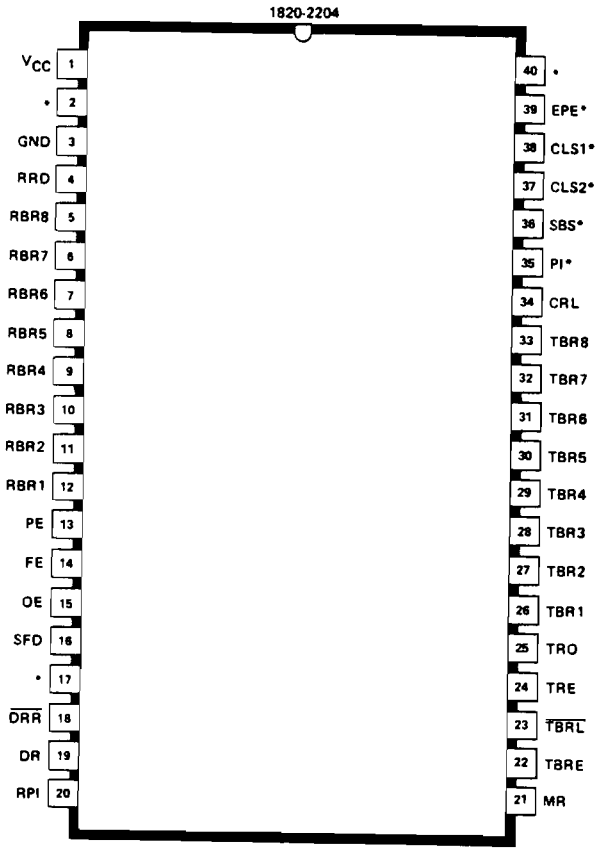


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 9 of 11)



CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

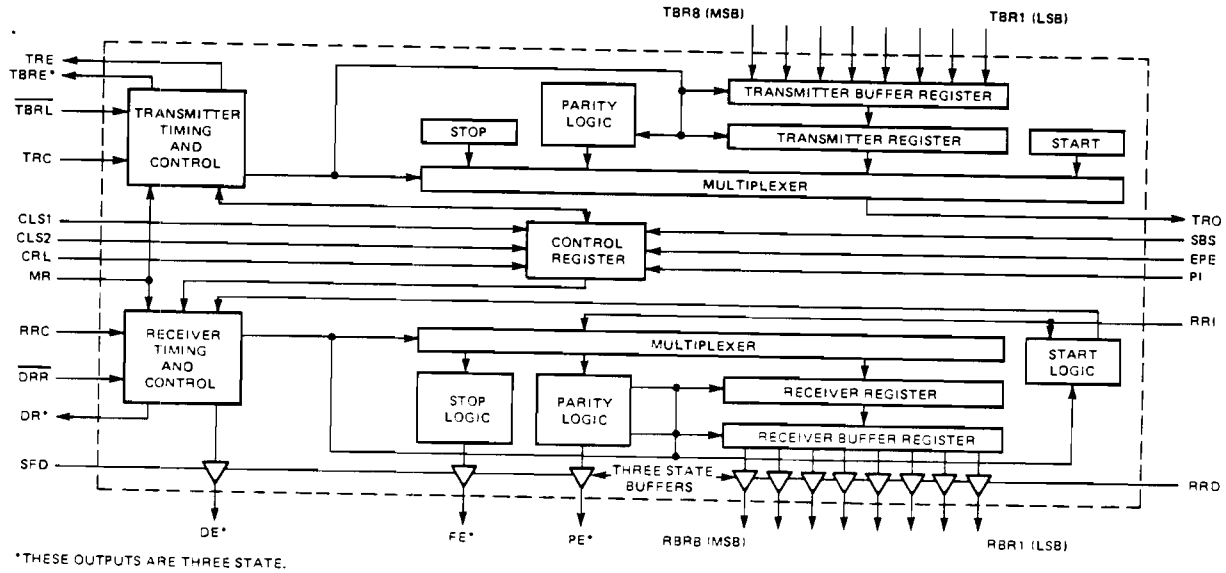
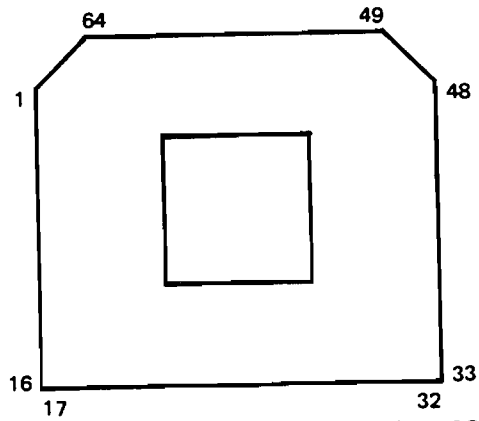


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 10 of 11)

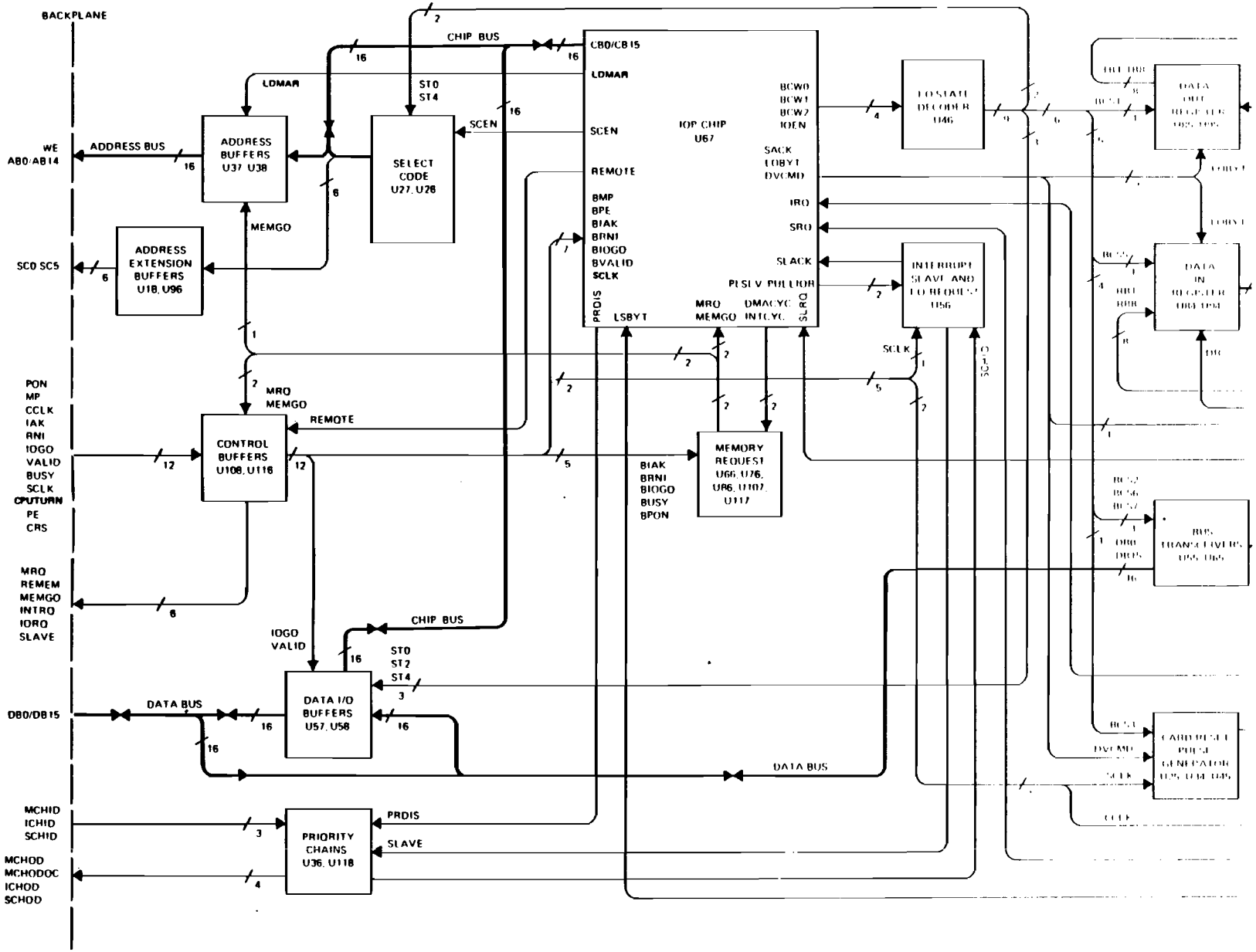


1AC5-6001 I/O PROCESSOR (IOP) CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DMACYC –	17	GND	33	RNI +	49	VCC
2	LOADMAR +	18	VDD	34	CRS +	50	GND
3	SCEN –	19	CW1 –	35	IEN –	51	VDD
4	REMEM –	20	BCW2 +	36	DIAG –	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD –	53	CB8 +
6	DMAEN –	22	BCW0 +	38	PULSLV +	54	CB9 +
7	LOBYT –	23	VALID +	39	PON +	55	CB10 +
8	SACK –	24	IOGO +	40	SLACK +	56	CB11 +
9	NC	25	ICHID –	41	SLRQ –	57	CB12 +
10	SCLK +	26	IAK +	42	CB0 +	58	CB13 +
11	LSBYT –	27	CFF –	43	CB1 +	59	CB14 +
12	PE +	28	IORQ –	44	CB2 +	60	CB15 +
13	MP –	29	IOEN –	45	CB3 +	61	MGO +
14	SRQ –	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ –	31	PRDIS –	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 11 of 11)


BACKPLANE
CHIP BUS
LDMAR
ST0
ST4
SCEN
WE
AB0/AB14
ADDRESS BUS
ADDRESS BUFFERS U37, U38
SELECT CODE U27, U26
IOP CHIP U67
CB0/CB15
REMOTE
BMP
BPE
BIAK
BRNI
BIOGO
BVALID
SCLK
PRDIS
LSBYT
BCW0
BCW1
BCW2
IOEN
SACK
LOBYT
DVCMD
IRQ
SRQ
SLACK
PESLV PULLDOWN
MRQ
MEMGO
DMACYC
INTCYC
SLRQ
IO STATE DECODER U46
INTERRUPT SLAVE AND IO REQUEST U56
SC0 SC5
ADDRESS EXTENSION BUFFERS U18, U96
MEMGO
MRQ
MEMGO
REMOTE
PON
MP
CCLK
IAK
RNI
IOGO
VALID
BUSY
SCLK
CPUTURN
PE
CRS
CONTROL BUFFERS U108, U116
MEMORY REQUEST U66, U76, U86, U107, U117
BIAK
BRNI
BIOGO
BUSY
BPON
MRQ
REMEM
MEMGO
INTRQ
IORQ
SLAVE
IOGO
VALID
CHIP BUS
ST0
ST2
ST4
DB0/DB15
DATA BUS
DATA I/O BUFFERS U57, U58
DATA BUS
MCHID
ICHID
SCHID
PRIORITY CHAINS U36, U118
PRDIS
SLAVE
MCHOD
MCHODOC
ICHOD
SCHOD
DATA IN REGISTER
BUS TRANSCEIVERS
CARD RESET PULSE GENERATOR

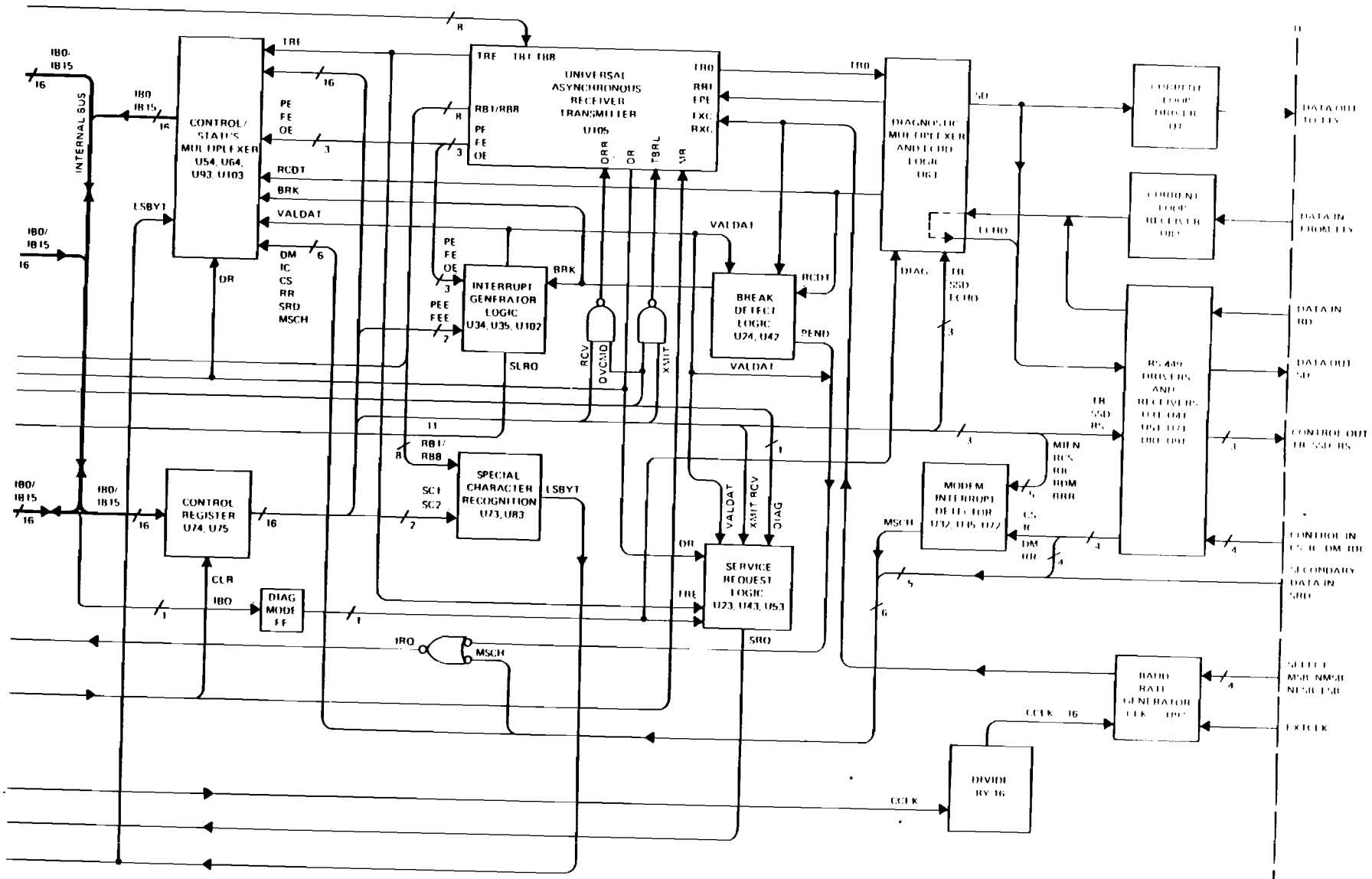


Figure 7-2 Asynchronous Serial Interface Detailed Functional Block Diagram

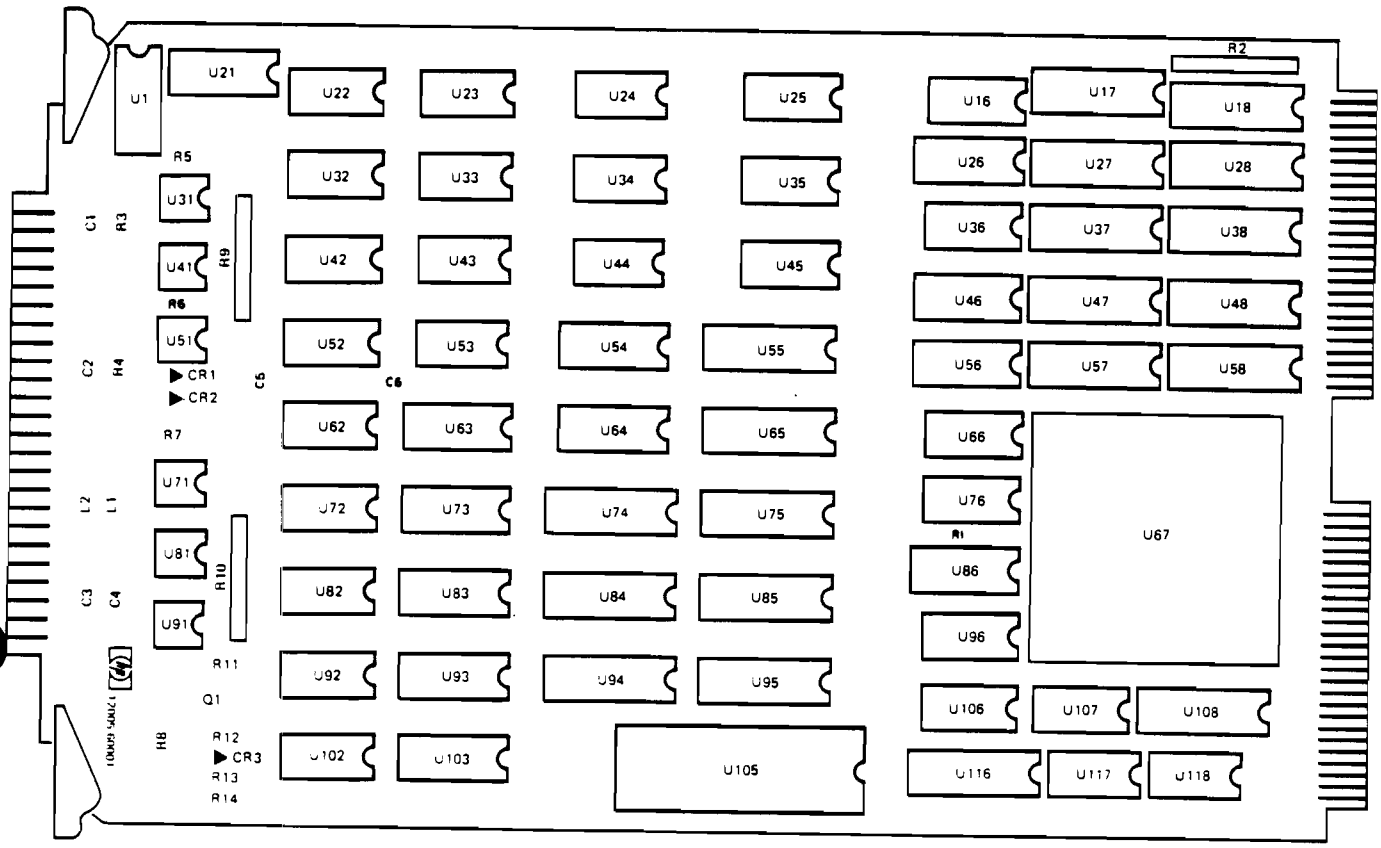


Figure 7-3. Asynchronous Serial Interface Parts Location Diagram

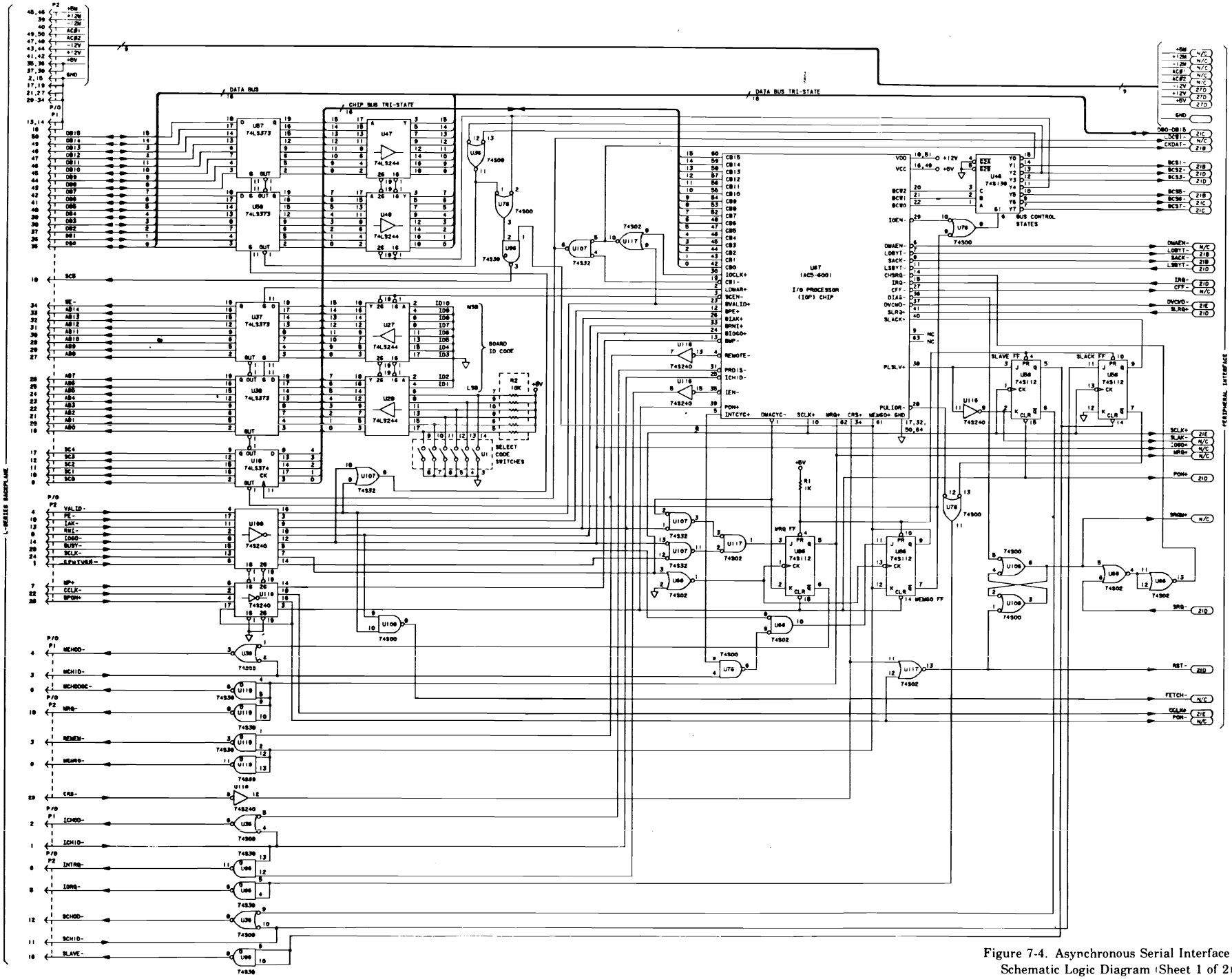


Figure 7-4. Asynchronous Serial Interface Schematic Logic Diagram (Sheet 1 of 2)

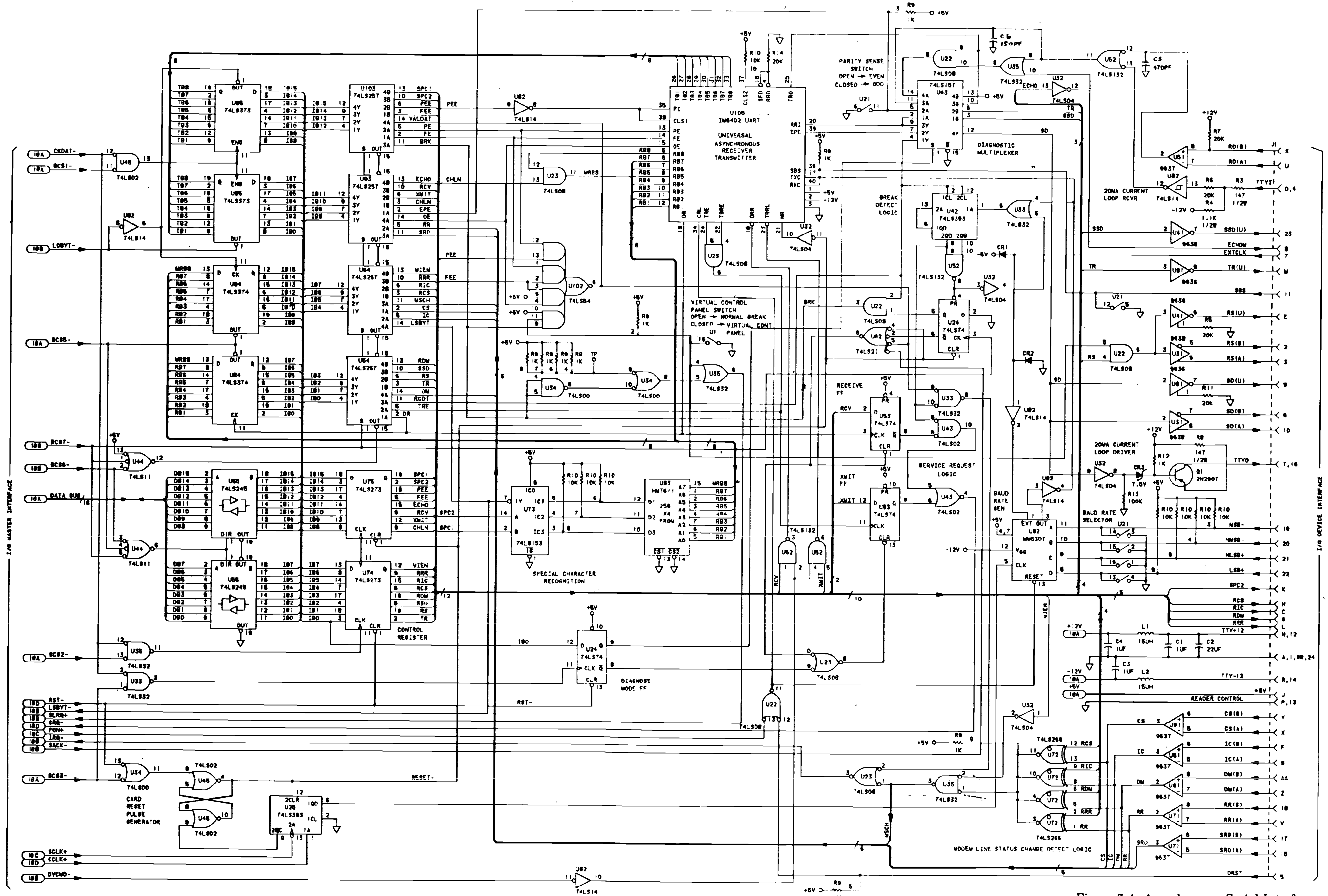


Figure 7-4. Asynchronous Serial Interface Schematic Logic Diagram (Sheet 2 of 2)

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