HEWLETT PACKARD

HP 1000 L-Series Model 5 Microsystem

based on product numbers 2122A and 2142A

The HP 1000 Model 5 is a complete L-Series Microcomputer System (Microsystem) that offers large-computer features (real-time multiprogramming, high-level program languages, data base management, distributed systems networking, including remote data base access, and graphics software support with up to 512k byte main memory capacity), all in a compact desktop package. Integration of the L-Series processor with Minifloppy discs and a choice of integrated terminal capabilities offers L-Series performance in a complete system at an unprecedented low price.

Integrated terminal choices let you select the terminal that best meets your needs, from minimal interactive, alphanumeric capability at lowest price to a terminal with forms and soft-key capabilities, with or without a built-in thermal printer for hard copy of the display. If faster disc access and/or more mass storage is desired, a hard disc with 12 or 19.6 Megabyte capacity can be added.

The Model 5 is offered in two versions. One of these (2122A) is a low-priced execute only microcomputer with 64k bytes of memory, or, optionally, 128k bytes to as much as 512k bytes. The other (2142A) is an application development support Microsystem with 128k bytes of memory, expandable to 512k bytes that can support program development in FORTRAN 4X, Pascal, Real-Time BASIC, and Assembly language. Both the execute-only and applications development Microsystems can support the IMAGE/1000 Data Base Management System and Graphics/1000-II software. Both products also support DS/1000-IV Network communications with other HP 1000 Computer Systems.

Features

- Low-cost integrated real-time microsystem building block for OEMs and End Users designing their own L-Series based application products
- Standard L-Series CPU, memory, and I/O
- 64k, 128k, or up to 512k bytes of RAM main memory
- Built-in capacity to interface up to 13 devices via the Hewlett-Packard Interface Bus (HP-IB)
- Three card cage slots available for user's application needs
- Real-time multiprogramming executive operating system
- Choice of program languages (FORTRAN 4X, Pascal, BASIC, and Assembly) plus interactive editor and relocating loader to support programming in application development Microsystem
- Support for IMAGE/1000 Data Base Management and Graphics/1000-II graphics software and DS/1000-IV Distributed Systems Networking
- 540k bytes of Minifloppy storage in two drives can be augmented by 12M bytes or 19.6M bytes of hard disc memory
- High reliability and maintainability through the use of SOS LSI, reduced circuit area, and simple packaging
- Instruction and program compatibility with other members of the HP 1000 family protects software investment of current OEMs and end users and gives users access to a broad base of proven software
- Built-in memory protect, time base generator, and self test
- Power fail detection and auto restart with optional battery backup
- On-line system generation with application development Microsystem
- Bootstrap loaders included for automatic boot-up from:
  - Other computer system in a DS/1000-IV Distributed Systems Network
  - Disc drive
  - PROM Storage Module
- Remote loading and diagnosis for programming and operation of Microsystems at remote sites
- Modular packaging for easy system design and maintenance
- HP-IB disc interface and serial terminal interface are included; a broad range of other interfaces is available
- Designed for compliance with UL, CSA, and VDE safety standards and VDE and FCC RFI standards

Model 5 L-Series CPU description

The CMOS/SOS LSI central processor chip of the Model 5 Microsystem executes the same HP 1000 base instruction set (arithmetic and extended arithmetic, memory reference, and register reference instructions) as other HP 1000 (M-, E-, and F-Series) Computers. In addition to making possible a compact central processor, the LSI CPU chip includes memory protect and a time base generator, which are optional accessories that take additional logic card space in other computers. Other standard features include integer arithmetic, automatic parity generation and checking, self-test, bootstrap loaders, power fail/auto restart, and virtual control panel.

Auto boot-up

As noted previously, the L-Series central processor includes bootstrap loaders. These can be used for automatic boot-up at power on, from the following sources:

- Another computer system via a 12007A or 12044A HDLC interface.
- A disc memory via the 12009A HP-IB interface.
- A 12008A PROM Storage Module.

Virtual Control Panel (VCP)

In the Model 5, a Virtual Control Panel (VCP) program enables an operator to perform control panel functions via the integrated terminal or a remote terminal. This includes examining the contents of registers and memory locations. It also includes the ability to enter values into registers and memory locations, to control program execution, and to select a bootstrap loader and initiate the boot-up of a system. System boot-up using the VCP can activate the remote forced load of a complete operating system without operator intervention. Because of its remote potential, the VCP can be used for remote isolation of system faults, which can help to minimize maintenance costs of OEM products that use the Model 5 Microsystem.

The Model 5 Microsystem takes advantage of L-Series Distributed Intelligence Architecture to boost I/O efficiency and simplify programming

Of the principal functions of a computer, computation and input/output are usually both controlled by the central processor. In the Model 5 Microsystem, the high circuit density and cost savings realized by using CMOS/SOS/LSI circuits have made it practical to relieve the central processor of the burden of I/O processing. That function is instead performed by individual, custom-designed SOS/LSI I/O processors (IOPs) on each interface card. The IOPs provide highly-efficient DMA-per-channel I/O, minimizing overhead and speeding throughput. The central processor, the IOPs on interfaces, and memory all communicate with each other via a common bus, as shown in Figure 1.

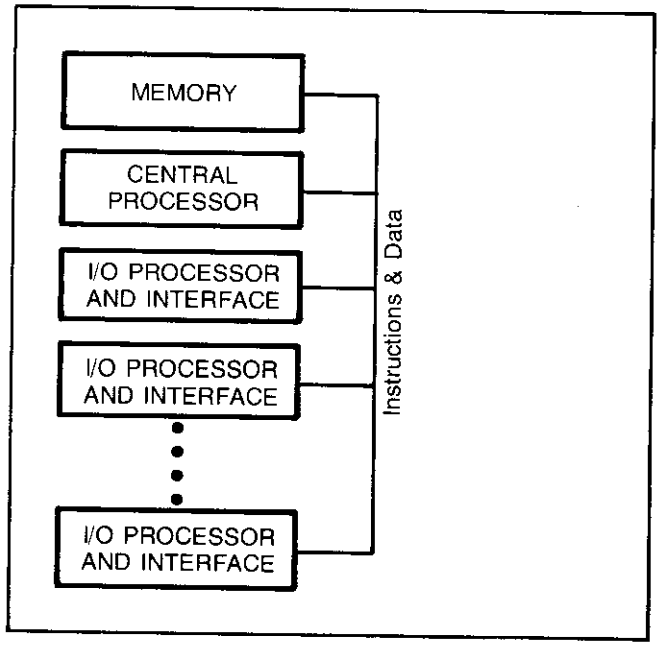


Figure 1. L-Series Functional diagram

Program compatibility

Model 5 L-Series CPU instructions are identical to the same instructions in other HP 1000 (M-, E-, and F-Series) Computers and I/O instructions are similar. This makes the Model 5 Microsystem largely program compatible with other HP 1000 Computer Systems. However, certain aspects of the I/O design, such as interface pre-addressing, will require minor changes in your existing HP 1000 application programs. Of course, the DMA-per-channel capability of the Model 5 will make it worthwhile to revise existing I/O programs to realize the significantly greater I/O efficiencies of the Model 5.

Extensive software support

Supported software	2122A with RTE-L	2122A with RTE-XL	2142A with RTE-XL
92854A Pascal/1000 Compiler (consult HP for availability)	T	T	D, HR
92834A FORTRAN 4X Compiler	T	T	D
92076A BASIC/1000L	N	T	D
Assembler	T	T	D
92073A IMAGE/1000 without QUERY	T, H	T, H	D, H
92069A IMAGE/1000 with QUERY (effective with software revision 2101)	N	T, H	D, H
92841A Graphics/1000-II Device-Independent Graphics Library	T	T	D, H
92842A Graphics-II Advanced Graphics Package 3D — Req. 29841A	N	T	D, H
91750A DS/1000-IV Network software (consult HP availability)	T	T	D, H

T = Target (execute only) system; D = Applications Development system;
N = Not currently supported; HR = Hard disc required for support;
H = Hard disc strongly recommended for support.

System capacity specifications

Memory capacity and available card cage slots

Memory Capacity	Provided with or by	Avail. Card Cage Slots
64k bytes	2122A Microcomputer	3
128k bytes	2142A System Processing Unit or 2122A Microcomputer with Opt. 011	3
256k bytes	128k bytes, as above, plus one 12003A 128kb Memory Array Card	2
384k bytes	128k bytes, as above, plus two 12003A 128kb Memory Array Cards	1
512k bytes	128k bytes, as above, plus three 12003A 128kb Memory Array Cards	0
512k bytes	2122A or 2142A with Option 012 (preferred means of obtaining 512kb)	3

Available HP-IB capacity

The 12009A HP-IB interface included in the Model 5 Microsystem as the disc interface can accommodate up to 13 additional HP-IB connected devices.

Flexible disc memory

Capacity: 270k bytes in each of two Minifloppy drives (540k bytes total).

Average transfer rate: 31.25kb/sec, which is based on the minimum time required to transfer one track without overrun.

Spindle motor start time: 250 milliseconds, maximum.

Average access time with disc rotating: 120 milliseconds (17-track stroke).

Specifications of optional hard discs

Product Number	Capacity (M bytes)	Average Transfer Rate*	Average Access Time
7910H	12.1	493kb/s	80.0ms
7906H	19.6	881kb/s	33.3ms

**Average transfer rate is based on the minimum time required to transfer one track without overrun.*

Terminals usable in the Model 5 Microsystem

**NOTE: The selected terminal must be ordered with option 090, which alters its physical configuration for use with the Model 5 Microsystem.*

HP 2621A Interactive Terminal (provides basic capability at lowest price)

HP 2621P Interactive Terminal (same capability as 2621A, but with integral thermal printer for hard copy of the display)

HP 2624A Display Terminal (adds block mode, forms, softkey control, and more display memory to the base capability of the 2621A; 2624A Option 050 can be ordered to add an integral thermal printer)

HP 2626A Display Station (adds multiple workspaces and split screen capabilities to the capabilities of the 2624A; 2626A Option 050 can be ordered to add an integral thermal printer)

L-Series processor specifications

Architecture

Type: Distributed intelligence with separate CPU and I/O Processors communicating with each other and with memory via a single bus, as shown in Figure 1.

Implementation: Hardwired with SOS/LSI and MSI hardware.

Data path width: 16 bits.

Bus structure: Single backplane bus for memory, processor, and I/O.

Bus speed: Up to 2.7 megabytes/sec.

Interrupt system: Vectored priority interrupt structure with the following priority assignments. Note that select codes need not match priorities.

Priority	Select Code	Function
1	00005	Memory parity interrupt
2	00010	Unimplemented instruction interrupt
3	00007	Memory protect interrupt
4	00017	Special interrupts
5	00004	Power fail interrupt
6	00006	Time Base Generator interrupt
	00011-00016	Reserved functions
7-54	00020-00077	

Central Processor Board

Accumulators: 2 (A and B), 16 bits each, implicitly addressable, also explicitly addressable as memory locations.

Memory registers: 3 (T,P), 16 bits each, and (M), 15 bits.

Supplementary registers: 2 (overflow and extend), one bit each.

Instruction types: Memory-to-memory, Memory-to-accumulator, and Direct register modification.

Instruction formats: Combined single word, Double word, and Single word.

Addressing modes: Direct, Multilevel-indirect, Register implicit, Double word, Single word, and Bit.

Instruction execution times (microseconds):

Instruction	Time (μs)*
Memory Reference Group	
ADA/B, AND, IOR, XOR	4.5
LDA/B, STA/B	4.1
CPA/B without skip	4.5
CPA/B with skip	5.0
ISZ without skip	5.9
ISZ with skip	6.4
JMP	2.7
JSB	4.1
Indirect addressing (per level)	1.8
Shift-Rotate Group	3.2
Alter-Skip Group	3.6
Overflow bit manipulation	
STO, CLO, SOS, SOC	3.6
HaLT (HLT)	15.2
Extended Arithmetic Instructions	
DLD,DST	7.7
MPY	28.1
DIV	8.6-33.1
ASL, ASR, LSL, LSR, RRL, RRR, Basic w/1 shift	2.3
Per additional shift	0.45

**These figures assume no DMA intervention; DMA intervention may increase execution times.*

Power fail provisions: When primary line power falls below a predetermined level while the computer is running, a power fail warning signal from the Model 5 power supply causes an interrupt to memory location 00004. Memory location 00004 is intended to contain a Jump-to SuBroutine (JSB) instruction to RTE's power fail subroutine or a user-written subroutine. A minimum of 5 milliseconds is available to execute the power fail subroutine.

Auto restart: If the optional 12013A Battery Backup Card is installed, restoration of power triggers a power-on signal that enables the CPU to automatically jump to and resume execution of the program that was running when power failed.

Memory protect:

1. Protects a selected block of memory of any size, from a settable "fence" address downward, against alteration or entry by programmed instructions, except those involving the A and B registers.
2. Prohibits execution of I/O instructions, except those referencing select code 01 (the CPU status register and the overflow register). This limits control of I/O operations to interrupt control only, which is used to give exclusive control of the I/O system to the RTE-L or RTE-XL executive operating system.
3. In response to a memory protect violation, interrupts the computer and saves the address of the violating instruction in memory location 00007, from which it can be made accessible in the A or B register by a single Assembly language instruction.

Time Base Generator interrupt: A Time Base Generator interrupt is provided for maintaining a real-time clock. The interrupt request is made when the CPU signals, at 10-millisecond intervals, that its internal clock is ready to roll over.

Unimplemented instruction interrupt: An unimplemented instruction interrupt is requested when the CPU chip signals that the last instruction fetched was not recognized by it. This interrupt provides a straightforward entry into software routines for the execution of instruction codes not recognized by the L-Series, or for the design of custom co-processors which can share the L-Series backplane and memory.

Memory board

Memory structure: 32, 64, 128, 192, or 256 pages of 2048 bytes, with direct access to current and base (page 0) pages, indirect access to all pages.

Memory cycle time: 680 nanoseconds.

Memory parity checking: Parity logic on the Memory board continuously generates correct parity for all words written into memory and monitors the parity of all words read out of memory. Either odd or even parity can be selected. A parity error will generate an interrupt to memory location 000005, which can contain a JSB to a user-written parity error handling subroutine or a HaLT instruction.

I/O Master

Purpose: The I/O Master is the standard interface circuitry to the L-Series backplane. It includes the I/O Processor chip, which executes I/O instructions, and other circuits that make high speed transfers possible. Every HP 1000 L-Series I/O interface card, including the 12010A Breadboard Interface, has the I/O Master circuitry.

Determination of I/O address: I/O address select code is set for each interface by select code switches on the interface and is therefore independent of interface card position along the backplane bus.

I/O addressing: I/O interfaces are pre-addressed by presetting their select codes into a Global Register (GR). This leaves the six select code bits of I/O instructions available for subsequent selective addressing of registers or other functions on the interface.

Instruction execution times (microseconds):

Instruction	Time (μs)*
STC, CLC, STF, CLF	3.6
LIA/B, MIA/B, OTA/B	6.4
SFC,SFS without skip	3.6
SFC,SFS with skip	5.0

**These figures assume no DMA intervention; DMA intervention may increase execution times.*

I/O device interrupt priority: Depends upon I/O interface card position along the card cage bus. The interface closest to the CPU card has highest priority, with the other interfaces in card slots farther from the CPU having successively lower priorities.

I/O interrupt procedure:

1. One or more I/O interfaces requests an interrupt.
2. The CPU responds to the interrupt request of the highest priority interface by executing the instruction in a memory location that corresponds to the select code of the interface.

Interrupt masking: The I/O Master logic includes an interrupt mask register which provides for selective inhibition of interrupts from specific interfaces under program control. This capability can be programmed to temporarily cut off undesirable interrupts from any interfaces that could interfere with crucial transfers.

Interrupt latency when there is no DMA interference: 0.88 to 33.1 microseconds; 1.6 microseconds typical. (Interrupts cannot be serviced until a DMA cycle or an instruction in progress has completed execution; the worst-case latency of 33.1 microseconds is based upon time to complete an integer divide, the longest instruction.)

Interrupt latency when DMA is completely monopolizing the backplane: 95 to 828 microseconds, depending upon the instruction mix.

Direct Memory Access (DMA): The IOP chip supports DMA capability on each I/O interface, the use of which reduces the number of interrupts from one per data item (byte or word) to one per complete DMA block transfer, greatly reducing overhead and increasing throughput of all interfaces.

DMA Latency: Time interval from Service Request by an I/O device through completion of the I/O data transfer to/from the I/O interface is 0.908 microsec for input, 1.135 microsec for output for the interface with highest hardware priority.

Self-configured, chained DMA: The IOP chip also supports a self configuring mode of operation. In this mode, instead of interrupting after a block transfer, the IOP fetches a new set of control words for the next transfer, reconfigures itself, and initiates another block transfer. This process continues for as long as additional control word sets are available.

Data packing under DMA: When byte mode is specified in control word instructions, the IOP automatically packs or unpacks bytes.

Maximum achievable DMA rate: 1.35 million words/sec (2.7 megabytes/sec).

I/O Master signals and timing: Refer to the HP 1000 L-Series I/O interfacing guide 02103-90005.

Electrical specifications

AC Power requirements of 2122A/2142A and Terminal

2122A/2142A Line voltage: 90-138V (115V nominal) or 190-260V (230V nominal).

2122A/2142A Line frequency: 47 to 63 Hz.

262x terminal line voltage:

100V +5%/−10% (90-105V) (Opt. 014/016)
120V +5%/−10% (108-126V) (Std)
220V +5%/−10% (198-231V) (Opt. 015)
240V +5%/−10% (216-252V) (Opt. 013)

262x terminal line frequency: 60 Hz ±5% (57-63 Hz) 262x std and Opt. 014; 50 Hz ±5% (47.5-52.5 Hz) 262x Opt. 013/015/016.

Maximum power required: 300W for 2122A/2142A plus power requirement of the selected integral terminal, selected from the following:

2621A	Interactive Terminal:	50W
2621P	Interactive Terminal:	100W
2624A	Display Terminal:	120W
-050	Integral Printer:	50W
2626A	Display Station:	75W
-050	Integral Printer:	50W

Cold start input surge: 30 amperes, maximum.

Mating power receptacle: One 15A grounded receptacle at 110V (7A receptacle at 220V).

DC current available (+) and required (−) for I/O interfaces and accessories

	Current available (+)/required (−)		
L-Series product	+5V dc	+12V dc	−12V dc
2122A Microcomputer	+26.1A	+2.2A	+1.5A
2122A Opt 011 (128kb memory)	−1.8A	0.0A	0.0A
2122A Opt 012 (512kb memory)	−2.1A	0.0A	0.0A
2142A System Processing Unit	+24.3A	+2.2A	+1.5A
2142A Opt 012 (512kb memory)	−0.3A	0.0A	0.0A
12005A Async Serial Interface	−1.6A	−0.1A	−0.1A
12006A Parallel Interface	−1.9A	−0.2A	0.0A
12007A HDLC Modem Interface	−2.5A	−0.3A	−0.2A
12008A PROM Storage Module	−2.0A	−0.1A	0.0A
12009A HP-IB Interface	−2.1A	−0.1A	0.0A
12010A Breadboard Interface*	−0.8A	−0.1A	0.0A
12011A Extender Card	n/a	n/a	n/a
12012A Priority Jumper Card	n/a	n/a	n/a
12013A Battery Backup Card	0.0A	−0.1A	0.0A
12040A 8-Ch Multiplexer I/F	−2.5A	0.0A	−0.1A
12044A HDLC Direct Conn I/F	−2.4A	−0.3A	−0.1A

**Current requirement listed here for 12010A Breadboard Interface is for the I/O Master circuitry only; logic added by the user will require additional current.*

Physical characteristics

Dimensions (including terminal and terminal keyboard)

45cm (17.7 in) high by 39.1 cm (15.4 in) wide by 73.7cm (29 in) deep.

Weight (including terminal)

31.8kg (7016).

Ventilation

Two 70 cfm fans provide cooling for the terminal, SPU card cage, and power supply.

Maximum heat dissipation

404 kilogram-calories/hr (1604 BTU/hr).

Environmental specifications

Temperature

Operating: 10° to 40°C (50° to 104°F); with printing terminal, minimum temperature must be 5°C (41°F).

Storage: −40° to 60°C (−40° to 140°F).

Relative humidity

20% to 80% non-condensing.

Altitude

Operating: To 4.6km (15,000 ft).

Non-operating: To 15.3km (50,000 ft).

Vibration and shock

HP 1000 L-Series products are type tested for normal shipping and handling shock and vibration (contact factory for review of any application that requires operation under continuous vibration).

Safety and RFI qualification

The Model 5 Microsystem has been UL listed and CSA certified to meet Underwriter's Laboratory (UL) and Canadian Standards Association (CSA) standards for safety. The Model 5 Microsystem has also been designed to meet Verband Deutches Electrotechnikes (VDE) and Federal Communications Commission (FCC) standards for RFI. VDE and FCC approvals are pending.

Ordering information

2122A Microcomputer

The 2122A Microcomputer includes:

1. HP 1000 L-Series 64k byte memory card.
2. HP 1000 L-Series CPU card.
3. 12005A Asynchronous Serial (terminal) Interface card.
4. Terminal data cable.
5. Terminal power cable.
6. 12009A HP-IB Interface card.
7. Minifloppy controller card.
8. 8-Slot card cage.
9. Power supply.
10. Dual 270 kilobyte 5-inch Minifloppy disc drives (540kb total).
11. Minisystem package with power cord (power cord not supplied with option 015).
12. RTE-L Primary system on Minifloppy disc. HP 92070E Right to Execute RTE-L must be purchased separately.
13. HP 1000 Model 5 Computer Service Manual (02142-90002).
14. HP 1000 L-Series Computer Reference Manual (02103-90007).
15. HP 12005A Asynchronous Serial Interface Reference Manual (12005-90001).
16. HP 12009A HP-IB Interface Reference Manual (12009-90001).
17. Getting Started with the HP 1000 Model 5 Microsystem (manual) (02142-90001).

NOTE: HP 2122A will require installation by a technically qualified person.

2122A Options

011: 128k byte memory and RTE-XL primary system instead of 64k byte memory and RTE-L primary system. HP 92071E Right to Execute RTE-XL must be purchased separately. Expansion beyond 128k bytes requires one or more 12003A 128k byte Memory Array Cards and may also require a 12028B/C connector. Not compatible with Opt. 012.

012: 512k byte memory and RTE-XL primary system instead of 64k byte memory and RTE-L primary system. HP 92071E Right to Execute RTE-XL must be purchased separately. Not compatible with Opt. 011.

015: Operation from 230V ac power. Terminal power option must be ordered separately.

2142A System Processing Unit

The 2142A System Processing Unit includes:

1. HP 1000 L-Series 128k byte memory card.
2-11. Same as items 2 through 11 for 2122A, above.
12. RTE-XL Master, RTE-XL Primary system, and Diagnostics on Minifloppy discs with rights to use on the 2142A System Processing Unit.
13-17. Same as items 13 through 17 for 2122A, above.
18. On-site installation assistance by Hewlett-Packard service engineer.

2142A Options

012: 512k byte memory instead of 128kb memory.

015: Operation from 230V ac power. Terminal power option must be ordered separately.

Model 5 Plug-in hardware accessories

12003A Memory array card to increase memory from base 128k bytes of 2122A with option 011 or 2142A to a maximum of 512k bytes, in 128k byte increments. A 12028B/C connector will also be required for installation of two or three 12003A cards. (NOTE: 2122A/2142A option 012 is strongly recommended for applications that will ultimately require 512k bytes of memory.)

12005A Asynchronous Serial Interface for connection of one additional terminal (one 12005A interface is included in the 2122A/2142A).

12006A Parallel Interface for 16-bit duplex I/O from/to external devices.

12007A HDLC Modem Interface for DS/1000-IV communication with other HP 1000 Computer Systems via telephone lines.

12008A PROM Storage Module for mounting up to 64k bytes of PROMS for non-volatile program storage.

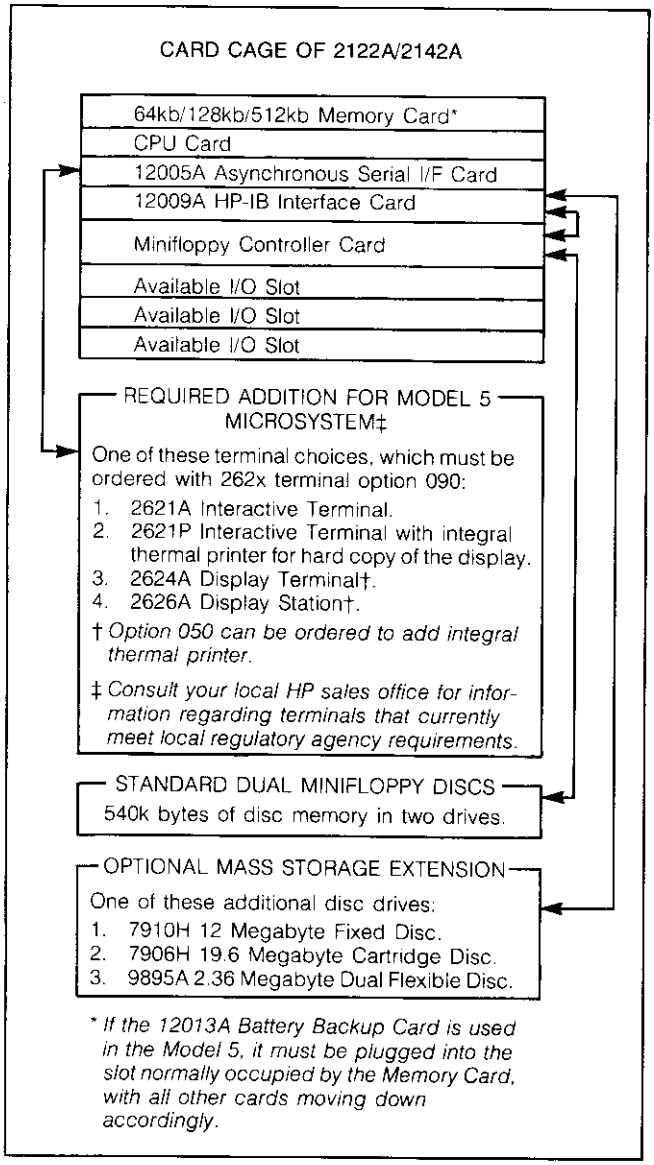
12009A HP-IB Interface for connection of disc memories, printers, graphics peripherals, instruments, and other HP-IB devices (one 12009A interface is included in the 2122A/2142A).

12010A Breadboard Interface for user-implemented, special-purpose interfaces (includes the I/O Master circuitry common to all HP 1000 L-Series interfaces).

12011A Extender card to aid servicing.

12012A Priority jumper card for continuation of hardware priority chain through card cage bus position not occupied by an I/O interface or other plug-in accessory card.

Additional requirements and mass storage extensions for Model 5 Microsystems



12013A Battery Backup Card provides power to sustain memory for 1 hour in the event of power failure.

12040A 8-Channel asynchronous multiplexer card for connection of multiple terminals and/or printers to the Model 5 via a single interface and a 12828A Multiplexer Panel (not usable for the first terminal).

12044A HDLC direct connect interface card for DS/1000-IV communication with other HP 1000 Computer Systems connected via user-installed cables.

Additional software available for Model 5

See Extensive Software Support table on page 2.

L-Series Plug-in hardware accessories not supported by the Model 5 Microsystem

The following L-Series plug-in accessories require 25kHz ac power in addition to dc power requirements. Because 25kHz ac power is not provided by the 2122A/2142A power supply, these accessories are not supported in the Model 5 Microsystem.

12060A High Level Analog Input Card

12061A Expansion Multiplexer Card

12063A 16 input/16 output Isolated Digital Card

Printed in U.S.A. 3/81 (22) 5953-4284