HEWLETT PACKARD

Service Manual

HP 4951C
PROTOCOL ANALYZER

SERIAL NUMBERS

This manual applies to instruments with serial numbers prefixed 2647A

Manual Part No: 04951-90703
Microfiche Part No: 04951-90704

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SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual must be heeded. Refer to Section 1 for general safety considerations applicable to this product.

WARRANTY

This Hewlett-Packard Instrument product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

For Warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designed by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance. No other warranty is expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

EXCLUSIVE REMEDIES

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products. For any assistance, contact your nearest Hewlett-Packard Sales and Service Office.

CW&A 4/84

WARNING

SAFETY

If this instrument is to be energized via an auto-transformer for voltage reduction, make sure the common terminal is connected to the earthed pole of the power source.

BEFORE SWITCHING ON THIS INSTRUMENT, the protective earth terminals of this instrument must be connected to the protective conductor of the (mains) power cord. This mains plug shall only be inserted in a socket outlet provided with a protective earth contact. This protective action must be negated by use of an extension cord (power cable) without a protective conductor (grounding).

Make sure that only fuses with the required rated current and of the specified type (normal blow, time delay, etc.) are used for replacement. The use of repaired fuses and the short-circuiting of fuse holders must be avoided.

Whenever it is likely that the protection offered by fuses has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

GROUNDING

Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal can make this instrument dangerous. Intentional interruption is prohibited.

HIGH VOLTAGE

Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and, when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.

Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

Adjustments and service described herein are performed with power supplied to the instrument while protective covers are removed. Energy available at many points,if contacted, result in personal injury.

CAUTION

LINE VOLTAGE

BEFORE SWITCHING ON THIS INSTRUMENT, make sure instrument requirements match the voltage of the power source.

GROUNDING

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that all devices connected to this instrument are connected to the protective (earth) ground.

BEFORE SWITCHING ON THIS INSTRUMENT, ensure that the line power (mains) plug is connected to a three-conductor line power outlet that has a protective (earth) ground. Grounding one conductor of a two-conductor outlet is not sufficient.

IEC SYMBOLS

Following is a list of key IEC symbols used by Hewlett-Packard. All symbols are normally applied adjacent to the device requiring the symbol. They shall not be placed on removable parts likely to be detached or lost.

Instruction Manual symbol: If necessary, to preserve the apparatus from damage, it is necessary for the user to refer to the instruction manual, then shall the apparatus be marked with this symbol (IEC 348;16a).

Terminal devices fed from the interior by live voltages that may be dangerous when connecting to or disconnecting from those devices shall be marked with the flash shown when the voltage exceeds 1 KV: The flash shall be red (IEC 348;18c).

Earth Terminals. If the use of this symbol for the protective earth terminal is not permitted by National Standards, it may be modified, for example, by being placed inside a circle (IEC 348;18a).

AC current (IEC 117-1, symbil No. 3).

DC current (IEC 117-1, symbol No. 2).

AC or DC current (IEC 117-1, symbol No. 8).

Frame or chassis connection. The hatching may be completely or partly omitted if there is no ambiguity. If the hatching is omitted, the line representing the frame or chassis shall be thicker (IEC 117-7, symbol 87).

A Ampere (IEC 117-4, symbol No. 356).

V Volt (IEC 117-4, symbol No. 357).

VA Voltapere (IEC 117-4, symbol No. 358).

W Watt (IEC 117-4, symbol No. 360).

Wh Watthour (IEC 117-4, symbol No. 361).

VAh Voltamperehour (IEC 117-4, symbol No. 362).

Hz Hertz (IEC 117-4, symbol No. 365).

Contactor, normally closed. In order to avoid confusion with the symbol for a capacitor, the distance between the horizontal (as drawn here) lines should be at least equal to the length of those lines (IEC 117-3, symbol No. 215.2).

In addition, the following describes the use of Warnings, Cautions, and Notes used in HP Automatic Test System Manuals.

Warnings, cautions, and notes. (All) Warnings and cautions shall precede the text to which each applies but notes may precede or follow applicable text depending on the material to be highlighted. Warnings, cautions, and notes shall not contain procedural steps nor shall they be numbered. When a warning, caution, or note consists of two or more paragraphs, the heading WARNING, CAUTION, NOTE, shall not be repeated above each paragraph. If it is ever necesaarry to precede a paragraph by both a warning and a note, or a caution and a note, etc, they shall appear in the sequence as noted, namely, warnings, cautions, notes. Such inserts in the text shall be short and concise and be used to emphasize important critical instructions.

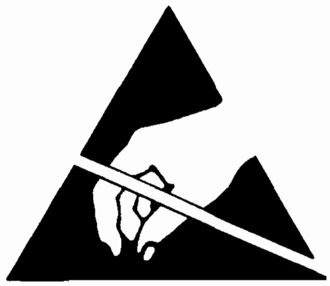
WARNING

An operating procedure, practice, etc. which, if not correctly followed, could result in personal injury or loss of life.

CAUTION

An operating procedure, practice, etc. which, if not strictly observed, could result in damage to, or destruction of, equipment.

Health hazards precaution data. (All) When hazardous chemicals or adverse health factors, in the environment or use of the equipment cannot be eliminates, appropriate precautionary requirements shall be included.



ATTENTION
Static Sensitive Devices

This instrument was constructed in an ESD (electro-static discharge) protected environment. This is because most of the semiconductor devices used in this instrument are susceptible to damage by static discharge.

Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity of a static charge. The results can cause degradation of device performance, early failure, or immediate destruction.

These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction.

Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service circuitry with these devices.

In all instances measures must be taken to prevent static charge build-up on work surfaces and persons handling the devices.

For further information on ESD precautions, refer to "SPECIAL HANDLING CONSIDERATIONS FOR STATIC SENSITIVE DEVICES" in Section VIII Service Section.

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TABLES

SECTION I
GENERAL INFORMATION

1-1. INTRODUCTION

This manual contains technical information for the Hewlett-Packard Model 4951C Protocol Analyzer, the HP 18174A RS-449/422A/423A Interface Pod, the HP 18177 V.35 Interface Pod, the HP 18179A RS-232C/V.24 Interface Pod, and the HP 18180 Combination RS-232C/V.24 and RS-449/422A/423A Interface pod. This manual together with the HP 4951C Operating Manual provides complete documentation for the HP 4951C Protocol Analyzer.

Throughout the remainder of this manual, the Model 4951C Protocol Analyzer is referred to as the HP 4951C, the Protocol Analyzer, or the instrument. Figure 1-1 shows the HP 4951C.

This manual is divided into eight sections and contains the following information:

Section I - General Information - identifies the instruments that are documented by this manual. A description of the instrument, the available options and accessories, and the specifications are also included in Section I.

Section II - Installation - provides information about initial inspection, preparation for use, storage, and shipment.

Section III - Operation - references the HP 4951C Operating Manual which gives detailed operating instructions for the instrument.

Section IV - Performance Tests - describes the built-in performance tests that verify the performance of the instrument.

Section V - Adjustments - provides instructions for properly adjusting the instrument.

Section VI - Replaceable Parts - lists all replaceable parts and assemblies along with ordering information.

Section VII - Manual Changes - contains information necessary to document all serial prefixes listed on the title page of this manual.

Section VIII - Service - provides service and troubleshooting information. This includes Theory of Operation, Block Diagrams, Troubleshooting Procedures, Component Locators, and Schematics.

The Interface Pods are described in the appendices.

The part number for the Service Manual is listed on the title page.

The title page also lists the part numbers for the microfiche version of the Service Manual. The microfiche package also includes the latest Manual Changes supplement.

1-2. DESCRIPTION

The HP 4951C is a portable data communications protocol analyzer that contains the essential features required to install and maintain data networks up to 19.2 kbps. With it you can monitor and decode data transmission, simulate datacomm network components, perform bit error tests, and remotely transfer data and programs to any member of the Hewlett-Packard family of protocol analyzers. The operating characteristics of the 4951C are:

Protocols - X.25, HDLC, SDLC (NRZI), BSC, and most character asynchronous or synchronous protocols.

Data Transfer Rates (bps) - The HP 4951C can capture a complete buffer full of data at line speeds up to 64 kbps. (Bit oriented protocols only).

Data Codes - ASCII, EBCDIC, Baudot, Six Bit Transcode, IPARS, and EBCD.

Mass Storage Memory - Disc drive: Up to 618 kbytes for storing data, timing information, menu configurations, and application programs.

Triggers - 63 triggers consisting of characters, errors, interface lead transitions, or timer values.

Timers - Five timers, each of which has a maximum count of 65535 msec. Resolution 1 msec.

Counters - Five counters, each of which can be incremented up to 9999.

Keyboard - Full ASCII keyboard with six softkeys and cursor control.

Display - 12.7 cm (5 in.) diagonal with 16 lines and 32 characters per line.

Remote Capability - Over the RS-232C/V.24 link: transfer data, setups, and programs.

Self Test - Extensive self test and verification routines for isolating failures to a functional component group. Built-in signature analysis permits fault isolation to the component level.

Bit Error Rate Testing - Simultaneously measure bit errors, block errors, error seconds, and percent error free seconds. Inject single errors or bursts of errors.

Auto-Configure - Automatically determines a line's protocol, data code, speed, parity, and error checking.

1-3. SPECIFICATIONS

Weight

Net: 5.9 kg. (13 lbs.)
Shipping: 12.2 kg. (27 lbs.)

Size

Height: 16.0 cm, Width: 27.9 cm, Depth: 34.3 cm. (6.3 x 11.0 x 13.5 in.)

Temperature

**Operating: $0^{\circ}C$ to $+55^{\circ}C$ ($+32^{\circ}F$ to $+131^{\circ}F$)
Storage: $-40^{\circ}C$ to $+75^{\circ}C$ ($-40^{\circ}F$ to $+167^{\circ}F$)

** The disc drive should only be operated from $+5^{\circ}C$ to $+50^{\circ}C$ ($+41^{\circ}F$ to $+122^{\circ}F$) and stored from $+4^{\circ}C$ to $+53^{\circ}C$ ($+39^{\circ}F$ to $+127^{\circ}F$).

Altitude

Operating: 4600 m (15000 ft).
Storage: 15300 m (50000 ft).

Power Requirements

100 to 240 Vac, -10% to +10%;
48 to 66 Hz single phase.

1-4. SAFETY CONSIDERATIONS

When internal circuits are exposed, caution must be used. Observe all warnings and cautions marked on the instrument or listed in the procedures.

WARNING

8000 volts may be present in the HP 4951C even when the instrument is turned off. To avoid personal injury, observe all safety precautions and warnings stated on the instrument and in the manual. This product is a Safety Class 1 instrument which must be connected to a protected earth ground. The HP 4951C and all related documentation must be reviewed for familiarization with safety markings and instructions before operation or servicing.

WARNING

An Isolation Transformer should be used when working on the power supply section of this instrument.

CAUTION

The internal circuits of this instrument are static sensitive. Refer to Section VIII for handling procedures.

1-5. INSTRUMENTS COVERED BY THIS MANUAL

Attached to the instrument is a serial number plate. The serial number is in the form: 0000A00000. It is in two parts: the first four digits and the letter are the serial number prefix and the last five digits are the suffix. The prefix is the same for all identical instruments; it changes only when a change is made to the instrument. The letter in the prefix designates the country in which the instrument was manufactured (A=USA; F=France; G=West Germany; J=Japan; S=Singapore). The suffix changes to identify the individual instrument.

Figure 1-2. Serial Number Tag

The contents of this manual apply to all instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page. An instrument manufactured after the printing of this manual may have a serial prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those described in this manual. Manuals accompanying this newer instrument include a Manual Changes supplement. This supplement contains change instructions to adapt the manual to the newer instrument.

The HP 4951C is manufactured in two locations, one in Europe and one in the United States. When ordering parts or service it is important to correctly identify the manufacturing location so that Hewlett-Packard may give you the best possible service. The manufacturing location is a part of the serial number, the serial number tag is on the back panel of your HP 4951C and is similar to that in Figure 1-2.

For information concerning a serial prefix number that is not listed on the title page contact the nearest Hewlett-Packard Sales and Service office.

1-6. ACCESSORIES SUPPLIED

Accessories supplied with the instrument are listed here.

Power Cord 2.3m (7.5 ft)	Depends on Destination
Pod-Instrument Cable (for all pods)	HP 04951-61618
Operating Manual	HP 04951-90702
Jumper Cable	HP 8120-4218
Y Jumper Cable	HP 8120-4219

The power cable is selected at the factory according to the country of destination. Part numbers of the available power cables are listed in Section II.

1-7. ACCESSORIES AVAILABLE

The following accessories are available for the HP 4951C.

18174A	RS-449/422A/423A Interface Pod
18177A	V.35 Interface Pod
18179A	RS-232C/V.24 Interface Pod with Breakout Box and 3-state LEDs
18180A	Combination RS-232C/V.24 and RS-449/422A/423A Interface Pod
18190A	Soft Vinyl Carrying Case
18331D	Advanced Protocol Analysis SW (SNA Analysis, DDCMP, X.25 Support)
18332D	3270 Installation and Maintenance SW
18347A	HP 4951C Customer Training
92192A	Box of 10 blank discs
92205A	Hayes Smartmodem 1200
2225D	RS-232C/V.24 ThinkJet Printer
9211-1290	Hard Transit Case

1-8. OPTIONS

Standard options are modifications installed at the factory and can be ordered by contacting a Hewlett-Packard sales office.

Option 002	Deletes Integral Disc Drive
Option 003	Katakana (JIS 7, JIS 8, EBCDIK datacodes)
Option 101	Adds accessory 18174A (RS-449/422A/423A)
Option 102	Adds accessory 18180A (RS-232C/V.24 and RS-449/422A/423A)
Option 103	Adds accessory 18179A (RS-232C/V.24 and Breakout Box)
Option 105	Adds HP 18177A (V.35)
Option 500	Substitutes Japanese Operating Manual and Getting Started Guide
Option 501	Substitutes French Operating Manual and Getting Started Guide
Option 502	Substitutes German Operating Manual and Getting Started Guide
Option 915	Service Manual (Part Number 04951-90703)
Option 916	Extra operating manual (Part Number 04951-90702)
Option W30	Two year extended Hardware Support
Opt.4953A+N00	Software Notification Service

1-9. SERVICE SUPPORT

Hewlett-Packard provides service support in three ways for your HP 4951C: *on-site repair, service center repair* and *customer repair.*

On-site Repair

For on-site repair, an HP Field Service Engineer goes to the customer's site and troubleshoots and repairs the HP 4951C at the assembly level. The defective assembly is then exchanged for a new or reconditioned assembly. This is the fastest way to get the instrument up and running.

Service Center Repair

For service center repair, the customer returns the defective HP 4951C to an HP Service Office. An HP Service Engineer repairs the instrument to a component level and returns it to the customer.

Customer Repair

Customers have the option of repairing their own instrument. Troubleshooting information to repair the HP 4951C to a component level is provided in this manual and the major HP 4951C assemblies are available for assembly level repairs.

1-10. RECOMMENDED TEST EQUIPMENT

The test equipment listed in Table 1-1 is recommended to service the HP 4951C. This equipment is used for the adjustments and for troubleshooting to the component level. Equivalent equipment may be substituted.

Table 1-1. Recommended Test Equipment for Troubleshooting

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Signature Multimeter	DC volts 250V Freq. 10 MHz Resistance 10 M	HP 5005A/B
Oscilloscope	>20 MHz bandwidth	HP 1740A
Voltmeter	1000 VDC	HP 3466A
Function Generator	Triangle Waveform 50 kHz	HP3310B
DC Supply	18 VDC, 2 amp	HP 6263B
Universal Counter	$\leq$ 1% Accuracy	HP 5328A/B

1-11. TROUBLESHOOTING ACCESSORIES

The equipment listed in Table 1-2 is recommended to service the HP 4951C. This equipment is used for troubleshooting the different areas of the HP 4951C.

Table 1-2. Troubleshooting Accessories

DESCRIPTION	PART NUMBER	RECOMMENDED QUANTITY
4951C/52A Service Kit	5060-7183	1
*Disc System Service Assy.	5060-7184	1
*Disc Drive Extender Cable	5060-7180	1
*40 Pin IC Clip	1400-1290	1
*28 Pin IC Clip	1400-1289	1
*24 Pin IC Clip	1400-1288	1
*20 Pin IC Clip	1400-1286	1
*16 Pin IC Clip	1400-1285	1
*14 Pin IC Clip	1400-1418	1
*Jumper Wire,Single	8120-4218	4
*Jumper Wire,Double	8120-4219	4
*Jumper Wire,Single Resistor	8120-4892	3
*Jumper Wire,Double Resistor	8120-4893	3
*IC Leg Grabber	10230-62601	10
*Test Points	1251-8360	10
*Power Supply Load Resistor	0811-1655	1
*Power Supply Load Resistor	0811-1656	1
*Disc 3.5 inch Micro Floppy	9164-0243	2
Exchange Micro Floppy Disc Drive	5080-8600	1
Isolation Transformer	9100-4605	1

* These items are included in the 5060-7183 Service Kit, or can be ordered separately.

1-12. CLEANING AND HANDLING PRECAUTIONS

When cleaning the instrument or handling and repairing PC boards, the following precautions should be observed.

Cabinet Cleaning

To clean the instrument cabinet, use only a damp cloth and a mild detergent. Do not allow water to penetrate inside the cabinet.

When cleaning the CRT window, use only a non-abrasive cleaner and a soft cloth.

PC Board Cleaning

When repairing PC boards, only RMA type solder should be used. This type is low in chlorides which are the main cause of most contamination problems.

It is recommended that the solder flux and resin be left on the board after a repair. This residue does not cause any electrical problems. Flux remover makes the board look good but leaves a film that can cause intermittents.

Do not use a pencil eraser to clean PC board edge connectors. All erasers leave a film which causes intermittent problems.

The correct procedure is to clean the connectors with a 50/50 solution of water and isopropyl alcohol using a lint-free cloth (HP P/N 9310-0039). Do not use abrasive paper wipes.

The water/alcohol solution dissolves the chemicals that get on the connectors from the soldering process. The lint-free cloth provides the mechanical rubbing action needed to free the contact fingers of all contamination.

PC Board Handling

All of the HP 4951C PC boards should be protected from contaminants such as oils and greases, fingerprints, body perspiration (sodium-chloride residue) and cleaning solutions with ionic detergents.

All of the HP 4951C PC boards have a Dry Film, High Impedance surface.

When handling a PC board, touch only the board edges, or wear clean cotton gloves.

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section provides installation instructions for the HP 4951C. Also included in this section is information pertinent to initial inspection, preparation for use, storage, and shipment.

2-2. INITIAL INSPECTION

WARNING

To avoid hazardous electrical shock, do not conduct any tests when there are signs of shipping damage to any portion of the outer covers and panels.

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked mechanically and electrically. The electrical performance is checked automatically at the time of power on. If there are any selfcheck failures refer to Section IV for a description of the tests. If there is mechanical damage or defects, or if the instrument does not pass the electrical performance test, notify the nearest Hewlett-Packard Sales and Service office. If the shipping container or the cushioning materials show signs of damage, notify the carrier as well as the Hewlett-Packard office. Keep the shipping material for the carrier's inspection.

NOTE

A transportation disc should be inserted in the disc drive when you receive your instrument. If it is not, please notify the nearest HP Sales and Service office. The transportation disc should be in the unit any time it is in transit.

2-3. POWER REQUIREMENTS

No line range selection is necessary on the HP 4951C. The instrument requires a power source of 100 to 240 volts +/- 10% ac at a frequency of 48 to 66 Hz.

WARNING

This is a Safety Class I product (provided with a protective earth terminal). An uninterrupted safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied cable set. If this instrument is to be energized via an auto transformer or voltage reduction, make sure the common terminal is connected to the earth pole of the power source. The main plug must be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet does not provide an instrument ground.

CAUTION

If the line fuse burns out, do not replace it until the fault has been determined and repaired by a qualified service person.

2-4. POWER CABLE

The instrument power cable has three wires. When connected to an appropriate power receptacle this cable grounds the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination (see Table 2-1). If the appropriate power cable is not included with the instrument, notify the nearest Hewlett-Packard Sales and Service office for a replacement.

2-5. OPERATING ENVIRONMENT

The operating environment for the HP 4951C should be within the following limits:

Temperature 0° C to 55° C (32° F to 131° F)
(Disc Drive should only be operated from $+5^{\circ}$ C to $+40^{\circ}$ C ($+41^{\circ}$ F to $+104^{\circ}$ F)

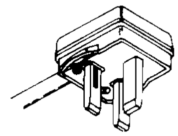
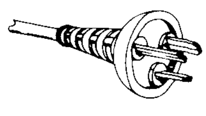
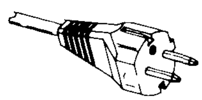
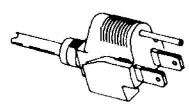
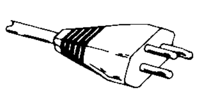
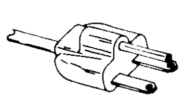
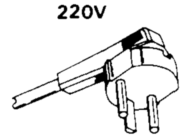
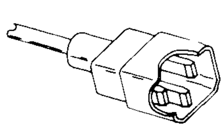
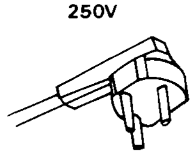
CAUTION

Do not block the fan or ventilation holes. Avoid environment extremes that might cause condensation within the instrument.

NOTE

A transportation disc should be inserted in the disc drive when you receive your instrument. If it is not, please notify the nearest HP Sales and Service office. The transportation disc should be in the unit any time it is in transit.

Table 2-1. Power Cable Part Numbers

Plug Type	Cable HP Part Number	C D	Plug Description	Cable Length (inches)	Cable Color	For Use In Country
250V 	8120-1351 8120-1703	0 6	Straight *BS1363A 90°	90 90	Mint Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Rhodesia, Singapore
250V 	8120-1369 8120-0696	0 4	Straight *NZSS198/ASC112 90°	79 87	Gray Gray	Australia, New Zealand
250V 	8120-1689 8120-1692	7 2	Straight *CEE7-Y11 90°	79 79	Mint Gray Mint Gray	East and West Europe, Saudi Arabia, Egypt, So. Africa, India (unpolarized in many nations)
125V 	8120-1348 8120-1398 8120-1754 8120-1378 8120-1521 8120-1676	5 5 7 1 6 2	Straight *NEMA5-15P 90° Straight *NEMA5-15P Straight *NEMA5-15P 90° Straight *NEMA5-15P	80 80 36 80 80 36	Black Black Black Jade Gray Jade Gray Jade Gray	United States, Canada, Japan (100V or 200V), Mexico, Philippines, Taiwan
250V 	8120-2104	3	Straight *SEV1011 1959-24507 Type 12	79	Gray	Switzerland
250V 	8120-0698	6	Straight *NEMA6-15P			United States Canada
220V 	8120-1957 8120-2956	2 3	Straight *DHCK 107 90°	79 79	Gray Gray	Denmark
250V 	8120-1860	6	Straight *CEE22-VI (Systems Cabinet use)			
250V 	8120-4600 8120-4211	8 7	Straight BS 546/SABS 164 90°	98 98	Black Black	So. Africa, India

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.
E = Earth Ground; L = Line; N = Neutral

2-6. PACKAGING

Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett Packard for service, attach a tag indicating the type of service required, return address, model number, and full serial number. Mark the container FRAGILE to ensure careful handling. In correspondence, refer to the instrument by model number and full serial number.

Other Packaging

The following general instructions should be used for repackaging with commercially available materials:

A. A transportation disc (HP p/n 5060-7177) should be inserted in the disc drive.

B. Wrap the instrument in antistatic material.

C. Wrap the instrument in heavy paper or plastic.

D. Use a strong shipping container. A double-walled carton made of 350-pound test material is suitable.

E. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and to prevent movement inside the container.

F. Seal shipping container securely.

G. Mark shipping container FRAGILE to ensure careful handling.

H. In any correspondence, refer to the instrument by model number and full serial number.

WARNING

A transportation disc should be inserted in the disc drive when you receive your instrument. If it is not, please notify the nearest HP Sales and Service office. The transportation disc should be in the unit any time it is in transit. WARRANTY may be voided if transport is attempted without this disc inserted.

SECTION III
OPERATION

3-1. INTRODUCTION

This section contains a brief description of the operating procedures for the HP 4951C. Complete operating procedures for the HP 4951C Protocol Analyzer are located in the Operating Manual (HP Part Number 04951-90702).

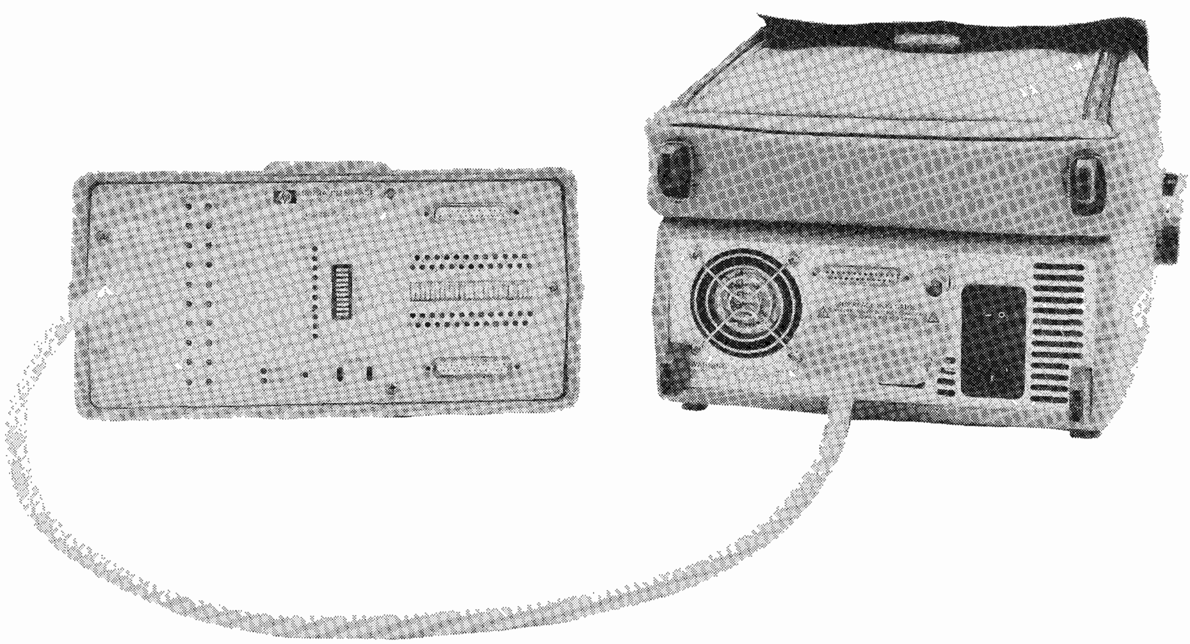


Figure 3-1. Connecting the Interface Pod to the HP 4951C

3-2. TURN ON THE HP 4951C

Before turning the instrument on, connect the Interface Pod to the HP 4951C using the instrument pod cable and securely fastening the two together. Figure 3-1 shows the correct procedure for connecting the Pod to the HP 4951C. Protection circuitry has been installed to guard against problems associated with unplugging the Interface Pod while the instrument is turned on, however, it is strongly recommended that the pod is always connected or disconnected while the instrument is turned off.

3-3. OPERATION

Press the switch on the back of the instrument to 'ON'. The HP 4951C Protocol Analyzer will automatically perform the Performance Verification Test sequence. When the test passes, the Top Level Menu is displayed on the screen and the HP 4951C is ready for operation. If the HP 4951C does not come up to the Top Level Menu, refer to the troubleshooting procedure in Section VIII of this manual.

Six software defined keys, or softkeys, provide operator access to the different operations within the HP 4951C. To select a particular procedure, press the corresponding key on the keyboard. 'EXIT' acts like a halt key during a testing sequence. Press EXIT to stop running a test sequence at any time you need to terminate an operation. Press 'MORE' to see the second or third set of softkeys in any menu.

SECTION IV
PERFORMANCE VERIFICATION

4-1. INTRODUCTION

Each time the HP 4951C is powered on, the Performance Verification tests are run automatically. The tests are completed in about 15 seconds and the internal circuits of the instrument do not have to be accessed by the operator. If the HP 4951C fails any of the Performance Verification tests, send the instrument to an authorized HP Repair Center or refer to the Service Section (VIII) of this manual. When the Performance Verification tests are complete, with no errors, the Top Level Menu is displayed.

NOTE

If the Disc Test fails at power up, it is not immediately reported. In order to check the results of this test, you must enter the Mass Store Menu. Do this by softkey stroke <More> followed by <Mass Store>. If an error has occurred during the Disc Test, it is reported within the Mass Store Menu.

4-2. SELF TEST MENUS

The operator may manually enter the Self Test menu and execute a variety of performance tests that are not performed during the power up test sequence. To do this execute the following softkey strokes: <More> and <Self Test>. The following tests are available from the Self Test Menu:

<LOOP> - Pressing this softkey causes the instrument to loop through its power up test sequence once. Any errors are reported in this menu. To exit this test, press the <Exit> key.

<CRT TESTS> - Pressing this softkey gives you another menu. Softkeys are defined as <Test Ptrn>, <Char Set 1>, and <Char Set 2>. These softkeys cause a specific pattern to be displayed. There is a hidden softkey function within this menu. It is a full raster display. You can enable this function by pressing the right most softkey when the other CRT function softkeys are displayed. To get out of this menu, press the <Exit> key.

<KBD TEST> - Pressing this softkey enables the user to test the keyboard functions. When an individual key on the keyboard is pressed, the corresponding character is displayed as the "Last Key Pressed". The lower case, upper case, and control function character sets can be verified by this test. To exit this test, press the <Exit> key.

<EXT DLC> - Pressing this key initiates a test for an external pod interface. The interface pod must be connected to the pod interface cable in order for the test to function properly. Pass or fail conditions are then reported on the display. To exit this test, press the <Exit> key.

<DISC TESTS> - Pressing this key puts you into the Disc Test Menu. <Disc Cal> and <Self Test> are the available functions. Pressing <Disc Cal> puts the Disc Controller system into a calibration mode. This mode is for Factory and Service use only. Pressing the <Self Test> softkey causes the instrument to perform the same disc test that was executed at power up. Pass or fail conditions are then reported to the display. Press <Exit> to leave this menu level.

<CONTINUOUS TEST LOOP> - This is a hidden function that is executable from the first level Self Test Menu. After entering into the Self Test Menu from the Top Level Menu by pressing <More> and <Self Test>, the hidden loop key is the foremost right softkey. Pressing this softkey puts the instrument into a continuous Performance Test Loop. Any errors are displayed on the screen. This mode of self test is useful for verifying intermittent failures. This mode continues as long as the instrument has power. To leave this test mode, hold down the <Exit> key until the Top Level Menu is displayed.

Figure 4-1 shows the softkey configurations for the Self Test Menus.

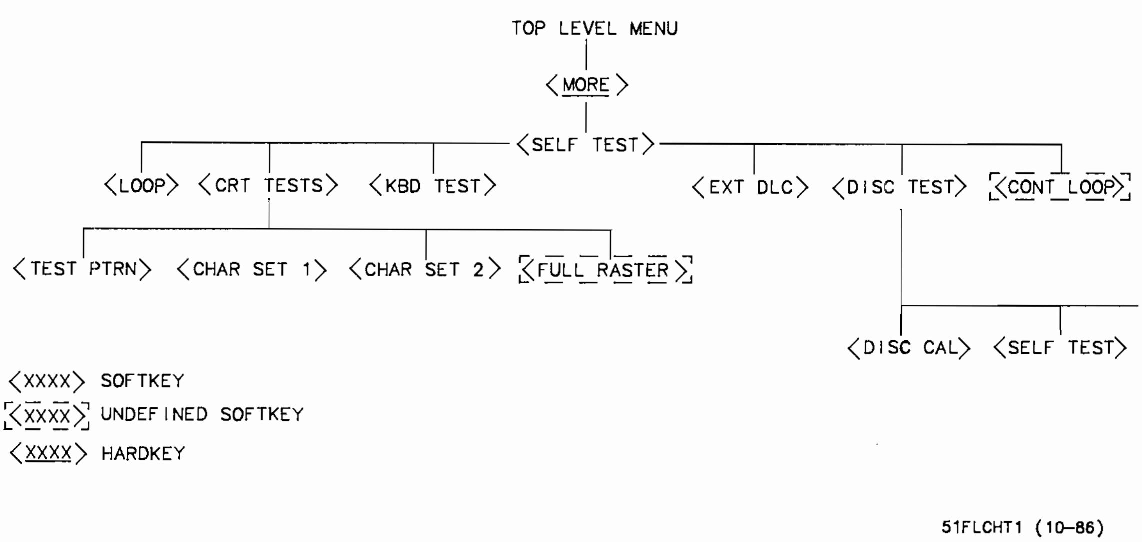


Figure 4-1. Softkey Menu Guide

4-3. RECOMMENDED TEST EQUIPMENT

No equipment is required for the Performance Verification Tests.

4-4. PERFORMANCE VERIFICATION TESTS

This test sequence verifies the functional operation of 95% of the HP 4951C Protocol Analyzer. There are eight parts to the automatic test sequence. To begin testing, turn on the HP 4951C. The tests outlined in Figure 4-2 are automatically performed. The operator may then manually select the other available performance tests, or start using the Protocol Analyzer.

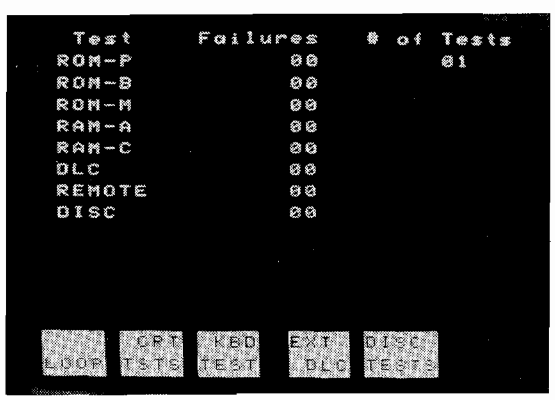


Figure 4-2. Error Table for HP 4951C Performance Verification Tests

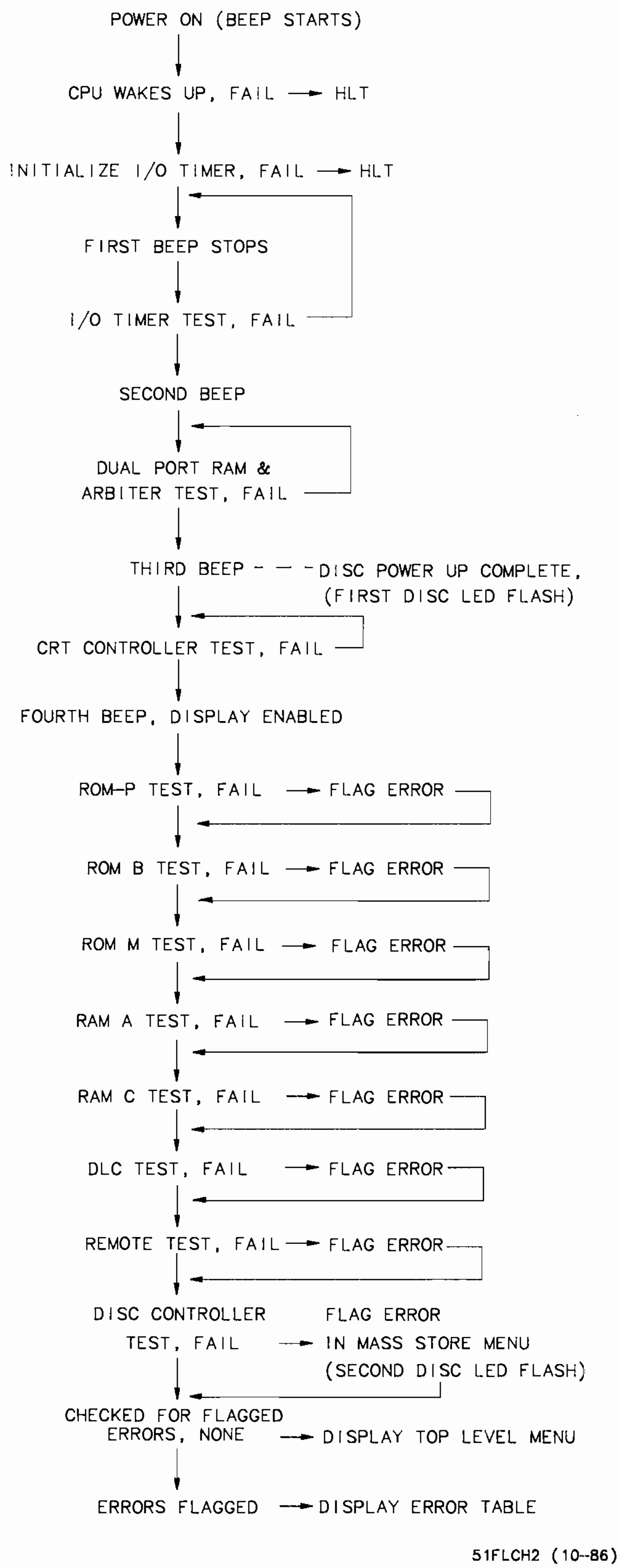


Figure 4-3. Performance Verification Flowchart

4-5. PERFORMANCE VERIFICATION TEST DESCRIPTIONS

The following is a description of the Performance Verification tests done automatically at instrument turn on. They are referenced to the flowchart in Figure 4-3. Troubleshooting procedures are located in the Service Section (VIII). The Top Level Menu is displayed when the instrument passes the Performance Verification tests. If there is a failure, the Failure Table remains on the display. An "01" appears in the Failure Column by the failed test denoting the test was executed and a failure occurred. Press <Exit> to access the Top Level Menu.

A. TURN ON INSTRUMENT / MICROPROCESSOR WAKES UP

Test Failure Code: Continuous beep.
Description: When the beep stops, the microprocessor and the power supply are working.

B. I/O TIMER

Test Failure Code: Continuous beep or one beep only.
Description: This test checks the functions of the I/O Timer.

C. DUAL PORT RAM AND ARBITER TEST

Test Failure Code: Continuous beep or one or two beeps, no display.
Description: This test checks the functions of the arbiter and Dual Port Ram.

D. CRT CONTROLLER INITIALIZATION TEST

Test Failure Code: Three or four beeps, no display.
Description: This test checks the functions of the CRT Controller.

E. ROM P TEST (Page ROM (0), U304)

Test Failure Code: Continuous beep, one beep or failure reported on the Error Table.
Description: This test checks the checksum of ROM P.

F. ROM B TEST (Bank ROM, U403)

Test Failure Code: Continuous beep, Remote-System Error or reported on the Error Table.
Description: This test checks the checksum of ROM B.

G. ROM M TEST (Mass Store ROM, U407)

Test Failure Code: Continuous beep, Disc-System error or reported on the Error Table.
Description: This test checks the checksum of ROM M.

H. RAM A TEST (Application RAM, U406)

Test Failure Code: Continuous beep, lock up in Remote Test, or reported on the Error Table.
Description: This test checks the memory locations of the RAM.

I. RAM C TEST (Capture Buffer RAM, U409)

Test Failure Code: Continuous beep, RAM C and Disc failure reported, or reported on the Error Table.
Description: This test checks the memory locations of the RAM.

J. DLC TEST (SCC)

Test Failure Code: Error reported on the Error Table.
Description: This test checks a limited amount of the functions of the SCC and other circuitry.

K. REMOTE TEST

Test Failure Code: Error reported on the Error Table.
Description: This test checks the functions of the Remote Port of the instrument.

L. DISC TEST

Test Failure Code: The error would be flagged in the Mass Store Menu. Any error is evident when the user enters the Mass Store Menu. If the Disc Test is called via the <Loop> key from the Self Test Menu, an error is reported on the Error Table.
Description: This test checks the function of the Disc Controller Assembly.

4-6. CRT TESTS

Description: The CRT tests are nothing more than a visual check of patterns that are generated by the instrument. Checking these patterns verifies that the CRT Controller circuitry is operating properly.

Set Up: Turn on the HP 4951C. Press <More>, <Self Test>, and <CRT Tests>. You now have three patterns to select from. These checks are optional.

Procedure: Once the display pattern is displayed, one can check for irregularities in the patterns. This is strictly a visual test by the operator.

To exit this test, press the <Exit> key.

4-7. KEYBOARD TEST

Description: The keyboard test is performed by the operator. It verifies that the HP 4951C can correctly identify each key pressed on the keyboard.

Set Up: Turn on the HP 4951C. Press <More>, <Self Test>, and <KBD Tst>.

Procedure: Press any key on the keyboard. The display should read:
LAST KEY PRESSED: "(name of key pressed is displayed)"

Press <Exit> to end the test and display the Self Test Menu.

NOTE

The Cursor Down and Return keys effectively make the cursor perform the same operation. When the RETURN key is pressed, CURSOR DOWN is displayed.

4-8. INTERFACE POD TEST (EXTERNAL DLC)

Description: The EXT DLC test is performed by the operator. It verifies the interface from the instrument to the Pod Interface as well as the Pod Interface itself.

Set Up: Turn on the HP 4951C. Be certain that there is an Interface Pod connected to the HP 4951C. Press <More>, <Self Test>, and <EXT DLC>.

Procedure: When the <EXT DLC> softkey is pressed, the Interface Pod Test is automatically executed.

One of the following error messages may appear:

- No pod attached
- DTE failed
- DCE failed
- DCE/DTE failed

If all tests pass, the message "DLC test passed" is displayed.

To exit from this test, simply press the <Exit> key.

4-9. DISC CONTROLLER TEST

Description: This test is executed at power up or can be executed by the operator. It checks the basic functions of the Disc Controller.

Set Up: Power up the HP 4951C. Press <More>, <Self Test>, and <Disc Tests>.

Procedure: Press the <Self Test> key to execute the Disc Test.

One of the following error messages may appear:

- Self Test Time Out Error
- Self Test Failed DMAC
- Self Test Failed FDC
- Self Test Failed DMAC/FDC

If all testing passes, the message "Self Test Passed" is displayed.

To exit this test field, press the <Exit> key.

4-10. DISC WRITE/READ TEST

Description: This test can be executed any time there is a need to see if the read and write functions of the Disc Controller Board are working properly.

Set Up: To create a data file for this test start with a blank 92192A flexible disc that has been formatted. If the disc has not been formatted, you can do this by going into the 'Mass Store Menu'. Execute the following program by first going to the Set Up Menu and changing the appropriate fields to the Following:

Set Up Menu:	Default Configuration
Bits/Sec:	19200
Disp Mode:	DCE

Now enter the following program in the Simulate Menu:

Simulate: DCE

Block 1
Start Display
And Then
Start Disc

Block 2
Send "Disc Test"
And Then
Goto Block 2

Now press <Run Menu> and <Simulate>. You will be asked for a file name to give to the data, enter "DTEST", and then press <Execute>. The test will now begin executing. Notice that information is now being stored to the disc. This test will run for about 2.5 minutes. Once the test is complete the message "DISC FULL"should be displayed. If no errors have been reported, the 'write' phase of the test has been completed. The data file has now been created and data has been written to the entire area of the disc.

Procedure: To read the data that has been written to the flexible disc do the following procedure:

Using the disc that the data file has been created on, go to the Mass Store Menu and load the "Menu & Data" file. Exit the Mass Store Menu and go to the Examine Data Menu (Note: The typical size of the file should be 2449 sectors as indicated in the Mass Store Directory).

Using the <More> key find the <Spec Block> key and press. The current block should be #16. Manually enter 999. After you press the last '9' the display should default to '308'. This is the maximum block number allowed by the HP 4951C. Press <Return>. The message "Searching" should appear and you should see occasional activity of the disc drive as the system searches through the file to find block #308.

When this test is complete, the message "End of Disc File: Last Part of Disc Data in Buffer" should appear. If no errors have occurred, the Disc Drive and Disc Controller Board are writing and reading data correctly.

NOTE

If this test is to be repeated, the data file must be deleted and the disc must be packed. Otherwise the HP 4951C will reject the disc as having the same file name or being full of data.

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

This section describes the adjustments that are necessary to return the HP 4951C to its normal specifications after repairs have been made. Normally, adjustments are necessary only when repairs to associated circuitry have been made or if the instrument has gone out of adjustment.

WARNING

Adjustments are performed with the power applied to the instrument. Adjustments should be performed only by service-trained personnel who are aware of the hazards involved. Read the safety summary at the front of this manual before making any adjustments.

To access the instrument's internal circuits, follow the disassembly procedure outlined in Section VI. For your protection and to avoid damage to the instrument, all listed warnings and cautions should be followed. Follow the correct procedure for handling static sensitive devices in Section VIII when working on exposed circuits.

WARNING

8000 volts can be present in the HP 4951C circuitry even when the instrument is turned off.

When adjustments are in the high voltage circuitry, tools used should be insulated or made of non-conductive materials. Safety glasses should be worn when replacing the CRT or working on the power supply

5-2. RECOMMENDED EQUIPMENT

HP 5328 Universal Counter
HP 1740A Oscilloscope
HP 5005A/B Signature Multimeter
Hexagonal Plastic Core Adjustment Tool
Small Insulated Screwdriver
CRT Adjustment Magnets

5-3. CRT ADJUSTMENTS

There are six adjustments that are used to align the HP 4951C CRT to its original specifications. Figure 5-1 shows the parts that are used for the CRT adjustments.

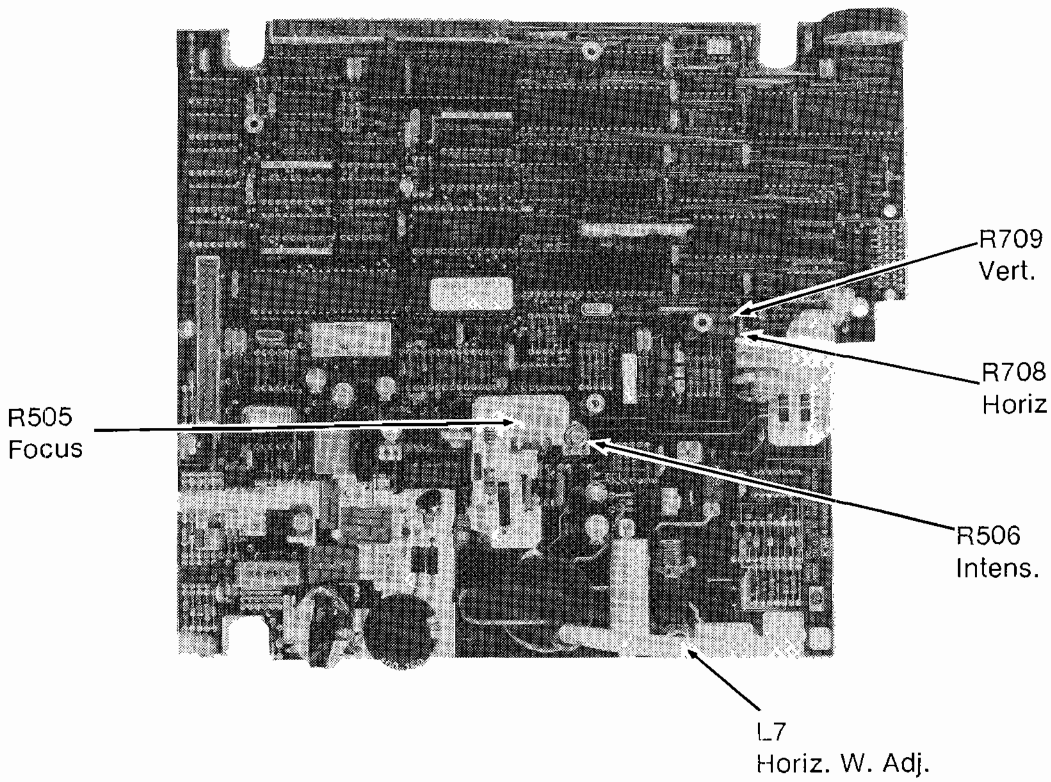


Figure 5-1. CRT Adjustment Points

To get to the display menu that is used for making CRT adjustments, perform the following procedure:

Turn on the HP 4951C
Press MORE
Select <SELF TEST>
Select <CRT TSTS>
Select <TEST PTRN>

The screen that should be displayed is pictured in figure 5-2.

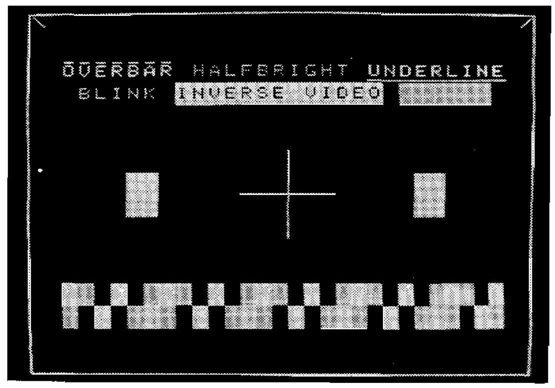


Figure 5-2. CRT Adjustment Pattern

NOTE

All of the CRT Adjustments may have to be used in conjunction with each other to achieve the proper alignment on the display.

Focus

While observing the displayed test pattern adjust A1 R505 (Focus Adjustment) to achieve the maximum clarity of characters.

Intensity

With an insulated adjustment tool, adjust A1 R506 (Intensity Adjustment) so that the brightness level provides a clear distinction between the character types on the display. Look for a clear difference between the half bright and full bright levels.

Vertical Height

With an insulated adjustment tool turn A1 R709 (Vert. Height Adjustment) until the frame around the display is like that in figure 5-2.

Display Centering

Using figure 5-2, adjust A1 R708 (Vert Center Adjustment) so that the frame around the edge of the display is Centered with respect to the plastic mask of the front panel.

Horizontal Adjustments

Adjust A1 L7 (Horizontal Width Adjustment) with a plastic core adjuster until the display is the desired width.

Centering Adjustments

The centering rings on the CRT Yoke should be rotated together until the desired horizontal balance is achieved. Each centering ring tab should be kept opposite of the other. This allows for a cancelling effect of magnetic forces that would adversely affect pin cushioning of the CRT. Loosen the CRT Yoke Clamp Screw and rotate the yoke assembly to obtain 'squareness' of the displayed pattern.

Pincushioning

'Pincushioning' is a process that is used to straighten the horizontal and vertical lines on the edges of the display. It should be used after the proportional adjustments have been made. Magnets of increasing strength are put on the CRT Yoke and rotated to obtain straight lines on the CRT. After the adjustments are correct, the magnets must be secured by using hot glue or other method of affixing the magnets so they won't fall off the Yoke.

5-4. DISC CONTROLLER BOARD ADJUSTMENTS

The Disc Controller Board (A3) has several adjustments that may need to be adjusted in order to assure proper operation of the Disc Controller System. There are three adjustments that are used to bring the HP 4951C Disc Controller Board to its original specifications. Figure 5-3 shows the parts that are used to make the adjustments.

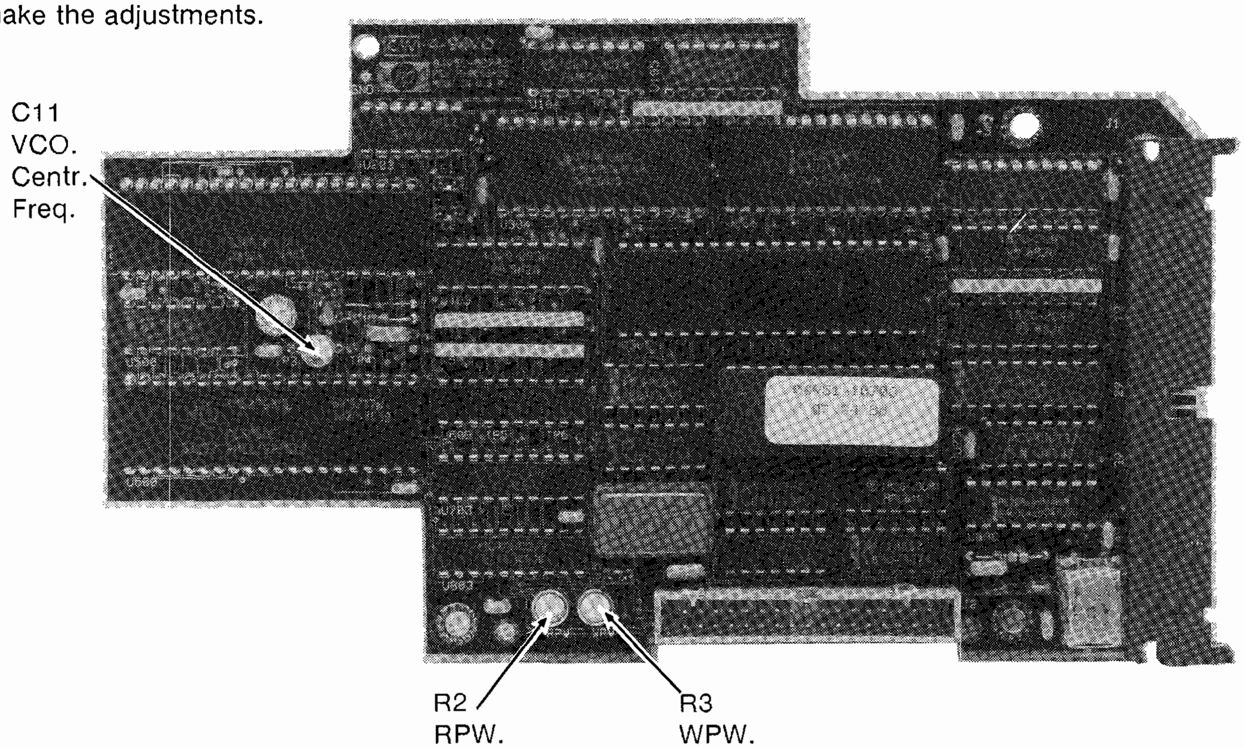


Figure 5-3. Disc Controller Adjustment Points

In order to make the adjustments to the Disc Controller board, it must be put into a calibration mode. This can be done by executing the following keystrokes. With the HP 4951C in the Top Level Display Menu, press:

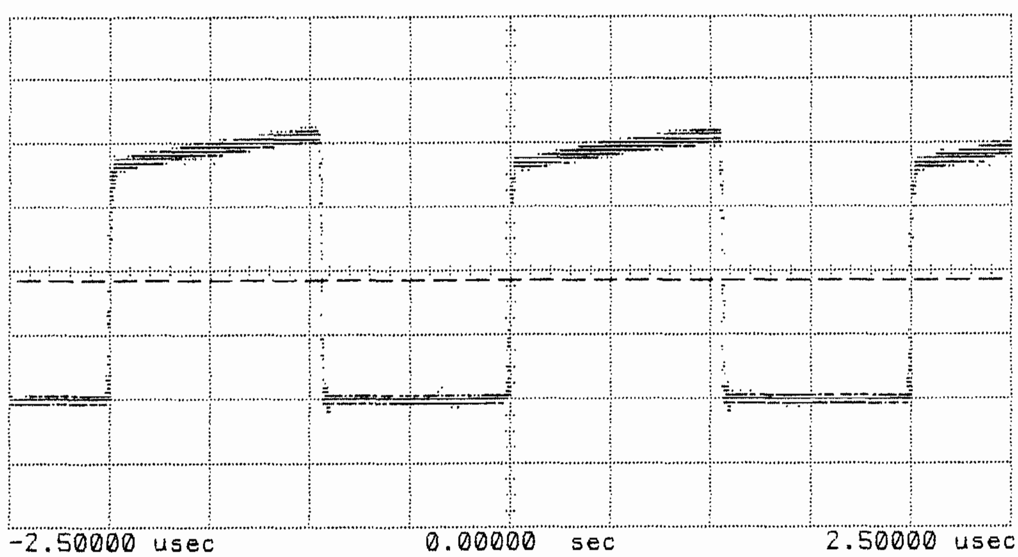
<MORE>
Select <SELF TEST>
Select <DISC TESTS>
Select <DISC CAL>

Completing this sequence puts the HP 4951C into the Disc Controller Calibration Mode. This is indicated by the message that is displayed. The instrument must be in the Calibration Mode during all of the disc adjustment procedures.

VCO Center Frequency

Using an HP 5328A/B Universal Counter, monitor TP5 on the A3 board. Use a high impedance scope probe to avoid loading the signal. Adjust A3C11 to obtain a frequency measurement of 500 Khz +/- 5 Khz (495 Khz to 505 Khz). Be sure to remove the adjustment tool from C11 and recheck the measurement as the adjustment tool affects the measurement. An HP 5005A/B Signature Multimeter may be used as a second reference for this frequency measurement.

The waveform shown in Figure 5-4 is a representation of the desired waveform using an oscilloscope.



Ch. 1	=	1.000 volts/div	Offset	=	2.040 volts
Timebase	=	500 nsec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	500.065 KHz

Figure 5-4. VCO Center Waveform

Read Pulse Width

Using an HP 5328A/B Universal Counter, monitor TP3 on the A3 board. The Universal Counter should be configured to measure the time interval between channel A, + slope trigger and channel B, - slope trigger. Manual triggering should be used as opposed to preset triggering. Adjust A3R2 (RPW) to obtain a measurement of 250 nsec +/- 12.5 nsec (237.50 nsec to 262.50 nsec).

The waveform shown in Figure 5-5 is a representation of the desired waveform using an oscilloscope.

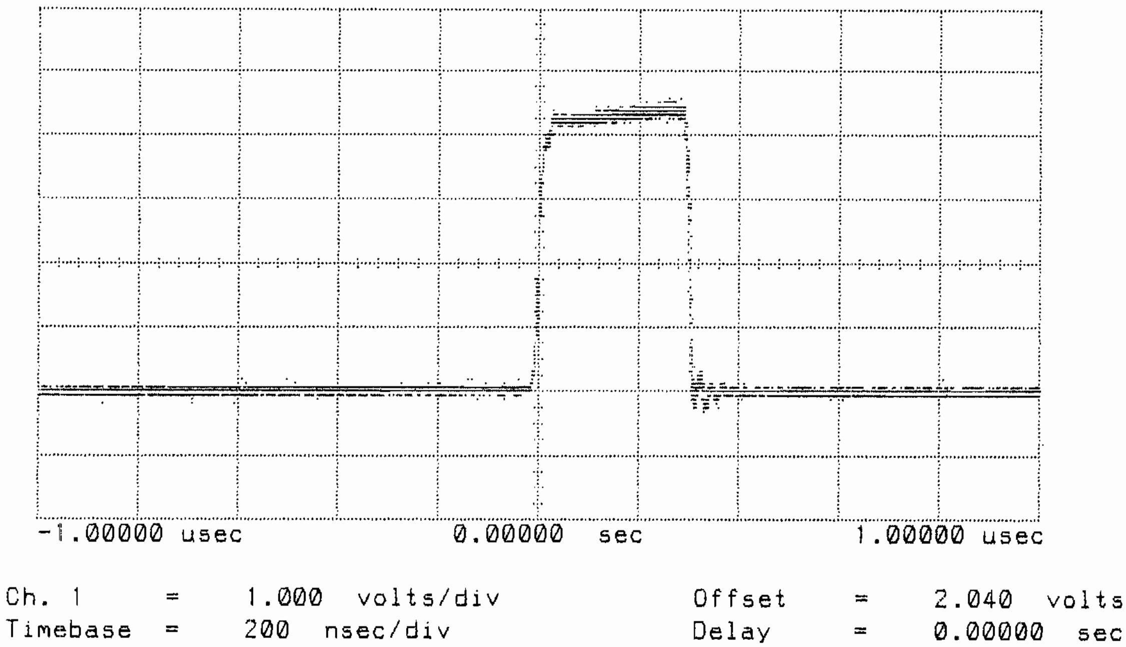


Figure 5-5. Read Pulse Width Waveform

Write Pulse Width

Using an HP 5328A/B Universal Counter, monitor TP6 on the A3 board. The Universal Counter should be configured to measure the time interval between channel A, + slope trigger and channel B, - slope trigger. Manual triggering should be used as opposed to preset triggering. Adjust A3R3 (WPW) to obtain a measurement of 125 nsec +/- 6.25 nsec (118.75 nsec to 131.25 nsec).

The waveform shown in Figure 5-6 is a representation of the desired waveform using an oscilloscope.

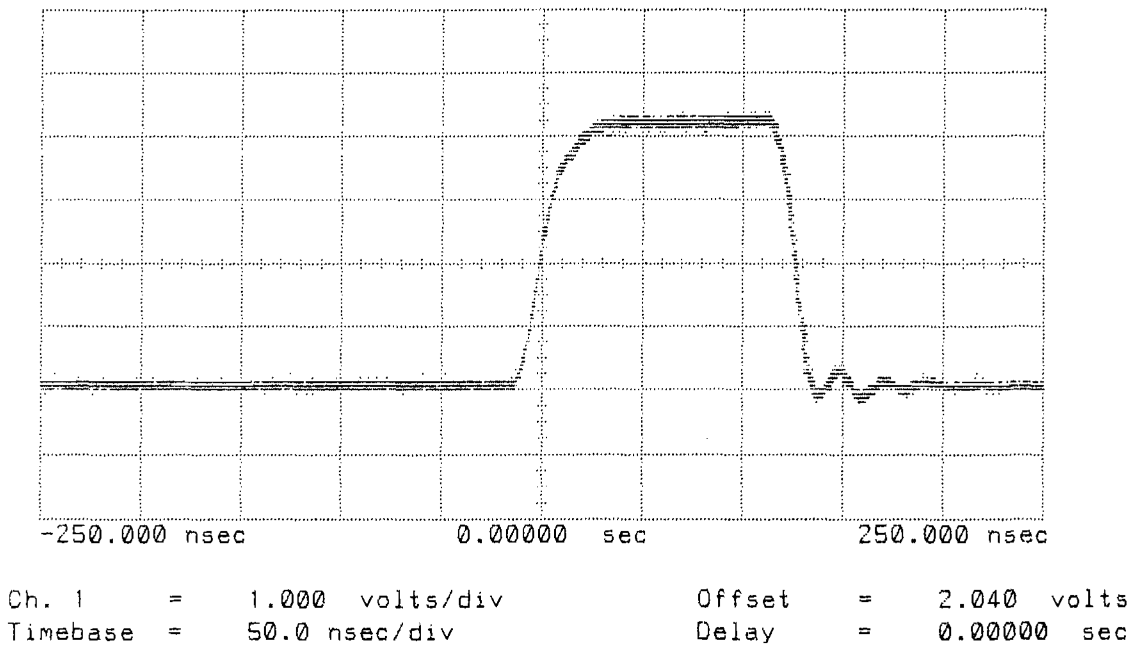


Figure 5-6. Write Pulse Width Waveform

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering parts and assembly removal procedures. The figures in this section are used to identify the mechanical and hardware parts you need. Component locators in Section VIII can be used to identify a part on a PC board. After finding the part in one of the figures, look up the reference designator in the parts list for ordering information.

6-2. REPLACEABLE PARTS LISTS

The replaceable parts lists are located in the tables at the end of this section. Parts are listed in order by the board number and the reference designation. Information is given for the Description, Quantity, and HP Part Number. Mechanical parts for the front and rear panel assemblies are listed under their respective photographs.

6-3. ORDERING INFORMATION

To order a part that is listed in this manual, quote the HP Part Number, indicate the quantity needed, and send the order to the nearest Hewlett-Packard office. When ordering a part not listed include the instrument model number, serial number, physical, and functional description of the part.

6-4. DISASSEMBLY / ASSEMBLY PROCEDURES

CAUTION

Whenever internal circuits of the HP 4951 are accessed, procedures for handling static sensitive devices must be observed. For correct handling see paragraph 8-5.

WARNING

8000 volts can be present even when the HP 4951C is turned off. Opening the HP 4951 case exposes high voltage circuits. Disconnect the instrument from all voltage sources before opening the HP 4951C case.

Recommended Equipment

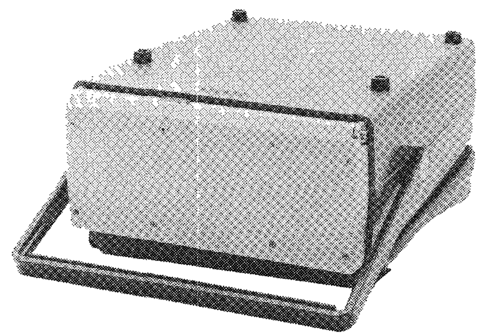
#1 Posidrive Screwdriver
#2 Posidrive Screwdriver
Needle Nose Pliers
Static Safe Work Area
1/2" Nut Driver

A. Remove Top Cover -

Open the soft pouch and remove the right front screw.

Lay the instrument upside down on a clean surface. Remove the four screws that secure the feet and the case halves.

Hold the halves of the case together and turn the instrument right side up. Carefully pull the case top up and off. Remove the handle.



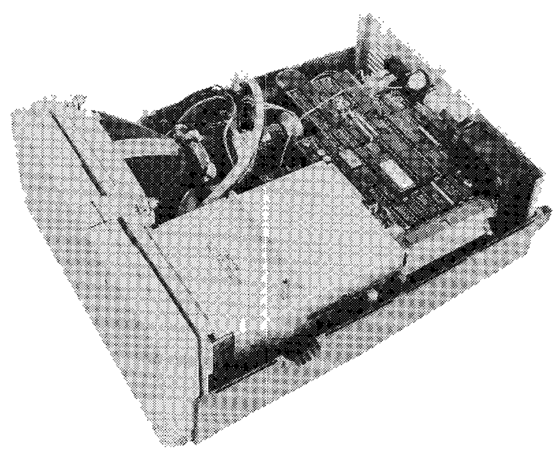
B. Remove the Floppy Disc & Disc Controller Board

Remove the external video wire that is connected from the main board (A1E609) to the rear panel.

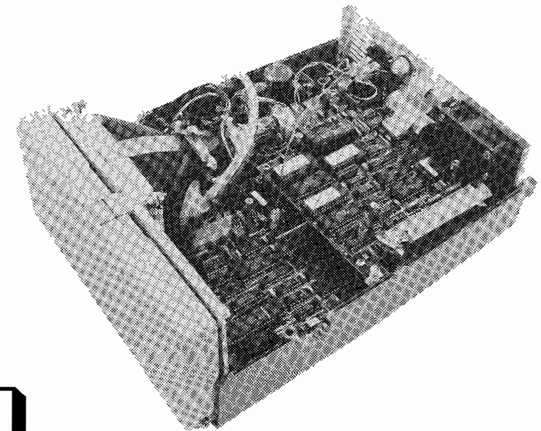
Disconnect A3J2, the cable between the disc and the controller board. Disconnect A3J1, the cable between the controller board and the memory board.

Remove the 4 screws that hold the controller board and lift the board out of the instrument.

Remove the 2 screws that secure the disc to the front panel and the 1 screw that fastens to the standoff on the main board and lift the disc out of the instrument.



C. Remove the Memory Board



Disconnect A2J1, the cable between the memory board and the main board. Remove A2J2, the remote/printer cable that goes to the rear panel.

Remove the 2 screws and 2 spacers that secure the memory board. Lift the memory board out of the instrument.

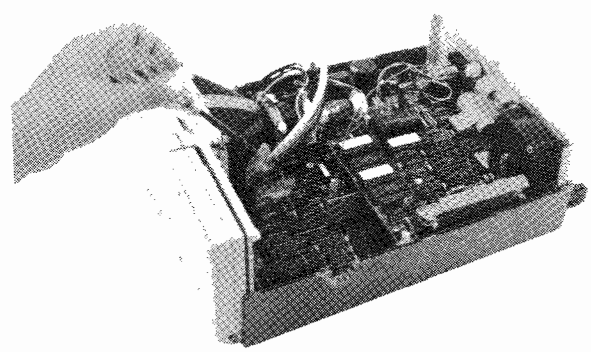
D. CRT and Front Panel Removal

WARNING

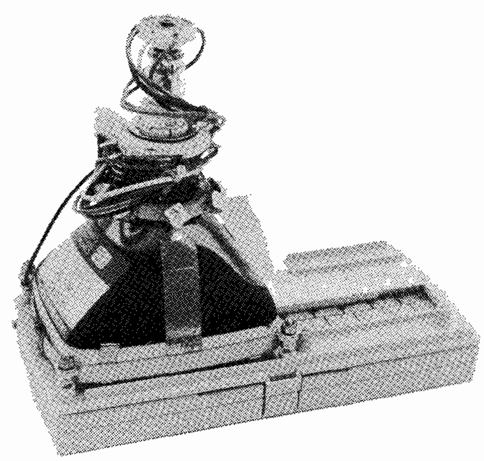
Wear safety glasses when handling the CRT

WARNING

Be sure the HP 4951C is turned off and unplugged from any power source before attempting any work on the CRT or surrounding area. High voltages exist in this area of the instrument.



To discharge the CRT to ground, slide a screwdriver with an insulated handle under the PA cable cover and touch the metal part of the screwdriver to one of the metal screws on the CRT or another metal surface which is ground. Be careful not to touch the bracket around the Disc Controller Assembly. Use needle nose pliers to squeeze together the two leads in the PA cable and remove the prongs from the CRT.



Remove the two cables from the yoke and the base of the CRT to the main board(J3 & J4). Remove the front panel keyboard cable A1J6 from the main board by sliding the fastener to the right on A1J6.

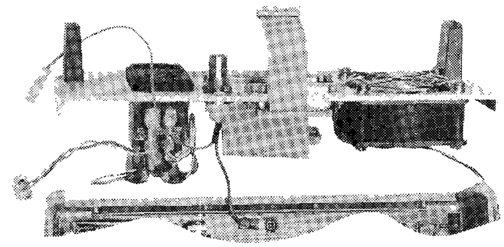
Slide the CRT and front panel assembly up and out of the lower case. Close the keyboard and set the front panel on a clean dry surface.

Remove the 4 lock nuts that hold the CRT to the front panel. Lift the CRT off the front panel.

E. Rear Panel Removal

Disconnect the cable A1J2 and the 2 jumpers, E208 and J5, that connect from the rear panel to the main board.

Lift the rear panel out of the case and remove the screw that connects the ground lug from the rear panel to the main board.



F. Main Board Removal

Remove the three plastic stand-offs and lift the main board up and out of the lower case.

To reassemble the HP 4951C, follow the preceeding procedure in reverse order. Note the following assembly procedures when reassembling the HP 4951C. Be sure that all parts and hardware are put back together properly.

A. The wires from the line module must be dressed in a certain way to keep them from rubbing with other components in the instrument. Failure to dress these wires properly could result in a safety problem. The wires should be bent back towards the rear panel so that they do not touch any of the PC boards. See the proper way to dress these wires in Figure 6-1.

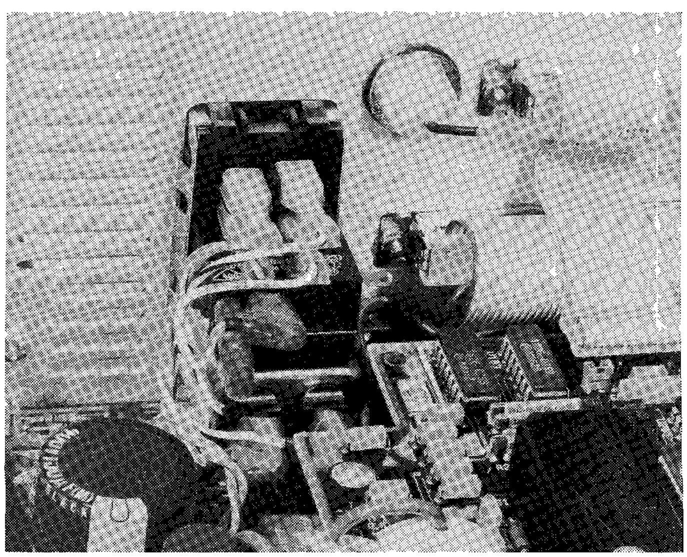


Figure 6-1. Line Module Wire Dressing

B. Be sure the keyboard cable connector is securely fastened to the A1 Main Board. You should be aware that the connector can be "locked" without being seated properly on the board. A visual check of the wire locks should be made anytime this connector has been removed. You should be able to see the wire locks on both sides of the connector on the bottom of the PC board. After the keyboard cable has been reconnected, you should run the keyboard verification test again.

C. Be sure the proper hardware is used when reassembling the disc drive. The three screws (2360-0476) used to attach the mounting bracket to the disc drive are metric. When replacing the Disc Controller Cable, be sure that all parts are keyed correctly. The #1 pin on both the Disc Controller Board and the Disc Controller Assembly should match with the #1 pins on the cable.

D. There are three different screws that hold the case halves together. With the instrument turned upside down, the shortest screw (2510-0063) goes in the front left hole, the longest screw (2510-0324) goes in the right front hole, and the two medium screws (2510-0296) go in the two holes in the back of the instrument.

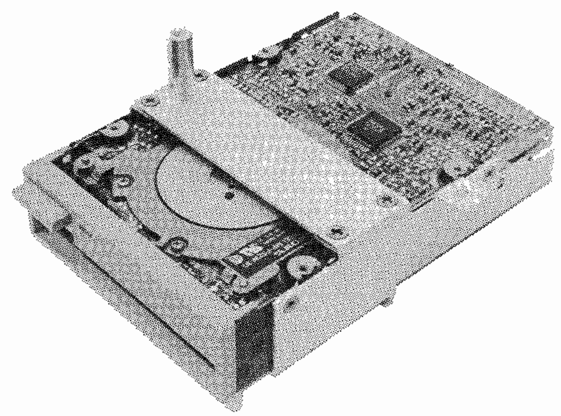


Figure 6-2. Disc Drive Assembly

Table 6-1. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	J	= electrical connector (stationary portion); jack	TB	= terminal board
B	= fan; motor	L	= coil; inductor	TP	= test point
BT	= battery	MP	= misc. mechanical part	U	= integrated circuit; microcircuit
C	= capacitor	P	= electrical connector (movable portion); plug	V	= electron tube; glow lamp
CR	= diode; diode thyristor; varactor	Q	= transistor; SCR; triode thyristor	VR	= voltage regulator; breakdown diode
DL	= delay line	R	= resistor	W	= cable
DS	= annunciator; lamp; LED	RT	= thermistor	X	= socket
E	= misc electrical part	S	= switch; jumper	Y	= crystal unit (piezo-electric or quartz)
F	= fuse	T	= transformer		
FL	= filter				
H	= hardware				

ABBREVIATIONS

A	= amperes
AC	= alternating current
ADD	= address
ADJ	= adjust, adjustment
AL	= aluminum
AR	= as required
ASM	= algorithmic state machine
ASSY	= assembly
B	= base
BCD	= binary coded decimal
BeCu	= beryllium copper
BIN	= binary
BLK	= black
BLU	= blue
BP	= band pass
BRN	= brown
BRS	= brass
BTU	= British thermal unit
C	= collector
CATH	= cathode
CCW	= counterclockwise
CD PL	= cadmium plate
CER	= ceramic
CERMET	= ceramic met flm
CKTS	= circuits
C FLM	= carbon film
CLK	= clock
CLR	= clear
CMOS	= complementary metal oxide semiconductor logic
COM	= common
COML	= commercial
COMP	= composition
COMPL	= complete
COND	= conductor
CONN	= connector
CONT	= contact
CPRSN	= compression
CTL	= complementary-transistor logic
CW	= clockwise
D	= diameter
DC	= direct current
DEPC	= deposited carbon
DIA	= diameter
DIP	= dual in-line package
DPDT	= double-pole, double-throw
DPST	= double-pole, single-throw
DR	= drive
DRVR	= driver
DSPL	= display
DTL	= diode-transistor logic
E	= emitter
ECL	= emitter-coupled logic
ELECT	= electrolytic
ENCAP	= encapsulated
EXT	= external
EXTR	= extractor
F	= female, farads
FF	= flip-flop
FLM	= film
FRNT	= front
FXD	= fixed
G	= giga (10^9)
GE	= germanium
GL	= glass
GND	= ground(ed)
GP	= General Purpose
GRA	= gray
GRN	= green
H	= henries
HDW	= hardware
HEX	= hexagon, hexagonal, six
HP	= high pass
HR	= hour(s)
HZ	= Hertz
IC	= integrated circuit
ID	= inside diameter
IF	= intermediate frequency
IN.	= inch, inches
INCAND	= incandescent
INCL	= include(s)
INSUL	= insulation, insulated
INT	= internal
INTL	= internal
K	= kilo (10^3), kilohm
LED	= light emitting diode
LFT	= left
LG	= long
LH	= lefthand
LKWR	= lockwasher
LP	= low pass
LS	= low power Schottky
LSB	= least significant bit
M	= milli (10^{-3}), male, mega (10^6), megohm
MET FLM	= metal film
MET OX.	= metal oxide
MHZ	= megahertz
MFR	= manufacturer
MINTR	= miniature
MISC	= miscellaneous
MOM	= momentary
MOS	= metal oxide semiconductor
MSB	= most significant bit
MTCHD	= matched
MTG	= mounting
MTLC	= metallic
N	= nano (10^{-9})
N.C.	= normally closed, no connection
NE	= neon
NO.	= number
N.O.	= normally open
NP	= No Polarity
NPN	= negative-positive-negative
NPO	= negative-positive zero (zero temperature coefficient)
NRFR	= not recommended for field replacement
NS	= normally shorting, nanosecond
NSR	= not separately replaceable
NYL	= nylon
OBD	= order by description
OD	= outside diameter
ORN	= orange

Table 6-1. Reference Designations and Abbreviations (cont)

ABBREVIATIONS

P	=	pico (10^{-12})	RVT	=	rivet	TRN	=	turn
PC	=	printed circuit	RWV	=	reverse working voltage	TTL	=	transistor-transistor logic
PCA	=	printed-circuit assembly				TYP	=	typical
PF	=	picofarad	S	=	second			
PIV	=	Peak Inverse Voltage	SB	=	slow blow	U (μ)	=	micro (10^{-6})
PK	=	peak	SCR	=	silicon controlled rectifier	UF	=	microfarad
PNL	=	panel	SE	=	selenium	US	=	microseconds
PNP	=	positive-negative-positive	SGL	=	single			
P-P	=	peak-to-peak	SI	=	silicon	V	=	volt(s)
PPM	=	parts per million	SHK	=	shank	VAR	=	variable
POLYC	=	polycarbonate	SIP	=	single in-line package	VCO	=	voltage controlled oscillator
POLYE	=	polyethylene	SKT	=	socket			
POLYSTY	=	polystyrene	SLDR	=	solder	VDCW	=	direct current working volts
PORC	=	porcelain	SPCG	=	spacing	VIO	=	violet
POSN	=	position(s)	SPDT	=	single-pole, double-throw	VNP	=	no polarity voltage
POZI	=	pozidrive	SPST	=	single-pole, single-throw			
PRV	=	peak reverse voltage	SST	=	stainless-steel	W	=	watts
PWV	=	peak working voltage	STL	=	steel	WT	=	weight
P/O	=	part of	SZ	=	size	WW	=	wirewound
						WHT	=	white
R	=	ring	T	=	tip	WIP	=	wiper
RAM	=	random access memory	TA	=	tantalum	WIV	=	working inverse voltage
ROM	=	read only memory	TEL	=	telephone	WSHR	=	washer
RECT	=	rectifier	T.C.	=	Temp. Compensated, temp. coefficient			
RF	=	radio frequency				X	=	times, multiple
RH	=	right hand	THKNS	=	thickness			
RMS	=	root-mean-square	TI	=	titanium	YEL	=	yellow
RND	=	round	TGL	=	toggle			
RT	=	right hand	THD	=	thread	ZNR	=	zener
RTL	=	resistor-transistor logic	THK	=	thick			
RTNT	=	retainer	TOL	=	tolerance	ϕ	=	phi, phase
RTRY	=	rotary	TRMR	=	trimmer			

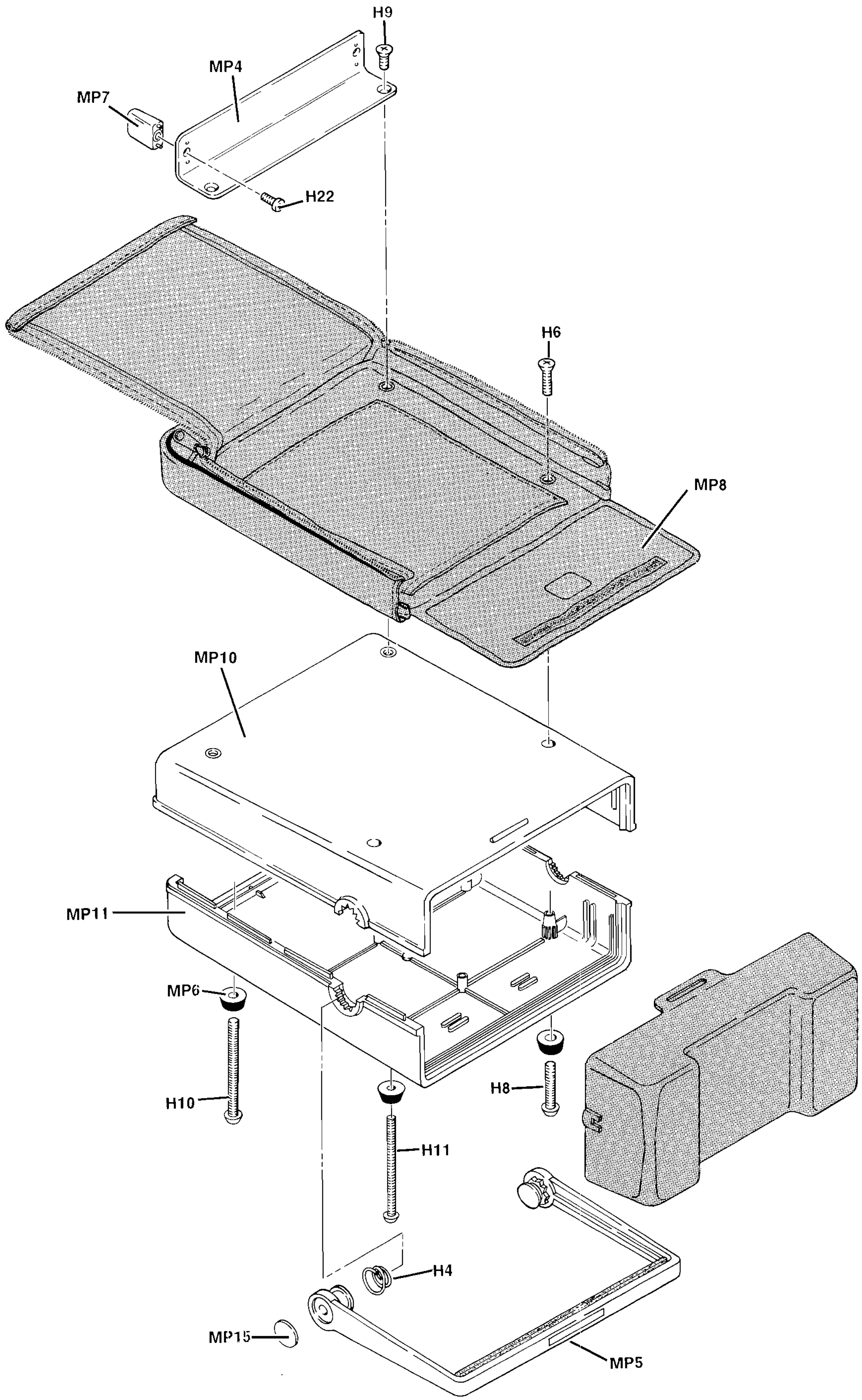


Figure 6-3. Case and Covers Assembly Exploded View

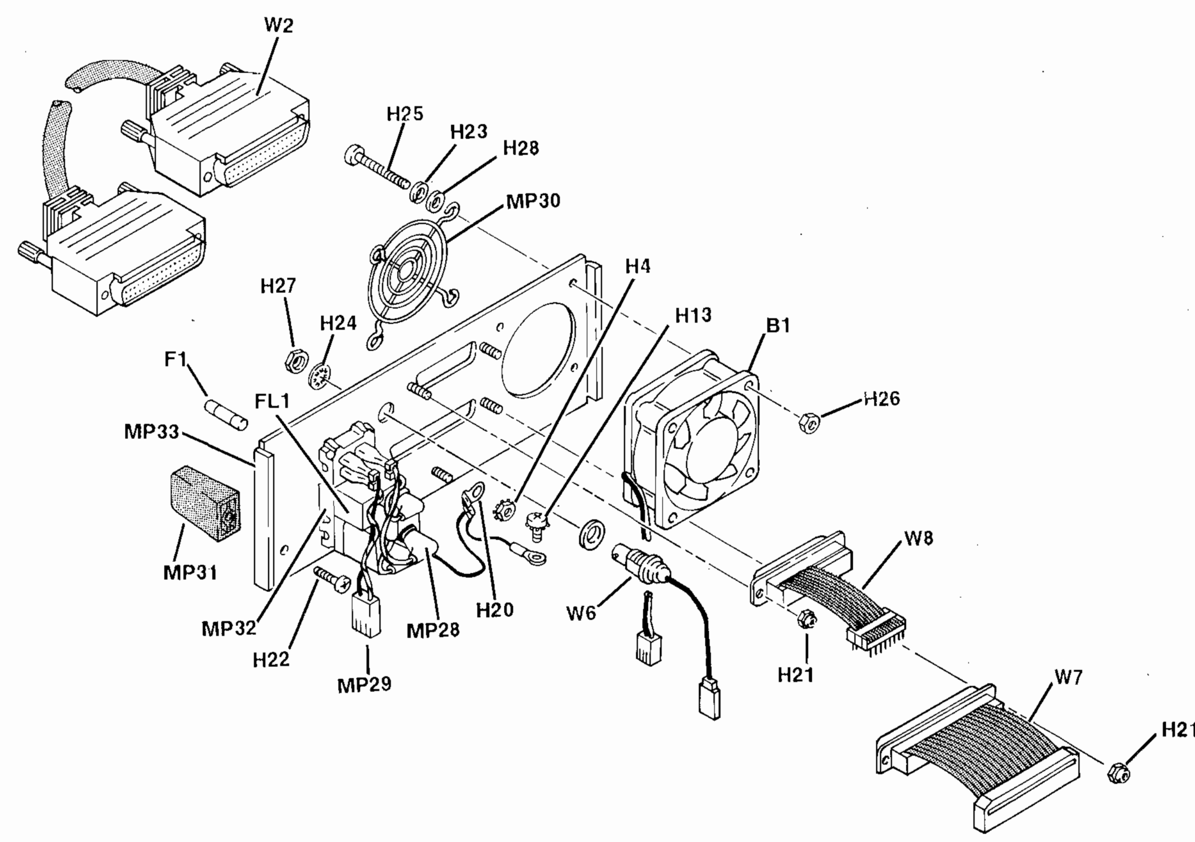


Figure 6-4. Rear Panel Assembly Exploded View

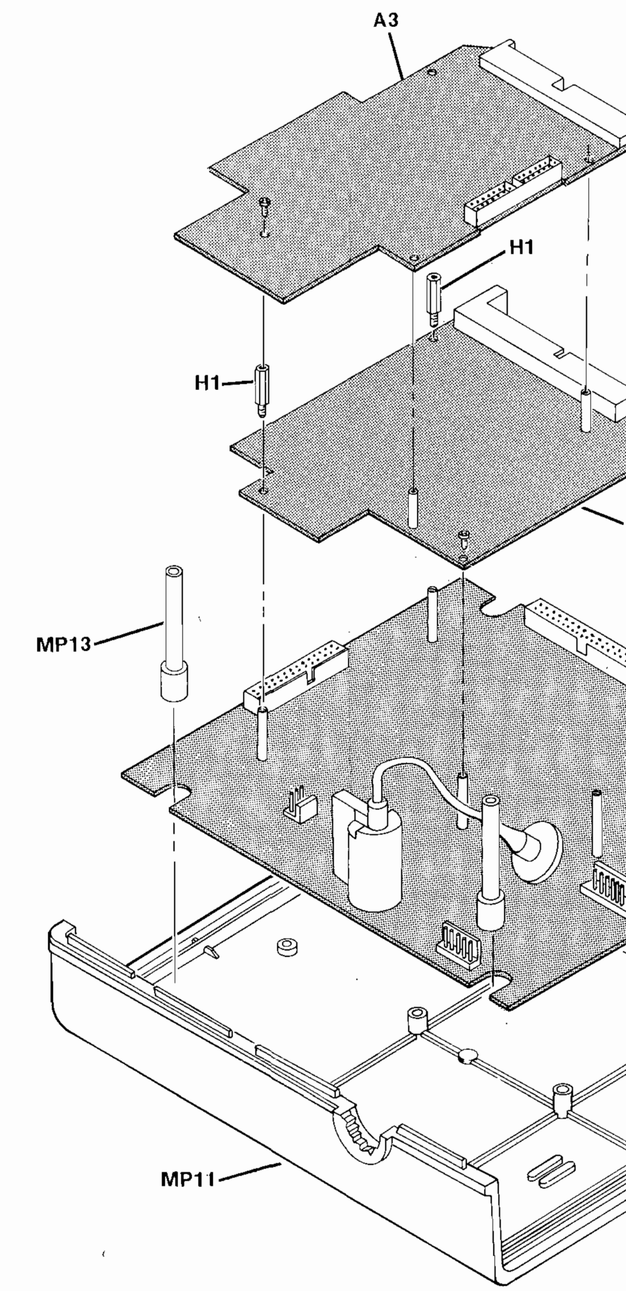
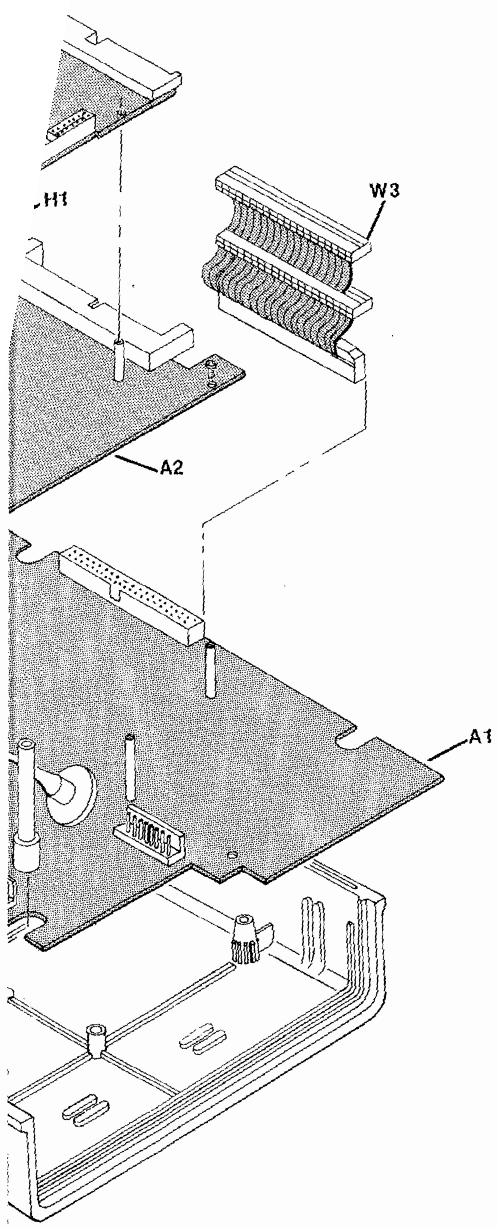


Figure 6-5. Internal Assembly Explod



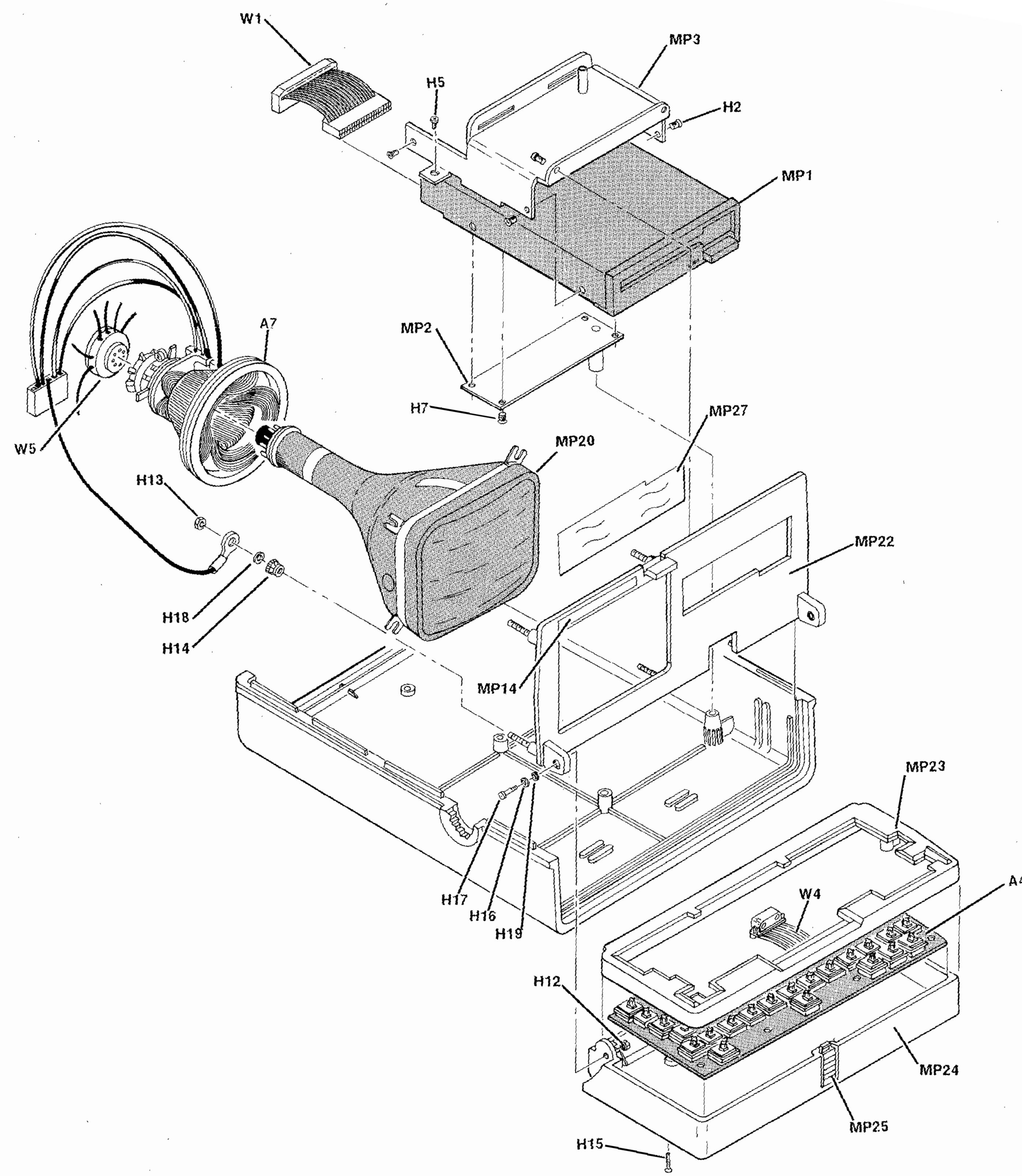


Figure 6-6. Front Panel Assembly Exploded View

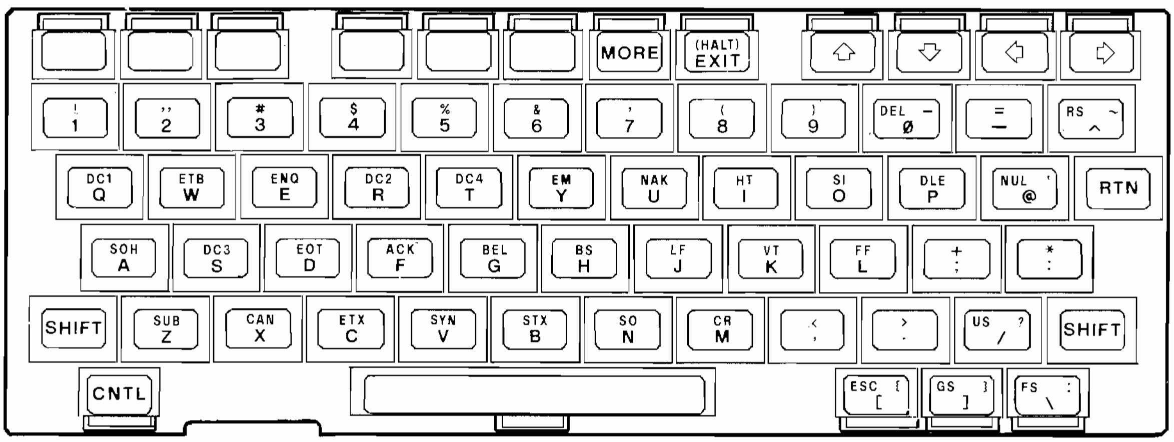


Figure 6-7. Keyboard Exploded View

Table 6-2. Manufacturer's Code List

Mfr Code	Manufacturer Name	Address	Zip Code
C0633	RIFA	BROMMA SE	
S0166	FUJI KOHKI LTD	JP	
S0482	SONY CORP	TOKYO JP	141
S4013	HITACHI AMERICA LTD	SUNNYVALE CA US	94086
S4307	SCHAFFNER AG	LUTERBACH SW	
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO INC	EL PASO TX US	79935
01295	TEXAS INSTRUMENTS INC	DALLAS TX US	75265
01456	MICROWAVE DEVELOPMENT LABS INC	NEEDHAM HTS MA	02194
01961	PULSE ENGINEERING INC	SAN DIEGO CA	92111
03888	K D I PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA INC SEMI-COND PROD	PHOENIX AZ US	85008
05791	LYN-TRON INC	BURBANK CA US	91505
07047	MILTON ROSS CO	SOUTHHAMPTON PA	18966
07263	FAIRCHILD CORP	MOUNTAIN VIEW CA US	94042
07653	FIDELITY CHEMICAL PRODUCTS CO	NEWARK NJ	07114
08806	GE CO MINIATURE LAMP PROD DEPT	CLEVELAND OH	44112
18546	VARO SEMICONDUCTOR INC	GARLAND TX US	75046
11236	CTS CORP BERNE DIV	BERNE IN US	46711
15454	AMETEK INC RODAN DIV	ANAHEIM CA US	92806
16299	CORNING ELECTRONICS	RALEIGH NC US	27604
17856	SILICONIX INC	SANTA CLARA CA	95054
19209	GE CO ELEK CAP & BAT PROD DEPT	GAINSVILLE FL	32601
19701	MEPCO/CENTRALAB INC	WEST PALM BEACH FL US	33407
22526	DUPONT CONNECTOR SYSTEMS	CAMP HILL PA US	17011
24546	CORNING ELECTRONICS	SANTA CLARA CA US	95050
25403	NV PHILIPS ELCOMA DEPT	EINDHOVEN HL	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA CA US	95052
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
34344	MOTOROLA INC	FRANKLIN PARK IL US	60131
34371	HARRIS CORP	MELBOURNE FL US	32901
34649	INTEL CORP	SANTA CLARA CA US	95054
51642	CENTRE ENGINEERING INC	STATE COLLEGE PA	16801
52840	WESTERN DIGITAL CORP	NEWPORT BEACH CA	92626
55322	SAMTEC	NEW ALBANY IN	47150
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
71400	COOPER INDUSTRIES/BUSSMANN	ELLISVILLE MO US	63021
72982	ERIE TECHNOLOGICAL PRODUCTS INC	ERIE PA	16512
73138	BECKMAN INDUSTRIAL CORP	FULLERTON CA US	92632
76385	MINOR RUBBER CO INC	BLOOMFIELD NJ	07003
83701	ELECTRONIC DEVICES INC	YONKERS NY	10710
9M011	INTL RECTIFIER CORP	EL SEGUNDO CA US	90245
9N171	UNITRODE CORP	LEXINGTON MA US	02173
91637	DALE ELECTRONICS INC	EL PASO TX US	79936

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	04951-60701	8	1	MAIN BOARD ASSEMBLY	28480	04951-60701
A1C1	0180-3377	2	2	CAPACITOR-FXD 47UF+-20% 50VDC AL	28480	0180-3377
A1C2	0160-5863	3	1	CAPACITOR-FXD 330PF +-1% 100VDC CER	16299	CAC02C0G331F100A
A1C3	0160-4567	2	1	CAPACITOR-FXD 3900PF +-1% 100VDC CER	28480	0160-4567
A1C4	0160-3879	7	12	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C6	0160-6684	8	1	CAPACITOR-FXD .15UF +-10% 250VAC(RMS)	C0633	PME 271 M 615
A1C7	0160-4810	8	3	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A1C8	0160-0576	5	4	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C9	0160-3508	9	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C10	0160-3878	6	1	CAPACITOR-FXD 1000PF +-20% 100VDC CER	28480	0160-3878
A1C14	0160-5298	8	21	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C20	0160-5332	1	8	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C21	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A1C22	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1C23	0160-4811	9	1	CAPACITOR-FXD 270PF +-5% 100VDC CER	28480	0160-4811
A1C24	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C25	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C26	0160-4807	3	5	CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A1C27	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A1C28	0180-3641	3	1	CAPACITOR-FXD 1000UF+-20% 10VDC AL	28480	0180-3641
A1C29	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C31	0180-3814	2	1	CAPACITOR-FXD 150UF+-20% 400VDC AL	28480	0180-3814
A1C32	0160-4810	8		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-4810
A1C33	0180-3643	5	2	CAPACITOR-FXD 470UF+-20% 25VDC AL	28480	0180-3643
A1C34	0180-3858	4	1	CAPACITOR-FXD 470UF+-20% 35VDC AL	28480	0180-3858
A1C35	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C36	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C37	0180-3643	5		CAPACITOR-FXD 470UF+-20% 25VDC AL	28480	0180-3643
A1C38	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A1C39	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C40	0160-4808	4	2	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
A1C41	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C43	0180-0491	5	1	CAPACITOR-FXD 10UF+-20% 25VDC TA	28480	0180-0491
A1C44	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A1C45	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C46	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C47	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C48	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C49	0160-0996	3	1	CAPACITOR-FXD .01UF +-20% 2KVDC CER	72982	828-012-Z5U0-103M
A1C50	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C51	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C52	0160-4953	0	2	CAPACITOR-FXD .027UF +-5% 50VDC CER	28480	0160-4953
A1C53	0160-4370	5	1	CAPACITOR-FXD 1000PF +-5% 200VDC CER	51642	200-200-NP0-102J
A1C54	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C55	0160-4788	9	1	CAPACITOR-FXD 18PF +-5% 100VDC CER 0+-30	28480	0160-4788
A1C56	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C57	0180-3859	5	1	CAPACITOR-FXD 1000UF+-20% 35VDC AL	28480	0180-3859
A1C58	0160-4663	9	3	CAPACITOR-FXD 2.2UF +80-20% 100VDC CER	28480	0160-4663
A1C59	0160-4663	9		CAPACITOR-FXD 2.2UF +80-20% 100VDC CER	28480	0160-4663
A1C60	0180-3377	2		CAPACITOR-FXD 47UF+-20% 50VDC AL	28480	0180-3377
A1C61	0160-5304	7	1	CAPACITOR-FXD 8.2PF +-10% 200VDC CER	28480	0160-5304
A1C62	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A1C63	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100VDC CER 0+-30	28480	0160-4807
A1C64	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C65	0180-3071	1	1	CAPACITOR-FXD 10UF +-10% 100VDC	01456	17UB106K
A1C66	0160-4953	0		CAPACITOR-FXD .027UF +-5% 50VDC CER	28480	0160-4953
A1C67	0160-4579	6	1	CAPACITOR-FXD .1UF +-5% 160VDC MET-POLYC	28480	0160-4579
A1C68	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C69	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C70	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C71	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C72	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C73	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C74	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C75	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C76	0160-0128	3	1	CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-0128
A1C77	0160-4663	9		CAPACITOR-FXD 2.2UF +80-20% 100VDC CER	28480	0160-4663
A1C78	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C79	0160-4804	0	2	CAPACITOR-FXD 56PF +-5% 100VDC CER 0+-30	28480	0160-4804
A1C80	0170-0040	9	1	CAPACITOR-FXD .047UF +-10% 200VDC POLYE	56289	292P47392
A1C81	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C82	0160-4230	6	3	CAPACITOR-FXD .01UF +80-20% 1KVDC CER	28480	0160-4230
A1C83	0180-0291	3	1	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C84	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C85	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A1C86	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
A1C87	0160-4804	0		CAPACITOR-FXD 56PF +-5% 100VDC CER 0+-30	28480	0160-4804
A1C88	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C89	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	28480	0160-4230
A1C90	0160-4230	6		CAPACITOR-FXD .01UF +80-20% 1KVDC CER	28480	0160-4230
A1C91	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C92	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C93	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1C94	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A1CR1	1902-1344	2	1	DIODE-ZNR 4.3V 2% DO-35 PD=.25W	28480	1902-1344
A1CR2	1902-0202	9	1	DIODE-ZNR 15V 5% PD=1W IR=5UA	28480	1902-0202
A1CR3	1901-1080	1	3	DIODE-SCHOTTKY 20V 1A	04713	1N5817(RELAXED)
A1CR4	1901-1173	3	2	DIODE-PWR-S 45V 7.5A TO-220AC	04713	MBR745
A1CR5	1901-0871	6	2	DIODE-PWR RECT 150V 2.5A 25NS	28480	1901-0871
A1CR6	1902-3063	6	1	DIODE-ZNR 3.92V 2% DO-35 PD=.4W	28480	1902-3063
A1CR7	1902-3105	7	1	DIODE-ZNR 5.62V 2% DO-35 PD=.4W	28480	1902-3105
A1CR8	1902-3191	1	1	DIODE-ZNR 13V 2% DO-35 PD=.4W TC=+.06%	28480	1902-3191
A1CR9	1902-0244	9	1	DIODE-ZNR 30V 5% PD=1W IR=5UA	28480	1902-0244
A1CR10	1901-1080	1		DIODE-SCHOTTKY 20V 1A	04713	1N5817(RELAXED)
A1CR11	1901-1164	2	5	DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A1CR12	1901-1223	4	1	DIODE-HV RECT 600V 1.6A 100NS	25403	BYV36C
A1CR13	1901-0919	3	1	VOLTAGE SUPPRESSOR VRM=287V	28480	1901-0919
A1CR14	1901-0871	6		DIODE-PWR RECT 150V 2.5A 25NS	28480	1901-0871
A1CR15	1901-1141	5	1	DIODE-SWITCHING 200V 2A 25NS	25403	BYV27-200
A1CR16	1901-1080	1		DIODE-SCHOTTKY 20V 1A	04713	1N5817(RELAXED)
A1CR17	1902-3169	3	1	DIODE-ZNR 10.7V 2% DO-35 PD=.4W	28480	1902-3169
A1CR18	1901-0896	5	1	DIODE-PWR RECT 600V 1A 250NS	83701	RC60
A1CR19	1901-0845	4	1	DIODE-HV RECT 2KV 50MA 250NS	1B546	VG-2X
A1CR20	1901-1173	3		DIODE-PWR-S 45V 7.5A TO-220AC	04713	MBR745
A1CR21	1902-0080	1	1	DIODE-ZNR 14.7V 2% DO-14 PD=.4W TC=+.08%	28480	1902-0080
A1CR22	1901-1179	9	1	DIODE-SCHOTTKY 40V 1A	28480	1901-1179
A1CR23	1901-1105	1	2	DIODE-HV RECT 1KV 50MA	1B546	VB10X
A1CR24	1902-3323	1	1	DIODE-ZNR 42.2V 5% DO-35 PD=.4W TC=+.08%	28480	1902-3323
A1CR25	1901-1105	1		DIODE-HV RECT 1KV 50MA	1B546	VB10X
A1CR27	1901-1164	2		DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A1CR28	1901-0692	9	1	DIODE-PWR RECT 200V 3A 200NS	04713	MR852
A1CR29	2140-0013	5	1	LAMP-GLOW 5AB-A 70/57VDC 300UA T-2-BULB	08806	5AB-A(NE-23A)
A1CR30	1901-1164	2		DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A1CR31	1901-1164	2		DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A1CR32	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1901-0518
A1CR33	1902-0949	1	1	DIODE-ZNR 4.3V 5% DO-35 PD=.4W TC=+.017%	28480	1902-0949
A1CR34	1901-1164	2		DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A1CR35	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1901-0518
A1CR36	1902-3092	1	1	DIODE-ZNR 4.99V 2% DO-35 PD=.4W	28480	1902-3092
A1CR810	1906-0074	1	2	DIODE-ARRAY 50V 400MA	07263	FSA3157P
A1CR811	1906-0074	1		DIODE-ARRAY 50V 400MA	07263	FSA3157P

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1E208	1251-8360	5	25	CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E307	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E307	1258-0209	9	13	JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E308	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E308	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E309	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E309	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E314	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E314	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E404	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E404	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E406	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E406	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E407	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E407	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E408	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E408	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E409	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E409	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E410	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E410	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E606	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E606	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E609	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E707	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E707	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1E810	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E810	1258-0217	9	1	JUMPER 8 GOLD PLTD PHOSPHOR BRONZE	28480	1258-0217
A1E815	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1E815	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A1J1	1251-5595	2	1	POLARIZING KEY-POST CONN	28480	1251-5595
A1J1	1251-8827	9	1	CONN-POST TYPE .100-PIN-SPCG 60-CONT	28480	1251-8827
A1J2	1251-8828	0	1	CONN-POST TYPE .100-PIN-SPCG 40-CONT	28480	1251-8828
A1J3	1251-3825	7	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-3825
A1J4	1251-3751	8	1	CONNECTOR 8-PIN M POST TYPE	28480	1251-3751
A1J5	1251-4246	8	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-4246
A1K208	0490-1320	8	1	RELAY 4A 5VDC-COIL 4A 250VAC	28480	0490-1320
A1L1	9140-1209	0	1	INDUCTOR-FIXED LOC(PINS 1-2): 4 MH MIN	01961	PE 64590
A1L2	9140-1188	4	1	INDUCTOR-FIXED L:70 UH (TYP); L(NO D.C.)	01961	92104K
A1L3	9140-1192	0	2	INDUCTOR - 330 UH 1 AMP	28480	9140-1192
A1L4	9140-1192	0		INDUCTOR - 330 UH 1 AMP	28480	9140-1192
A1L5	9100-1788	6	1	CORE-FERRITE CHOKE-WIDEBAND;IMP:>680	28480	9100-1788
A1L6	9140-1069	0	1	INDUCTOR-FIXED L(TYP):25 UH; L(NO D.C.)	01961	92100
A1L7	9140-0407	8	1	COIL-VAR 10UH-40UH PC-MTG	28480	9140-0407
A1L8	9140-0319	1	1	INDUCTOR-FIXED LINEARITY; DEFL CURRENT	28480	9140-0319
A1LS916	9164-0235	0	1	AUDIO TRANSDUCER PIEZO CERAMIC TYPE; 50V	28480	9164-0235
A1LUG1	0590-1054	7	1	THREADED INSERT-NUT 6-32 .065-IN-LG SST	28480	0590-1054
A1Q101	1853-0459	3	2	TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
A1Q102	1855-0082	2	1	TRANSISTOR J-FET P-CHAN D-MODE SI	28480	1855-0082
A1Q103	1854-1028	6	5	TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A1Q105	1826-0282	3	1	IC V RGLTR TO-92	04713	MC79L12ACP
A1Q106	1855-0509	8	4	TRANSISTOR MOSFET P-CHAN E-MODE TO-220	9M011	IRF9520
A1Q107	1855-0509	8		TRANSISTOR MOSFET P-CHAN E-MODE TO-220	9M011	IRF9520
A1Q108	1854-1028	6		IC V RGLTR-V-REF-ADJ 3/30V TO-92 PKG	28480	1826-0643
A1Q109	1855-0525	8	1	TRANSISTOR MOSFET N-CHAN E-MODE SI	17856	VN0300M
A1Q204	1855-0679	3	1	TRANSISTOR MOSFET N-CHAN E-MODE TO-220	25403	BUZ80A
A1Q205	1854-1028	6		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A1Q206	1884-0293	8	1	THYRISTOR-SCR	04713	MCR69-2
A1Q207	1853-0459	3		TRANSISTOR PNP SI PD=625MW FT=200MHZ	28480	1853-0459
A1Q307	1854-1028	6		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A1Q405	1855-0509	8		TRANSISTOR MOSFET P-CHAN E-MODE TO-220	9M011	IRF9520
A1Q406	1855-0509	8		TRANSISTOR MOSFET P-CHAN E-MODE TO-220	9M011	IRF9520

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1Q407	1826-0276	5	1	IC 78L05A V RGLTR TO-92	04713	MC78L05ACP
A1Q604	1855-0524	7		TRANSISTOR MOSFET N-CHAN E-MODE TO-220	9M011	IRF640
A1Q605	1854-1028	6		TRANSISTOR NPN SI TO-92 PD=350MW	04713	2N3904
A1Q606	1854-0659	7	1	TRANSISTOR NPN SI PD=12.5W FT=50MHZ	04713	MJE180
A1Q607	1853-0436	6	1	TRANSISTOR PNP SI PD=1.5W FT=50MHZ	04713	MJE170
A1Q702	1853-0536	7	1	TRANSISTOR PNP SI TO-92 PD=350MW	04713	MPS6534
A1Q704	1854-0730	5	2	TRANSISTOR NPN SI TO-92	04713	MPS6531
A1Q708	1826-0285	6	1	IC V RGLTR TO-92	04713	MC79L05C
A1Q804	1854-0730	5		TRANSISTOR NPN SI TO-92	04713	MPS6531
A1R1	0757-0280	3	9	RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R2	0698-3452	1	1	RESISTOR 147K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1473-F
A1R3	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
A1R4	0698-3155	1	1	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-4641-F
A1R5	0683-4705	8	1	RESISTOR 47 5% .25W CF TC=0-400	01121	CB4705
A1R6	0698-3446	3	1	RESISTOR 383 1% .125W F TC=0+-100	24546	CT4-1/8-T0-383R-F
A1R7	0683-0335	2	2	RESISTOR 3.3 5% .25W CF TC=0-400	01121	CB33G5
A1R8	0683-0335	2		RESISTOR 3.3 5% .25W CF TC=0-400	01121	CB33G5
A1R9	8110-0046	7	2	WIRE-RES 1.852-OHM/FT .0126-DIA	28480	8110-0046
A1R10	0698-3150	6	1	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2371-F
A1R11	0698-3157	3	1	RESISTOR 19.6K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1962-F
A1R12	0757-0442	9	9	RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R13	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	CT4-1/8-T0-51R1-F
A1R14	0757-0465	6	6	RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R15	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R16	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R17	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	5033R-1/8-T0-9091-F
A1R18	0757-0444	1	1	RESISTOR 12.1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1212-F
A1R19	0698-8827	4	1	RESISTOR 1M 1% .125W F TC=0+-100	28480	0698-8827
A1R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R21	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R22	0757-0463	4	1	RESISTOR 82.5K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-8252-F
A1R23	0837-0359	7	1	THERMISTOR DISC 33-OHM TC=+15%/C-DEG	28480	0837-0359
A1R24	0837-0252	9	1	THERMISTOR-SURGE PTCTR 20 OHM AT 25 DEG	15454	SG230
A1R25	0757-0145	9	2	RESISTOR 750K 1% .25W F TC=0+-100	19701	5043R-1/4-T0-7503-F
A1R26	0757-0145	9		RESISTOR 750K 1% .25W F TC=0+-100	19701	5043R-1/4-T0-7503-F
A1R27	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R28	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2611-F
A1R29	8110-0046	7		WIRE-RES 1.852-OHM/FT .0126-DIA	28480	8110-0046
A1R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R31	0698-3450	9	1	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-4222-F
A1R32	0698-3158	4	2	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2372-F
A1R33	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-6192-F
A1R34	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R35	0757-0458	7	2	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-5112-F
A1R36	0757-0199	3	2	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2152-F
A1R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R37	0757-0458	7		RESISTOR 51.1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-5112-F
A1R38	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	CT4-1/8-T0-511R-F
A1R40	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R41	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
A1R42	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R43	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R44	0698-3430	5	1	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A1R45	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R46	0757-0290	5	1	RESISTOR 6.19K 1% .125W F TC=0+-100	19701	5033R-1/8-T0-6191-F
A1R47	0757-0401	0	4	RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-T0-101-F
A1R48	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2152-F
A1R49	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R50	0698-3154	0	1	RESISTOR 4.22K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-4221-F
A1R51	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	CT4-1/8-T0-751-F
A1R52	0698-3389	3	1	RESISTOR 17.8 1% .5W F TC=0+-100	28480	0698-3389
A1R53	0757-0797	7	1	RESISTOR 90.9 1% .5W F TC=0+-100	28480	0757-0797
A1R54	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	28480	0757-0346
A1R55	0757-0279	0	1	RESISTOR 3.16K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-3161-F

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R56	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R57	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-T0-101-F
A1R58	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R59	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R60	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-T0-101-F
A1R61	0698-0084	9	1	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2151-F
A1R62	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R63	0698-3161	9	2	RESISTOR 38.3K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-3832-F
A1R64	0698-3161	9		RESISTOR 38.3K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-3832-F
A1R65	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	CT4-1/8-T0-51R1-F
A1R66	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R67	0698-7842	1	1	RESISTOR 26.1K .1% .125W F TC=0+-25	19701	5033R-1/8-T9-2612-B
A1R68	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A1R69	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	CT4-1/8-T0-101-F
A1R70	0698-3158	4		RESISTOR 23.7K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-2372-F
A1R71	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A1R72	0686-1045	9	3	RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A1R73	0686-1045	9		RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A1R74	0686-1045	9		RESISTOR 100K 5% .5W CC TC=0+882	01121	EB1045
A1R75	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A1R76	0698-4479	4	1	RESISTOR 14K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1402-F
A1R101	1810-0985	0	4	NETWORK-RES 6-SIP 52.0K OHM X 5	91637	CSC6A-02-5202F
A1R102	1810-0985	0		NETWORK-RES 6-SIP 52.0K OHM X 5	91637	CSC6A-02-5202F
A1R103	1810-0985	0		NETWORK-RES 6-SIP 52.0K OHM X 5	91637	CSC6A-02-5202F
A1R104	1810-0985	0		NETWORK-RES 6-SIP 52.0K OHM X 5	91637	CSC6A-02-5202F
A1R105	1810-0224	0	1	NETWORK-RES 8-SIP 33.0K OHM X 4	11236	750-83-R33K
A1R106	1810-0445	7	1	NETWORK-RES 6-SIP100.0 OHM X 3	11236	750-63-R100
A1R107	1810-0986	1	2	NETWORK-RES 6-SIP MULTI-VALUE	91637	CSC06-00-S28
A1R108	1810-0986	1		NETWORK-RES 6-SIP MULTI-VALUE	91637	CSC06-00-S28
A1R210	1810-0280	8	3	NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A1R213	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A1R310	1810-0406	0	5	NETWORK-RES 8-SIP 10.0K OHM X 4	11236	750-83-R10K
A1R414	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A1R505	2100-3908	9	1	RESISTOR-TRMR 1M 10% CC TOP-ADJ 1-TRN	28480	2100-3908
A1R506	2100-3966	9	1	RESISTOR-TRMR 200K 10% C TOP-ADJ 1-TRN	28480	2100-3966
A1R516	1810-0368	3	3	NETWORK-RES 6-SIP 10.0K OHM X 5	11236	750-61-R10K
A1R609	1810-0368	3		NETWORK-RES 6-SIP 10.0K OHM X 5	11236	750-61-R10K
A1R708	2100-3096	6	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 17-TRN	28480	2100-3096
A1R709	2100-3089	7	1	RESISTOR-TRMR 5K 10% C TOP-ADJ 17-TRN	28480	2100-3089
A1R809	1810-0368	3		NETWORK-RES 6-SIP 10.0K OHM X 5	11236	750-61-R10K
A1R813	1810-0281	9	1	NETWORK-RES 10-SIP 100.0K OHM X 9	91637	CSC10A01-104G/MSP10A01-
A1R909	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	11236	750-83-R10K
A1R910	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	11236	750-83-R10K
A1R911	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	11236	750-83-R10K
A1R912	1810-0406	0		NETWORK-RES 8-SIP 10.0K OHM X 4	11236	750-83-R10K
A1T201	04951-62702	3	1	XFMR/FOIL ASSY	28480	04951-62702
A1T405	9140-1189	5	1	INDUCTOR-FIXED L: 49 UH MIN; FREQ: 10	01961	PE-52619
A1T501	9100-4568	6	1	TRANSFORMER-FLYBACK CABLE LENGTH BODY TO	28480	9100-4568
A1TP102	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP202	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP205	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP308	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP309	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP408	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP606	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP708	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1TP715	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1U102	1826-1545	3	1	IC V RGLTR-SWG 8-DIP-P PKG	9N171	UC2842N
A1U105	1826-1256	3	2	IC V RGLTR-SWG 8-DIP-P PKG	28480	1826-1256
A1U111	1820-3350	0	1	IC MUXR/DATA-SEL CMOS/74HC 4-TO-1-LINE	27014	MM74HC153N
A1U112	1820-3007	4	2	IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	04713	MC74HC86N
A1U113	1820-3185	9	1	IC SCHMITT-TRIG CMOS/74HC INV HEX	27014	MM74HC14N
A1U114	1820-3208	7	1	IC CNTR CMOS/74HC BIN ASYNCHRO	27014	MM74HC393N
A1U115	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	04713	MC74HC86N
A1U209	1820-3515	9	1	IC-SERIAL COMMUNICATIONS CONTROLLER 6MHZ	07653	Z8530ACS
A1U211	1820-3082	5	5	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A1U212	1820-3082	5		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U213	1820-2921	9		IC INV CMOS/74HC HEX	27014	MM74HC04N
A1U214	1820-2924	2	1	IC GATE CMOS/74HC NOR QUAD 2-INP	04713	MC74HC02N
A1U215	1820-2998	0	2	IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A1U306	1826-1256	3		IC V RGLTR-SWG 8-DIP-P PKG	28480	1826-1256
A1U311	1820-3081	4	3	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC74N
A1U312	1820-3791	3	1	IC BFR CMOS/74HC INV HEX	27014	MM74HC368N
A1U313	1820-3079	0	1	IC DCDR CMOS/74HC 3-TO-8-LINE	04713	MC74HC138N
A1U409	04952-10005	1	1	CRT CHAR ROM	28480	04952-10005
A1U411	1818-3183	2	1	IC CMOS 65536 (64K) STAT RAM 150-NS 3-S	S4013	HM6264LP-15
A1U412	1820-3082	5		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A1U413	1820-2998	0		IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A1U415	1820-3436	3	1	IC-8-BIT MICROPROCESSOR; 4MHZ CLOCK	27014	NSC800N-4
A1U507	1820-3373	7	1	IC MV CMOS/74HC MONOSTBL CLEAR DUAL	27014	MM74HC221AN
A1U510	1820-4116	8	1	IC GATE-ARY CMOS	S0166	C440H
A1U511	1820-2921	9		IC INV CMOS/74HC HEX	27014	MM74HC04N
A1U512	1820-3191	7	3	IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC257N
A1U513	1820-3191	7		IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC257N
A1U514	1820-4703	9	1	IC-PROGRAMMABLE CRT CONTROLLER, 4.5MHZ	S0166	MB89321
A1U515	1820-2889	8	1	IC GATE TTL ALS AND TPL 3-INP	01295	SN74ALS11N
A1U608	1826-1222	3	1	IC OP AMP H-SLEW-RATE QUAD 14-DIP-C PKG	28480	1826-1222
A1U611	5080-8573	3	1	VIDEO HYBRID	28480	5080-8573
A1U612	1820-3297	4	1	IC DRVR CMOS/74HC BUS OCTL	04713	MC74HC244N
A1U613	1820-3330	6	1	IC TRANSCEIVER CMOS/74HC BUS OCTL	27014	MM74HC245N
A1U615	1820-3196	2	1	IC GATE CMOS/74HC NOR DUAL 4-INP	04713	MC74HC4002N
A1U710	1820-3097	2	1	IC GATE CMOS/74HC AND QUAD 2-INP	27014	MM74HC08N
A1U711	1818-1738	9	1	IC CMOS 16384 (16K) STAT RAM 200-NS 3-S	S4013	HM6116LP-4
A1U712	1820-3082	5		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A1U713	1820-3191	7		IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC257N
A1U714	1820-3298	5	1	IC GATE CMOS/74HC OR QUAD 2-INP	27014	MM74HC32N
A1U715	1820-3081	4		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC74N
A1U716	1826-1439	4	1	IC MISC 8-DIP-P PKG	01295	TLC555CP
A1U805	1820-3674	1	1	IC BFR CMOS/74HC BUS QUAD	27014	MM74HC125N
A1U810	1820-2923	1	1	IC GATE CMOS/74HC NAND TPL 3-INP	04713	MC74HC10N
A1U812	1820-3082	5		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC374N
A1U814	1820-3552	4	1	IC-RAM I/O TIMER, 4 MHZ, I-TEMP RANGE	27014	NSC810AN-4I
A1U915	1820-3081	4		IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC74N
A1XL3	5080-8578	8	2	PC BD INSULATOR	28480	5080-8578
A1XL4	5080-8578	8		PC BD INSULATOR	28480	5080-8578
A1XU209	1200-0654	7	3	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU409	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A1XU415	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU814	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1Y1	0340-1136	7	3	SPACER-COMPONENT FOR FREQ CRYSTAL CANS	07047	10433-DAP
A1Y1	0410-1387	9	1	XTAL 3.6864MHZ	28480	0410-1387
A1Y2	0340-1136	7		SPACER-COMPONENT FOR FREQ CRYSTAL CANS	07047	10433-DAP
A1Y2	0410-1520	2	1	CRYSTAL-QUARTZ 8.064 MHZ HC-18/U-HLDR	28480	0410-1520
A1Y3	0340-1136	7		SPACER-COMPONENT FOR FREQ CRYSTAL CANS	07047	10433-DAP
A1Y3	0410-0733	7	1	CRYSTAL-QUARTZ 5.0688 MHZ HC-18/U-HLDR	28480	0410-0733
	0380-1883	5	4	STANDOFF-RVT-ON 1.125-IN-LG 6-32-THD	05791	BR6910B-1.125-43
	0590-0810	1	2	NUT-HEX-DBL-CHAM 4-40-THD .124-IN-THK	00000	ORDER BY DESCRIPTION
	0890-0025	6	1	SPIRAL WRAP .188-2-DIA POLYETH	28480	0890-0025
	2200-0105	4	2	SCREW-MACH 4-40 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2200-0704	9	2	SCREW-MACH 4-40 .375-IN-LG BDG-HD-SLT	00000	ORDER BY DESCRIPTION
	04951-20701	4	1	MAIN PC BD	28480	04951-20701
	2260-0009	3	2	NUT-HEX-W/LKWR 4-40-THD .094-IN-THK	00000	ORDER BY DESCRIPTION

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	04951-60708	5	1	KATAKANA MAIN BOARD ASSY	28480	04951-60708
	04951-80711	2	1	LABEL-60708	28480	04951-80711
				THE KATAKANA MAIN BOARD ASSEMBLY USES THE SAME PARTS AS THE 04951-60701 ASSEMBLY EXCEPT FOR ANY PARTS LISTED ABOVE.		

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	04951-60702	9	1	MEMORY BD ASSY	28480	04951-60702
A2B1	1420-0264	1	1	BATTERY 3.6V .065A-HR NI-CD PIN	19209	41B013AD00201 (DS3GT)
A2C1	0160-5298	8	9	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C1	0380-1489	7		SPACER-SNAP-IN .375 IN LG; .280 IN OD	28480	0380-1489
A2C2	0160-5332	1	7	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C3	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C5	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C7	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A2C8	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C9	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C10	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C11	0160-5332	1		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A2C12	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A2C13	0160-4535	4	2	CAPACITOR-FXD 1UF +-10% 50VDC CER	28480	0160-4535
A2C14	0160-4535	4		CAPACITOR-FXD 1UF +-10% 50VDC CER	28480	0160-4535
A2C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C18	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A2C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A2CR1	1901-1080	1	1	DIODE-SCHOTTKY 20V 1A	04713	1N5817(RELAXED)
A2CR2	1901-1164	2	1	DIODE-SWITCHING 80V 200MA 2NS DO-35	07263	FDH9838
A2E2	1251-8360	5	42	CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2E2	1258-0218	0	2	JUMPER 16 GOLD PLTD PHOSPHOR BRONZE	28480	1258-0218
A2E3	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2E3	1258-0218	0		JUMPER 16 GOLD PLTD PHOSPHOR BRONZE	28480	1258-0218
A2E5	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2E5	1258-0209	9	2	JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A2E6	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2E6	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A2J1	1251-8822	4	1	CONN-POST TYPE .100-PIN-SPCG 60-CONT	28480	1251-8822
A2J4	1200-0607	0	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A2R1	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1002-F
A2R2	0757-0461	2	1	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-6812-F
A2R3	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-6192-F
A2R4	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-5112-F
A2R5	0757-0403	2	1	RESISTOR 121 1% .125W F TC=0+-100	24546	CT4-1/8-T0-121R-F
A2R6	0683-1565	2	1	RESISTOR 15M 5% .25W CC TC=-900/+1200	01121	CB1565
A2R203	1810-0679	9	3	RES NETWK SIP 4	28480	1810-0679
A2R204	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A2R205	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A2R206	1810-0219	3	1	NETWORK-RES 8-SIP 220.0 OHM X 4	11236	750-83-R220
A2R207	1810-0368	3	1	NETWORK-RES 6-SIP 10.0K OHM X 5	11236	750-61-R10K
A2R208	1810-0206	8	1	NETWORK-RES 8-SIP 10.0K OHM X 7	11236	750-81-R10K
A2TP1	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2TP2	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2TP3	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2TP4	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A2U102	1826-0753	3	1	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A2U103	1826-0759	9	1	IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A2U106	1820-3176	8	1	IC MUXR/DATA-SEL CMOS/74HC 8-TO-1-LINE	27014	MM74HC151N
A2U107	1820-3177	9	1	IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC157N
A2U204	1820-3298	5	3	IC GATE CMOS/74HC OR QUAD 2-INP	27014	MM74HC32N

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2U205	1820-3298	5		IC GATE CMOS/74HC OR QUAD 2-INP	27014	MM74HC32N
A2U206	1820-3082	5	1	IC FF CMOS/74HC D-TYPE POS-EDGE TRIG	04713	MC74HC374N
A2U207	1820-1779	3	1	IC GEN CMOS	04713	MC14411P
A2U209	1820-3938	0	1	IC SER-XMTR/RCVR CMOS ASYNCHRO	S4013	HD6350P
A2U304	04951-10702	4	1	MEM PROM B	28480	04951-10702
A2U306	1820-3014	3	1	IC DCDR CMOS/74HC 2-TO-4-LINE DUAL	27014	MM74HC139N
A2U307	1820-3298	5		IC GATE CMOS/74HC OR QUAD 2-INP	27014	MM74HC32N
A2U308	1820-3097	2	1	IC GATE CMOS/74HC AND QUAD 2-INP	27014	MM74HC08N
A2U309	1820-3007	4	1	IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	04713	MC74HC86N
A2U310	1820-2922	0	1	IC GATE CMOS/74HC NAND QUAD 2-INP	04713	MC74HC00N
A2U403	04951-10701	3	1	MEM PROM A	28480	04951-10701
A2U406	1818-3981	8	2	IC CMOS 262144 (256K) STAT RAM 120-NS	S4013	HM62256LP-12
A2U407	04951-10704	6	1	MEM PROM M	28480	04951-10704
A2U409	1818-3981	8		IC CMOS 262144 (256K) STAT RAM 120-NS	S4013	HM62256LP-12
A2U411	1820-2998	0	1	IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A2XU304	1200-0567	1	2	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A2XU403	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A2XU407	1200-1278	3	1	SOCKET-IC 28-CONT DIP DIP-SLDR	55322	ICO-628-NGT
A2Y1	0410-1004	7	1	CRYSTAL-QUARTZ 1.8432 MHZ HC-33/U-HLDR	28480	0410-1004
	0380-1489	7	2	SPACER-SNAP-IN .375 IN LG; .280 IN OD	28480	0380-1489
	04951-20702	5	1	MEMORY BOARD	28480	04951-20702

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	04951-60707	4	1	KATAKANA MEMORY BD ASSY	28480	04951-60707
	04951-20702	5	1	MEMORY BOARD	28480	04951-20702
	04951-80708	7	1	LABEL-60707	28480	04951-80708
A2U304	04951-10706	8	1	KATA MEM P	28480	04951-10706
A2U403	04951-10705	7	1	KATA MEM B	28480	04951-10705
A2U407	04951-10707	9	1	KATA MEM M	28480	04951-10707
				THE KATAKANA MEMORY BOARD ASSEMBLY USES THE SAME PARTS AS THE 04951-60702 ASSEMBLY EXCEPT FOR ANY PARTS LISTED ABOVE.		

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	04951-60703	0	1	DISC CONT ASSY	28480	04951-60703
A3C1	0160-3879	7	16	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C2	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C3	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C4	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C5	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C7	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C8	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C10	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C11	0121-0552	5	1	CAPACITOR-V TRMR-CER 7-60PF 250V PC-MTG	28480	0121-0552
A3C12	0160-5332	1	1	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-5332
A3C14	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C15	0160-3508	9	2	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C16	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C17	0160-3876	4	2	CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A3C18	0160-3876	4		CAPACITOR-FXD 47PF +-20% 200VDC CER	28480	0160-3876
A3C19	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C20	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C21	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C22	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C23	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3C24	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A3CR1	1901-0539	3	1	DIODE-SM SIG SCHOTTKY	28480	1901-0539
A3E1	1251-8360	5	15	CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3E1	1258-0209	9	5	JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A3E2	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3E2	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A3E3	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3E3	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A3E4	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3E4	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A3E5	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3E5	1258-0209	9		JUMPER-REMOVABLE 2 POSITION; .200 IN	28480	1258-0209
A3J1	1252-1606	0	1	CONN-POST TYPE .100-PIN-SPCG 60-CONT	22526	65496-049
A3J2	1251-8601	7	1	CONN-POST TYPE .100-PIN-SPCG 34-CONT	28480	1251-8601
A3R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1001-F
A3R2	2100-1738	9	2	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	82PR10K
A3R3	2100-1738	9		RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	73138	82PR10K
A3R4	0757-0465	6	1	RESISTOR 100K 1% .125W F TC=0+-100	24546	CT4-1/8-T0-1003-F
A3R105	1810-0280	8	4	NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A3R403	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A3R408	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A3R503	1810-0280	8		NETWORK-RES 10-SIP 10.0K OHM X 9	91637	CSC10A01-103G/MSP10A01-
A3TP3	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3TP4	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3TP5	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3TP5	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3TP6	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A3U104	1820-3079	0	1	IC DCDR CMOS/74HC 3-TO-8-LINE	04713	MC74HC138N
A3U105	1820-3191	7	2	IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC257N
A3U203	1820-2922	0	1	IC GATE CMOS/74HC NAND QUAD 2-INP	04713	MC74HC00N
A3U304	1818-3981	8	1	IC CMOS 262144 (256K) STAT RAM 120-NS	S4013	HM62256LP-12
A3U306	1820-4671	0	1	IC-CMOS PROGRAMM. INTERRUPT CONTR. 5MHZ	34649	P82C59A-2
A3U308	1820-2998	0	4	IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A3U400	1820-4702	8	1	IC-PROGRAMMABLE DMA CONTROLLER	34371	P82C374
A3U403	1820-2998	0		IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A3U408	1820-2998	0		IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A3U500	1820-3191	7		IC MUXR/DATA-SEL CMOS/74HC 2-TO-1-LINE	04713	MC74HC257N

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U505	1820-4100	0	1	IC-8-16 BIT CMOS MPU, 5MHZ	34371	CP80C88
A3U508	1820-2998	0		IC LCH CMOS/74HC D-TYPE OCTL	04713	MC74HC373N
A3U600	1820-3659	2	1	IC-FLOPPY DISK FORMATTER/CONTROLLER	52840	WD2793APL02-07
A3U603	1820-3456	7	1	IC DRVR CMOS/74HC LINE OCTL	27014	MM74HCT244N
A3U604	1820-3298	5	1	IC GATE CMOS/74HC OR QUAD 2-INP	27014	MM74HC32N
A3U606	04951-10703	5	1	DISC EPROM ASSY	28480	04951-10703
A3U608	1820-3330	6	1	IC TRANSCEIVER CMOS/74HC BUS OCTL	27014	MM74HC245N
A3U703	1820-3630	9	1	IC DRVR CMOS/74HC BUS OCTL	27014	MM74HCT240N
A3U704	1820-2921	9	2	IC INV CMOS/74HC HEX	27014	MM74HC04N
A3U706	1820-2921	9		IC INV CMOS/74HC HEX	27014	MM74HC04N
A3U707	1820-3081	4	1	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	04713	MC74HC74N
A3U708	1820-4084	9	1	IC DCDR CMOS/74HC 3-TO-8-LINE	04713	MC74HC137N
A3U803	1820-3399	7	1	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG COM	04713	MC74HC273N
A3U804	1813-0164	3	1	IC OSC HYBRID	34344	K1100A-2.0MHZ
A3U806	1820-3180	4	1	IC SHF-RGTR CMOS/74HC SYNCHRO SERIAL-IN	27014	MM74HC164N
A3U807	1820-3674	1	1	IC BFR CMOS/74HC BUS QUAD	27014	MM74HC125N
A3U808	1820-3488	5	1	IC-CMOS CLOCK GENERATOR DRIVER	34371	CP82C84A
A3UX505	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3UX606	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XY1	0890-0377	1	1	TUBING-HS .5-IN-D/.25-IN-RCVD	00000	ORDER BY DESCRIPTION
A3Y1	0410-1328	8	1	CRYSTAL-QUARTZ 15 MHZ HC-18/U-HLDR	28480	0410-1328
	1251-5595	2	2	POLARIZING KEY-POST CONN	28480	1251-5595
	04951-20703	6	1	DISC CONT BD.	28480	04951-20703

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				MECHANICAL PARTS		
A1	04951-60701	8	1	MAIN BRD ASSY	28480	04951-60701
A2	04951-60702	9	1	MEMORY BD ASSY	28480	04951-60702
A3	04951-60703	0	1	DISC CONT ASSY	28480	04951-60703
A4	5060-7171	3	1	KEYBOARD ASSY	28480	5060-7171
A5	04952-62601	2	1	REAR PNL ASSY	28480	04952-62601
A6	04951-62701	2	1	FRONT PNL ASSY	28480	04951-62701
A7	04951-62608	8	1	YOKE ASSY	28480	04951-62608
B1	04952-62604	5	1	FAN ASSY	28480	04952-62604
F1	2110-0758	2	2	FUSE .6A 250V TD 1.25X.25 UL	71400	MDL.6
FL1	9135-0316	7	1	LINE MODULE-FILTERED OPERATING VOLTAGE	S4307	FS2467-1-16-L-D-22
H1	0380-1892	6	2	STANDOFF-HES .844-IN-LG 6-32-THD	05791	SS6981-0.844-01
H2	0515-0890	9	4	SCREW-MACH M3 X 0.5 6MM-LG 90-DEG-FLH-HD	28480	0515-0890
H3	1400-0249	0	1	CABLE TIE .062-.625-DIA .091-WD NYL	28480	1400-0249
H4	1460-2096	5	2	SPRING-CPRSN 24.9-MM-OD 12.7-MM-OA-LG	28480	1460-2096
H5	2360-0113	2	10	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H6	2360-0212	2	1	SCREW-MACH 6-32 .875-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H7	2360-0476	0	4	SCREW-MACH 6-32 .188-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H8	2510-0063	0	1	SCREW-MACH 8-32 1.5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H9	2510-0124	4	3	SCREW-MACH 8-32 .625-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H10	2510-0296	1	1	SCREW-MACH 8-32 4-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H11	2510-0324	6	2	SCREW-MACH 8-32 3.75-IN-LG PAN-HD-POZI	28480	2510-0324
H12	0590-0076	1	2	NUT-HEX-PLSTC LKG 4-40-THD .143-IN-THK	28480	0590-0076
H13	0590-0157	9	4	NUT-HEX-PLSTC LKG 6-32-THD .178-IN-THK	28480	0590-0157
H14	0590-0167	1	4	NUT-THUMB 6-32-THD BRS	00000	ORDER BY DESCRIPTION
H15	0624-0672	6	8	SCREW-TPG 4-40 .625-IN-LG 82 DEG	28480	0624-0672
H16	2190-0795	5	2	WASHER-SPR BLVL NO. 5 .13-IN-ID	28480	2190-0795
H17	3030-0832	4	2	SCREW-SHLDR 4-40 .312-IN-LG SST-303	00000	ORDER BY DESCRIPTION
H18	3050-0100	1	4	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0100
H19	3050-0105	6	2	WASHER-FL MTLC NO. 4 .125-IN-ID	28480	3050-0105
H20	0360-1859	3	1	TERMINAL-SLDR LUG PL-MTG FOR-#5-SCR	28480	0360-1859
H20	0380-1489	7	1	SPACER-SNAP-IN .375 IN LG; .280 IN OD	28480	0380-1489
H21	0590-0663	2	4	NUT-HEX-PLSTC LKG 4-40-THD .11-IN-THK	00000	ORDER BY DESCRIPTION
H22	0624-0208	4	2	SCREW-TPG 6-32 .5-IN-LG PAN-HD-POZI STL	28480	0624-0208
H23	2190-0018	5	4	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
H24	2190-0068	5	1	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
H25	2360-0219	9	4	SCREW-MACH 6-32 1.375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H26	2420-0023	1	4	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	28480	2420-0023
H27	2950-0054	1	1	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H28	3050-0010	2	4	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0010
MP1	0950-1798	0	1	DISC DRIVE (NEW)	28480	0950-1798
MP1	5062-2104	0	1	DISC DRIVE (EXCHANGE)	28480	5062-2104
MP2	5000-5535	3	1	DISC DR SUP BRKT	28480	5000-5535
MP3	5000-5536	4	1	DISC DR MTG BRKT	28480	5000-5536
MP4	5000-5537	5	1	FOOT BRACKET	28480	5000-5537
MP5	5040-4470	7	1	HANDLE-CASE	28480	5040-4470
MP6	5041-6750	2	4	BUMPER FOOT	28480	5041-6750
MP7	5041-7504	6	4	REAR FOOT	28480	5041-7504
MP8	5041-7509	1	1	SOFT POUCH	28480	5041-7509
MP9	5041-7514	8	1	CLAM SHELL INSUL	28480	5041-7514
MP10	5041-7516	0	1	CASE-TOP	28480	5041-7516
MP11	5041-7517	1	1	CASE-BOTTOM	28480	5041-7517
MP12	5080-8572	2	1	TRNSPT DISC LBL	28480	5080-8572
MP13	04951-20007	3	4	SPACER-CASE	28480	04951-20007
MP14	04951-80703	2	1	FRONT PANL LBL	28480	04951-80703
MP15	04951-80704	3	2	LBL-HANDLE	28480	04951-80704
MP16	0400-0301	4	1	KYBD CBL STR RLF	76385	25133-FCP
MP17	9164-0287	2	2	MAGNET 32 GAUSS	28480	9164-0287
MP18	9164-0288	3	2	MAGNET 8 GAUSS	28480	9164-0288
MP19	9164-0289	4	2	MAGNET 13 GAUSS	28480	9164-0289
MP20	2090-0202	7	1	CRT	28480	2090-0202

Table 6-3. Replaceable Parts (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP22	5041-6777	3	1	FRONT PANEL	28480	5041-6777
MP23	5041-6778	4	1	UPR KYBD HSG	28480	5041-6778
MP24	5041-6779	5	1	LOWER KYBD HSG	28480	5041-6779
MP25	5041-7503	5	1	LATCH BUTTON	28480	5041-7503
MP26	5041-7511	5	1	CBL INSULATOR	28480	5041-7511
MP27	5080-8575	5	1	FT PNL GND STRIP	28480	5080-8575
MP28	0890-0706	0	1	TUBING-HS .093-IN-D/.046-IN-RCVD	28480	0890-0706
MP29	1251-4580	3	1	CONNECTOR 3-PIN F POST TYPE	28480	1251-4580
MP30	3160-0491	6	1	FINGER GUARD	28480	3160-0491
MP31	5041-7504	6		REAR FOOT	28480	5041-7504
MP32	02932-00038	1	2	RETAINER CLIP	28480	02932-00038
MP33	5000-5539	7	1	REAR PANEL	28480	5000-5539
MP34	5041-7521	7	1	REPLACEMENT SET OF KEYCAPS	28480	5041-7521
W1	5060-7179	1	1	DISC DRIVE CBL	28480	5060-7179
W2	04951-61618	8	1	POD CABLE	28480	04951-61618
W3	04951-61701	0	1	BUSS CABLE	28480	04951-61701
W4	5060-7170	2	1	KEYBOARD CABLE	28480	5060-7170
W5	04951-61616	6	1	CRT CABLE	28480	04951-61616
W6	5060-7169	9	1	EXT VIDEO CBL	28480	5060-7169
W7	5060-7176	8	1	C ASSY REAR PNL	28480	5060-7176
W8	04952-61601	0	1	REMOTE CABLE	28480	04952-61601
W9	04952-61604	3	1	CBL GRN/Y 4.5L	28480	04952-61604
W10	04952-61605	4	1	CBL GRN/Y 4.0L	28480	04952-61605
W11	04952-61606	5	1	CBL W/R/GY 4.5L	28480	04952-61606
W12	04952-61607	6	1	CBL GY 4.5L	28480	04952-61607
W13	04952-61608	7	1	CBL W/BR/GY 4.25	28480	04952-61608
W14	04952-61609	8	1	CBL W/BK/GY 3.0L	28480	04952-61609
W15	04952-61610	1	1	CBL W/GY 3.0L	28480	04952-61610

SECTION VII
MANUAL CHANGES

7-1. INTRODUCTION

This section contains information to backdate this manual for instruments with serial prefix numbers lower than the serial prefix shown on the Title Page.

7-2. MANUAL CHANGES

To adapt this manual to your instrument, make changes to your HP 4951C as listed in table 7-1. Changes are listed by serial prefix number. The sequence of changes should be performed in the order shown. For instruments with serial prefixes greater than the serial prefix shown on the Title Page, changes are described in a yellow MANUAL CHANGES supplement.

Table 7-1. Manual Changes

Instrument Serial No.	Make Changes
2631A	1

MANUAL CHANGE INSTRUCTIONS

General Changes

SA Loops - 04951-60701 Main Board - On revision A main boards, jumper A1E314 should be moved to the 'N' position instead of the 'T' position.

Change 1

Page 6-14 - Q108 Part number 1854-1028 should be changed to 1826-0643.

SECTION VIII
SERVICE

8-1. INTRODUCTION

This section contains information designed to help you understand and service the HP 4951C. Section VIII is divided into three major parts - Theory, Troubleshooting, and Block Diagrams and Schematics.

8-2. THEORY

The Theory part of Section VIII contains an overview of the major parts of circuitry that make up the HP 4951C.

8-3. TROUBLESHOOTING

The Troubleshooting Section contains information about how to identify and repair problems that may occur with the HP 4951C. It contains troubleshooting information, troubleshooting procedures and Signature Analysis Tables. The organization of the section follows the same form that is outlined in Section IV - Performance Verification. When a problem occurs with the instrument look at the Performance Verification Flowchart and Tests to isolate the problem to a specific area of circuitry and then proceed to the part of Section VIII needed to help fix the problem.

The SA Tables are designed for quick identification of a problem. They are set in the individual sections of circuitry that they are associated with. Key Data is highlighted to give you a fast way to check the circuit under question. Under each part that is checked in the SA Tables is a number where the part can be found on the corresponding schematic at the end of Section VIII. This is designed to help you quickly go to an area and isolate the problem.

8-4. BLOCK DIAGRAMS AND SCHEMATICS

The Block Diagrams and Schematics part of Section VIII is organized primarily by the different assemblies in the HP4951C. Each Block Diagram describes a part of circuitry in the instrument. This is followed by a component locator which highlights the area of circuitry laid out in the Block Diagram and Schematic. Power and grounds are identified for each part given, and a cross reference chart for parts that are used on more than one schematic is included. Each schematic is labeled with the board number and individual schematic number. Data or control lines that are shared between schematics are labeled with additional schematic numbers and the origin of that line is highlighted with a box around the schematic number.

8-5. GENERAL HANDLING OF STATIC SENSITIVE DEVICES

The HP 4951C has many static sensitive components. Observe the following guidelines when handling these devices:

A. Wear a wrist strap which contacts the bare skin and is properly grounded.
B. All equipment, such as soldering irons, fixtures, and so on should be grounded.
C. Work areas should be clear of non-conductive material.
D. Clothing should never come in contact with components or assemblies.
E. Use antistatic solution on all work benches, table mats, hand tools, storage containers, and other related equipment.
F. Static sensitive devices must be protected at all times. Keep the devices in their antistatic packaging.
G. All work should be performed at a static safe work station. A static safe work station has the following:
    1. Conductive table mat connected to ground through a 1 M resistor.
    2. Wrist strap grounded through a 1 M resistor.
    3. All test equipment is tied to one common ground.

8-6. POWER SUPPLY THEORY

The HP 4951C power supply converts ac line voltage from the power cord to the proper voltages for use by the rest of the system. It provides outputs of +5, +12, and -12 volts and a power supply fail signal. The line voltage is rectified and filtered to provide dc voltage to a high-voltage switching converter. This converter uses pulse-width modulation to provide an isolated 22 volt output. Two independent regulators step the 22 volt supply down to +5 volts and +12 volts. A flyback winding on the output stage of the +12 volt filter provides a -12 volt output. Overvoltage protection is provided for the +22, +5, and +12 volt outputs and current limit protection is provided on the +5 and +12 volt outputs. Refer to the Power Supply Block Diagram and the Power Supply Schematic located at the end of Section VIII as needed when reading through this section.

Off-line AC to DC Converter

Line Module

The line module contains the main power switch, a safety fuse, and filtering to reduce conducted interference. No line range selection is necessary. The input should be between 90 and 264 volts ac at a frequency of 48 to 66 Hz.

Half-Wave Bridge Rectifier

A half-wave bridge rectifier (A1CR12) rectifies the ac input from the line module. 'Ground' for the off-line section of the power supply tracks the more negative of the hot and neutral lines while the working voltage of 100 to 350 volts tracks the more positive of the two.

Filter Stage

The rectified voltage going to the power supply is filtered by storing charge on a 150uF capacitor (A1C31). A pair of thermistors (A1RT23 and A1RT24) limit the inrush current at power up. High-frequency differential noise from the supply is filtered by an LC network to the mains. Common mode noise is filtered by the line module.

Start Up Circuit

Charge Storage

The working voltage supplies a trickle charge through about 87 K ohms (A1R101, A1R102, and A1R103) to a capacitor (A1C1). The voltage on the capacitor ramps up to about 16 volts. This voltage supplies the pulse-width modulator IC (A1U102). After power up the supply augments the trickle charge.

Control Circuit

The pulse-width modulator draws less than 1mA of current until its supply reaches 16 volts. The IC then enables the internal voltage reference (pin 8), oscillator (pin 4), and gate drive (pin 6) to the primary switch. Six volts of hysteresis in the sense circuit results in continued operation of the IC until the supply voltage drops to about 10 volts, a condition which occurs at power down or during excessive duty cycle limiting.

Undervoltage Lockout

The 'v-working' voltage is divided down to drive the base of a PNP transistor (A1Q101). When the input voltage exceeds a level great enough to reverse bias the base-emitter junction, a resistor on the collector drives the error amp input (pin 2) low such that the output is enabled. Otherwise the primary switch is held off. The supply will operate when the ac input exceeds about 80 volts.

Isolating DC to DC Converter

100KHz Isolation Transformer

The 'v-working' voltage of 100 to 350 volts is switched across the primary winding of the isolation transformer to develop ac on the secondary. A flyback winding of 12 turns releases the energy stored in the transformer's core on each half cycle. This energy is dumped into the 15 volt supply for the control circuit. Surplus energy is dissipated in a 15 volt zener clamp diode (A1CR2). When switched at the proper duty cycle, for a given input voltage, the rms voltage on the isolated secondary is about 22 volts.

PWM Control

The PWM control is implemented by a pulse-width modulation IC (A1U102). The input voltage is applied to a switched capacitor through 260 K ohms. The capacitor is switched to ground while the primary switch is held off. The voltage on the capacitor is then allowed to rise as long as the primary switch is on. This voltage is buffered and level shifted to overdrive the current sense input of the IC. When the capacitor's voltage reaches about 7 volts, the current sense input will exceed the 1 volt threshold and the switch is turned off. A constant volt-usec product is obtained. The duty cycle is further limited if the current sense signal exceeds the 1 volt threshold due to excessive primary current in the transformer. The duty cycle is zero when the supply to A1U102 falls below about 10 volts or when the working voltage is below about 75 volts ac.

100 KHz Switch

The drive signal from the pulse-width modulator IC(A1U102), pin 6, controls the gate of a 800 volt FET (A1Q204) to switch one end of the primary winding to ground at 100 KHz. This drive signal also controls the gate of the P-chanel JFET (A1Q102) which is used to derive a constant volt-usec time. Two 3.3 ohm, 1/4 w resistors (A1R7 and A1R8), in parallel, act as the current sense device. The voltage across the resistance is sensed through an RC network (A1R6 and A1C7) and a schottky diode (A1CR3). The maximum primary current is, therefore, about 0.8 amps.

Half-wave Rectification and Filter

The secondary voltage of 22 vrms is rectified by a diode (A1CR14) and then filtered by a two-pole LC arrangement (A1L4 and A1C34). The current in the inductor is continuous in order to maintain the rms voltage and not peak charge the capacitor. A load of four watts is required to maintain regulation (less if the input is below 130 volts ac).

DC to DC Converter - +5V Output

+5 Volt Step Down Regulator

The step down regulator (A1U105) provides pulse width modulation for the +5 volt supply. The duty cycle is reduced if overcurrent or overvoltage is sensed. Overcurrent is sensed by monitoring the voltage dropped across a current sensing resistor (A1R9). If the voltage at pin 7 is greater than the voltage at pin 6 minus .3 volts, the step down regulator will current limit. The regulator monitors the +5 voltage through a zener diode (A1CR6) in the feedback path. If the feedback voltage is too high, the step down regulator will modulate the duty cycle of the output.

50KHz Switch and I Sense

A drive signal from the +5 volt Step Down Regulator Control section operates a pair of P-channel MOSFETs (A1Q106 and A1Q107) to switch the supply voltage through a current sense resistor and into a filter stage. When operated at the correct duty cycle, the output is +5 vrms. The voltage dropped across the current sense resistor is fed back to the control IC for overcurrent detection.

Rectifiers and Filters

A catch diode (A1CR4) provides a current path for the filter choke (A1L2) during the switch's off cycle. This enables a continuous current condition as in the filter stage of the isolating converter. Note, however, that continuous conduction is not necessary to maintain regulation since the output is fed back to the PWM Control. If the output is above 5 volts then the control IC simply reduces the duty cycle to 0. The supply operates properly from no load to 2 amps.

DC to DC Converter - +/- 12V Output

The +/- 12 volt output works in the same manner as the +5 volt output.

+12 Volt Step Down Regulator

The step down regulator (A1U306) provides the pulse width modulation for the +12 volt supply. The duty cycle is reduced if overcurrent or overvoltage is sensed. Overcurrent is sensed by monitoring the voltage dropped across a current sensing resistor. If the voltage at pin 7 is greater than the voltage at pin 6 minus .3 volts, the step down regulator will current limit. The regulator monitors the +12 voltage through a zener diode (A1CR17) in the feedback path. If the feedback voltage is too high, the step down regulator will modulate the duty cycle of the output.

50KHz Switch and I Sense

A drive signal from the +12 volt Step Down Regulator section operates a pair of P-channel MOSFETs (A1Q405 and A1Q406) to switch the supply voltage through a current sense resistor (A1R29) and into a filter stage. When operated at the correct duty cycle, the output is +12 vrms. The voltage dropped across the current sense resistor is fed back to the control IC for overcurrent detection.

Rectifiers and Filters

A catch diode (A1CR20) provides a current path for the filter choke (A1T405) during the switch's off cycle. This enables a continuous current condition as in the filter stage of the isolating converter. Note, however, that continuous conduction is not necessary to maintain regulation since the output is fed back to the PWM Control. If the output is above 12 volts then the control IC will simply reduce the duty cycle to 0. The supply will operate properly from no load to 2 amps.

Transformer

A second winding on the filter choke produces a 1:1 transformer to provide an additional output. The polarity of this secondary winding is such that a -12 volt output is obtained. Note that the negative supply obtains power from the energy stored in the core, on the flyback portion of the cycle (switch off). This means that the negative output is limited by the amount of current in the positive output and by the duty cycle. Typically, the negative output is able to provide 50% of the current that is present on the positive output.

Overvoltage Protection

Overvoltage Sense Circuit

The Overvoltage Sense Circuitry is comprised of zener diodes corresponding to the three inputs: the 22 volt input feeds a 30 volt zener (A1CR9), the 12 volt input supplies a 13 volt zener (A1CR8), and a 5.6 volt zener (A1CR7) is across the 5 volt supply. If any of the supplies go high enough to cause a zener to avalanche, the common anode connection will drive the crowbar circuit on.

SCR Crowbar

A transistor (A1Q207) provides gain to the anodes of the sensing circuit. This amplified signal then drives the gate of the SCR (A1Q206) to clamp the 22 volt supply. This not only prevents the other supplies from rising, it also clamps them through the integral diodes of the power MOSFETs used in each regulator. Clamping the supplies does not blow the fuse in the line module but simply causes the primary of the isolating converter to enter the current limit condition, in which case insufficient energy is supplied from the core to the +15 volt supply and the entire supply shuts down until the start up circuit fires again.

8-7. CENTRAL PROCESSING UNIT (CPU) THEORY

The NSC800 Microprocessor (A1U415) is the Central Processing Unit for the 4951C. It uses a multiplexed address/data bus for input/output operations. The clock output has a frequency of 4 MHz which is derived from a crystal of 8 MHz (A1Y2). This clock is used as the system clock for the HP 4951C.

The 16-bit address/data bus is divided into a high-order 8-bit bus that handles bits 8-15 of the address, and a low-order 8-bit multiplexed address/data bus that handles bits 0-7 of the address and bits 0-7 of the data. During an input or output instruction the CPU duplicates the lower half of the address (AD0-AD7) onto the upper half (A8-A15). IO/~M indicates whether the present cycle accesses memory or I/O.

The interrupt lines (NMI, ~RSTA, ~RSTB, ~RSTC, ~INTR) which are generated from other devices in the system cause the CPU to service the appropriate interrupt. NMI is a non-maskable interrupt and has the highest priority of all interrupt signals. ~INTR is the lowest priority interrupt and comes from the Data Link Controller area of the HP 4951C. ~INTACK is the signal that allows information from the DLC to go to the CPU. ~RSTA is the interrupt that comes from the Tick Clock Generator. ~RSTB is a softkey interrupt. ~RSTC is the interrupt from the Disc Controller board.

The control lines (~RD, ~WR, and ALE) tell the system that a valid memory or I/O address is available and if it is being input to the CPU or if it is output by the CPU. The control line IO/~M indicates whether the current cycle is an I/O or memory operation. RESETIN is used with an R-C network (A1R22 and A1C43) to ensure proper power-up conditions for the CPU. The CPU is not allowed to wake up until the Power Supply is up and stable.

Bus Request (BREQ) is used when another device is requesting control of the system bus. The CPU issues a Bus Acknowledge (~BACK) signal to the requesting device when it is ready for the requesting device to take control of the system bus.

8-8. DATA LINK CONTROL THEORY

The Data Link Control (DLC) section controls the data, clock, and control signals that allow the HP 4951C to interact with an external network.

Serial Communications Controller (SCC)

The SCC (A1U209) is programmed by the CPU as an I/O device. The Serial Communications Controller is responsible for converting serial to parallel data during monitor modes, and parallel to serial data during simulate modes. Channel A receives DTE data and channel B receives DCE data. Data can be transmitted from either channel. It is capable of supporting full duplex transmit and receive operations. It can also drive and/or monitor various physical interfaces.

The internal clock for the SCC is PCLK (pin 20). It is derived from a 3.68 MHz crystal (A1Y1). The SCC has an internal baud rate generator (BRG) and a 16-bit programmable divider to generate common baud rates to +/- .003% of nominal. The Baud Rate Generator is used for asynchronous data generation. For synchronous data operations, the transmit and receive clocks are used. Transmit and receive clock sources come to the SCC (TXCLK) through A1U111 (pins 3 and 4) to reflect the test to be performed.

The SCC generates an interrupt, ~INTR (pin5) to the CPU whenever the status of the interface changes or when it requires servicing. Upon receiving an interrupt acknowledge, ~INTA (pin8), the SCC will generate one of eight vectors that describes the nature of the interrupt by pointing to the appropriate service routine.

The SCC is a dual channel device that can be programmed for either channel A or channel B (pin 34). The D/~C input (pin 32) defines the type of information that will be transferred to or from the SCC. These inputs are controlled by the CPU.

Data being received comes into the SCC (RXDA and RXDB) through A1U112 (pins 6 and 8). Data being transmitted from the SCC (TXDA and TXDB) is transferred through A1U111 (pin 9) and A1U112(pin 3). The Address/Data Bus (AD0-AD7) is used to transfer data or control signals from the SCC to the CPU, or from the CPU to the SCC.

SCC Decoder

The SCC Decoder (A1U515 and A1U213) uses IO/~M. A14, and A15 from the CPU to generate a signal that is the Chip Enable input to the SCC. An active low output on A1U213 pin 4 will enable the SCC to select a read or write operation. Another output from the SCC Decoder is the 810 Chip Enable input (A1U515 pin 12) to the NSC810 I/O Timer. A high on this line allows the transfer of information between the SCC and the I/O Timer.

Latch Decode

The Latch Decode circuitry (A1U714) is used to ensure a smooth flow of data and control signals coming into and going out of the pod latches. Using Pod, ~RD, and ~WR as inputs, A1U714 decodes the clock and output control lines of the Pod Latches, A1U211 and A1U212 for the setup of operating modes for the interface pod and the control lines for the Multiplexer (A1U111).

Pod Latches

The pod Latches (A1U211 and A1U212) configure the data and control lines for the DLC and the interface pod to the application that has been selected. The control lines for the multiplexer (A1U111) are generated by the pod latches.

2:1 Multiplexer

The DTE and DCE clocks coming into the HP 4951C are multiplexed through A1U111. The inverted output of this signal is TXCLK which is used by the SCC as inputs ~TRXCB and ~RTXCA, and by the interface pod as TXCLK. Data coming out of the SCC is multiplexed through A1U111 and becomes TD going to the interface pod. The control lines for the multiplexer (A1U111pins 2 and 14) come from the pod latch A1U211.

8-9. SYSTEM I/O DECODE THEORY

I/O Timer

The NSC810 I/O Timer (A1U814) is a three port Input/Output device. The NSC810 is programmed and controlled by the system CPU using AD0-AD7 and discrete system control signals. Port A (PA0-PA7) is used primarily for system memory decoding and enabling. PA5 is used as a system interrupt to the Disc Controller Board (A3). PA7 is used to generate the ~HOLD signal used by the Arbiter section of the CRT Gate Array (A1U510). Port B (PB0-PB7) is used as part of the keyboard scan circuitry along with latch A1U812. Port C (PC0-PC3) has several output functions. PC0 is used as the Horizontal Drive enable to the CRT Deflection circuitry. PC1 and PC2 are used to reset the interrupt circuits for ~RSTB and ~RSTC. PC3 is used as an output enable or disable for the beeper circuit A1U716. T0OUT and T1OUT are used in conjunction with the Tick Clock Generator circuitry to provide time marks with data that is input to the system capture buffer (A2U406).

Keyboard Latch

The Keyboard Latch (A1U812) is used in conjunction with the system CPU as it writes row and column scan addresses to the HP 4951C keyboard Assembly. Scan information (AD0-AD7) is written to the Keyboard through this latch when the CPU is doing an I/O write to the keyboard. The latch clock signal is derived through A1U714 from the CPU, ~WR, and the Keyboard select from I/O Decoder A1U313 pin 12. The Key stroke status information is returned to the system from the keyboard via the NSC810 Port A.

Keyboard

The keyboard assembly (A4) of the HP 4951C system is a simple 8 X 8 row and column matrix. Each key is assigned a specific row and column. The CPU will write to the keyboard, using the keyboard latch (A1U812) and activate a row to be sampled. The CPU will then read the status of the addressed row via Port A of the NSC810 (A1U814). Any keys activated on that row will be detected by the column value and read back via Port A. This process repeats and is called the Keyboard Scan Routine.

Softkey Decode

The HP 4951C uses a technique known as "Menu Driven" or "Softkey Driven" menus as the main interface. This allows the user to step their way through the system functions and control by means of selecting singly defined keys. These are the F1-F6 keys, More key, and Exit key located just under the main display screen. The function of the key is displayed at the base of the display. As these keys are pressed, their function changes. Many levels of commands are available using the different levels of softkeys. Certain Softkey functions are detected and decoded through the use of the Softkey Decode circuitry (A1U615 & A1U715). The result of specific Softkey activation results in RSTB becoming active to the system CPU. The appropriate interrupt service routine is then executed by the system.

Beeper Circuit

The system beeper is comprised of a 555 Timer (A1U716), a speaker (A1LS916) and discrete analog components. PC3 of the NSC810 controls the ~RST input of A1U716. The removal of A1E815 disables the speaker of the beeper circuit. This jumper is commonly removed when troubleshooting system failures. Note that the beeper circuit is powered by +12 vdc.

I/O Decoder

This device is used to generate chip enables to several I/O device circuits. The I/O Decoder (A1U313) Address consists of A11- A13 and the chip enable consists of A14-A15 and IO/~M from the system CPU. The decoder is enabled only when A14-A15 are low and IO/~M is high. The proper I/O select address on A11-A13 is then decoded and the proper I/O Device enable is generated.

DECODER OUTPUT	I/O DEVICE ENABLE
Y0 pin 15	unused
Y1 pin 14	CRT Controller (A1U514)
Y2 pin 13	POD Latches (A1U211 & A1U212)
Y3 pin 12	Keyboard Latch (A1U812)
Y4 pin 11	Tick Clock Latch
Y5 pin 10	unused
Y6 pin 9	Remote Latch & ACIA (A2U206 & A2U209)
Y7 pin 7	unused

Tic Clock Generator

The HP 4951C system uses a scheme known as "Tick Marks" or sometimes called "Time Stamps" to keep track of real-time events during data monitoring or simulating processes. These Tick Marks are inserted into the system Capture Buffer (A2U406) during run time operations of the system. The tick mark is generated with reference to TOOUT from the NSC810 to the clock input of the Tick Counter (A1U114). For every 64 counts QC (A1U114 pin 9) goes high and generates a ~RSTA to the system CPU.

The system then updates the timing information in the Capture Buffer by means of an appropriate interrupt service routine. During operations where a time remainder is generated, the remainder count value of the Tick Clock Counter (A1U114) can be sent to the system by means of the Tick Clock Latch (A1U712). To enable the Tick Clock Latch, the system must do an I/O Read to the Tick Clock Latch. Each time the Latch Read occurs the Tick Clock Counter is cleared or reset by means of A1U114 pins 2 and 12.

8-10. DUAL PORT RAM THEORY

The Dual Port RAM (A1U411) allows two asynchronous processes to share a common section of memory. The circuitry is designed to minimize the amount of system overhead in performing the task of refreshing the CRT. The basic responsibility of this circuitry however, is to preserve system integrity by preventing bus contentions and hashing on the CRT.

CPU Address Latch

The CPU Address Latch is an eight bit latch (A1U413) used to demultiplex address and data on the input side of the Arbiter Multiplexers (A1U513, A1U512, and A1U713). The latch is enabled by ALE from the system CPU. Note that A8-A11 to A1U713 is not sent through the address latch A1U413. This is because A8 through A15 from the system CPU is address only. There is no data associated with this bus.

CRTC RAM

As display information is read from the Dual Port RAM, it is written to the CRTC RAM (A1U711). Since the display must be refreshed 60 times per second, this copy of the information is used to update the display when the CPU has control of the Dual Port RAM and the CRTC is locked out.

Dual Port Address Multiplexers

The Dual Port Address Multiplexer and 2 to 1 multiplexers are used by the system to allow addressing of the Dual Port RAM (A1U411) by means of the system CPU (A1U415) and the CRT Controller (A1U514). Depending on the level of the ~A/B select line (A1U512, A1U513 & A1U713 pin 1) generated from the Arbiter ~EN (A1U510 pin 36), the address value enabled to the Dual Port RAM will be from the system CPU (A0- A12) or the CRT Controller (MA0-MA10).

Dual Port RAM

The Dual Port RAM circuitry accepts the address and data bus of either the system CPU or the CRTC to the RAM under the control of the memory arbiter section of the CRT Gate Array. Normally, the CRT is refreshed real-time with the CRTC given continuous access to the Dual Port RAM. In this mode, the arbiter continuously samples the ~MREQ input waiting for a memory access request from the system. The sampling of this line occurs at the character transfer rate.

When a memory request is detected, the arbiter asserts the WAIT line which halts the system CPU until the current CRTC read cycle is completed. At the completion of the read cycle in progress the arbiter gives the system CPU access to the Dual Port RAM and causes the next refresh character to be read from the copy stored in the CRTC RAM. When the ~MREQ line is de-asserted, the arbiter, at the beginning of the next CRTC read cycle, will return control of the Dual Port RAM to the CRTC.

The Dual Port RAM provides enough memory to support two screens of information. The page of information displayed is determined by the start address programmed into the CRTC, and is under the control of the system CPU. A new start address can be programmed at any time. The CRT Controller will begin accessing the new display data at the beginning of the next refresh cycle.

CRT RAM Data Latch

The CRT RAM Data Latch is a dual 4 bit latch used as a single 8 bit latch. Its purpose is to latch character information being output from the Dual Port RAM to the CRT Controller Character Data Bus (CD0-CD7). Its enable (~EN) is generated by the Arbiter circuit contained within the CRT Gate Array (A1U510). Note that the same enable signal (~EN) inverted is used to enable the CRT RAM (A1U711). This indicates whether the Character Data is taken from the CRT RAM or the Dual Port RAM via Latch A1U612.

CPU Transceiver

The Transceiver (A1U613) in the data path isolates the system data line outputs from the Dual Port RAM. When the CRTC reads from the Dual Port RAM, buffer A1U612 is enabled and the transceiver is disabled and information is brought into the CRTC RAM from the Dual Port RAM.

8-11. CRT CONTROLLER THEORY

CRTC

The function of the CRT Controller (CRTC) is to obtain character and attribute information from the system memory and convert it to the desired serial dot pattern. In addition, the CRTC (A1U514) also provides synchronization signals for video timing and horizontal and vertical deflection (DE, HS, VS). These signals as well as the memory refresh addresses (MA0-MA9), and the character row addresses (R0-R3) are generated by the LSI controller chip (A1U514).

The CRT Controller obtains character and attribute information from the Dual Port RAM (A1U411) and uses a character ROM (A1U409) and the CRT Gate Array (A1U510) to create the desired dot pattern to be displayed on the CRT. The HP 4951C supports ASCII, EBCDIC, EBCD, BAUDOT, TRANSCODE, IPARS, KATAKANA, HEX and custom character sets. Each character can be assigned any or all of the following display attributes: overbar, underline, blink(2Hz), cursor(4Hz), inverse video, and half-bright.

Refresh addresses are gated to the Dual Port RAM during real-time refresh of the CRT. The least significant bit of the refresh address is the character clock (A1U510pin27). CCLK is derived from dot clock(DC) which is generated by the CRT Gate Array. For each character displayed two bytes of information must be read from the Dual Port RAM. Display data stored in the Dual Port RAM is interleaved with character information on even address boundaries and attribute data on odd boundaries.

As character and attribute data are transferred to the CRT Controller, a copy of the screen information is written into the CRTC RAM (A1U711). This copy is created in the event that the CRTC is denied access to the Dual Port RAM. When this occurs, the CRTC uses the data from the CRTC RAM to refresh the CRT.

The use of CCLK as the least significant address bit allows two bytes (character and attribute) to be transferred to the CRT Controller in a single character time. The dots are modified on a character basis according to the assigned video attributes and then resynchronized with the dot clock before driving the video amplifier.

Each attribute may be assigned independent of any other. Overbar and underline are encoded into the character ROM for every character. These two attributes are enabled by the appropriate attribute bits and character scan line. The Blink and Cursor rates are generated by extracting the 60 Hz vertical refresh rate from the video blanking signal (DE) and then dividing it down to the desired 2Hz and 4Hz rates.

Character Latch

The CRTC latches the character and attribute bytes at the appropriate times. The character latch (A1U412) outputs (C0-C7) are used to address the character ROM (A1U409).

Character ROM

The character ROM (A1U409) is programmed to output the correct dot pattern for the current scan line and character selected. The desired character code segment is encoded in the two most significant bits of the attribute byte (CD6, CD7) which drive the ROM address lines A13 and A12. The least significant ROM address lines (A0-A3) decode the character scan line and are driven by the row address lines (R0-R3). The eight bit output from the Character ROM is input to the CRT Gate Array where the signals are resynchronized and sent to the video amplifier.

CRT Gate Array

Arbiter

Two asynchronous devices, the CPU and the CRTC, share the same address space in the Dual Port RAM. The Arbiter area of the CRT Gate Array switches control of the Dual Port RAM between the CPU and the CRTC during normal operation. The CRTC generally controls the Dual Port RAM. When the CPU requests access to update the display information, the arbiter puts the CPU into a wait state. Once the last instruction/character of the CRTC is finished, the arbiter switches control of the address and data lines to the CPU.

The arbiter has one additional mode that is controlled by the system. By asserting the ~HOLD input, the arbiter will lock out the CRTC from the Dual Port RAM and give the system CPU continuous access to this section of memory. This input is used for starting and stopping the display during runtime and can also be used to setup the entire display with new information before actually displaying it on the CRT.

External Video

The External Video circuit (A1U611) allows an external monitor to be used in conjunction with the HP 4951C. The inputs to the circuit consist of signals containing the video information as well as DC power supply inputs, all taken directly from the main board of the instrument. The information signals are taken from the video portion of the main board and consist of Half Bright Drive (HBDR), Full Bright Drive (FBDR), Horizontal Sync (HS), Vertical Sync (VS), and Character Clock (CCLK).

The DC power supply inputs come directly from the power supply on the main board and consist of +5, -5, and Ground. The output of the circuit is a composite video signal which attaches through a 75 ohm coaxial cable to the back panel of the instrument and is one of the four following values:

-0.9V	Horizontal and Vertical Retrace
-0.3V	Dark Screen
+0.3V	Half Bright
+0.9V	Full Bright

This signal is compatible with the RS-170 standard. The horizontal retrace signals occur at a 15.750 kHz rate and the vertical retrace occurs at a 60 Hz rate.

8-12. CRT DEFLECTION THEORY

Vertical Synchronization

The Vertical Sync (VS) signal from the CRT Controller generates the vertical deflection for the CRT. The 60 Hz signal is changed to an analog signal during the duty cycle (A1U507). The output of the duty cycle drives a Dual Slope integrator (A1U608) which creates a sawtooth wave. Amplitude and DC offset for proper centering must be manually adjusted to create the proper deflection size.

Video

Half Bright (HB), Full Bright (FB), and the Active Pull Up (APU) are the inputs to the Video circuitry. The decoded outputs of Half Bright and Full Bright provide a drive signal for the circuitry. The Half Bright or Full Bright voltage is applied to the cathode of the CRT.

Horizontal Synchronization

The Horizontal Sync (HS) and high voltage are generated from the same circuit. HS drives the flyback transformer (A1T501) which provides supply voltages and the horizontal deflection. Duty cycle correction adjusts the signal for correctly driving the deflection circuitry.

Drive Enable Circuit

The Drive Enable circuit is controlled by NMI and HZEN. At power up this signal is disabled. Once the HP 4951C passes self-test and the CRT Controller is programmed, HS goes high. The output from the Drive Enable Circuit is shifted from 5 to 12 volts to drive the flyback FET (A1Q604) which goes to the transformer(A1T501).

Flyback Transformer

The flyback transformer generates the supply voltages and provides the proper signal for the horizontal deflection. It sends a video amplifier supply voltage of 28 volts which is routed through the active pull up and provides the post accelerator voltage. The other outputs provide biasing for the CRT, intensity adjust, and focus adjustment.

WARNING

8000 volts may be present in the HP 4951C even when the instrument is turned off. To avoid personal injury, observe all safety precautions and warnings stated on the instrument and in the manual. This product is a Safety Class 1 instrument which must be connected to an earth ground.

8-13. SYSTEM MEMORY THEORY

Address Latch

This eight bit single direction latch (A2U411) is used to demultiplex A0-A7 from AD0-AD7 on the rising edge of ALE from the system processor. The true address values are sent to each ROM and RAM device residing on the system address bus. Note that A0-A7 does not have the same electrical continuity as AD0-AD7.

Upper/Lower Memory Decode

The logic that A2U310 forms is used to enable the upper or lower half of memory decode from the Dual 2 to 4 Memory Decoder (A2U306). The decoder uses the value of A15 for the upper/lower half indicator. IO/~M from the system CPU must be low for A2U310 outputs (pins 6 & 8) to go active low. This denotes addressing to the system memory and not an I/O device.

Memory Decode

The Memory Decode device is a Dual 2 to 4 Decoder. Decoder 1 is used to generate enable signals (A2U306 pins 4-7) for the upper half of the system memory. Inputs include A13, A14, and ~LM from A2U310 pin 8. Decoder 2 is used to generate enable signals (A2U306 pins 9-12) for the lower half of the system memory. Inputs include PA0, PA4 from the NSC810, and ~HM from A2U310 pin 6.

Discrete Decode Logic

Discrete logic (A2U205, A2U307, A2U308, & A2U309) is used to generated chip enables to all of the memory devices used in the system memory (A2U304, A2U403, A2U406, A2U407, & A2U409). Inputs to this circuitry consist of memory decode enables from A2U306, signals from the NSC810 Port A, and other signals from the system CPU.

Page ROM (ROM P)

The Page ROM (A2U304) is a 512 kbit (64 kbyte) CMOS EPROM. It contains system code that is essential for power up (PV BOOT CODE). ROM P is segmented into pages, thus the name "Page ROM". This is accomplished by PA1 and PA2 on address pins 26 and 27. A2E6 is used to enable the output of the Page ROM during CPU NO-OPS testing. Data outputs (B0-B7) can be electrically removed from the system Address/data bus by removal of bus jumper A2E2.

Bank ROM (ROM B)

The Bank ROM (A2U403) is a 512 kbit (64 kbyle) CMOS EPROM. It contains the system code. ROM B is segmented into 32 kByte banks, thus the name "Bank ROM". This is accomplished by ~MC from the memory decoder A2U306. For testing, the data bus (AD0-AD7) can only be electrically removed from the system bus by lifting A2U403 pins 11- 13 and pins 15-19.

Mass Store ROM (ROM M)

The Mass Store ROM (A2U407) is a 256 kbit (32 kbyte) CMOS EPROM. It contains code used for some of the Mass store operations involving the A3 Disc Controller Board. The upper half of address space contains the actual code. The upper half of address space within ROM M is always enabled by tying A14 of A2U407 high via A2E5. Data outputs (B0-B7) on ROM M can also be electrically removed from the system bus (AD0-AD7) by the removal bus jumper A2E2.

Application RAM (RAM A)

The Application RAM (A2U409) is a 256 kbit (32 kbyte) CMOS RAM. It is used by the system application programs that can be used by the HP 4951C. These application programs can be loaded from a controller or another HP 4951C using the rear Remote interface port. Some applications are included with the the HP 4951C and reside in system ROM. The programs must still be loaded to the Application RAM in order to be executed by the system CPU. Data outputs (B0-B7) on RAM A can be electrically removed from the system bus (AD0-AD7) by the removal of the bus jumper A2E2. The contents of this RAM can be retained when power is removed from the HP 4951C. This is accomplished by a battery (A2BAT1) connected to the Vcc pin on A2U409.

Capture Buffer RAM (RAM C)

The Capture Buffer RAM (A2U406) is a 256 kbit (32 kbyte) CMOS RAM. It is used by the system as the main storage area for data being brought in by the system DLC. Timing information generated by the Tick Clock Generator is also stored here. Information stored in RAM C can be viewed by the user in the Examine Data Menu of the HP 4951C. Data outputs (C0-C7) on RAM C can be electrically removed from the system bus (AD0-AD7) by the removal of bus jumper A2E3. The contents of this RAM can also be retained when power is removed from the HP 4951C system. This is accomplished by a battery (A2BAT1) connected to the Vcc pin on A2U406.

8-14. REMOTE INTERFACE THEORY

The Remote Interface circuitry provides the HP 4951C with a second Input/Output port. It allows an external remote device or external printer to be connected to the HP 4951C. The CPU is connected to the Remote Circuitry through five control lines and an address/data bus. The Remote Circuit toggles an interrupt line to the microprocessor when there is information to be read. The Remote Circuit shifts the TTL level information from the HP 4951C to RS-232C level to the external device. It can also shift RS-232C level information to TTL level information.

Device Select

The Device Select decode circuitry (A2U204) converts the control signals coming from the system to an input for the Program Latch (A2206).

Program Latch

The address/data bus goes to the Program Latch (A2U206) which controls the baud rate generator circuit and to the Asynchronous Serial Interface. The signal output from the latch controls five different functions of the Remote/Printer Circuit:

- Sets the selected output baud rate
- Sends the DTR signal to the output stage
- Enables the output stage
- Disables the output stage
- Sends a clock signal to the Loopback Multiplexer

Clock Generator and Speed Multiplexer

The baud rates are created by a crystal controlled bit rate generator (A2U207) and the outputs are applied to an eight-to-one multiplexer (A2U106). The output of the multiplexer goes to the Asynchronous Serial Interface (A2U209) and is also the data transmit/receive clock.

Asynchronous Serial Interface

The microprocessor uses the Asynchronous Serial Interface (A2U209) as an input/output port to control the transmission and reception of the data to and from the HP 4951C. The Asynchronous Serial Interface converts parallel data from the memory of the HP 4951C to serial format and incoming data from serial to parallel. Information is transferred to and from the Asynchronous Serial Interface across the data bus AD0-AD7. The read and write lines from the microprocessor control the direction of the data flow through the Interface.

Output Disable

Disabling the Remote Interface circuitry is accomplished by setting A2U204 pins 9 & 12 high. This is done by the Remote Control Latch (A2U206) on pin 19. Disabling will cause activity on TXD and ~RST outputs to halt. Note that part of A2U204 is also used as the clock enable to the Remote Control Latch (A2U206).

Loop Back Multiplexer

The Loop Back Multiplexer has two functions. First, it routes the input data to the Asynchronous Serial Interface. Second, it loops the TXD, RTS, and DTR signals back to the Asynchronous Serial Interface during the self test mode which serves as a complete self test for the Remote Circuitry.

RS232 Drivers and Receivers

Data coming from the memory section of the HP 4951C routed through the Asynchronous Serial Interface is converted from TTL levels to RS232C levels through the logic level shifting circuitry (A2U102).

Data coming into the system is converted to TTL levels from RS232C levels through the Receiver Circuitry (A2U103). After the inputs are level-shifted, the signal goes through the Loopback Multiplexer to the Asynchronous Serial Interface.

8-15. FLOPPY DISC CONTROLLER THEORY

The HP 4951C Floppy Disc Controller board handles commands for data transfers to and from the Floppy Disc Drive. It controls the commands for the correct operation of the disc drive, as well as controlling whether data is going to the disc drive or being read from it.

80C88 Processor

The 80C88 (A3U505) is an 8-bit CHMOS microprocessor which can operate in two modes: minimum mode or maximum mode. It is used in the minimum mode on the A3 Floppy Control board by tying the min/max pin high. The 80C88 has a 20 bit address bus with the lower eight bits of the address bus multiplexed with the eight bit data bus (AD0-AD7). The upper four address bits (A16-A19) are also time multiplexed. The CLK, RESET, and READY control inputs come from the Clock Generator/Ready Sync (A3U808). The INT interrupt to the processor is driven by the Programmable Interrupt Controller (A3U306). The HOLD input (driven by the DMA Controller A3U400) is used to request access of the 80C88 buses. Control outputs from the processor indicate read and write memory or I/O cycles (~RD, ~WR, IO/~M), when a valid address is on the AD0-AD7 bus (ALE), when data is on the AD0-AD7 bus (~DEN), and the direction of data flow between the 80C88 and the NSC800 system processor (DT/~R). There is also an interrupt acknowledge (~INTA), and a signal which indicates that the 80C88 has relinquished control of its address and data buses (HLDA).

The 80C88 can address up to 64k I/O locations using address lines AD0-AD7 and A8-A15. Address lines A16-A19 are low during I/O operations. Each processor bus cycle consists of at least four clock cycles (T1-T4).

Internal "bus-hold" circuitry is used on the address and data buses and control signals (~DEN, DT/~R, IO/~M, ~RD, ~WR, HLDA, and HOLD) to prevent high current conditions caused by floating inputs. These bus-hold circuits maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source goes into high impedance).

Read Cycle

The 80C88 can read the I/O and memory devices on the Floppy Control board, or it can read the NSC800 system memory. The read cycle begins in T1 with the assertion of the address latch enable signal (ALE). The trailing of ALE is used to latch the lower eight bits of address information from the AD0-AD7 bus during T1. Address lines A8-A15 do not need to be latched because they are not multiplexed and are valid throughout the entire bus cycle. From T1-T4 the IO/~M signal indicates whether the read cycle is a memory or I/O cycle. At T2 the address information is removed from the AD bus and the bus goes tri-state. After a slight delay into T2 (to provide time for the bus to float) the ~RD signal goes low. If the read cycle is to the NSC800 system memory (rather than to a memory or I/O device on the Floppy Control board), the 80C88 also provides the DT/~R and ~DEN signals to enable the Data Transceiver (A3U608) on the AD0-AD7 bus. The addressed device enables its internal data bus drivers to output data onto the data bus. When the 80C88 pulls ~RD high, the addressed device tri-states its bus drivers.

Write Cycle

A write cycle begins with the assertion of ALE, valid address information being put onto the AD0-AD7 and A8-A15 address buses, and IO/~M indicating the type of write operation. During T2 the 80C88 puts the data to be written to the addressed device onto the AD0-AD7 bus. The data remains valid at least until the middle of T4. At the beginning of T2 ~WR is asserted to the addressed device.

Clock Generator / Ready Sync

The Clock Generator (A3U808) is used to generate three control signals to the 80C88 processor (RESET, CLK, and READY), and the OSC signal that is used to clock the Shift Register (A3U806). The 5 MHz clock is derived by dividing the 15 MHz input frequency by three. The timing of RESET is determined by the RC network on the ~RES input. Because the ~ASYNC input is tied high, the clock generator synchronizes an incoming high READY signal to the falling edge of the clock before the active high READY output is generated to the processor. In this way the processor can be held off by keeping the READY output low.

Address Latches

A3U508 latches the lower eight bits of address information from the AD0-AD7 bus on the falling edge of ALE when HLDA is low. The address output of A3U508 (A0-A7) are put onto the system's multiplexed address/data bus (AD0-AD7) by A3U308. A3U408 puts the A8-A15 address bits onto the upper system address bus (A8-A15).

Data Transceiver

A3U608 is used to transfer data between the 80C88 and the NSC800 system processor. The DT/~R control signal from the 80C88 determines which direction data flows. When DT/~R is high the 80C88 is transmitting data to the NSC800.

Read/Write Mux

The ~RD and ~WR signals from the 80C88 are multiplexed by A3U105 to produce separate I/O and memory read/write signals (~IORD, ~IOWR, ~MEMRD, and ~MEMWR). IO/~M from the 80C88 determines which read or write output from the multiplexer is active (low). The multiplexer is enabled when HLDA is low (the 80C88 is controlling the bus).

Memory Select Decoder

A3U708 is a 3-to-8 decoder which decodes address bits A18 and A19 to select the 80C88's on-board memory devices (RAM or ROM), or to generate ~BREQ to the NSC800 system processor to ask for access to the system memory device. The decoder is enabled when HLDA is low (80C88 has control of the bus) and ALE is high (valid address information is on A18 and A19).

ROM

The 32 kbyte ROM (A3U606) resides in the upper portion of the 80C88's memory range and F8000H-FFFFFH. It contains all the software that initializes and controls the devices on the Floppy Control board as well as the Floppy Drive. At RESET the 80C88 jumps to location FFFF0H to begin execution.

RAM

The 32 kbyte RAM (A3U304) resides in the lower portion of the 80C88's memory range at address 00000H-007FFH. The RAM is used for all internal variables, the stack area, the interrupt vector area, and the runtime caches that are used for transferring data to and from the Floppy Control board and the Floppy Disc.

I/O Select Decoder

A 3-to-8 decoder (A3U104) decodes A5-A7 to select the I/O devices of the 80C88. The on-board I/O devices are the Programmable Interrupt Controller (A3U306), the DMA Controller (A3U400), the Floppy Disc Controller (A3U600), and the Disc Latch (A3U803). An interrupt to the NSC800 system processor (~FLPINT) is generated by the least significant decoder output (~INTSYS). The decoder is enabled when HLDA is low (80C88 has control of the bus) and IO/~M is high (I/O cycle).

DECODER OUTPUTS	I/O ADDRESS RANGE
~INTSYS	00-1FH
~PICCS	20-3FH
~DMACS	40-5FH
~FDCCS	60-7FH
~DISCLATCH	80-9FH

System Interface Timing Generator

When the 80C88 needs to communicate with the NSC800 system processor it pulls ~BREQ low to request use of the system bus. A serial to parallel shift register (A3U806), along with a Flip Flop (A3U707) and several miscellaneous gates, control the timing of the control signals used during communication between the 80C88 and the NSC800 system processor. When the NSC800 releases the system bus to the 80C88 ~BACK goes low. The inverse of ~BACK is used to propagate a one through the shift register. The shift register outputs control the sequence and timing of events that occur during the remainder of the cycle. Two bytes of data are transferred each time the 80C88 has control of the bus.

Programmable Interrupt Controller (PIC)

The PIC (A3U306) is an I/O device of the 80C88, and is used to manage all interrupts on the Floppy Control board. The PIC can be programmed to determine the order of priority of interrupts. the main functions of the PIC are:

- o Accept up to seven active high interrupts and determine which interrupt has the highest priority.
- o Determine whether or not an incoming interrupt has a higher priority than the interrupt currently being serviced.
- o Issue an interrupt (INT) to the 80C88 based on these decisions.

When the 80C88 receives INTR it sends an acknowledge pulse (~INTA) back to the PIC. When the PIC receives ~INTA it chooses the highest priority interrupt from all requests. The 80C88 then sends the PIC a second ~INTA pulse which causes the PIC to put vectoring information on the data bus. These are the interrupts which the PIC monitors:

- IR0 - NMI from the Power Supply indicates that the Power Supply is going down.
- IR1 - FDCINT from the Floppy Disc Controller (FDC A3U600) indicates that the FDC has completed a command.
- IR2 - SYSINT is derived from the ~INTFLP interrupt from the NSC800 system processor.
- IR3 - DISCCHG from the Floppy Drive indicates that a floppy disc has been installed.
- IR4 - ~DISCCHG from the Floppy Drive indicates that a floppy disc has been removed.
- IR5 - Used for SA or Test Conditions.
- IR6 - Used for SA or Test Conditions.
- IR7 - ~INDEX from the Floppy Drive indicates one revolution of a floppy disc occurred. The service routine for this interrupt updates the media wear counter located in the RAM. Once this counter reaches 1000 the counter field on track 79 of the floppy disc is updated. This is done to monitor the wear on a floppy disc. After a disc has been used for approximately 1.5 million rotations a warning message is generated to the user indicating that the disc should no longer be used.

DMA Controller

The DMA Controller (A3U400) is an I/O device of the 80C88. It is used to speed up data transfers between the Floppy Control board RAM and the floppy disc. The 80C88 can read the status of the DMA Controller or it an program it to perform DMA transfers by addressing the internal registers of the DMA Controller and writing to these registers on the AD0-AD7 bus. The DMA Controller drives the ~IORD, ~IOWR, ~MEMRD, and ~MEMWR lines during DMA transfers to access the I/O devices (the FDC A3U600 and the Disc Latch A3U803) and the memory device (RAM A3U304). It also issues HOLD to the 80C88 to request access of the bus for the transfer. The 80C88 responds with HLDA when it grants the DMA Controller the bus. The DREQ input of the controller is driven high by the FDC when it has data from the floppy disc to transfer, or when it is ready to receive data from RAM to transfer to the floppy disc. The DMA Controller responds to DREQ by pulling ~DACK low.

DMA Address Latch

Latch A3U403 is used during DMA transfers to latch the upper eight bits of address information from the DMA Controller. During a DMA transfer the controller puts the lower eight bits of address information directly onto the A0-A7 bus. The upper eight bits are put onto the AD0-AD7 bus. The controller generates AEN and ASTB to latch these eight bits onto the A8-A15 address lines.

DMA Transfers

The DMA Controller coordinates DMA transfers of data between the RAM and the Floppy Drive. Data can be transferred from the RAM to the Floppy Disc (memory to I/O mode) or from the floppy disc to the RAM (I/O to memory mode). The 80C88 sets up the DMA Controller using ~DMACS, ~IOWR, A0-A3, and AD0-AD7. 80C88 sets up the FDC using ~FDCCS, ~IOWR, A0, A1, and AD0-AD7.

If the transfer mode is memory to I/O, the FDC generates DREQ to the DMA Controller to say it is ready to receive data. If the transfer mode is I/O to memory, the FDC generates DREQ when it has data from the floppy disc. The DMA Controller asserts HOLD to the 80C88 to request the bus. The 80C88 sends the DMA Controller HLDA when it releases the bus. HLDA going high also selects the RAM.

The DMA Controller puts the address of where the data will come from or go to in RAM on the bus. The lower eight bits of the address are put onto the A0-A7 bus, and the upper eight bits are put onto the AD0-AD7 bus. The DMA Controller sends the DMA Address Latch AEN and ASTB to latch the information on the AD0-AD7 bus onto A8-A15.

The DMA Controller pulls ~DACK low. This selects channel B of the FDC Mux. The FDC chip select is pulled low and A0 and A1 are pulled high. This selects the internal data register of the FDC (where data will go to or come from). The DMA Controller pulls ~IOWR and ~MEMRD low, or ~IORD and ~MEMWR low depending on the transfer mode. The data is transferred on the data bus. The FDC issues the ~FDCINT to the PIC when the transfer is complete.

Floppy Disc Controller (FDC)

The Floppy Disc Controller (A3U600) handles commands for data transfer to and from the floppy disc. The FDC has two modes of operation: single density or double density. ~DDEN is tied to ground in this application to put the FDC in the double density mode. The FDC is reset by the 80C88 by pulling ~MSTRRES low. The CLK input is 2 MHz from A3U804.

FDC Mux

The FDC Multiplexer (A3U500) selects the address and control signals that go to the Floppy Disc Controller (FDC A3U600). The ~DACK output from the DMA Controller controls whether the A or the B inputs of the mux are routed to the FDC chip. Normally the ~DACK line is high which selects the B inputs. This connects the FDC chip select (~FDCCS) from the 80C88's I/O Select Decoder so that the 80C88 can read or write to the FDC. Address lines A0 and A1 are also connected to the FDC. The 80C88 uses these lines to access the internal registers of the FDC.

During DMA transfers when the DMA Controller receives a DREQ from the FDC, the DMA Controller responds by pulling ~DACK low. This selects the A inputs of the mux. The A input, which goes to the FDC chip select, is tied to ground to select the FDC. The A0 and A1 lines are tied high to address the internal data register of the FDC.

FDC Disc Latch

The Floppy Disc Controller (FDC A3U600) handles commands for data transfer to and from the floppy disc. It also, along with the Disc Latch (A3U803), controls the head move commands required for operation of the Floppy Drive. The FDC and the Disc Latch are I/O devices of the 80C88. The ~HALFCLK output of the Disc Latch is connected to the ~ENMF and ~5/8 control inputs, and tells the FDC to internally divide the clock by two. This creates a 1 MHz clock for use with 5 1/4 inch floppy discs.

80C88 and FDC Interface

The interface between the FDC and the 80C88 processor consists of an eight bit data bus (AD0-AD7), address lines A0 and A1, ~IORD, and the ~FDCCS chip select. Using these lines the 80C88 can read the status of the internal FDC registers or write to the registers.

FDC Adjustments and Control Signals

When the ~TEST output of the Disc Latch is driven low the FDC is put in a calibration mode and the VCO, WPW, and RPW signals can be adjusted using pots A3R2 and A3R3, and variable capacitor A3C11.

The FDC issues DREQ to the DMA Controller during DMA transfers when its internal data register has data ready to transfer, or when it is empty and ready to receive data.

FDCINT is the FDC's interrupt output which is monitored by the PIC (A3U306). FDCINT goes high at the completion of any command.

Floppy Drive Control Signals

The following signals are sent to the micro floppy disc drive from the A3 Disc Controller Assembly. They are used to initiate control and send data from the FDC (A3U600) to the Micro Floppy Disc Drive via A3U803 and A3U703.

~DRIVESEL (A3U803-2)

The select lines provide the mean to enable/disable all other interface lines. When the ~DRIVESEL line is true (low), the drive is enabled and is considered active. When the ~DRIVESEL line is false (high), all controlled inputs are ignored and all drive lines are disabled.

~MOTON (A3U803-5)

The disc motor is in a rotating mode at the falling edge of ~MOTON only when the drive is selected and continues to be in the same mode even if the drive is not selected. The disc motor starts rotating when a disc is inserted during this mode. The disc motor is in a non-rotating mode at the rising edge of ~MOTON only when the drive is selected. In this mode, the disc motor does not rotate even when a disc in inserted.

~STEP (A3U703-3)

A true (low) pulse on this line will cause the access to move the read/write head to the adjacent track. The direction of the motion is determined by the ~DIRECTION input at the trailing edge of the pulse. The drive should be able to seek to track 00 under control of the system even if there is no disc inserted at the time.

~DIRECTION (A3U703-5)

A false (high) level on this input will cause a STEP input to move the read/write head away from the disc spindle. A true (low) level will cause a STEP input to move the read/write head toward the drive spindle.

~HDSEL (A3U803-6)

A true (low) level on this input will cause Head 1 (upper) to be selected. A false (high) level on this input will cause Head 0 (lower) to be selected.

~WRGATE (A3U703-7)

When this line is true (low), the write current circuits are enabled and information may be written under control of the ~WRDATA output.

~WRDATA (A3U703-9)

A true pulse (low) causes a bit to be written on the disc if ~WRGATE is true (low). Pulses will not appear on this line when ~WRGATE is a false (high) level. No write pre-compensation will be required.

~CHGRES (A3U803-9)

When this line is low at the drive selected condition, and when a disc is installed, ~DISCCHG signal will be made false (high).

~INUSE (A3U703-12)

The disc drive LED is turned on at the falling edge of ~INUSE only when the drive is selected and continues to be on even when the drive is not selected. The disc drive LED is turned off at the rising edge of ~INUSE only when the drive is selected.

Floppy Drive Interface Signals

The following signals are sent from the Micro Floppy Disc Drive to the A3 Disc Controller Assembly. They are used to initiate drive feedback control and return data to the FDC (A3U600). The interface devices used for these signals are A3U603 and A3U703.

~INDEX (A3U603-8)

A true (low) pulse is to be provided for each revolution of the disc motor when the drive is selected and ~DRRDY signal is low (true).

~TRK0 (A3U603-11)

This line is true (low) when the read/write head is positioned on track 00 or on an outer position of track 00. It will be made false (high) otherwise. This track 00 indicator is derived from a sensor and not as a result of a track position counter.

~WRPRT (A3U603-13)

This line is true (low) if a disc which is write protected is installed. This line will be false (high) otherwise.

~RDDATA (A3U603-15)

A true (low) pulse is provided on this line for each bit detected on the disc when the drive is selected and ~DRRDY signal is low (true).

~DISCCHG (A3U603-17)

This line will be true (low) at power on and whenever a disc is removed from the drive. The line will remain true (low) until both the following conditions have been met:

A. A disc is installed, and
B. A ~STEP pulse or ~CHRES signal has been received when the drive is selected.

~DRRDY (A3U703-6)

This line is true (low) while the following conditions are met.

A. The drive is selected,
B. A disc is inserted,
C. The ~Index period of the disc drive motor stabilizes within 100 ms +/- 2.5%.

8-16. HP 4951C TROUBLESHOOTING

Servicing the HP 4951C Protocol Analyzer takes in account several troubleshooting techniques. A variety of electronic instrumentation is recommended as tools to help determine and isolate instrument problems. The following sections briefly discuss some topics that you need to be aware of while troubleshooting the HP 4951C.

Digital Signature Analysis

DSA is a form of troubleshooting that has been used in industry for years. The majority of the troubleshooting procedures for the HP 4951C utilize DSA. DSA techniques are used primarily in digital circuitry that is under some type of CPU control.

NOTE

Jumper A1E314 should be moved to the 'N' position instead of the 'T' position when using the SA Tables on Revision A main boards.

Key Data

Key Data is a term that refers to specific node or signature values that should be checked first within the specific DSA table being used. Usually key data nodes are the nodes that are at the end of the chain. All other nodes in the chain eventually lead to the key data nodes. Checking the key data generally will tell the user if there is a problem within that block of circuitry.

Totalized Measurements

One of several modes of the HP 5005A/B Signature Multimeter is the totalized mode. This type of measurement is used throughout the DSA procedures for the HP 4951C. It is primarily used to measure control signal activity. Valid signatures cannot be generated on control signals, therefore the use of Totalization was implemented to do so. Each DSA table has a legend to show the symbol which is used to mark the node that is used for the measurement.

Frequency Measurements

Another mode of the HP 5005A/B Signature Multimeter is the frequency mode. This configures the Multimeter as a frequency counter and allows for accurate measurement of CPU clocks or similar signals. This node is used in a variety of places in the DSA procedures for the HP 4951C. Each DSA table has a legend to show the symbol used to mark the node that is used for the measurement.

Standard Unit VS Katakana Unit

The HP 4951C is built in two similar versions - Standard and Katakana. The instrument firmware differs in each unit. Several of the DSA procedures result in different results. The DSA procedures that differ are associated with the memory contents and some display information. This manual provides both versions of DSA tables. In many cases the same DSA routine can be used for both Standard and Katakana instrument configurations. The procedures that are different are marked by the PCA title in the upper right hand corner of the DSA table. They are denoted by - KATAKANA OPT.3 ONLY.

DSA Procedures where IC pins are removed from Sockets

There are several DSA procedures that call out in the set up to leave certain IC pins out of the sockets. Doing this allows the pins to be removed from an associated bus. True data contents of the device can then be measured. Using these procedures should only be used to verify that the ROM is the true failure. The PV tests should have flagged an error associated with that ROM. You should previously verify the address/data and control to the device before using the DSA that calls out bending the IC legs. Reserve such type tests as a last resort to verify the failure in the instrument.

HP 4951C Service Kit

A Service Kit for the HP 4951C is available that provides the user with several troubleshooting accessories that are helpful in needed to diagnose and repair the instrument. Refer to section I of this manual for a parts list of the Service Kit.

Typical Troubleshooting Setups

Following are several figures that show the typical use of some of the items included in the HP 4951C Service Kit.

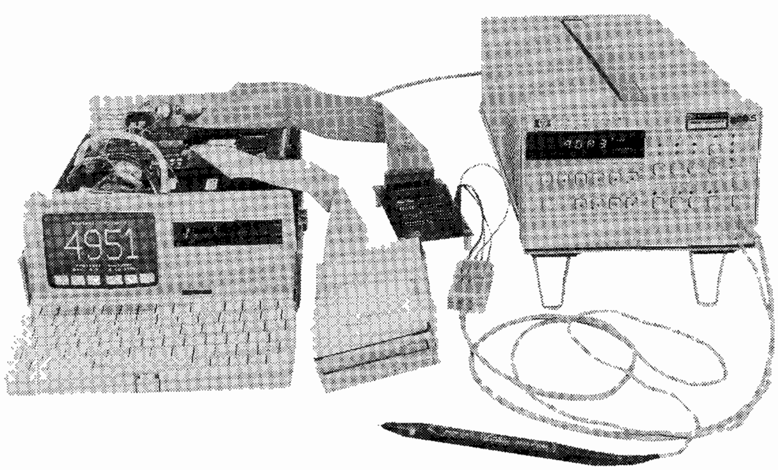


Figure 8-1. A3 Disc Controller Troubleshooting

Figure 8-1 illustrates the use of the Disc System Service Assembly and the Disc Drive Extender Cable. Note the Signature Multimeter connection points are located on the Disc System Service Assembly.

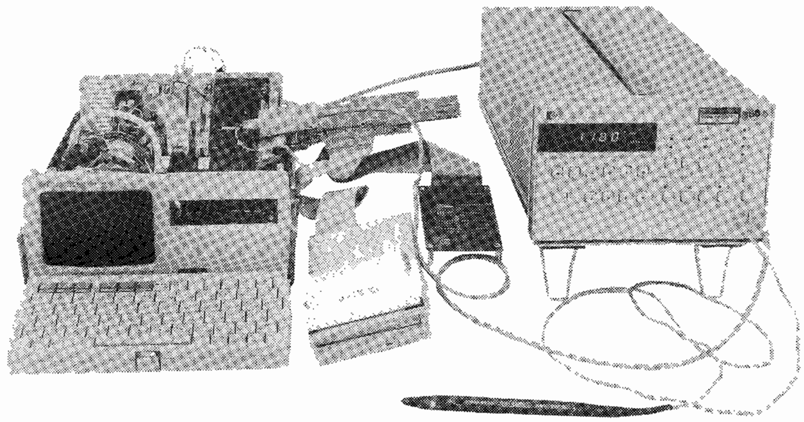


Figure 8-2. A2 Memory Board Troubleshooting

Figure 8-2 shows how the A3 Disc Controller Board and Disc Drive can be moved from the system and still operate properly. The intent of this figure is to show typical use of the IC clips provided in the HP 4951C Service Kit.

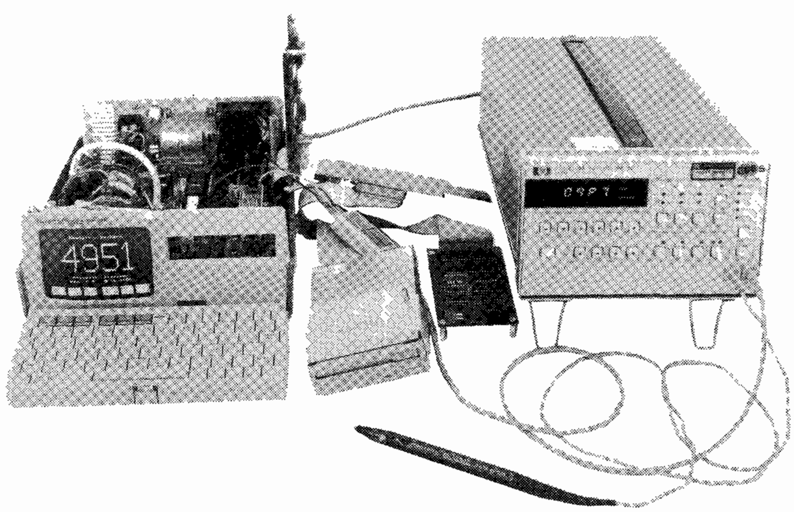


Figure 8-3. A1 Main Board DSA Troubleshooting

Figure 8-3 shows how the A2 board can be positioned vertically, allowing room to access the A1 main board assembly. Positioning of the A2 board is obtained by inserting the right hand corner tab of the A2 PC board into the slot in the lower case half. The tension provided by the bus cable is usually adequate to hold the A2 board in place. Note that IC clips are used on the A1 assembly.

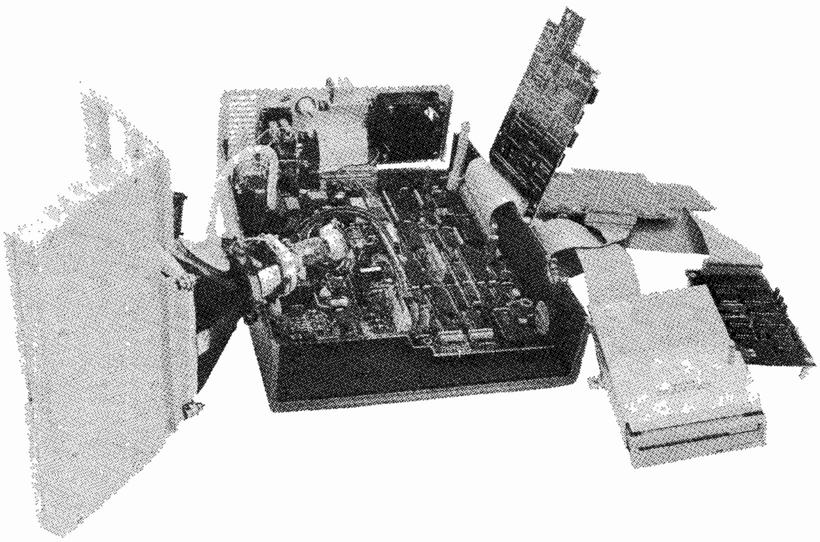


Figure 8-4. A1 Main Board Analog Troubleshooting

Figure 8-4 illustrates that the instrument can be fully spread out. Functionality is now limited due to the fact that the keyboard cable is not connected to the A1 main board. This setup is ideal for access into the CRT analog circuitry which is located below the CRT/YOKE assembly. Note that like the front panel, the rear panel can be removed and positioned away from the lower case half. This provides a means of accessing the power supply area which is normally congested by the line module assembly located on the rear panel.

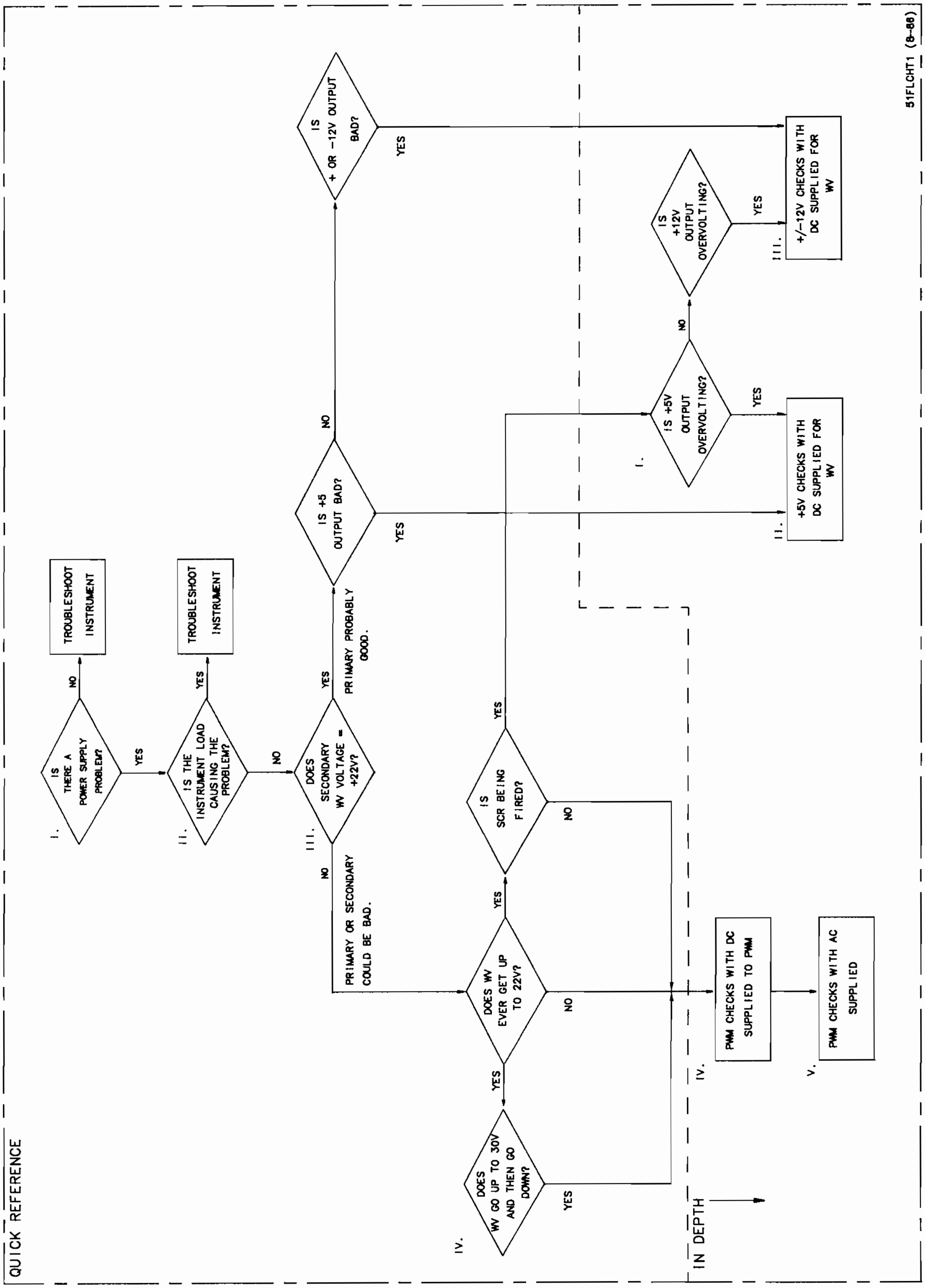


Figure 8-5. Power Supply Troubleshooting Overview

8-17. POWER SUPPLY TROUBLESHOOTING

The flow chart in Figure 8-5 is an overview of the troubleshooting procedures for the HP 4951C Power Supply. There are two general levels: Quick Reference Troubleshooting and In Depth Troubleshooting. The Quick Reference Troubleshooting is used to isolate the failure to a circuit level and the In Depth Troubleshooting is used to locate the failing circuit. The Power Supply Waveforms referenced here are located at the end of this section.

To begin troubleshooting go to the Power Supply Quick Reference Troubleshooting section.

8-18. POWER SUPPLY - QUICK REFERENCE TROUBLESHOOTING

The level of the secondary WV voltage is checked first. If WV is approximately +22 volts, the primary of the power supply is probably working and the secondary is troubleshot using the In Depth Troubleshooting procedure. If the WV voltage is not +22 volts, either the primary or the secondary could be bad. Once it determined which part of the supply is failing, the In Depth Troubleshooting procedure is used on the failing circuit.

CAUTION

Use an isolation transformer when troubleshooting any of the primary circuits with ac line voltage.

CAUTION

Secondary ground is NOT the same as primary ground.

I. <u>Symptoms:</u> **No Display or No Beeps at power on.**
<u>Action:</u> **Determine if there is a power supply failure by checking the fuse and output voltages.**

A. Check the fuse. If it is open, replace it and begin troubleshooting the Power Supply.

B. Following the disassembly procedures in Section VI and using a component locator, locate the power supply section on the A1 Main Board.

C. With ac line power supplied (120 vac or 240 vac), check the following output voltages:

A1TP203	+5.05 volts +-3%	(+4.90 to +5.20 volts)
A1TP204	+11.95 volts +-2.5%	(+11.65 to +12.25 volts)
A1TP308	-12 volts +-5%	(-11.40 to - 12.60 volts)
A1CR21 (Anode)	NMI approximately +4.28 volts (WV voltage minus the drop from zener A1CR21)	

D. If ALL the voltages in step c are correct, the problem is NOT in the power supply. Troubleshoot the instrument circuitry.

E. If ONLY the NMI voltage is incorrect troubleshoot the Power Fail Sense Circuit.

F. If ANY of the other voltages (+5, +12, or -12) are incorrect, go to the Quick Reference Troubleshooting step II.

II. Symptoms: At least one output voltage is bad when the instrument load is connected to the power supply.
Action: Determine if the instrument load is causing the problem by isolating the power supply and rechecking the output voltages.

A. Turn the power supply off and disconnect the HP 4951C instrument load from the power supply by removing the following jumpers:

A1XE307 (+5V)
A1XE308 (+12V)
A1XE309 (-12V)

B. Connect a 30 ohm/20 watt load between A1TP205 (WV) and secondary ground A1U105-4. Note that secondary ground is NOT the same as primary ground. One 20 ohm/20 watt resistor (part number 0811-1656) and one 10 ohm/20 watt resistor (part number 0811-1655) can be connected in series if a 30 ohm resistor is not available.

C Turn the ac back on and recheck the output voltages. If all the voltages are now correct, the problem is in the instrument load. Troubleshoot the instrument circuitry.

D. If at least one output voltage is bad, go to the Quick Reference Troubleshooting step III.

III. Symptoms: At least one output voltage is bad when the power supply is isolated.
Action: Determine whether the primary or the secondary is causing the problem by checking the secondary voltage at WV A1TP205.

Under normal operation, the primary supplies enough voltage on the secondary of A1T201 to produce approximately +22 vdc at WV (A1TP205). WV is stepped down to produce the +5, +12, and -12 volt outputs. If WV is +22 volts, the primary is probably working. If WV is not +22 volts, either the primary or the secondary could be failing.

A. Isolate the power supply from the instrument load by removing jumpers A1XE307, A1XE308, and A1XE309. Connect a 30 ohm load between WV A1TP205 and secondary ground A1U105-4.

B. Disconnect the ac line from the power supply. Connect ac to the HP 4951C through an isolation transformer, but do not turn the power on.

C. The rear panel can be pulled away from the instrument so that the power supply will be easier to access by unplugging the cables from A1J5, A1XE609, A1J2, and a1e208

D. Connect an oscilloscope between WV A1TP205 and secondary ground A1U105-4. Set the volts/div at 10 volts.

E. Turn the ac up to 110 or 240 vac through the isolation transformer, and watch the WV voltage on the oscilloscope. If the voltage goes up to +22 volts and stays there, the primary is probably good. Go to the In Depth Troubleshooting step II if the +5 volt output is bad. Go to the In Depth Troubleshooting step III if the +12 and/or the -12 volt outputs are bad.

F. If WV does not go up to +22 volts and stabilize, go to the Quick Reference Troubleshooting step IV.

IV. Symptoms: WV does not come up to +22 volts and stabilize.
Action: Determine whether the primary or the secondary is failing by watching how high WV goes at power on.

A. Cycle the ac power and watch the WV level closely. If the WV voltage never goes up to +22 volts, go to the In Depth Troubleshooting step IV to check the primary circuits.

B. If WV goes greater than approximately 30 volts, the secondary Overvoltage Sense circuit will fire the SCR Crowbar. Go to the In Depth Troubleshooting step IV to check the primary circuits.

C. If WV goes up to +22 volts and then goes down, the +5 or +12 volt supplies could be causing an overvoltage to fire the SCR Crowbar.

D. Connect an oscilloscope to the anode of A1CR8 with the volts/div set at 1 volt. This point is normally low. The voltage will rise to about +.8 volts to trigger the SCR if there is an overvoltage. Cycle the power and see if the SCR is being fired. If it is, go to the In Depth Troubleshooting step I to check the SCR.

E. If the SCR is not being fired, go to the In Depth Troubleshooting step IV to check the primary circuits.

8-19. POWER SUPPLY - IN DEPTH TROUBLESHOOTING

CAUTION

Use an isolation transformer when troubleshooting any of the primary circuits with ac line voltage.

CAUTION

Secondary ground is NOT the same as primary ground.

I. Symptoms: WV goes to +22 volts, but the SCR fires and shuts the supply down.
Action: Determine if the +5 or +12 volt outputs are overvolting, or if the SCR is bad

If the SCR is being triggered, either an overvoltage condition exists, or the Overvoltage Sense or SCR circuits are bad. A 5.62 volt zener monitors the +5 volt output, a 13 volt zener monitors the +12 volt output, and a 30 volt zener monitors the WV voltage. If any of these zeners are forced into an avalanche condition by an overvoltage, their common anode connection will trigger the SCR Crowbar Circuit. If no overvoltage exists and the SCR Crowbar Circuit is still firing, the transistor that drives the SCR gate could be bad (A1Q207), or the SCR could be bad.

A. Disconnect ac from the power supply. Connect a dc supply capable of supplying +20 vdc, 3 amps between WV A1TP205 and secondary ground A1U105-4.

B. Remove jumpers A1XE307, A1XE308, and A1XE309 to isolate the power supply from the rest of the instrument. Connect a 30 ohm/20 watt load between A1TP205 (WV) and secondary ground A1U105-4. Note that secondary ground is NOT the same as primary ground. One 20 ohm/20 watt resistor (part number 0811-1656) and one 10 ohm/20 watt resistor (part number 0811-1655) can be connected in series if a 30 ohm resistor is not available.

C. Disable the SCR by shorting the SCR trigger to secondary ground. The easiest way to do this is to short the anode of A1CR8 to A1U105-4.

D. Monitor the +5 volt output while turning the dc supply up to +22 volts. If it goes higher than +5 volts, turn the dc supply off and go to the In Depth Troubleshooting step II.

E. Monitor the +12 volt output while turning the dc supply up to +22 volts. If it goes higher than +12 volts, turn the dc supply off and go to the In Depth Troubleshooting step III.

F. If neither the +5 or +12 volt circuits are overvolting, remove the short from the anode of A1CR9. Disconnect the dc supply from WV A1TP205 and disconnect the 30 ohm load from between WV and secondary ground.

G. Connect the dc supply between +5 A1TP203 and secondary ground A1U105-4. Connect a voltmeter to the same points. Slowly turn the supply up towards +5.62 volts. When the dc supply reaches approximately +5.62 volts, zener A1CR7 should pull the supply voltage down to about +2.9 volts. If the supply voltage is pulled down before it reaches +5.62 volts, replace the zener.

H. Connect the dc supply between +12 A1TP204 and secondary ground A1U105-4. Connect a voltmeter to the same points. Slowly turn the supply up towards +13 volts. When the dc supply reaches approximately +13 volts, zener A1CR8 should pull the supply voltage down to about +2.7 volts. If the supply voltage is pulled down before it reaches +13 volts, replace the zener.

I. Connect the dc supply between WV A1TP205 and secondary ground A1U105-4. Connect a voltmeter to the same points. Slowly turn the supply up towards +30 volts. When the dc supply reaches approximately +30 volts, zener A1CR9 should pull the supply voltage down to about +.88 volts. If the supply voltage is pulled down before it reaches +30 volts, replace the zener.

II. Symptoms: +5 volt output is bad.
Action: Check the +5 volt circuits by running the secondary with dc supplied to WV.

A. Disconnect ac from the power supply. Connect a dc supply capable of supplying + 20 vdc, 3 amps between WV A1TP205 and secondary ground A1U105-4.

B. Remove jumpers A1XE307, A1XE308, and A1XE309 to isolate the power supply from the rest of the instrument. Connect a 30 ohm/20 watt load between A1TP205 (WV) and secondary ground A1U105-4. Note that secondary ground is NOT the same as primary ground. One 20 ohm/20 watt resistor (part number 0811-1656) and one 10 ohm/20 watt resistor (part number 0811-1655) can be connected in series if a 30 ohm resistor is not available.

C. Turn the dc supply up to +22 volts and check for the following voltages and waveforms in the +5 volt circuitry.

D. A1U105 pin 6 should be +22 volts.

E. A1U105 pin 2 should be approximately 7 volts.

F. A1U105 pin 3 should have a sawtooth waveform (waveform A - A1U105-3). If it does not, A1U105 is bad or in current limit, or the timing capacitor (A1C23) is bad.

G. A1U105 pins 1 and 8 should look like waveform C (A1U105-8).

H. A1U105 pin 7 should be within .3 volts of the voltage at pin 6.

I. The gates of the switching FETs (A1Q106 and A1Q107) should look similar to A1U105 pin 8.

J. The drains of the FETs should be switching between about -0.5 volts and +22 volts as in waveform E (A1Q107-D). It is easiest to access this point at the cathode of A1CR4. If this point is bad, then the FETs or the clamp diode could be bad.

K. If the FET drains are switching properly but there is no +5 volt output, check A1L2. If there is some output, check the feedback path (A1CR6 and part of A1R107) to A1U105 pin 5. The voltage at pin 5 should be approximately +1.25 volts.

III. Symptoms: +12 volt output is bad.
Action: Check the +/-12 volt circuits by running the secondary with dc supplied to WV.

A. Disconnect ac from the power supply. Connect a dc supply capable of supplying + 20 vdc, 3 amps between WV A1TP205 and secondary ground A1U105-4. Note that secondary ground is NOT the same as primary ground.

B. Remove jumpers A1XE307, A1XE308, and A1XE309 to isolate the power supply from the rest of the instrument. Connect a 30 ohm/20 watt load between A1TP205 (WV) and secondary ground A1U105-4. Note that secondary ground is NOT the same as primary ground. One 20 ohm/20 watt resistor (part number 0811-1656) and one 10 ohm/20 watt resistor (part number 0811-1655) can be connected in series if a 30 ohm resistor is not available.

C. Turn the dc supply up to +22 volts and check for the following voltages and waveforms in the +/-12 volt circuitry.

D. A1U306 pin 6 should be +22 volts.

E. A1U306 pin 2 should be approximately +7 volts.

F. A1U306 pin 3 should have a sawtooth waveform (waveform B - A1U306-3). If it does not, A1U306 is bad or in current limit, or the timing capacitor (A1C40) is bad.

G. A1U306 pins 1 and 8 should look like waveform D (A1U306-8).

H. A1U306 pin 7 should be within .3 volts of the voltage at pin 6.

I. The gates of the switching FETs (A1Q405 and A1Q406) should be similar to A1U306 pin 8.

J. The drains of the FETs should be switching between about -0.5 volts and +22 volts as in waveform F (A1Q406-D). It is easiest to access this point at the cathode of A1CR20. If this point is bad, then the FETs or the clamp diode could be bad.

K. If the FET drains are switching properly but there are no +12 and -12 volt outputs, check A1T405. If there are some outputs, check the feedback path (A1CR17 and part of A1R108) to A1U306 pin 5. The voltage at pin 5 should be approximately +1.25 volts. If only the -12 volt output is bad, check the cathode of A1CR22. It should look like waveform G (A1T405-1, A1CR22-C).

IV. Symptoms: WV goes too high, not high enough, or does not stabilize at +22 volts.
Action: Check the primary Pulse Width Modulator (PWM) by running the PWM using a dc supply.

The primary of the power supply can fail for several different reasons:

- bad PWM chip
- initial start-up failures (PWM can't start up at all)
- restart or "hiccup" mode failures (PWM starts up but a failure causes it to shut down and continuously try to restart)

A. Disconnect ac from the power supply. Connect a dc supply capable of supplying +20 vdc, 3 amps between VG A1TP102 and primary ground A1TP202.

B. Lift the cathode of A1CR14 to isolate the primary from the secondary. By doing this, the primary should be able to run without a load.

C. While slowly raising the dc power supply to +15 volts, observe the current being drawn. Not more than 1 mA should be drawn while the voltage is less than +15 volts. Raise the dc supply to +17 volts and then quickly reduce it to +15 volts. The current being drawn should be approximately 20 mA.

D. A1U102 pin 8 (Vref) should be approximately +5 volts.

E. A1U102 pin 4 (Rt/Ct) should have an approximately 100 kHz sawtooth waveform as in waveform H (A1U102-4). If it does not, check the timing elements R4 and A1C3.

F. A1U102 pin 3 (ISENSE) should be low.

G. A1U102 pin 2 (vfb) should be about +5 volts. Turn the dc power supply off and ground pin 2 to enable the output pin 6. Turn the dc supply back on, raising the voltage to +17 volts as before, and then lowering the voltage to +15 volts. Pin 6 should now be approximately 100 kHz with an amplitude of +15 volts, as in waveform I(A1U102-6). Check the gates of A1Q102 and A1Q204 for the same waveform.

H. Once PWM operation is established using dc, the primary can be checked during ac operation. Go to In Depth Troubleshooting step V.

V. Action: Check the rest of the primary circuits using ac to run the primary.

CAUTION

Be sure to use an isolation transformer when troubleshooting any of the primary circuits with ac line voltage.

CAUTION

Secondary ground is NOT the same as primary ground.

A. To check the primary circuits under ac operation, disconnect the dc supply from VG A1TP102 and ground A1TP202 and connect ac power (120 or 240 vac) through an isolation transformer. If the cable that goes to A1J5 was unplugged before, it needs to be connected. The cathode of A1CR14 should still be lifted to isolate the primary from the secondary.

B. Check the voltage at VG A1TP102 (A1C1 charge storage). The voltage present here will give an indication of how the supply is starting up. Under normal operation the voltage at A1C1 should ramp up from 0 to 16 volts and stabilize at 16 volts. If this occurs the primary circuits are starting up correctly. Go to step e to check the rest of the primary circuits.

C. If the voltage at A1C1 does not charge to +16 volts, check for something broken at this node. Under normal operation, the rectified ac input (VWORKING) is divided down through A1R101, A1R102 and A1R103 to charge A1C1.

D. If the voltage at A1C1 resembles a triangular wave similar to waveforms J (A1U102-7) or K (A1U102-7), the primary circuits are in a continuous restart or "hiccup" mode. There are several conditions which can cause the "hiccup" mode:

- No load or insufficient load on the WV supply (this should not occur since we lifted the cathode of A1CR16)
- Primary PWM Control Circuit draws > 20 mA
- Primary drive disabled or excessively limited

E. A1U102 pin 8 (Vref) should be about +5 volts.

F. A1U102 pin 2 (vfb) should be low. Under normal operation, the rectified ac input (VWORKING) is divided down through A1R101, A1R102, A1R103, and A1R2 to drive the base of A1Q101. A1Q101 holds A1U102 off by keeping A1U102 pin 2 high until the ac input is high enough to reverse bias the base-emitter junction of A1Q102 (approximately 65 vac). At this point A1U102 pin 2 should go low.

G. A1U102 pin 3 (Isense) should be low. There are two paths that can pull pin 3 high and cause A1U102 to current limit. One path senses the current through the primary of A1T201 (A1Q204, A1R1, A1R6, A1R7, A1R8, and A1CR3). The other path monitors the magnitude of the rectified ac input voltage (VWORKING) as it charges A1C2. Under normal operation, the output at A1U102 pin 6 controls the gate of A1Q102. When A1U102 pin 6 is on (high), VWORKING should charge A1C2 to about 7 volts. This voltage is buffered and level shifted by A1Q103 and A1CR1. If the voltage at A1U102 pin 3 goes greater than 1 volt, A1U102 will current limit. When A1U102 pin 6 is off (low), A1Q102 switches A1C2 to ground. See waveforms U and V (A1Q103 - Base).

H. Compare A1U102 pin 4 to waveform L (A1U102-3).

I. Compare A1U102 output pin 6 to waveforms M (A1U102-6) and N (A1U102-6).

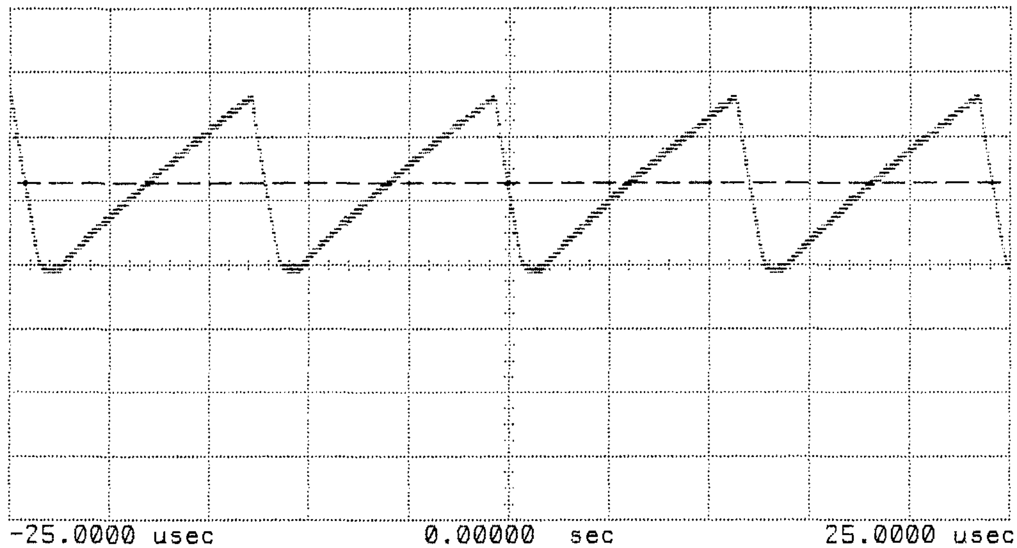
J. Compare the drain of A1Q204 to waveforms O (A1CR18-A) and P (A1CR18-A).

K. Compare A1T201 pin 4 to waveforms S (A1CR5-A) and T (A1CR5-A).

L. Compare A1T201 pin 7 to waveforms Q (A1L5) and R (A1L5).

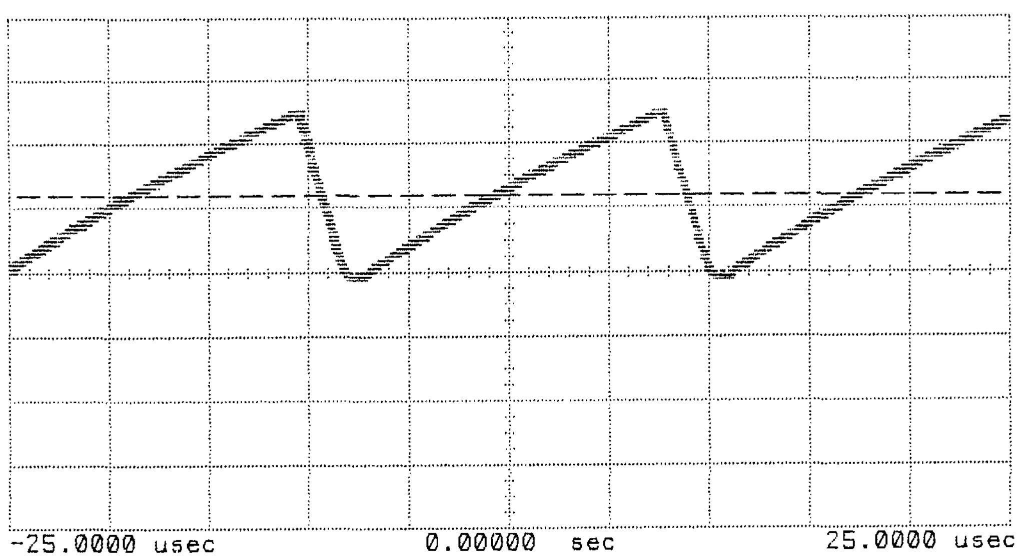
M. Once ac primary operation has been established with the secondary isolated, resolder the cathode of A1CR14, reconnect the 30 ohm load between WV A1TP205 and secondary ground A1U105-4, and try to run the power supply. The path from the secondary of A1T201 to WV was not checked when the primary was run with A1CR14 lifted, so it could still be bad.

N. If the power supply runs and all output voltages are correct, disconnect the 30 ohm load and reconnect the instrument load by installing jumpers A1XE307, A1XE308, and A1XE309.



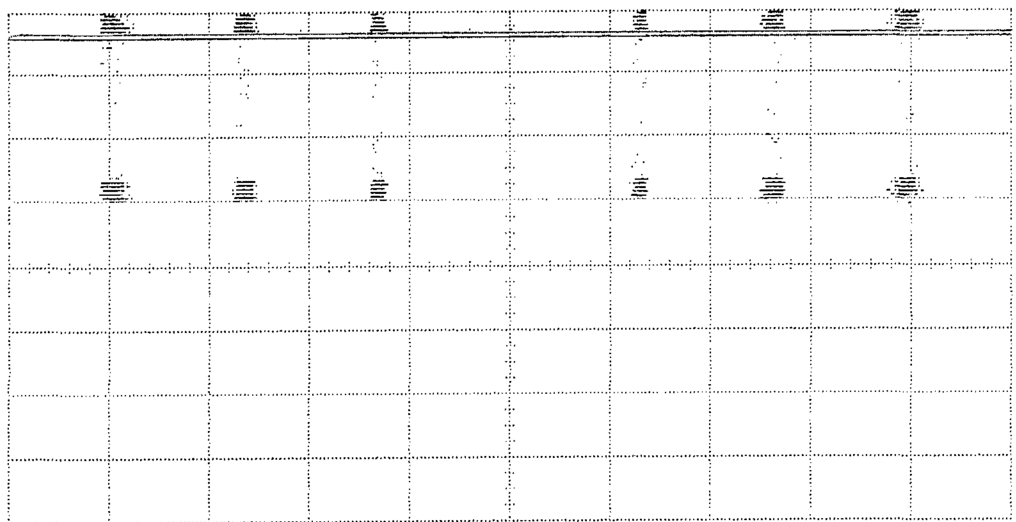
Ch. 1 = 500.0 mvolts/div Offset = 0.000 volts
Timebase = 5.00 usec/div Delay = 0.00000 sec
Ch. 1 Parameters Freq. = 82.6745 KHz

Power Supply Waveform A (A1U105-3)



Ch. 1 = 500.0 mvolts/div Offset = 0.000 volts
Timebase = 5.00 usec/div Delay = 0.00000 sec
Ch. 1 Parameters Freq. = 54.9796 KHz

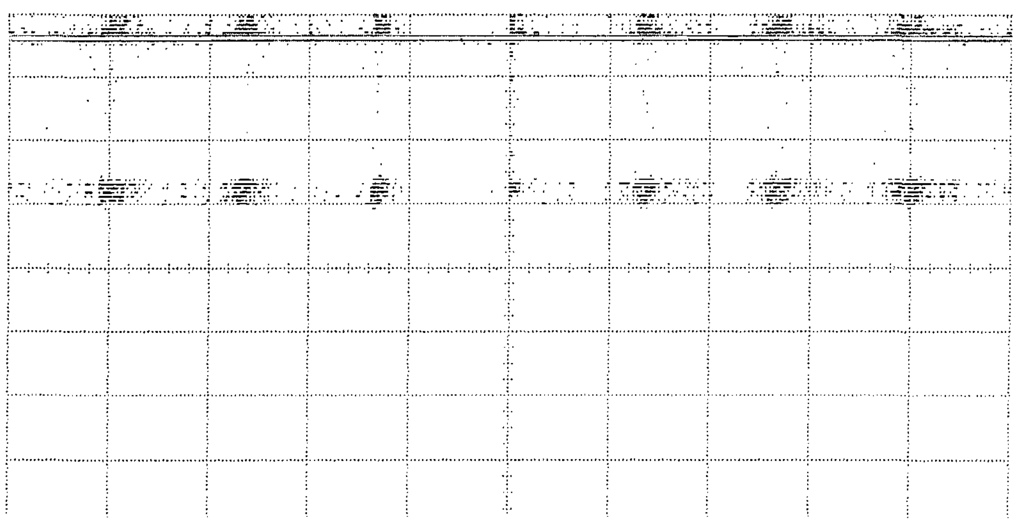
Power Supply Waveform B (A1U306-3)



-5.00000 msec 0.00000 sec 5.00000 msec

Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	1.00 msec/div	Delay	=	0.00000 sec

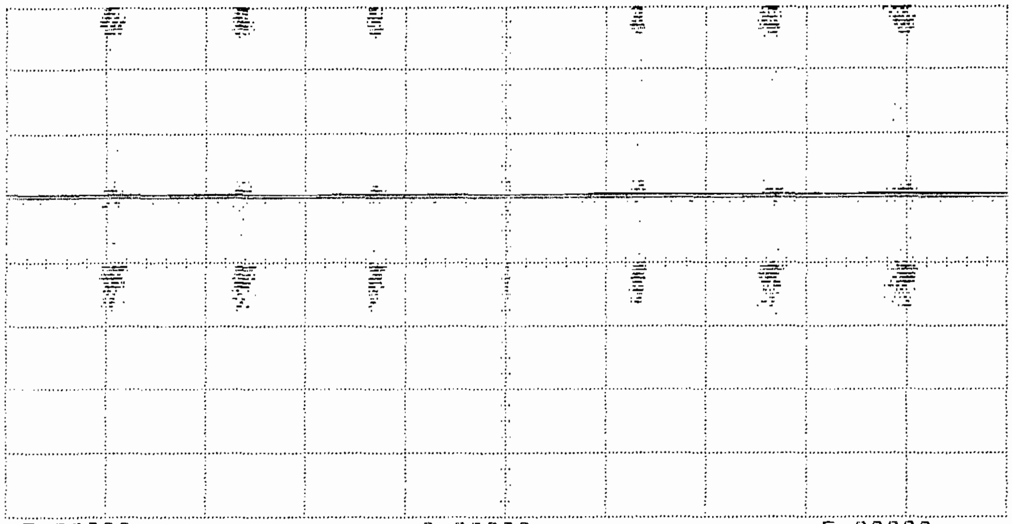
Power Supply Waveform C (A1U105-8)



-2.50000 msec 0.00000 sec 2.50000 msec

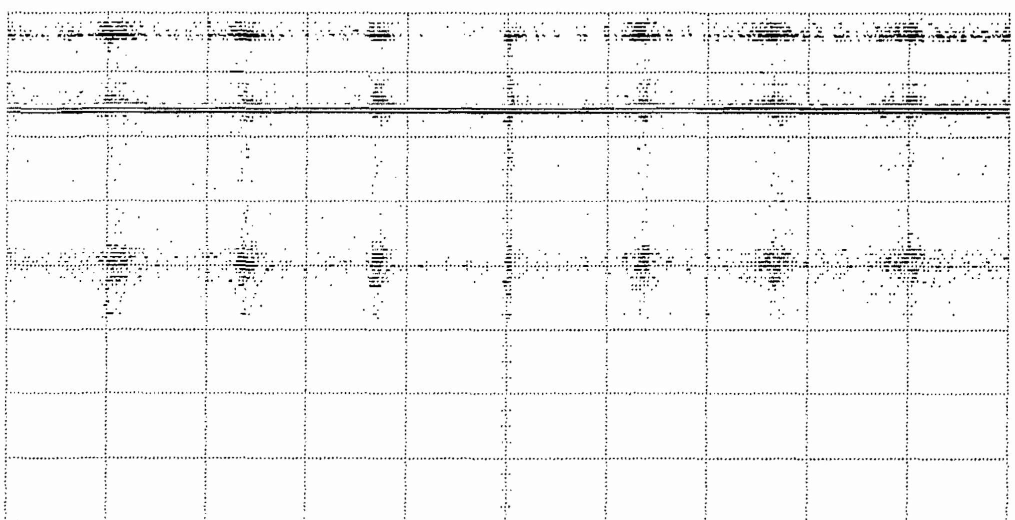
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	500 usec/div	Delay	=	0.00000 sec

Power Supply Waveform D (A1U306-8)



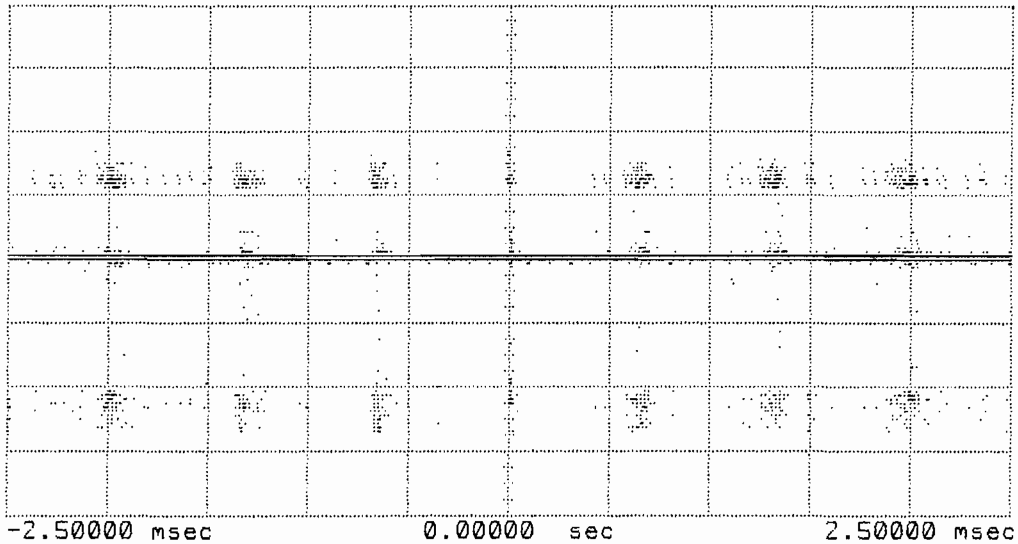
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	1.00 msec/div	Delay	=	0.00000 sec

Power Supply Waveform E (CR4 - Cathode)



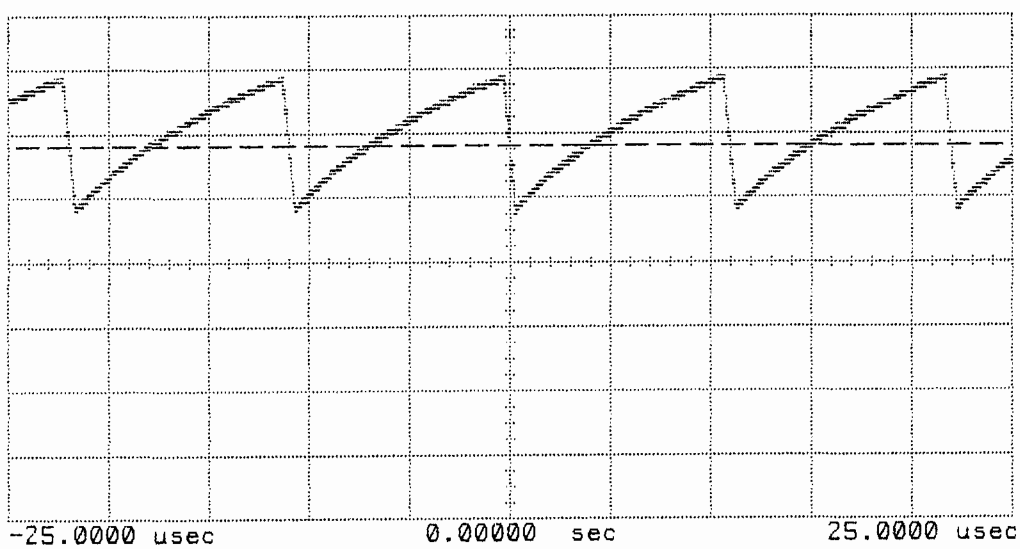
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	500 usec/div	Delay	=	0.00000 sec

Power Supply Waveform F (CR20 - Cathode)



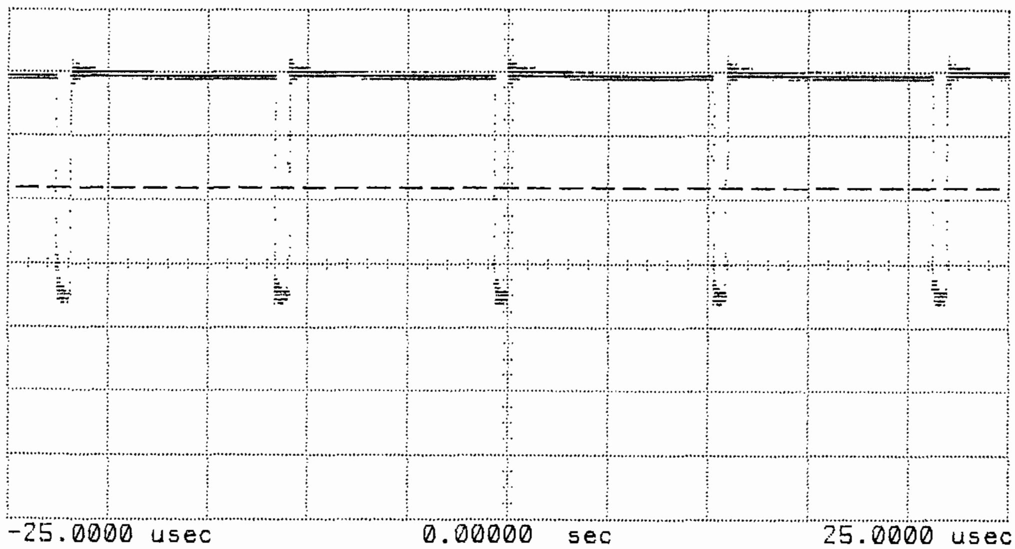
Ch. 1 = 5.000 volts/div
Timebase = 500 usec/div
Offset = 0.000 volts
Delay = 0.00000 sec

Power Supply Waveform G (CR22 - Cathode)



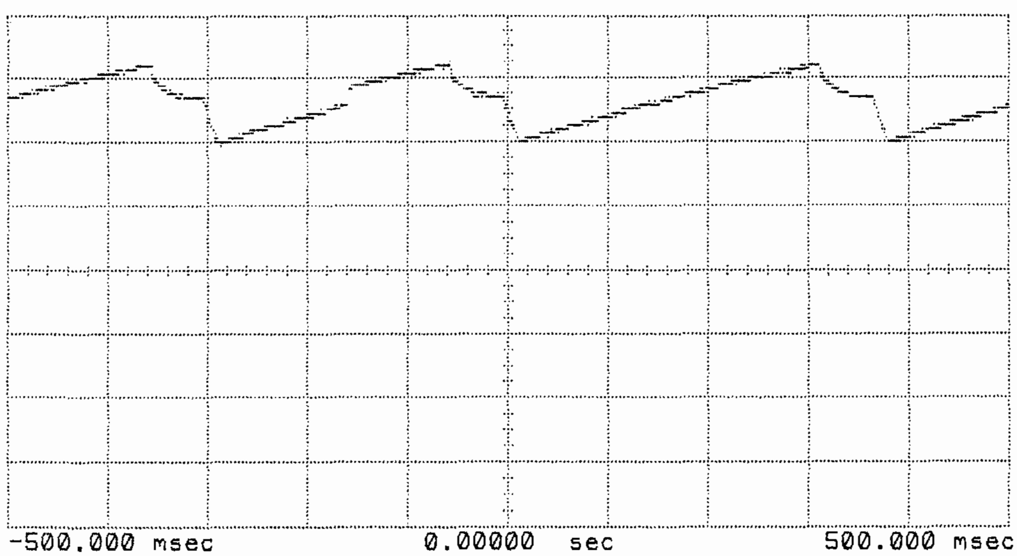
Ch. 1 = 1.000 volts/div
Timebase = 5.00 usec/div
Ch. 1 Parameters
Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 91.0924 KHz

Power Supply Waveform H (A1U102-4)



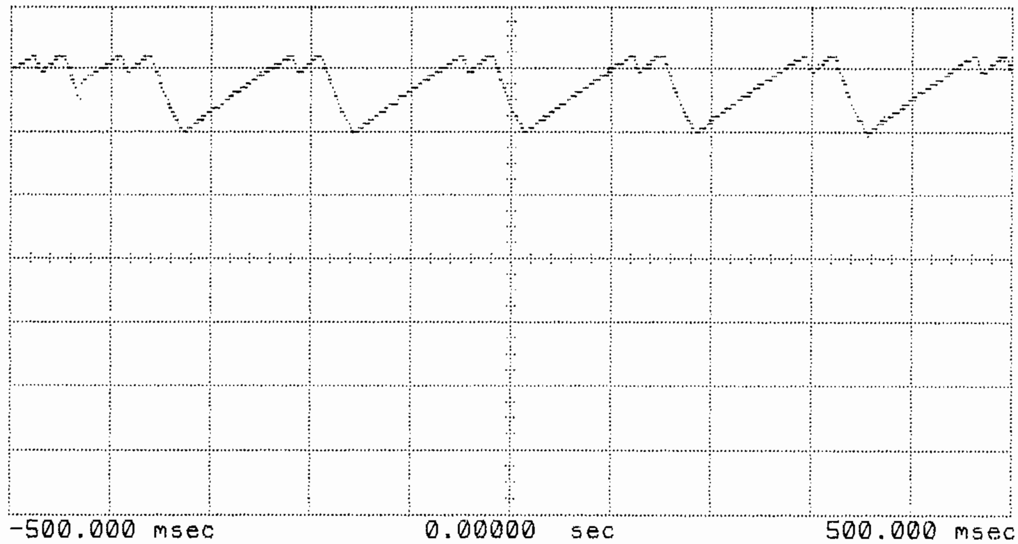
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	91.4217 KHz

Power Supply Waveform I (A1U102-6)



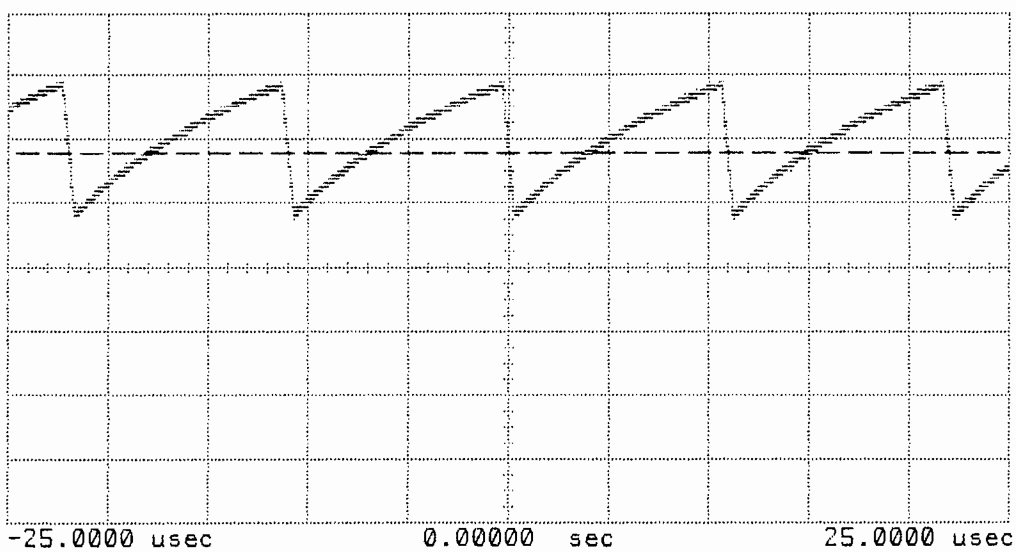
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	100 msec/div	Delay	=	0.00000 sec

Power Supply Waveform J (A1U102-7, 110 vac)



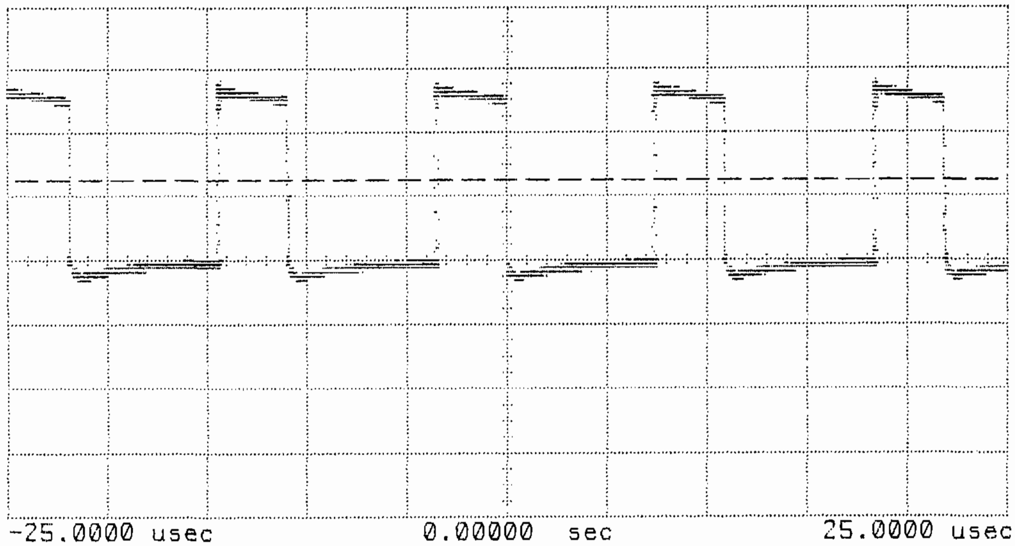
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	100 msec/div	Delay	=	0.00000 sec

Power Supply Waveform K (A1U102-7, 240 vac)



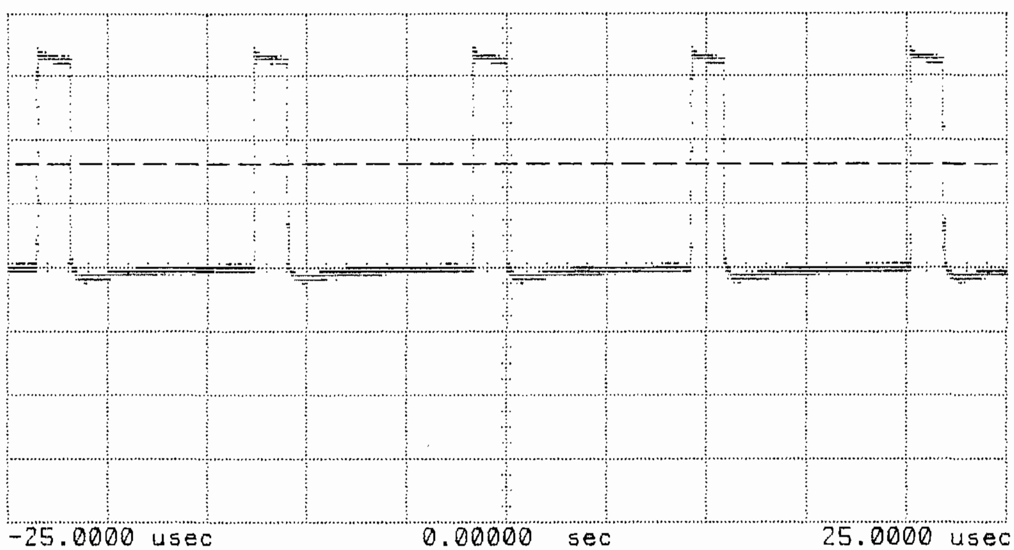
Ch. 1	=	1.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	91.0803 KHz

Power Supply Waveform L (A1U102-4 - same for 110 & 240 vac)



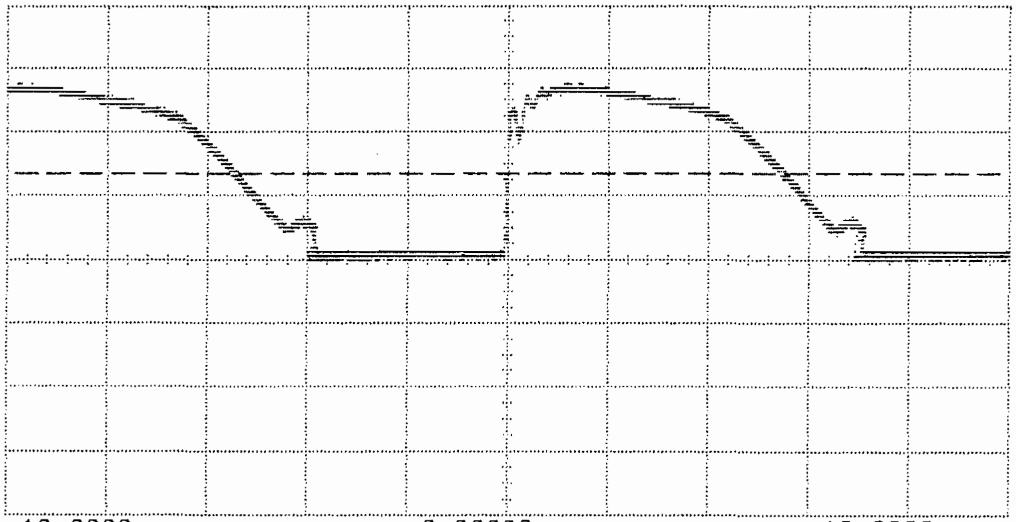
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	91.4734 KHz

Power Supply Waveform M (A1U102-6, 110 vac)



Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	91.4374 KHz

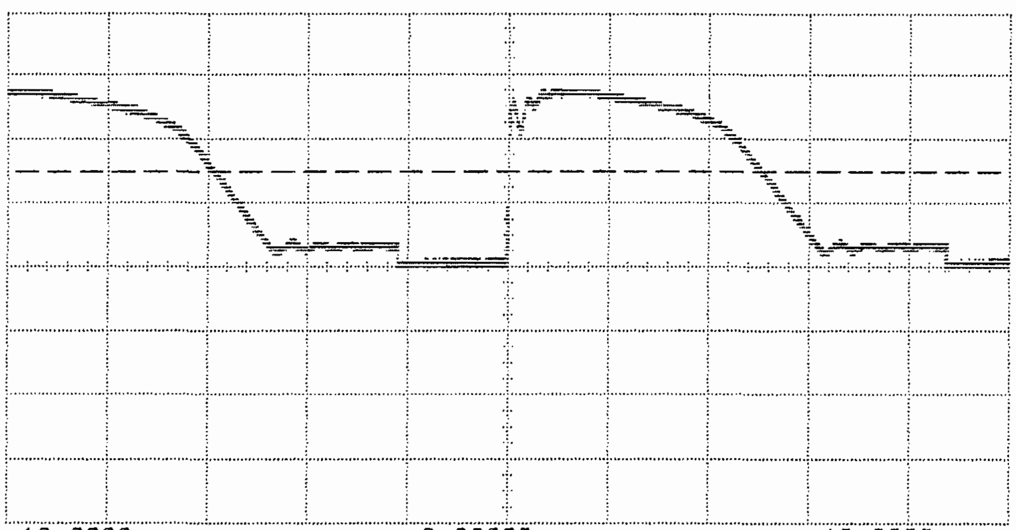
Power Supply Waveform N (A1U102-6, 110 vac)



-10.0000 usec 0.00000 sec 10.0000 usec

Ch. 1	=	50.00 volts/div	Offset	=	0.000 volts
Timebase	=	2.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	92.0442 KHz

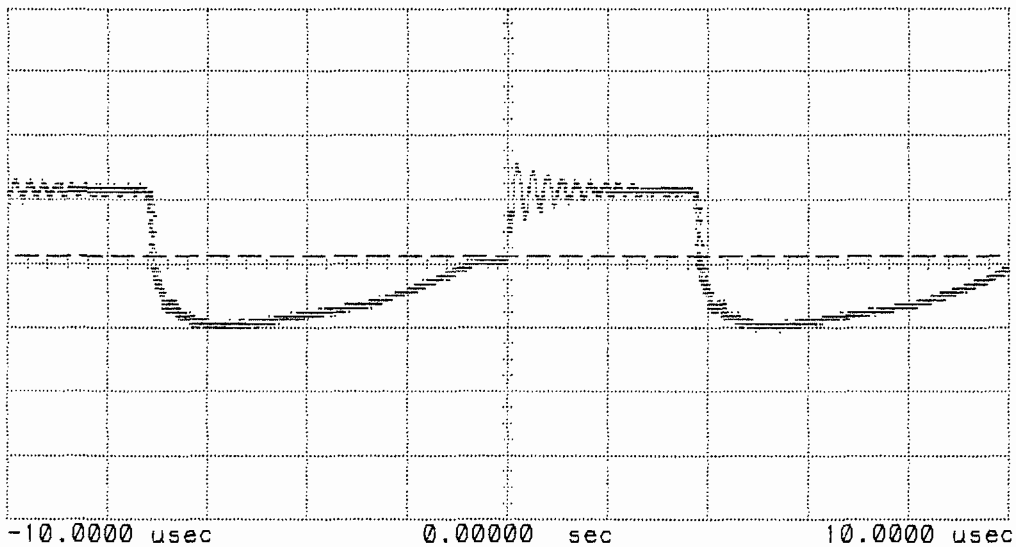
Power Supply Waveform O (A1CR18 - Anode, 110 vac)



-10.0000 usec 0.00000 sec 10.0000 usec

Ch. 1	=	50.00 volts/div	Offset	=	0.000 volts
Timebase	=	2.00 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	91.7177 KHz

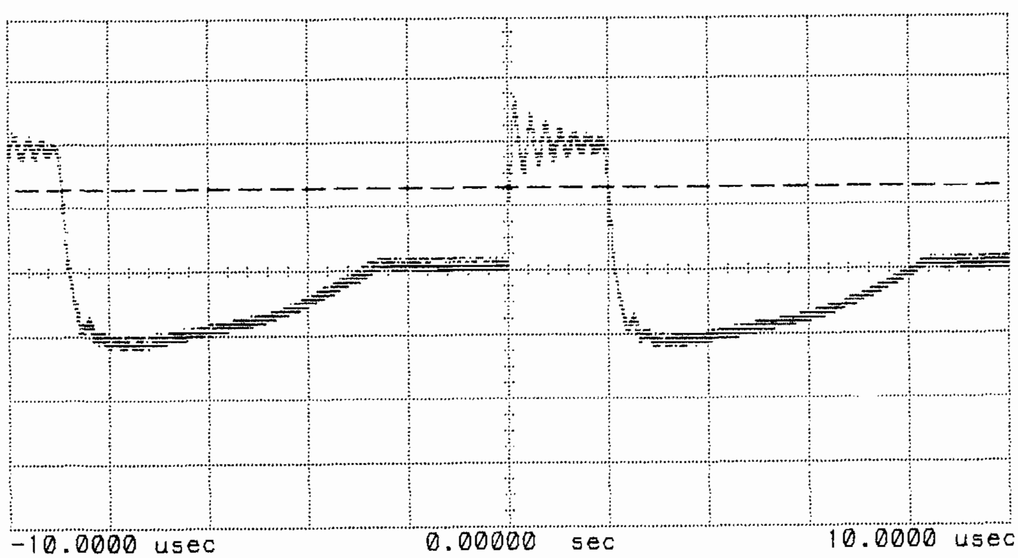
Power Supply Waveform P (A1CR18 - Anode, 240 vac)



Ch. 1 = 50.00 volts/div
Timebase = 2.00 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 91.3521 KHz

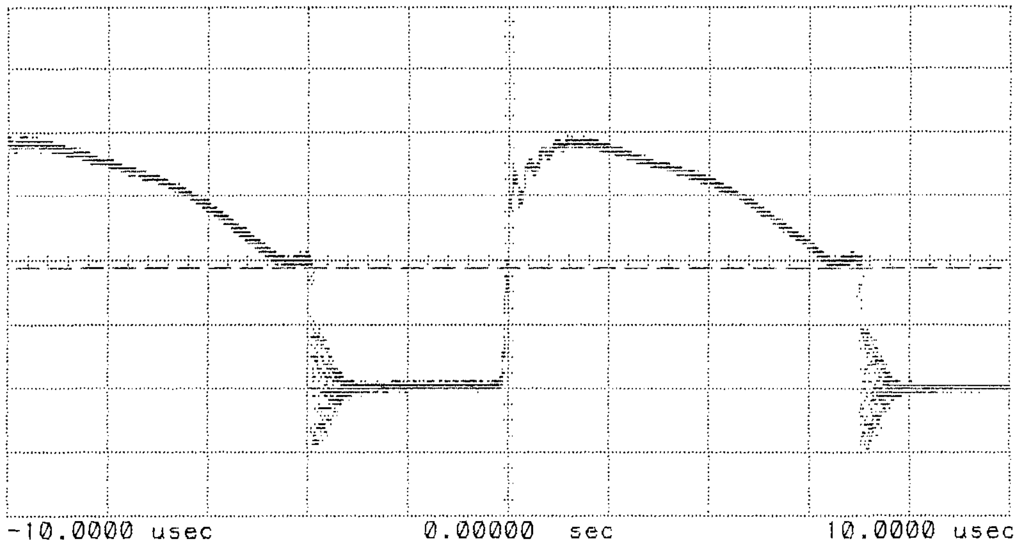
Power Supply Waveform Q (A1L5, 110 vac)



Ch. 1 = 50.00 volts/div
Timebase = 2.00 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 91.4419 KHz

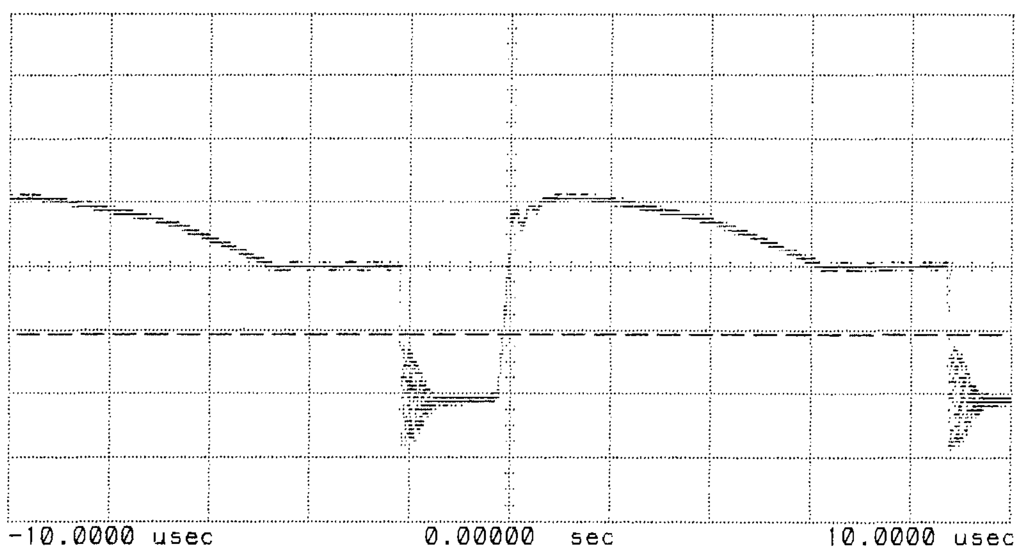
Power Supply Waveform R (A1L5, 240 vac)



Ch. 1 = 10.00 volts/div
Timebase = 2.00 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 91.9517 KHz

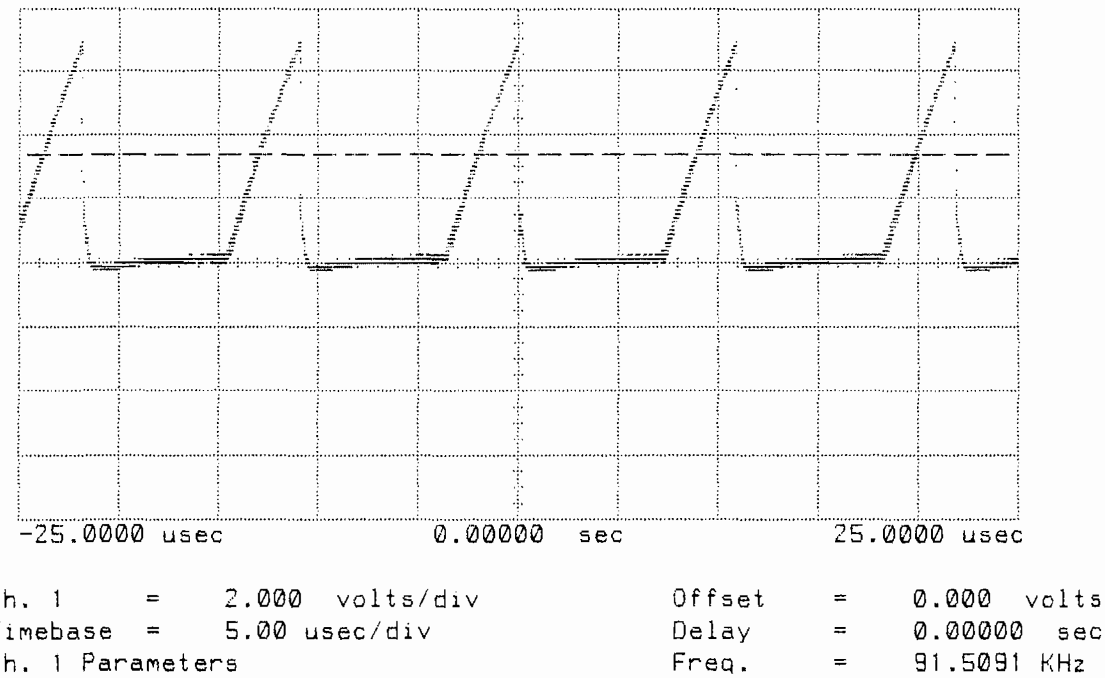
Power Supply Waveform S (A1CR5 - Anode, 110 vac)



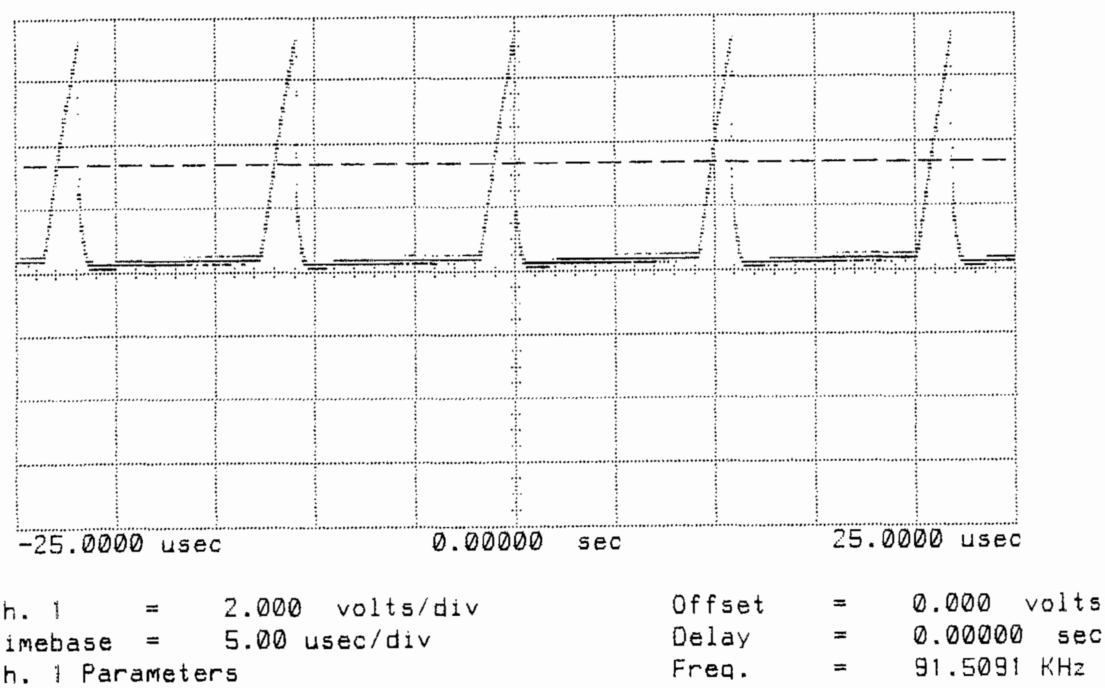
Ch. 1 = 20.00 volts/div
Timebase = 2.00 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 91.3751 KHz

Power Supply Waveform T (A1CR5 - Anode, 240 vac)



Power Supply Waveform U (A1Q103 - Base, 110 vac)



Power Supply Waveform V (A1Q103 - Base, 240 vac)

8-20. MICROPROCESSOR NO-OPS TROUBLESHOOTING (A1 - BUS, and Control)

The NSC800 Microprocessor No-op cycle is the central loop which forces the CPU to cycle in a continuous "free run" mode. During this test, the full 16 bit address range is exercised. This is accomplished by disconnecting the ~RD line from the CPU to the rest of the system (move A1E314 to the "T" position). Refer to this section for reference. The no-op routine is used in several other SA routines within the HP 4951C system.

This routine allows the lowest level of operation of the NSC800 system to be tested. Any failures associated with the circuitry being tested will cause failures in the lower levels of the Performance Verification Tests. You will want to use this routine when you get no beep or a continuous beep. This routine will function with the A1 board by itself or with any combination of the A2 and A3 boards installed. The A2 and A3 boards may be installed in any order on the main bus cable (J1) because it is a large parallel bus cable.

Sequence of Events

A. At power up, the CPU (A1U415) goes to address 00H. This signal is put onto the address bus. ~ALE is pulled low to latch the address to all devices on the bus.

B. The CPU then puts the AD0-AD7 bus in a tri-state mode to allow the data bus to be driven prior to the ~RD line being pulled low by the CPU. In this case AD0-AD7 is driven by an 8 bit latch (A1U215) which is enabled by ~RD from the CPU. This latch assures that during the read cycle AD0-AD7 will have a data value of 00H, which is seen as a "no-op" instruction to the CPU.

C. The CPU now drives ~RD low and AD0-AD7 is decoded by the CPU . If a no-op instruction (00H) is decoded, the CPU will increment its program counter and begin another opcode fetch cycle. The address bus A0-A15 is then exercised from 0000H to FFFFH. This process repeats each time a no-op instruction (00H) is read in to the CPU.

Circuitry Tested

These test conditions allow the bus structure to be tested through the Arbiter Multiplexers (A1U512, A1U513, & A1U713) and the Dual Port RAM address inputs (A1U411). The Transceiver (A1U613) is enabled to force signatures onto the Dual Port RAM (A1U411) data bus. Then latch A1U612 is enabled to force the no-op signatures onto the character data bus. This technique allows you to check the operation of the devices that interface with the different busses as well as checking continuity on the other busses. This test routine is also used to check the discrete circuitry of the DLC (A1U209) and the interface transceiver (A3U608) on the A3 Disc Controller board.

This diagnostic routine is used to check the main system bus. Any nodes attached to this bus may be checked for the proper signatures. With the loop intact, other busses may be checked by enabling buffers to allow the same signatures on the other existing busses. You will see this technique used in the Microprocessor No-ops SA loop. Transceiver A1U613 is enabled to force signatures from the NSC 800 address/data buss to the Dual Port RAM data bus.

8-21. MEMORY NO-OPS TROUBLESHOOTING (A2 - Decode and ROM 0)

This routine is part two of the troubleshooting scheme for the low level failures of the HP 4951C. Once the A1 board is verified, the same functional checks can be made on the memory board to verify the memory decoding, addressing, and ROM 0 contents. If the A2 memory board is still suspect, more detailed testing can be performed with the use of the MEMORY NO-OPS (A2 - Decode, ROM P, B, and M) routine.

Sequence of Events

The sequence of events is the same as the A1 board NSC800 NO-OPS routine. Some additional setup is required for the A2 board which is explained in the individual SA setups.

Circuitry Tested

This diagnostic routine uses the free run mode of the CPU (no-ops) to test the operation of the upper/lower memory select logic (A2U310) and the ROM and RAM Decoder (A2U306). When A1E2 is removed and A2E6 is moved to the "T" position, ROM 0 can be isolated so the data contents of the device can be verified as they are output onto the system Address/Data bus. The Address Latch (A2U411) is checked when A9-A15 signatures are taken on ROM 0 (A2U304).

8-22. MEMORY NO-OPS TROUBLESHOOTING (A2 - Decode, ROM P, B, and M)

This routine is most useful when system errors occur or when the A2 board is known to be defective. When a RAM failure is reported to screen, this routine can be used to verify some functions of the RAMs.

Sequence of Events

The sequence of events is the same as previously mentioned for the A1 and A2 no-op routines. Some additional setup is required for the A2 board which is explained in the Extensive Memory Setup in this section.

Circuitry Tested

This routine allows every memory location to be tested on ROM P, B and M (A2U304, A2U403 & A2U407). The decoding circuitry is tested the same as the previous routine.

The System RAM (A2U409, RAM A and A2U406, RAM C) is tested thoroughly by the Performance Verification routine performed at power up. Any RAM errors that occur are reported on the display. When the HP 4951C operates to the point where RAM errors can be reported, this routine can be used to verify the RAM addressing. The outputs can also be checked at this time. Note that the output of the RAMs during this test should be in a tri-state mode.

LOOP: Microprocessor NO-OPS
A1 - BUS, and CONTROL

PCA: A1 Main Board

SETUP: Move A1E314 to T position
Data Jumpers (A2E2 & A2E3) open or
A2 board disconnected
Disable Beeper (Remove A1E815)

* - Totalized Signature (+/- 1 count)
- Key Data (Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Normal		
START/STOP		+/+	A1U415 - 8 (A15)
QUAL			
CLOCK		-	A1U415 - 32 (~RD)
GROUND			A1U415 - 20

VHIGH = 0001

U415- A1-2

1-	HC89	(A8)
2-	2H70	(A9)
3-	HPP0	(A10)
4-	1293	(A11)
5-	HAP7	(A12)
6-	3C96	(A13)
7-	3827	(A14)
8-	755P	(A15)
9-	0004*	
12-	UUUU	(AD0)
13-	5555	(AD1)
14-	CCCC	(AD2)
15-	7F7F	(AD3)
16-	5H21	(AD4)
17-	0AFA	(AD5)
18-	UPFH	(AD6)
19-	52F8	(AD7)
21-	H	
22-	H	
23-	H	
24-	H	
25-	H	
26-	H	
27-	H	
28-	0001	
29-	H	
30-	0002*	
31-	H	
32-	0001*	
33-	H	
34-	L	
35-	H	
36-	H	
37-	L	
38-	H	
39-	H	

U411- A1-4

2-	HAP7
3-	52F8
4-	UPFH
5-	0AFA
6-	5H21
7-	7F7F
8-	CCCC
9-	5555
10-	UUUU
21-	HPP0
23-	1293
24-	2H70
25-	HC89

With the setup still in place, ground A1U613 pins 1 & 19 through a 100 ohm resistor and do the following:

U613- A1-4

2-	UUUU
3-	5555
4-	CCCC
5-	7F7F
6-	5H21
7-	0AFA
8-	UPFH
9-	52F8

Now ground A1U710 pin 4 through a 100 ohm resistor and do the following:

U412- A1-5

3-	UUUU
4-	5555
7-	CCCC
8-	7F7F
13-	5H21
14-	0AFA
17-	UPFH
18-	52F8

LOOP: Microprocessor NO-OPS
A1 - BUS, and CONTROL

PCA: A1 Main Board

SETUP: Move A1E314 to T position
Data Jumpers (A2E2 & A2E3) open or
A2 board disconnected
Disable Beeper (Remove A1E815)

* - Totalized Signature
(+/- 1 count)
- Key Data
(Rev. 4.0)

	EDGE:	NODE:
SA MODE: Normal		
START/STOP	+/+	A1U415 - 8 (A15)
QUAL		
CLOCK	-	A1U415 - 32 (~RD)
GROUND		A1U415 - 20

VHIGH = 0001

With A1U710 pin4 Ungrounded

U413-	2-	UUUU
A1-4	5-	5555
	6-	CCCC
	9-	7F7F
	12-	5H21
	15-	0AFA
	16-	UPFH
	19-	52F8
U513-	1-	H
A1-4	2-	UN
	4-	UUUU
	7-	5555
	9-	CCCC
	12-	7F7F
U512-	1-	H
A1-4	2-	UN
	4-	5H21
	7-	0AFA
	9-	UPFH
U713-	1-	H
A1-4	2-	UN
	4-	HC89
	7-	2H70
	9-	HPP0
	12-	1293

Ground A1U613 pins 1 & 19 and A1U710 pin 4 through a 100 ohm resistor and do the following:

U612-	3-	52F8
A1-4	5-	UPFH
	7-	0AFA
	9-	5H21
	12-	7F7F
	14-	CCCC
	16-	5555
	18-	UUUU
U510-	21-	0AFA
A1-5	22-	5H21
	23-	7F7F
	24-	CCCC
	25-	5555
	26-	UUUU

LOOP: Memory NO-OPS
A2 - DECODE and ROM 0

PCA: A2 MEMORY BOARD

SETUP: Move A1E314 to T position
Remove Data Jumpers (A2E2 & A2E3)
Jumper A2U306 pins 14 to 2 & 13 to 3
Move A2E6 to the T position
Disable Beeper (Remove A1E815)

* - Totalized Signature (+/- 1 count)
- Key Data (Rev. 4.0)

SA MODE: Qual	EDGE:	NODE:	
START/STOP	+	A2U304-1	(A15)
QUAL	-	A2U304-20	(~CE)
CLOCK	-	A1U415-32	(~RD)
GROUND		A2 TP GND	

VHIGH = 1180

U304- A2-1	1-	U3H4	U411- A2-1	2-	0U7U
	2-	H6AA		5-	052A
	3-	4PCC		6-	0108
	4-	A7A2		9-	1100
	5-	108P		11-	0002*
	6-	5342		12-	5342
	7-	1100		15-	108P
	8-	0108		16-	A7A2
	9-	052A		19-	4PCC
	10-	0U7U			
	11-	H656	U306- A2-1	1-	1180
	12-	7561		2-	U3H4
	13-	85AP		3-	0000
	15-	2ACC		4-	1180
	16-	1H18		5-	1180
	17-	2H0F		6-	1180
	18-	1P03		7-	1180
	19-	943U		9-	1180
	20-	0002*		10-	1180
	21-	0P0P		11-	P254
	22-	L		12-	U3H4
	23-	0F62		13-	0000
	24-	5HC4		14-	U3H4
	25-	FF4F		15-	0000
	26-	Tri-state			
	27-	Tri-state			

LOOP: Memory NO-OPS
A2 - DECODE and ROM 0

PCA: A2 MEMORY BOARD
KATAKANA OPT.003 ONLY

SETUP: Move A1E314 to T position
Remove Data Jumpers (A2E2 & A2E3)
Jumper A2U306 pins 14 to 2 & 13 to 3
Move A2E6 to the T position
Disable Beeper (Remove A1E815)

* - Totalized Signature
(+/- 1 count)
- Key Data
(Rev. 4.0)

SA MODE: Qual	EDGE:	NODE:	
START/STOP	+	A2U304-1	(A15)
QUAL	-	A2U304-20	(~CE)
CLOCK	-	A1U415-32	(~RD)
GROUND		A2 TP GND	

VHIGH = 1180

U304-	1-	U3H4	U411-	2-	0U7U
A2-1	2-	H6AA	A2-1	5-	052A
	3-	4PCC		6-	0108
	4-	A7A2		9-	1100
	5-	108P		11-	0002*
	6-	5342		12-	5342
	7-	1100		15-	108P
	8-	0108		16-	A7A2
	9-	052A		19-	4PCC
	10-	0U7U			
	11-	C0U6	U306-	1-	1180
	12-	1255	A2-1	2-	U3H4
	13-	U6AF		3-	0000
	15-	704U		4-	1180
	16-	U1C4		5-	1180
	17-	92A2		6-	1180
	18-	H59C		7-	1180
	19-	H974		9-	1180
	20-	0002*		10-	1180
	21-	0P0P		11-	P254
	22-	L		12-	U3H4
	23-	0F62		13-	0000
	24-	5HC4		14-	U3H4
	25-	FF4F		15-	0000
	26-	Tri-state			
	27-	Tri-state			

8-23. EXTENSIVE MEMORY SET UP

A. Open ~RD line from the system - move A1E314 from T to N position
remove A1E815 to disable Beeper
remove A2E2 and A2E3
move A2E6 to the T position

B. On A2U304: lift pins 1, 20, 26, and 27
On A2U403: lift pins 1, 11 through 20, and 22
On A2U407: lift pins 11 through 20, 22, and 27

Leave pin 14 (GND) connected

NOTE

Bend EPROM legs as little as possible to avoid excessive wearing of the device legs. Watch carefully that bent IC pins do not touch the IC socket pins on U407.

C. With double 0.0 ohm jumper wires and 5 IC leg clips connect:

A2U403 pin 1 to A2U304 pin 1 and A2U310 pin 12 (use 14 pin IC clip on A2U310)
A2U403 pin 27 to A2U304 pin 27 and A2U407 pin 27

D. With Single 0.0 ohm jumper wire and 2 IC leg clips connect:

A2U403 pin 26 to A2U304 pin 26

E. Jumper A2U306 pin 14 to pin 2 and A2U306 pin 13 to pin 3 using 0.0 ohm jumper wires.

F. Connect SA Meter:

ST/SP TO A2U310-5 ON IC CLIP	(A15)
GROUND TO GND TP ON A2 BOARD	(GND)
CLCK TO A1U415-32	(~RD)

NOTE

If EPROM outputs are not active, you may need to ground ~CE (20) or ~OE (22) of the inactive device. If any signals (PA0, PA1, PA2, PA4, or PA6) are not tristated (driven high or low), it may be necessary to remove A1U814 (NSC 810 I/O Timer) to allow the proper signatures to be taken at the gate outputs associated with these nodes on the A2 assembly.

LOOP: Memory NO-OPS
A2 - DECODE, ROM P, B, and M

PCA: A2 Memory Board

SETUP: See detailed set up on
Extensive Memory Test Set Up Sheet

* - Totalized Signature (+/- 1 count)
- Key Data (Rev. 4.0)

		EDGE:	NODE:	
SA MODE:	Norm			
START/STOP		+/+	A2U310-5	(A15)
QUAL				
CLOCK		-	A1U415-32	(~RD)
GROUND			A2 TP GND	

VHIGH = 0001

U304- A2-1	11-	U6U4	U407- A2-1	11-	26PU
	12-	U4U3		12-	4790
	13-	0718		13-	AFFU
	14-	L		14-	L
	15-	9FF5		15-	8A9U
	16-	HU74		16-	8FC0
	17-	6950		17-	C494
	18-	1671		18-	UC23
	19-	C5U0		19-	61AC

U403- A2-1	11-	HH37	U411- A2-1	2-	UUUU
	12-	1787		5-	5555
	13-	H66C		6-	CCCC
	14-	L		9-	7F7F
	15-	C11C		12-	5H21
	16-	FAF5		15-	0AFA
	17-	35U7		16-	UPFH
	18-	CAU6		19-	52F8
	19-	8F98			

LOOP: Memory NO-OPS (cont.)
A2 - DECODE, ROM P, B, and M

PCA: A2 Memory Board

SETUP: See detailed set up on
Extensive Memory Test Set Up Sheet

* - Totalized Signature (+/- 1 count)
- Key Data (Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A2U310-5 (A15)
QUAL			
CLOCK		-	A1U415-32 (~RD)
GROUND			A2 TP GND

VHIGH = 0001

U310- A2-1	1-	H	U205- A2-1	1-	AF5P	U308- A2-1	1-	4P0A
	2-	L		2-	L		2-	P255
	3-	H		3-	AF5P		3-	AF5P
	4-	H		4-	L		4-	PC01
	5-	755P		5-	F2A6		5-	12U3
	6-	755U		6-	F2A6		6-	U9U3
	8-	755P		8-	H		8-	64HP
	9-	755U		9-	4P0A		9-	0996
	10-	H		10-	3826		10-	6H49
	11-	755U		11-	H		11-	P255
	12-	755P		12-	H		12-	P255
	13-	H		13-	H		13-	H

U306- A2-1	1-	755U	U307- A2-1	1-	3827	U309- A2-1	1-	3827
	2-	3C96		2-	4P0A		2-	H
	3-	3827		3-	4P0A		3-	3826
	4-	4P0A		4-	0996		4-	Tri-state
	5-	12U3		5-	Tri-state		5-	H
	6-	PC01		6-	0996		6-	H
	7-	F2A6		8-	H		8-	03C1
	9-	P255		9-	H		9-	3827
	10-	U3H5		10-	0996		10-	3C96
	11-	0996		11-	P255		11-	L
	12-	6H49		12-	P255		12-	H
	13-	3827		13-	755P		13-	H
	14-	3C96						
	15-	755P						

LOOP: Memory NO-OPS
A2 - DECODE, ROM P, B, and M

PCA: A2 Memory Board
KATAKANA OPT.003 ONLY

SETUP: See detailed set up on
Extensive Memory Test Set Up Sheet

* - Totalized Signature
(+/- 1 count)
- Key Data
(Rev. 4.0)

	EDGE:	NODE:	
SA MODE: Norm			
START/STOP	+/+	A2U310-5	(A15)
QUAL			
CLOCK	-	A1U415-32	(~RD)
GROUND		A2 TP GND	

VHIGH = 0001

U304- A2-1	11-	042A
	12-	22H4
	13-	U123
	14-	L
	15-	C809
	16-	7HAC
	17-	437F
	18-	CF97
	19-	3AA4

U407- A2-1	11-	2HPC
	12-	FP6A
	13-	3H8F
	14-	L
	15-	9226
	16-	894F
	17-	8C56
	18-	UC23
	19-	7912

U403- A2-1	11-	7A17
	12-	6F3C
	13-	53U3
	14-	L
	15-	9123
	16-	8P16
	17-	8H34
	18-	2389
	19-	8908

U411- A2-1	2-	UUUU
	5-	5555
	6-	CCCC
	9-	7F7F
	12-	5H21
	15-	0AFA
	16-	UPFH
	19-	52F8

LOOP: Memory NO-OPS (cont.)
A2 - DECODE, ROM P, B, and M

PCA: A2 Memory Board
KATAKANA OPT.003 ONLY

SETUP: See detailed set up on
Extensive Memory Test Set Up Sheet

* - Totalized Signature (+/- 1 count)
- Key Data
(Rev. 4.0)

		EDGE:	NODE:	
SA MODE:	Norm			
START/STOP		+/+	A2U310-5	(A15)
QUAL				
CLOCK		-	A1U415-32	(~RD)
GROUND			A2 TP GND	

VHIGH = 0001

U310-	1-	H	U205-	1-	AF5P	U308-	1-	4P0A
A2-1	2-	L	A2-1	2-	L	A2-1	2-	P255
	3-	H		3-	AF5P		3-	AF5P
	4-	H		4-	L		4-	PC01
	5-	755P		5-	F2A6		5-	12U3
	6-	755U		6-	F2A6		6-	U9U3
	8-	755P		8-	H		8-	64HP
	9-	755U		9-	4P0A		9-	0996
	10-	H		10-	3826		10-	6H49
	11-	755U		11-	H		11-	P255
	12-	755P		12-	H		12-	P255
	13-	H		13-	H		13-	H

U306-	1-	755U	U307-	1-	3827	U309-	1-	3827
A2-1	2-	3C96	A2-1	2-	4P0A	A2-1	2-	H
	3-	3827		3-	4P0A		3-	3826
	4-	4P0A		4-	0996		4-	Tri-state
	5-	12U3		5-	Tri-state		5-	H
	6-	PC01		6-	0996		6-	H
	7-	F2A6		8-	H		8-	03C1
	9-	P255		9-	H		9-	3827
	10-	U3H5		10-	0996		10-	3C96
	11-	0996		11-	P255		11-	L
	12-	6H49		12-	P255		12-	H
	13-	3827		13-	755P		13-	H
	14-	3C96						
	15-	755P						

8-24. SCC DISCRETE CIRCUITRY TROUBLESHOOTING (NO-OPS Based)

Problems in the SCC circuitry can cause several different types of failures. They can range from a failure in the DLC test at power up, a failure in the External DLC test intended to test the pod interface, or a failure in some run time operations. The failure symptoms can vary for run time failures due to the large, but finite set of configurations of the DLC circuitry used during run time Simulation or Monitoring. Failures may occur during the post processing of data (running from the buffer). This routine should be used to eliminate the associated circuitry from being suspected as a failure. A large percentage of DLC and run time failures will generally be caused by a defective SCC chip (A1U209). This is due to the large percentage of DLC functional operations that the SCC performs.

Sequence of Events

The sequence of events for this routine are similar to that of the NSC800 no-ops routine. The NSC800 NO-OPS set up is used with some additional set up that is explained in the individual SA Routines. The circuitry of the SCC (A1U209) is set up to be driven by the no-op pattern present on the AD0-AD7 bus.

Circuitry Tested

During this diagnostics routine, the associated circuitry of the DLC circuit block is checked (A1U211, A1U112, A1U111, A1U209, A1U113, and A1U213). The Pod Interface Latch (A1U212) is not checked.

8-25. DLC TROUBLESHOOTING

This test should be used when a DLC or run time failure is evident. Not all of the set up conditions of the DLC are checked. In general the most efficient way to solve or isolate DLC problems is to initially replace the SCC (A1209) chip and retry the test that previously failed. This method is most effective due to the fact that a large percentage of the DLC failures seen are caused by the SCC. This applies to run time errors and Performance Verification errors more so than to the External DLC Test which is intended to test the Pod Interface circuitry.

Sequence of Events

During this diagnostics routine, the HP 4951C is programmed to simulate. During execution of the simulate menu, the DLC circuitry is active. Node measurements can be made at this time.

Circuitry Tested

During the execution of the simulate menu, the DLC circuitry is active and node activity measurements can be made. The SCC as well as the discrete circuitry can be checked for activity.

LOOP: SCC Discrete Circuitry

PCA: A1 Main Board

SETUP: Move A1E314 to T position. Remove A1E815 to disable Beeper. RS 232 Pod attached. Tie A1U113-5 to +5V, A1U211-3 to A1U211-11, A1U211-5 to A1U111-10 & 4, and A1U211-6 to A1U111-12 & 13. Remove A1U209 from socket.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:	
START/STOP	+/+	A1U415- 8	(A15)
QUAL			
CLOCK	-	A1U415-32	(~RD)
GROUND		A1U415-20	(GND)

VHIGH = 0001

U209- A1-2

1-	5555
2-	7F7F
3-	0AFA
4-	52F8
5-	H
6-	NC
7-	H
8-	H
9-	H
10-	NC
11-	U9C9
12-	5H90
13-	U9C9
14-	H
15-	FFFF
16-	H
17-	H
18-	H
19-	L
20-	UN
21-	H
22-	H
23-	NC
24-	H
25-	9696
26-	5H90
27-	U9C8
28-	H
29-	H
30-	NC
31-	L
32-	2H70
33-	H
34-	HC89
35-	H
36-	H
37-	UPFH
38-	5H21
39-	CCCC
40-	0001

U111- A1-2

1-	L
2-	34P0
3-	L
4-	FFFF
5-	L
6-	FFFF
7-	5H91
9-	H03C
10-	FFFF
11-	FFFF
12-	9696
13-	9696
14-	H42C
15-	L

LOOP: SCC Discrete Circuitry

PCA: A1 Main Board

SETUP: Move A1E314 to T position. Remove A1E815 to disable Beeper. RS 232 Pod attached. Tie A1U113-5 to +5V, A1U211-3, A1U211-11, A1U211-5 to A1U111-10 & 4, and A1U211-6 to A1U111-12 & 13. Remove A1U209 from socket.

* - Totalized Signature (+/- count)
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:	
START/STOP		+/+	A1U415- 8	(A15)
QUAL				
CLOCK		-	A1U415-32	(~RD)
GROUND			A1U415-20	(GND)

VHIGH = 0001

U211-	2-	H
A1-2	3-	0001
	4-	5555
	5-	FFFF
	6-	9696
	7-	CCCC
	8-	7F7F
	9-	H42C
	11-	0001
	12-	34P0
	13-	5H21
	14-	0AFA
	15-	U9C9
	16-	AA44
	17-	UPFH
	18-	52F8
	19-	FP47
U112-	1-	H03C
A1-2	2-	U9C9
	3-	2982
	4-	H/L
	5-	U9C8
	6-	U9C9
	8-	U9C8
	9-	U9C8
	10-	L
	11-	L
	12-	H
	13-	H

U113-	1-	Tristate/H
A1-2	2-	H/L
	3-	Tristate/L
	4-	H
	5-	H
	6-	FFFF
	8-	L
	9-	Tristate/H
	10-	UN/L
	11-	Tristate/H
	12-	L
	13-	H
U213-	2-	H
A1-2	3-	L
A1-3	4-	H
A1-4	5-	U9C9
	6-	U9C8
	8-	5H90
	9-	5H91
	10-	L
	11-	H
	12-	L/H
	13-	H/L

NOTE: Signatures with a '/' between them denote S.A.'s with different values when a pod is attached or not. EXAMPLE:
pod unattached / pod attached

8-26. DLC TEST SETUP

The following process assures that the Interface Pod is working correctly.

A. Connect the pod to the HP 4951C.
B. Input the proper DCE program for the Interface Pod from the appropriate appendix for the Interface Pod you are using.
C. Jumper the Pod as directed in the appendix.
D. Run the program.
E. Obtain access to the Memory Board without turning the instrument off.
F. Use the following tables to determine the failed component on the A1 board. Run the DCE program while checking for the states given in the tables.

Table 8-1. DLC Test Table

U112 Pin #	18174A	18179A	U211 Pin #	18174A	18179A
1	T	T	2	L	L
3	T	T	5	H	L
4	H	T	6	L	L
6	H	T	9	H	H
8	T	T	11	L	L
10	T	T	12	L	L
12	H	T	15	L	L
13	T	T	19	T	T

U209 PIN #	18174A	18179A	U212 PIN #	18174A	18179A
5	T	T	1	T	T
12	T	T	11	T	T
13	T	T			
14	H	T			
15	T	T			
16	T	T			
17	T	T			
18	T	T			
19	T	T			
21	T	T			
24	H	T			
25	T	T			
26	T	T			
27	T	T			
28	T	T			
29	L	L			

T= TOGGLING
H= LOGIC HIGH
L= LOGIC LOW

8-27. NSC810 I/O TIMER TROUBLESHOOTING

This test should be used when there is a continuous beep or one beep only. The lower level of the processor may have been verified earlier with the use of the previously mentioned SA routines. The beep begins when power is applied to the system. The beep will not be turned off until the CPU has properly come up and initialized the I/O Timer (A1U814). The second beep is generated after additional testing has been performed on the I/O Timer. Therefore, the failure symptoms could be a continuous beep or one beep.

Sequence of Events

At power up, the CPU enables and reads the Pod Interface Latch (A1U212). If a specific bit is set low, the CPU will begin executing a I/O Timer test routine from the system memory. The I/O Timer (A1U814) inputs and outputs will be exercised in a repetitive loop.

This routine is a firmware (ROM code) driven routine. It puts the I/O Timer (A1U814) into a repeating test sequence.

Circuitry Tested

This routine uses the repeating I/O Timer test to thoroughly check the NSC810 I/O Timer (A1U814). This routine can also be used to verify the RSTB and RSTC circuitry (A1U615, A1U715, and A1U915).

8-28. I/O Decoder TROUBLESHOOTING

This routine should be used when an I/O device (CRTC, Tick Clock gating, DLC, Pod Latch gating, or Remote Port Enable) fails to operate properly. Most I/O device failures are reported on the screen with the exception of the Tick Clock Generator and the CRT Controller. This routine's main function is to test the I/O Device enable circuitry of the HP 4951C. The A2 Memory board and the A3 Disc Controller board may be disconnected from the system.

Set Up Routine

For this routine the set up is the same as the NSC800 NO-OP routine. Any additional setup required to enable the I/O Decoder (A1U313) is described in the individual SA Routine.

Circuitry Tested

During this diagnostics routine the I/O Decoder (A1U313) is tested. The full address range of the I/O Decoder is exercised by the use of the CPU free run mode established by the setup conditions. Additional discrete circuitry (A1U714, A1U213, A1U312, & A2U204) is tested as well as the I/O Decoder. Trace continuity can be verified to the receiving nodes from the I/O Decoder.

LOOP: I/O Timer

PCA: A1 Main Board

SETUP: A1U212 pin 3 to ground
Disconnect Pod - Disconnect A3 Board
Remove A1E815 to disable Beeper
A2 Board must be connected.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:
START/STOP		+/+	A1U812-2 (AD0)
QUAL			
CLOCK		+	A1U814-9 (~RD)
GROUND			A1U814-20

VHIGH = A803

U814- A1-3	1-	H
	2-	45C5
	3-	45C5
	4-	L
	5-	L
	6-	H
	7-	602*
	8-	600*
	9-	2314*
	10-	602*
	11-	4423*
	12-	2F56
	13-	90AA
	14-	A9UU
	15-	3F27
	16-	73HH
	17-	CU86
	18-	35HC
	19-	P3PP
	20-	L
	21-	F1PF
	22-	7769
	23-	15H9
	24-	H5HC
	25-	95H1
	26-	8A31
	27-	C163
	28-	UU94
	29-	U07C
	30-	HHHA
	31-	4576
	32-	U576
	33-	6574
	34-	228F
	35-	AF58
	36-	UUP5
	37-	6783
	38-	16PP
	39-	H22C
	40-	H
U615- A1-3	1-	04P8
	2-	UUP5
	3-	AF58
	4-	228F
	5-	HHHA
U715- A1-3	3-	45C5
	9-	CPPH
	10-	16PP
U915- A1-3	3-	45C5
	9-	7A28
	10-	H22C

LOOP: I/O Decoder

PCA: A1 Main Board

SETUP: Move A1E314 to T position
Remove A2E2 & A2E3 or disconnect A2 Board
Remove A1E815 to disable Beeper
Pull A1U415 pin 34(IO/M) to +5V

* - Totalized Signature (+/- count)
- Key Data

(Rev. 4.0)

SA MODE:	Norm	**EDGE:**	**NODE:**
START/STOP		+/+	A1U415-8 (A15)
QUAL			
CLOCK		-	A1U415-32 (~RD)
GROUND			A1U415-20
VHIGH =	0001		

U313-	1-	1293
A1-3	2-	HAP7
	3-	3C96
	4-	3827
	5-	755P
	6-	H
	7-	1920
	9-	C34C
	10-	597C
	11-	UA87
	12-	4154
	13-	960F
	14-	84AF
	15-	3PCF

U714-	1-	H
A1-2	2-	4154
A1-3	3-	H
	4-	H
	5-	960F
	6-	H
	8-	H
	9-	H
	10-	UA87
	11-	H
	12-	H
	13-	960F

U213-	1-	Tri-state
A1-2	2-	H
A1-3	3-	29A7
A1-4	4-	29A6
	5-	H
	6-	L
	8-	L/H
	9-	H/L
	10-	L
	11-	H
	12-	L
	13-	H

U312-	1-	L
A1-2	2-	755P
A1-3	3-	755U
	4-	H
	5-	L
	6-	H/L
	7-	L/H
	9-	L
	10-	H
	11-	0001
	12-	0000
	13-	0000
	14-	0001
	15-	L

8-29. KEYBOARD VERIFICATION TROUBLESHOOTING

This procedure is useful once a keyboard failure has been verified by the Keyboard Test contained with in the Self Test Menu or if it is not possible to get to the keyboard test.

Set Up Routine

During this troubleshooting procedure the functional operation of of the keyboard is verified. The instrument should be in the Keyboard Test, of the Self Test Menu. During this set up the HP 4951C is in a free run keyboard scan mode. The instrument is idle while waiting to respond to any key that is activated by the user.

Circuitry Tested

Running the instrument in this mode allows for signal tracing from the Keyboard Latch outputs (A1U812) to the I/O Timer Port B inputs (A1U814). Signal activity through a key stroke completes a circuit path assigned by the keyboard matrix. Signal activity from the Keyboard Latch can be verified to the different rows of keys, with each key switch residing on a particular row. Signal activity from the key switch can be verified to the input port of the I/O timer. This signal activity denotes column activity.

8-30. KEYBOARD TROUBLESHOOTING

Set Up

From the Top Level Menu put the HP 4951C into the Keyboard Test contained within the Self Test Menu by pressing the following softkeys: <More>, <Self Test> and <Kbd Test>.

Using this test along with the keyboard schematic will allow you to isolate most types of failures associated with the Keyboard assembly. Individual key activity can be measured at the input port of the NSC810 I/O Timer (A1U814).

Verification

A1U812 (Keyboard Latch outputs):	Pin 2 should be high pulsing low. Pins 5-19 should be low pulsing high.
A1U814 I/O (Timer Port B inputs):	Pins 29-36 should be low.

A1U814 pins 29-36 (PB0-PB7) should become active with a signal that is low, pulsing high. Only one node should become active when the corresponding key is pressed. Each key that corresponds to the R0-R7 input can be derived from the keyboard schematic. Several keys share the same row or column depending on the physical arrangement of the keys in the keyboard circuitry. Use a scope for the signal measurements.

8-31. DUAL PORT RAM TROUBLESHOOTING

If a failure is associated with the Dual Port RAM, the symptoms generated will be two beeps and no display. This type of failure would be considered a low level failure associated with the kernel of the HP 4951C.

Sequence of Events

During a failure of the Dual Port RAM (A1U411), a 'Loop on Failure' condition exists. This 'Loop on Failure' mode is used to verify the problems associated with the Dual Port RAM. No system set up is required other than turning the power on and having a failure associated with the Dual Port RAM.

Circuitry Tested

This test's main objective is to verify the operation of the Dual Port RAM (A1U411). Address inputs, data outputs, and control inputs can be verified. The B bus to A bus direction can be checked on the transceiver A1U613. Note that the A bus to B bus direction of this transceiver can be checked in the NSC800 NO-OP routine described earlier in this section. During the A to B direction check, the ability to write to the Dual Port RAM can be verified as well as proper addressing. During the B to A direction check the ability of reading from the Dual Port RAM as well as its data storage integrity can be verified.

LOOP: Dual Port RAM

PCA: A1 Main Board

SETUP: No jumpers, two Beeps only.
Denotes Loop on Failure of Dual Port RAM PV Routine.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Qual	EDGE:	NODE:
START/STOP	+	A1U411-2 (A12)
QUAL	+	A1U411-22 (~OE)
CLOCK	+	A1U411-27 (~WE)
GROUND		A1U411-14 (GND)

VHIGH = P254

U411- A1-4

11-	1C5U	Data Out
12-	U90C	Data Out
13-	1C5U	Data Out
15-	U90C	Data Out
16-	6UUC	Data Out
17-	8HAU	Data Out
18-	6UUC	Data Out
19-	8HAU	Data Out
2-	603A	Address
3-	8AUC	Address
4-	65CA	Address
5-	46HC	Address
6-	C7A5	Address
7-	12U0	Address
8-	3HUA	Address
9-	FA11	Address
10-	5P33	Address
21-	AAHU	Address
23-	U665	Address
24-	1U5P	Address
25-	9241	Address
20-	L	Control
22-	P254	Control
26-	H	Control
27-	0000	Control
28-	H	Control

U613- A1-4

11-	8HAU
12-	6UUC
13-	8HAU
14-	6UUC
15-	090C
16-	1C5U
17-	090C
18-	1C5U

8-32. CRT CONTROLLER TROUBLESHOOTING

The CRT Controller circuitry is responsible for the process of displaying information to the screen of the HP 4951C. Testing of this circuitry is accomplished from the "Top Level" display of the HP 4951C.

This diagnostics routine is most effective when a display is visible but is corrupt or incorrect information is being displayed. To help assure the integrity of the signatures taken, the contents of the Dual Port RAM (A1U411) must be set to the default configuration. This can be done by removing power from the Dual Port RAM. Keep in mind that the Dual Port RAM and the System RAM contents are saved by a battery back up system contained on the A2 Memory board. To disable the battery the A2 board must be disconnected from the A1 board. Doing this will allow the contents of the Dual Port RAM to dissipate. The next time the system is powered up, corrupt menu information will be detected and the data contents of the Dual Port RAM will be programmed to the default configuration. This is the most effective way to assure consistent data contents in the Dual Port RAM. Keep in mind that this diagnostics routine is to be run with the instrument in the "Top Level" display.

Sequence of Events

During the power up Performance Verification testing the CRT Controller is initialized and checked. After this phase of testing is completed, the fourth and last beep of the beep sequence is generated. The CRT Controller is then allowed to enable the display. This begins the process of displaying predetermined information to the display screen. For this routine, the sequence of events is for the instrument to achieve the "Top Level" display. At this time the CRT Controller (A1U514) is in a free run mode of display tasks and all of the CRT Controller circuitry is active.

Circuitry Tested

Most of the CRT Controller circuitry is checked from the outputs of the CRT Controller (A1U514) to the outputs of the CRT Logic Gate Array (A1U510). CRT Controller addressing and data are checked at the Dual Port RAM (A1U411) as well as the gating of the Character Data Latch (A1U612). The operation of the CRT EPROM Address Latch (A1U412) is checked. Partial data contents of the CRT EPROM are checked at the inputs of the CRT Logic Gate Array (A1U510). Functional checks can be performed on the discrete logic that acts as the digital to analog interface to the CRT Analog circuitry.

For the following CRT tests, do the following procedure:

SETUP: Before powering up the instrument to do the next test, unplug the 4951C A2 board and let it sit for a few minutes. Then reconnect the board and power up the instrument for testing. You should get a "corrupt menus" message. Now press the exit key to get to the Top Level. Doing this will assure that the default information will be stored in the Dual Port RAM. This will insure the integrity of the signatures being taken on the instrument. After the HP 4951C is in the display mode you want to test, ground A1U710 pin 4 through a 100 ohm resistor/jumper wire and then check the signatures you want to verify. When switching display modes, disconnect A1U710 pin 4, select a different display mode, and then ground it again when you are ready to take more signatures.

LOOP: CRT Controller Circuitry

PCA: A1 Main Board

SETUP: Instrument at top level.
No Jumpers Removed. Ground A1U710 pin 4 through a 100 ohm resistor.

* - Frequency Measurement
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:	
START/STOP		+/+	A1U514-40	(VS)
QUAL				
CLOCK		+	A1U514-21	(CHCLK)
GROUND			A1U514-1	(GND)

VHIGH = 09P7

U411-	11-	AP62		35-	65H6	11-	49AA
A1-4	12-	6059		36-	6536	12-	0458
	13-	PA24		37-	A5CA	13-	2P39
	15-	7FUF		38-	507H	14-	UPP5
	16-	6UU9		39-	5P92	15-	72FH
	17-	9368				16-	09P7
	18-	6H14	U512-	4-	A682	17-	09P7
	19-	F1PP	A1-4	7-	3492	18-	09P7
				9-	374U	19-	CAC3
U412-	2-	H731		12-	F469	20-	UN
A1-5	5-	C02F				21-	9368
	6-	U512	U513-	4-	0000	22-	6UU9
	9-	3P7P	A1-4	7-	075H	23-	7FUF
	12-	C7UF		9-	UH34	24-	PA24
	15-	49C4		12-	990P	25-	6059
	16-	368A				26-	AP62
	19-	P0U7	U713-	4-	2F0C	27-	0000
			A1-4	7-	P049	28-	09P7
U514-	4-	075H		9-	H71F	29-	65H6
A1-5	5-	UH34		12-	L	30-	H
	6-	990P				31-	6536
	7-	A682	U510-	1-	2 HZ*	32-	A5CA
	8-	3492	A1-5	2-	30 HZ*	33-	507H
	9-	374U		3-	H	34-	H
	10-	F469		4-	H	35-	04F5
	11-	2F0C		5-	UN	36-	L
	12-	P049		6-	0000	37-	L
	13-	H71F		7-	F883	38-	H
	14-	L		8-	3A80	39-	UN
	18-	04F5		9-	CFF0	40-	UN

LOOP: CRT Controller Circuitry

PCA: A1 Main Board
KATAKANA OPT.003 ONLY

SETUP: Instrument at top level.
No Jumpers Removed. Ground A1U710 pin 4 through a 100 ohm resistor.

* - Frequency Measurement
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:
START/STOP		+/+	A1U514-40 (VS)
QUAL			
CLOCK		+	A1U514-21 (CHCLK)
GROUND			A1U514-1 (GND)

VHIGH = 09P7

U411- A1-4	11-	AP62
	12-	17U4
	13-	PA24
	15-	0C51
	16-	6UU9
	17-	P4F5
	18-	1AC9
	19-	F1PP
U412- A1-5	2-	H731
	5-	8CUA
	6-	U512
	9-	05A8
	12-	C7UF
	15-	7262
	16-	0H5F
	19-	P0U7
U514- A1-5	4-	075H
	5-	UH34
	6-	990P
	7-	A682
	8-	3492
	9-	374U
	10-	F469
	11-	2F0C
	12-	P049
	13-	H71F
	14-	L
	18-	04F5
	35-	65H6
	36-	6536
	37-	A5CA
	38-	507H
	39-	5P92
U512- A1-4	4-	A682
	7-	3492
	9-	374U
	12-	F469
U513- A1-4	4-	0000
	7-	075H
	9-	UH34
	12-	990P
U713- A1-4	4-	2F0C
	7-	P049
	9-	H71F
	12-	L
U510- A1-5	1-	2 HZ*
	2-	30 HZ*
	3-	H
	4-	H
	5-	UN
	6-	0000
	7-	658A
	8-	C30A
	9-	P43H
	11-	U22U
	12-	4CFP
	13-	1686
	14-	61A0
	15-	72FH
	16-	09P7
	17-	09P7
	18-	09P7
	19-	CAC3
	20-	UN
	21-	P4F5
	22-	6UU9
	23-	0C51
	24-	PA24
	25-	17U4
	26-	AP62
	27-	0000
	28-	09P7
	29-	65H6
	30-	H
	31-	6536
	32-	A5CA
	33-	507H
	34-	H
	35-	04F5
	36-	L
	37-	L
	38-	H
	39-	UN
	40-	UN

8-33. CRT RAM TROUBLESHOOTING (Read Cycle)

This routine should be used when visual failures are detected and the contents of the CRT RAM have been visually verified as being defective. This can be done by grounding A1U312 pin 4, which denies the CRT Controller access to the Dual Port RAM as previously explained. This will cause all information being displayed to be derived from the data contained within the CRT RAM.

Sequence of Events

The sequence of events for this routine is the same as the CRT RAM, Write Cycle. The major difference between the two routines is that the Write Cycle allows the system to operate under normal free run display conditions and the Read cycle requires that the CRT Controller be denied access to the Dual Port RAM (A1U411). This mode of operation is obtained by grounding A1U312 pin 4 through a 100 ohm resistor.

Circuitry Tested

This routine focuses on testing the storage integrity of the CRT RAM (A1U711). Address, control, and data contents being read from the CRT RAM are verified.

8-34. CRT RAM TROUBLESHOOTING (Write Cycle)

This diagnostics routine should be used in the event that visual failures are detected when the display information is being generated from the display data contained within the CRT RAM. A quick check of this process can be done by denying the CRT Controller access to the Dual Port RAM as explained previously. This routine should be used after the CRT RAM, Read Cycle routine has been used and incorrect data being written to the CRT RAM is the suspected failure mechanism.

Sequence of Events

During the power up Performance Verification testing, the CRT RAM (A1U711) is not tested. The HP 4951C can operate properly with out the CRT RAM existing in the system. However, some failures in the CRT RAM can be visually detected. Anytime the CRT Controller (A1U514) is forced access to the Dual Port RAM (A1U411) for display information, visual failures may be noted. Under normal system operation, the failure is only visible for a fraction of a second. In order to clearly see the contents of the CRT RAM over a period of time, the CRT Controller must be denied access to any character information held within the Dual Port RAM. This mode can be obtained by grounding A1U312 pin 4 through a 100 ohm resister. The true data contents of the CRT RAM will now be displayed on the display screen.

Circuitry Tested

During this diagnostics routine, the testing is focused on the system's ability to address, control, and present data to the CRT RAM (A1U711). This routine will measure the information that is to be stored into the CRT RAM.

LOOP: CRT RAM (Read Cycle)

PCA: A1 Main Board

SETUP: Instrument in some display mode.
Follow the same procedure as for
the CRT RAM (Write Cycle) Test. Ground
A1U312-4. The screen will be updated from
the CRT RAM only.

* - Totalized Signature
(+/- 1 count)
- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A1U711-19 (MA19)
QUAL			
CLOCK		+	A1U711- 8 (CCLK)
GROUND			A1U711-12 (GND)

VHIGH = 5159

Screen Mode:	Top Level	CRT Tst Keys	Full Raster	Char Set 2	Test Pattern
U711- 9-	U59F	8AAF	F44F	H37F	61C5
A1-4 10-	H0U6	345P	F44F	F95F	58P5
11-	A619	402H	F44F	92C6	61C5
13-	3CPF	90U3	F44F	49U8	58P4
14-	F9C7	5FA0	F44F	3A3U	UH1H
15-	7067	727H	UH1H	UH1H	F44F
16-	PP0P	4C2F	F44F	UH1H	F44F
17-	F44H	F44F	F44F	UH1H	UH1H
1-	3951	3951	3951	3951	3951
2-	3951	3951	3951	3951	3951
3-	UP73	UP73	UP73	UP73	UP73
4-	8HC4	8HC4	8HC4	8HC4	8HC4
5-	UACP	UACP	UACP	UACP	UACP
6-	1047	1047	1047	1047	1047
7-	30F8	30F8	30F8	30F8	30F8
8-	0000	0000	0000	0000	0000
19-	6808	6808	6808	6808	6808
22-	3951	3951	3951	3951	3951
23-	3951	3951	3951	3951	3951

LOOP: CRT RAM (Write Cycle)

PCA: A1 Main Board

SETUP: Instrument in some display mode. (Top Level, CRT Test Keys, Full Raster, Char Set 2, Test Pattern). CRT is in a mode where it is being written to.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Qual	EDGE:	NODE:
START/STOP	+	A1U711-19 (MA19)
QUAL	-	A1U711-21 (~WE)
CLOCK	+	A1U711- 8 (CCLK)
GROUND		A1U711-12 (GND)

VHIGH = 5159

Screen Mode:	Top Level	CRT Tst Keys	Full Raster	Char Set 2	Test Pattern
U711- 9-	U59F	8AAF	F44F	H37F	61C5
A1-4 10-	H0U6	345P	F44F	F95F	58P5
11-	A619	402H	F44F	92C6	61C5
13-	3CPF	90U3	F44F	49U8	58P4
14-	F9C7	5FA0	F44F	3A3U	UH1H
15-	7067	727H	UH1H	UH1H	F44F
16-	PP0P	4C2F	F44F	UH1H	F44F
17-	F44H	F44F	F44F	UH1H	UH1H
1-	3951	3951	3951	3951	3951
2-	3951	3951	3951	3951	3951
3-	UP73	UP73	UP73	UP73	UP73
4-	8HC4	8HC4	8HC4	8HC4	8HC4
5-	UACP	UACP	UACP	UACP	UACP
6-	1047	1047	1047	1047	1047
7-	30F8	30F8	30F8	30F8	30F8
8-	0000	0000	0000	0000	0000
19-	6808	6808	6808	6808	6808
22-	3951	3951	3951	3951	3951
23-	3951	3951	3951	3951	3951

LOOP: CRT EPROM Contents

PCA: A1 Main Board

SETUP: Instrument in some display mode. (Top Level, CRT Test Keys, Full Raster, Char Set 2, Test Pattern). GROUND A1U312-4. The screen will be updated from the CRT RAM only.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A1U711-19 (MA19)
QUAL			
CLOCK		+	A1U711- 8 (CCLK)
GROUND			A1U711-12 (GND)

VHIGH = 5159

Screen Mode:		Top Level	CRT Tst Keys	Full Raster	Char Set 2	Test Pattern
U412-	2-	7APF	4556	6226	104C	30HA
A1-5	5-	687C	9A2U	6226	1H5C	AF72
	6-	2AU9	A016	6226	C0AP	30HA
	9-	9HU6	F879	6226	HH09	5587
	12-	1H2P	2P50	6226	P4PA	077C
	15-	3833	F0FC	077C	077C	6226
	16-	U707	A596	6226	077C	6226
	19-	9CH3	6226	6226	077C	O77C
U510-	7-	UUU9	6CAH	3951	A0H0	A5U9
A1-5	8-	UUU9	6CAH	3951	A0H0	A5U9
	9-	3951	3951	3951	2HUC	A5U9
	11-	3951	3951	3951	3951	A5U9
	12-	3951	3951	3951	3951	A5U9
	13-	3951	3951	3951	3951	A5U9
	14-	6HAP	3951	3951	3951	A5U9
	15-	0000	0000	0000	0000	52UF

If different stable signatures are present, try pressing 'Norm' or toggle the SA meter clock in order to synchronize the SA Meter. Doing this should allow you to achieve the proper signatures.

LOOP: CRT EPROM Contents

PCA: A1 Main Board
KATAKANA OPT.003 ONLY

SETUP: Instrument in some display mode.
(Top Level, CRT Test Keys, Full Raster,
Char Set 2, Test Pattern). GROUND A1U312-4.
The screen will be updated from the CRT RAM
only.

* - Totalized Signature
(+/- 1 count)
- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A1U711-19 (MA19)
QUAL			
CLOCK		+	A1U711- 8 (CCLK)
GROUND			A1U711-12 (GND)

VHIGH = 5159

Screen Mode:		Top Level	CRT Tst Keys	Full Raster	Char Set 2	Test Pattern
U412-	2-	7APF	4556	6226	104C	30HA
A1-5	5-	687C	9A2U	6226	1H5C	AF72
	6-	2AU9	A016	6226	C0AP	30HA
	9-	9HU6	F879	6226	HH09	5587
	12-	1H2P	2P50	6226	P4PA	077C
	15-	3833	F0FC	077C	077C	6226
	16-	U707	A596	6226	077C	6226
	19-	9CH3	6226	6226	077C	077C
U510-	7-	UUU9	6CAH	3951	3951	A5U9
A1-5	8-	UUU9	6CAH	3951	3951	A5U9
	9-	3951	3951	3951	3951	A5U9
	11-	3951	3951	3951	3951	A5U9
	12-	3951	3951	3951	3951	A5U9
	13-	3951	3951	3951	3951	A5U9
	14-	6HAP	3951	3951	3951	A5U9
	15-	0000	0000	0000	0000	52UF

If different stable signatures are present, try pressing 'Norm' or toggle the SA meter clock in order to synchronize the SA Meter. Doing this should allow you to achieve the proper signatures.

8-35. EXTERNAL VIDEO TROUBLESHOOTING

This routine should be used only when the External Video Hybrid is the suspected part of an External Video failure. The External Video Hybrid should not be suspect in the event the HP 4951C display is malfunctioning as well as the External Video output. Both display systems are driven from the same signal source (A1U510 &A1U514).

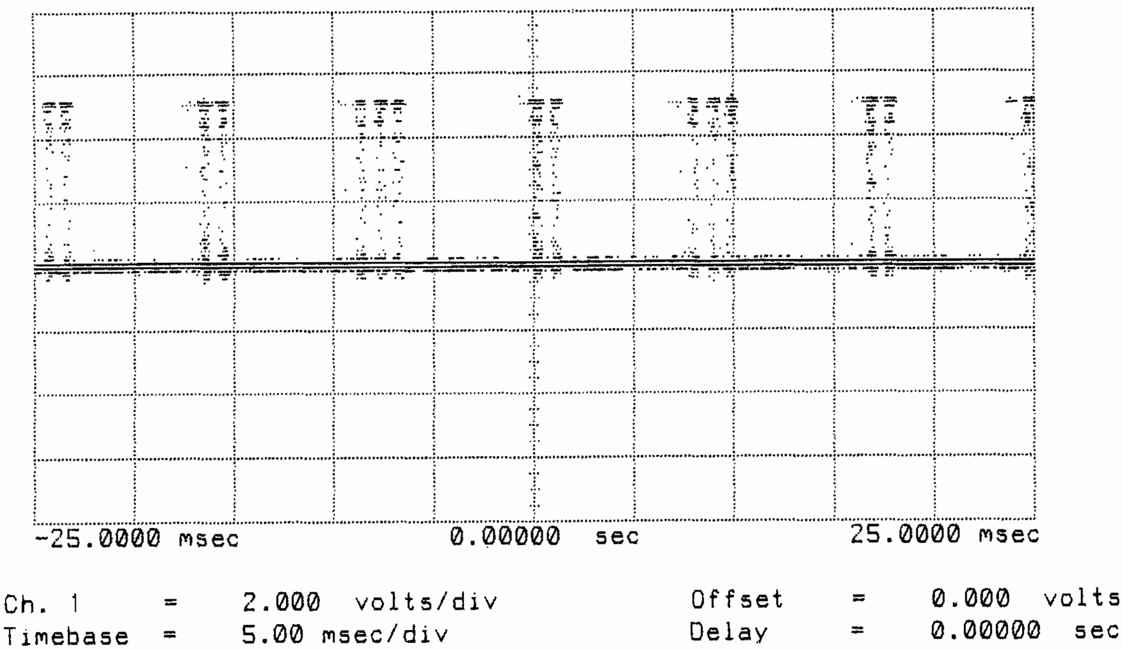
Sequence of Events

The sequence of events for this routine is the same as the previous CRT Controller routines in that the instrument is in the "Top Level" menu. The CRT Controller circuitry is active and in a free run mode. The External Video Hybrid (A1U611) is active whenever the display has been enabled by the CRT Controller (A1U514).

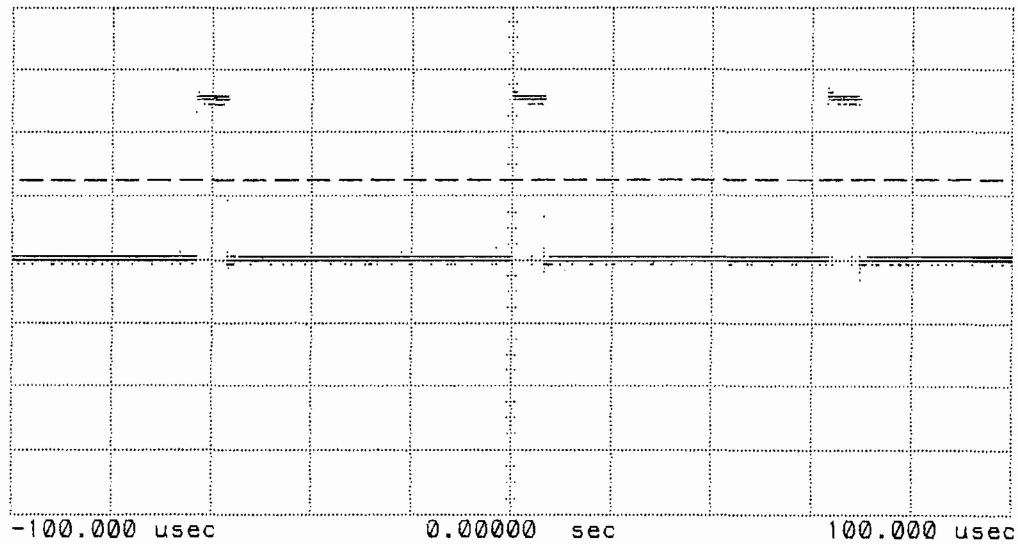
This diagnostics routine does not use any Signature Analysis. It uses manual signal checks with the use of an oscilloscope. The External Video waveforms follow below.

Circuitry Tested

During this routine the output of the CRT Logic Gate Array (A1U510), the External Video Hybrid (A1U611), and the cabling to the HP 4951C rear panel are verified.

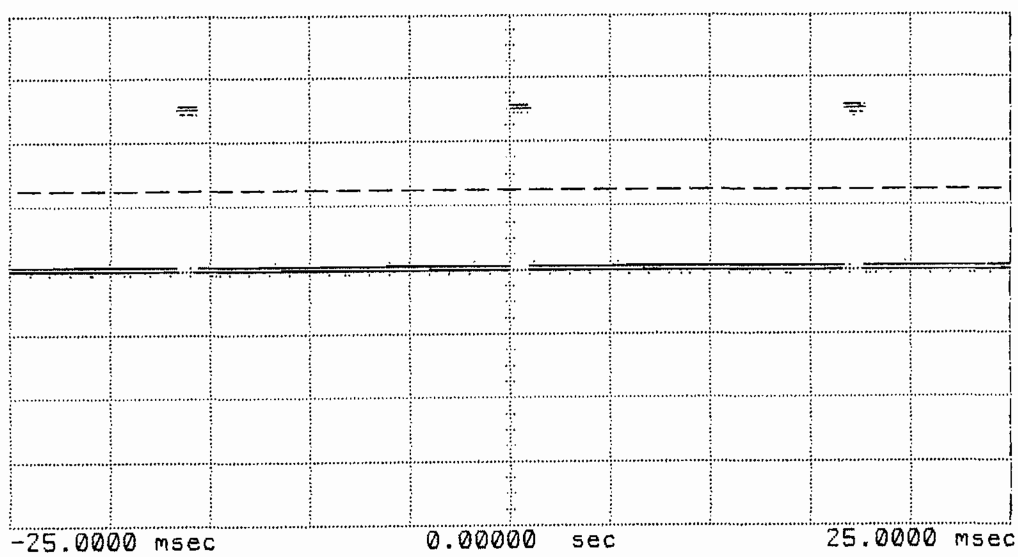


External Video Waveform - HBDR (U611 pin 2)



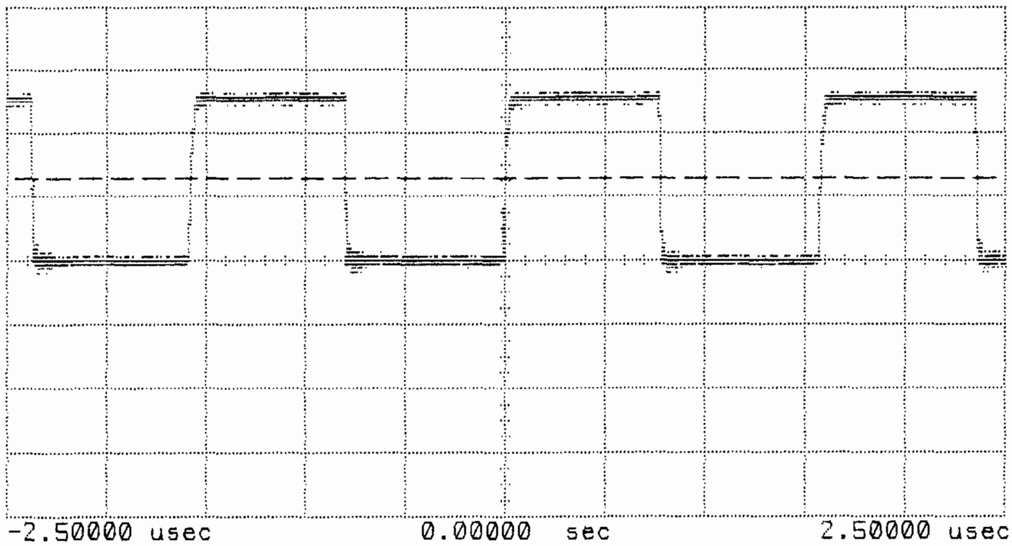
Ch. 1 = 2.000 volts/div
Timebase = 20.0 usec/div
Ch. 1 Parameters
Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 15.8438 KHz

External Video Waveform - HS (U611 pin 4)



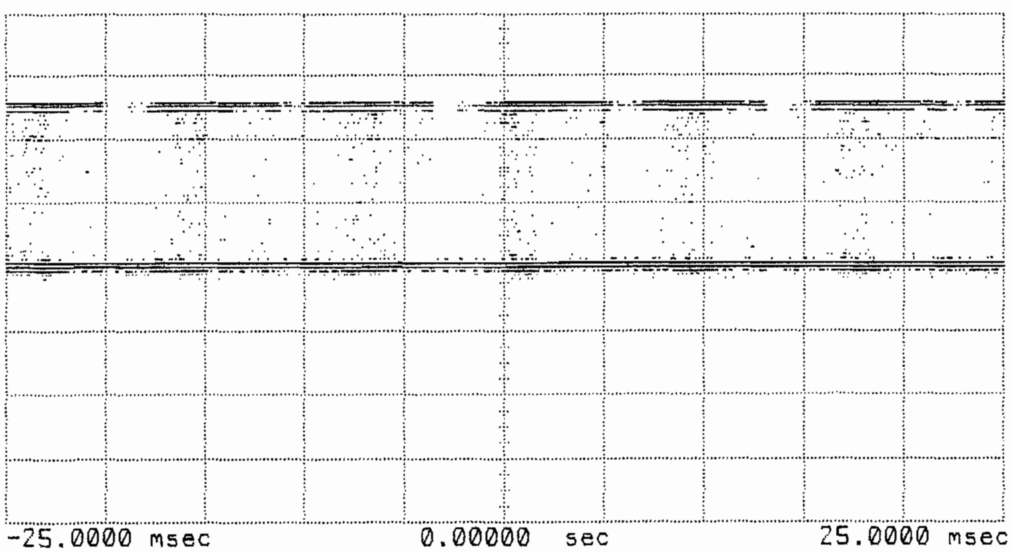
Ch. 1 = 2.000 volts/div
Timebase = 5.00 msec/div
Delta T = 0.00000 sec
Start = 25.0000 msec
Delta V = 0.000 volts
Vmarker1 = 2.500 volts
Offset = 0.000 volts
Delay = 0.00000 sec
Stop = 25.0000 msec
Vmarker2 = 2.500 volts

External Video Waveform - VS (U611 pin 5)



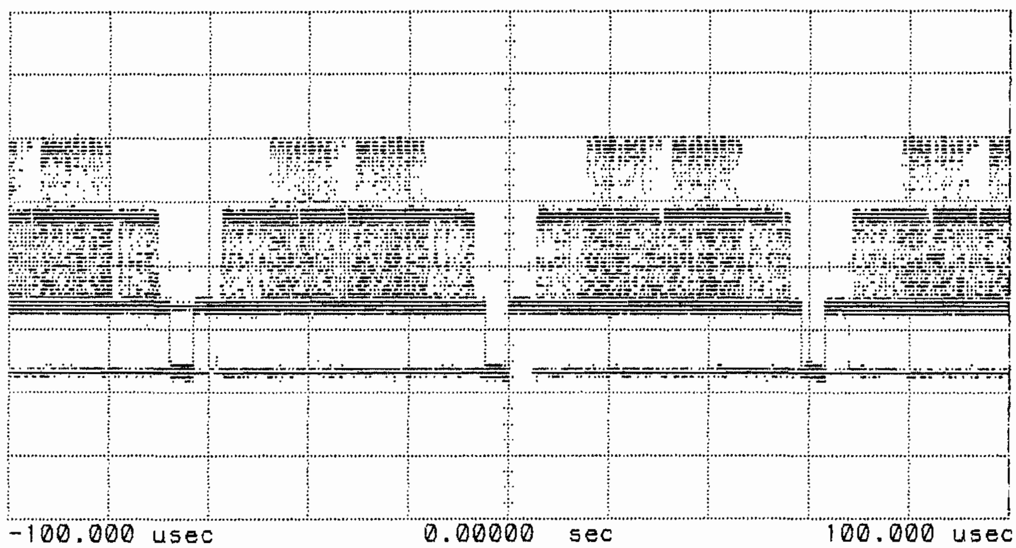
Ch. 1 = 2.000 volts/div   Offset = 0.000 volts
Timebase = 500 nsec/div   Delay = 0.00000 sec
Ch. 1 Parameters   Freq. = 633.794 KHz

External Video Waveform - CCLK (U611 pin 6)



Ch. 1 = 2.000 volts/div   Offset = 0.000 volts
Timebase = 5.00 msec/div   Delay = 0.00000 sec

External Video Waveform - FBDR (U611 pin 8)



Ch. 1	=	500.0 mvolts/div	Offset	=	0.000 volts
Timebase	=	20.0 usec/div	Delay	=	0.00000 sec
Delta T	=	0.00000 sec			
Start	=	25.0000 msec	Stop	=	25.0000 msec

External Video Waveform - Video Out (U611 pin 9)

8-36. CRT DRIVE AND DEFLECTION CIRCUITRY

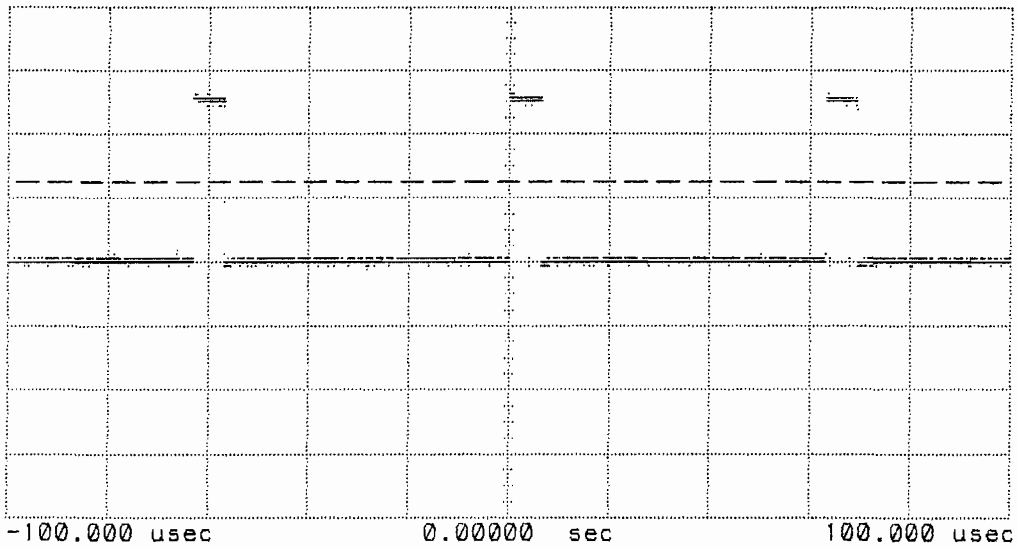
Within the HP 4951C CRT drive and deflection circuitry, there are several jumpers that are provided to aid in troubleshooting and problem isolation. With the use of these jumpers and the analog waveforms provided, problem isolation can be accomplished. Following is a list of these jumpers and a functional description of each:

E407 - used to remove +12j loading from CRT circuitry.
E406 - used to remove -12j loading from CRT circuitry.
E404 - used to remove +12c loading from CRT circuitry.
E707 - used to remove vertical deflection signal from CRT yoke assembly.
E810 - Used to remove FBDR, HBDR, and APU signals from CRT analog circuitry.

8-37. CRT ANALOG WAVEFORMS

Table 8-2. CRT Analog Waveforms

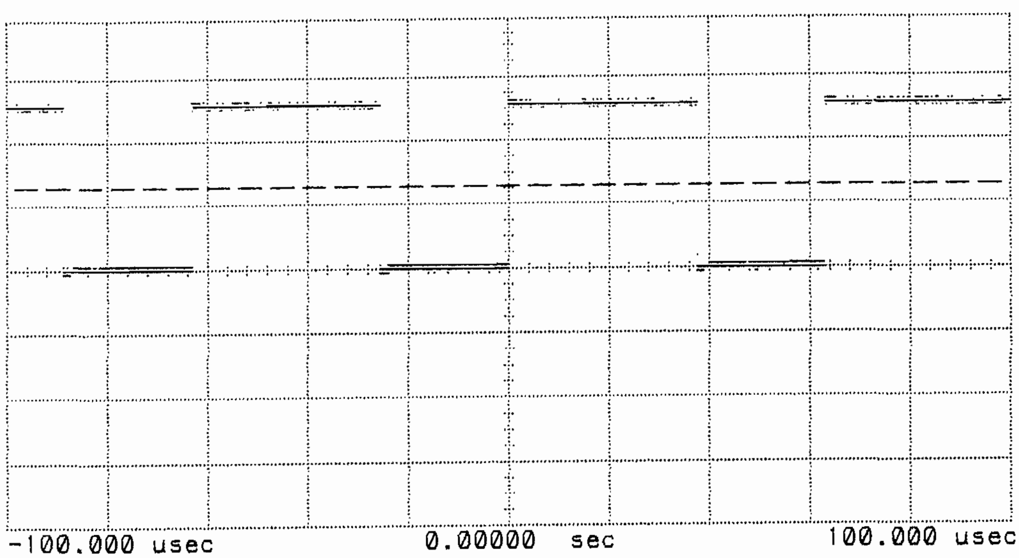
WAVEFORM #	SCHEMATIC NODE	WAVEFORM #	SCHEMATIC NODE
1.	U507 pin 10	11.	Q704 Collector
2.	U507 pin 12	12.	U805 pin 9
3.	Q605 Base	13.	Q702 Collector
4.	Q605 Collector	14.	CR25 Anode
5.	CR28 Cathode	15.	U507 pin 2
6.	U805 pin 5	16.	U608 pin 1
7.	Q804 Base	17.	U608 pin 7
8.	Q804 Collector	18.	U608 pin 8
9.	U805 pin 2	19.	U608 pin 14
10.	Q704 Base	20.	TP708 (Q606 & Q607 Emitters)



Ch. 1 = 2.000 volts/div
Timebase = 20.0 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 15.8438 KHz

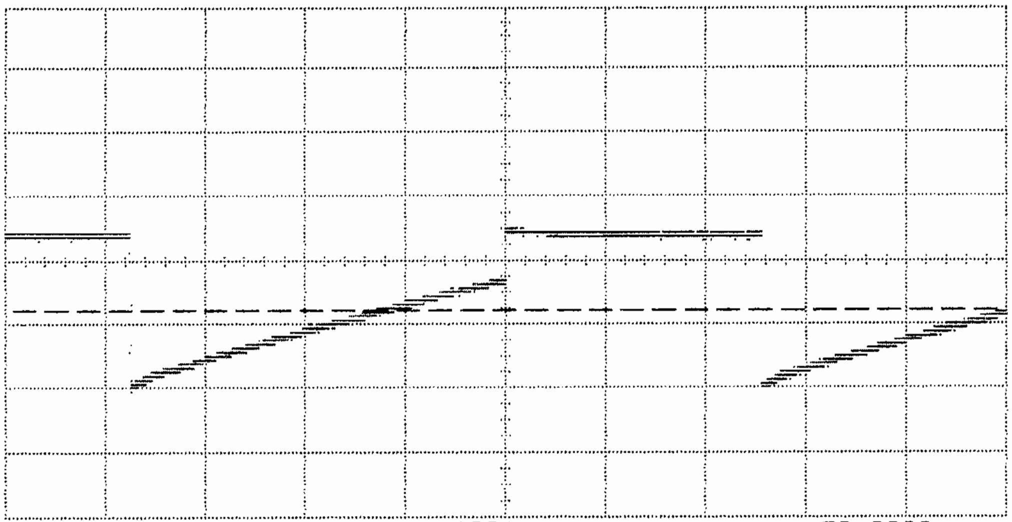
CRT Analog Waveform 1 (A1U507-10)



Ch. 1 = 2.000 volts/div
Timebase = 20.0 usec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 15.8410 KHz

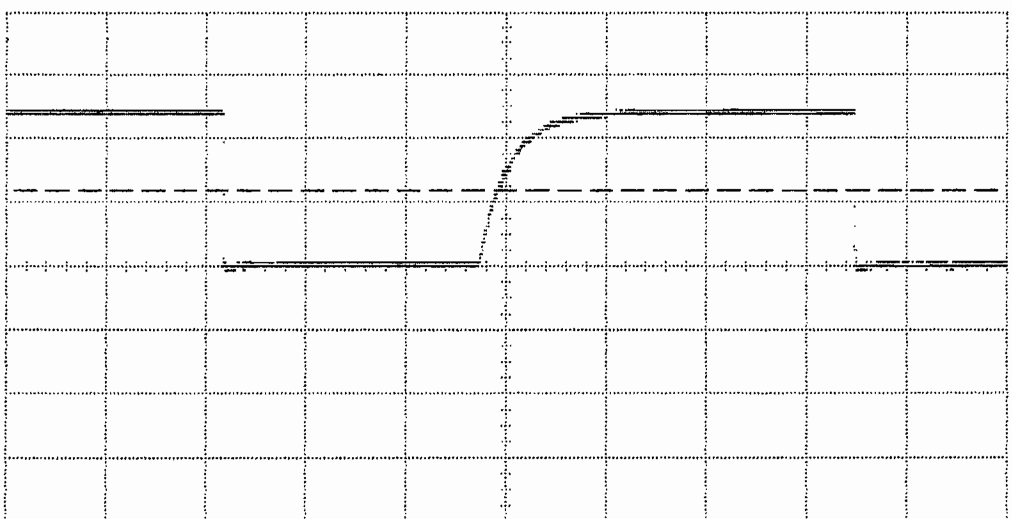
CRT Analog Waveform 2 (A1U507-12)



-50.0000 usec 0.00000 sec 50.0000 usec

Ch. 1	=	2.000 volts/div	Offset	=	0.000 volts
Timebase	=	10.0 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	15.8433 KHz

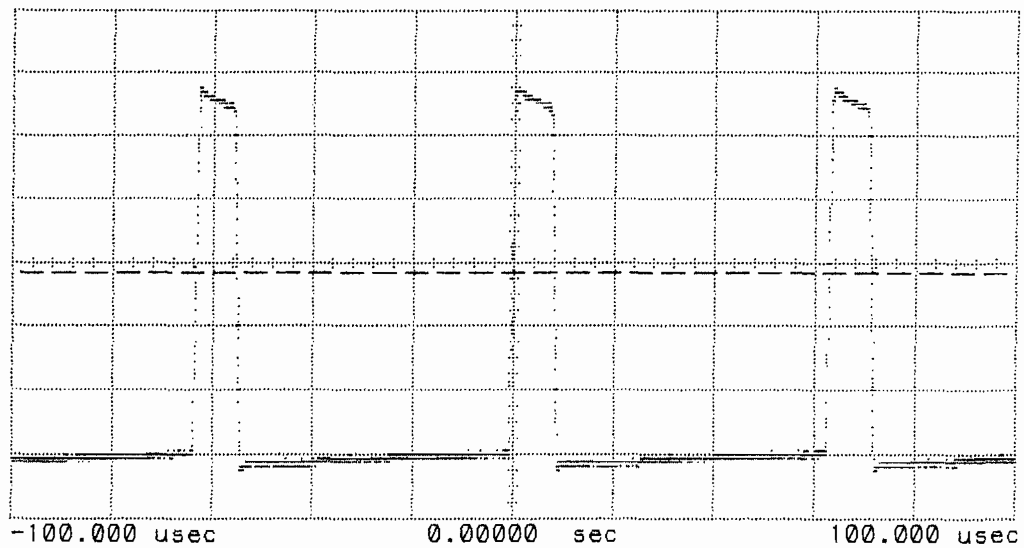
CRT Analog Waveform 3 (A1Q605 - Base)



-50.0000 usec 0.00000 sec 50.0000 usec

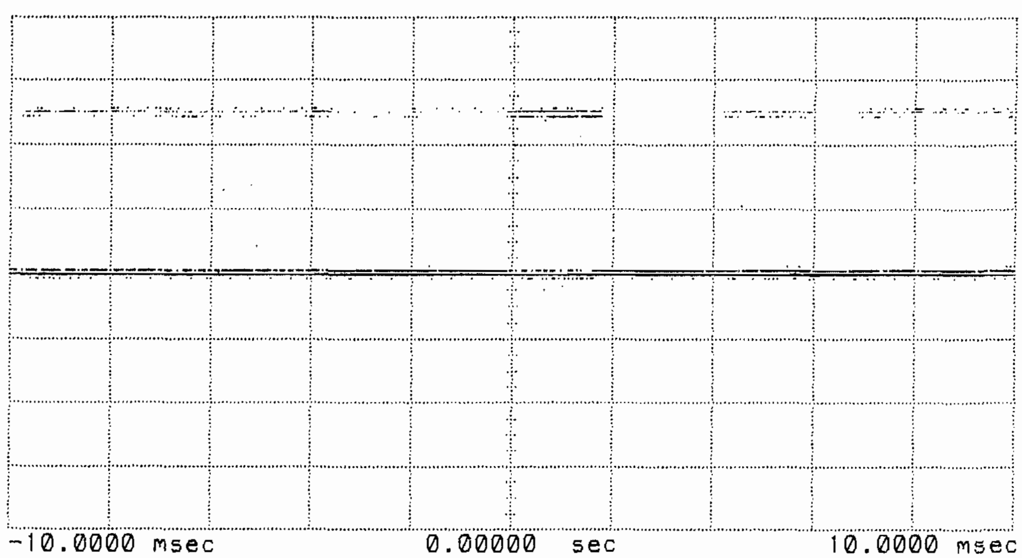
Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	10.0 usec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	15.8466 KHz

CRT Analog Waveform 4 (A1Q605 - Collector)



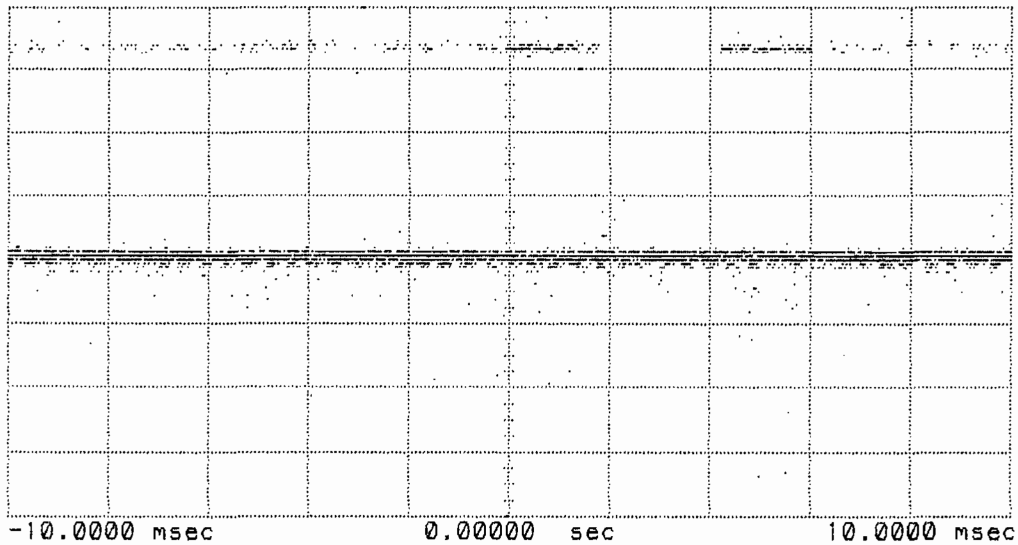
Ch. 1 = 10.00 volts/div Offset = 28.20 volts
Timebase = 20.0 usec/div Delay = 0.00000 sec
Ch. 1 Parameters Freq. = 15.8431 KHz

CRT Analog Waveform 5 (A1CR28 - Cathode)



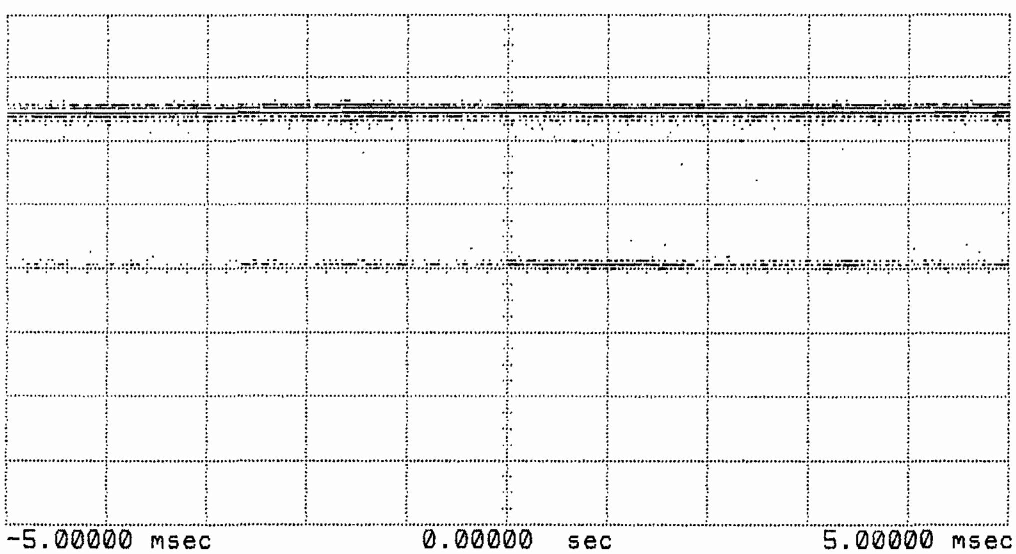
Ch. 1 = 2.000 volts/div Offset = 0.000 volts
Timebase = 2.00 msec/div Delay = 0.00000 sec

CRT Analog Waveform 6 (A1U805-5)



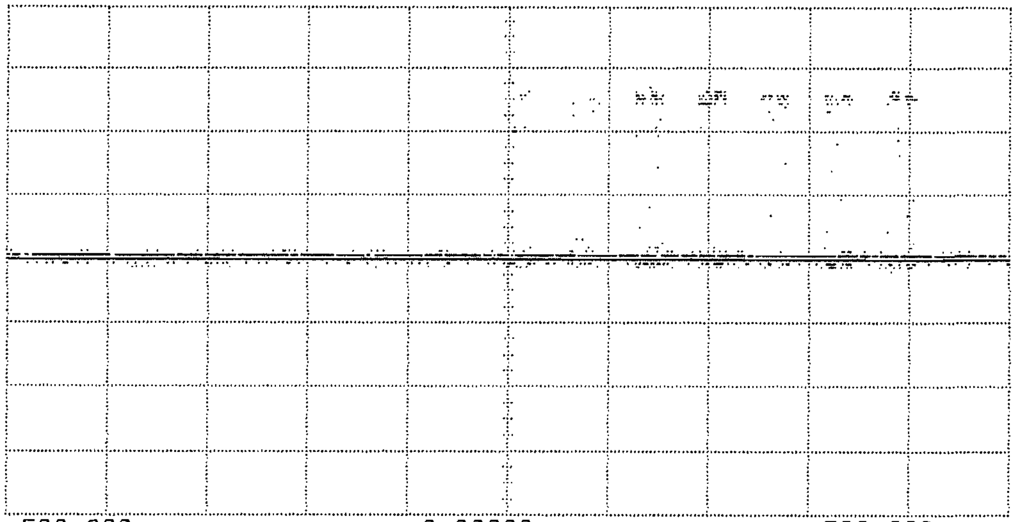
Ch. 1	=	200.0 mvolts/div	Offset	=	0.000 volts
Timebase	=	2.00 msec/div	Delay	=	0.00000 sec

CRT Analog Waveform 7 (A1Q804 - Base)



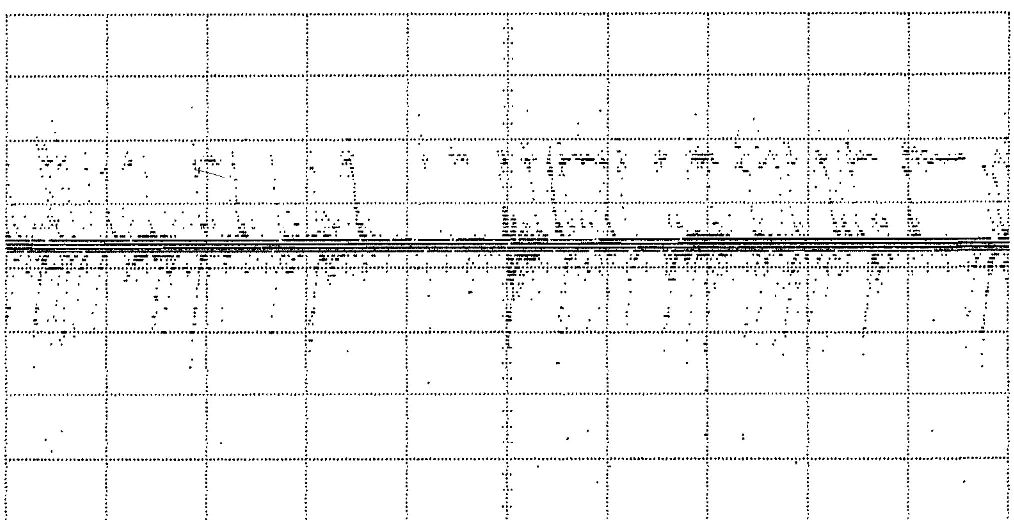
Ch. 1	=	10.00 volts/div	Offset	=	0.000 volts
Timebase	=	1.00 msec/div	Delay	=	0.00000 sec

CRT Analog Waveform 8 (A1Q804 - Collector)



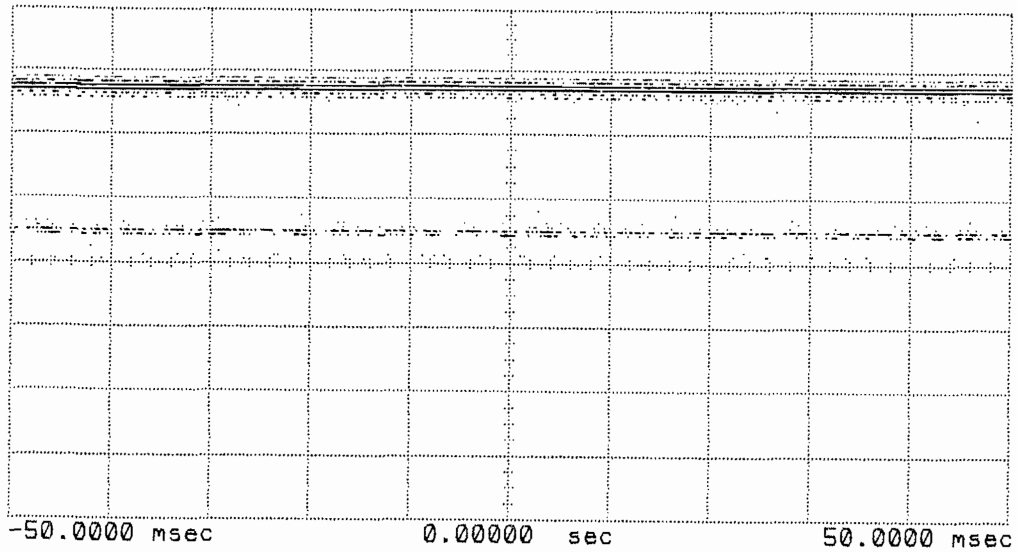
Ch. 1	=	2.000 volts/div	Offset	=	0.000 volts
Timebase	=	100 usec/div	Delay	=	0.00000 sec

CRT Analog Waveform 9 (A1U805-2)



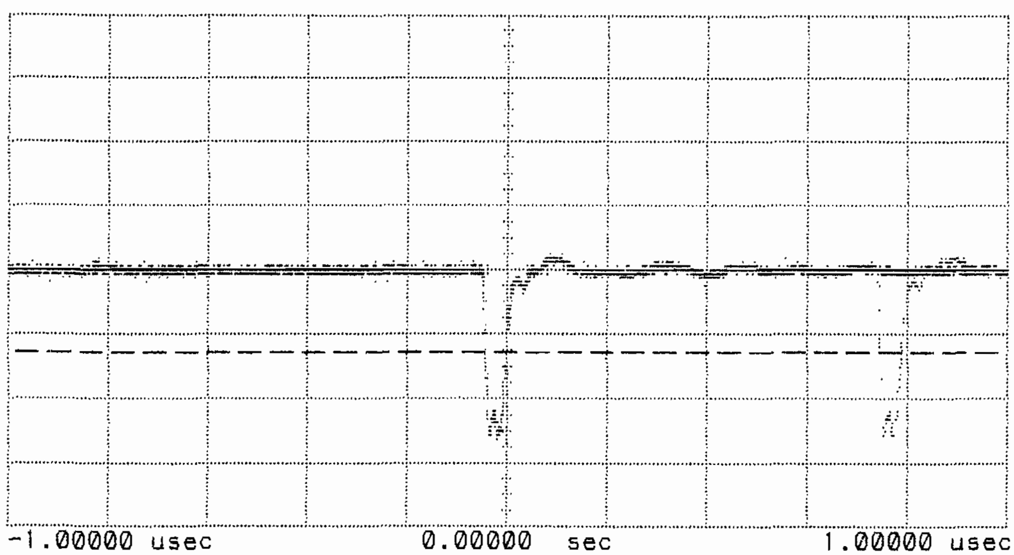
Ch. 1	=	500.0 mvolts/div	Offset	=	-160.0 mvolts
Timebase	=	2.00 usec/div	Delay	=	0.00000 sec

CRT Analog Waveform 10 (A1Q704 - Base)



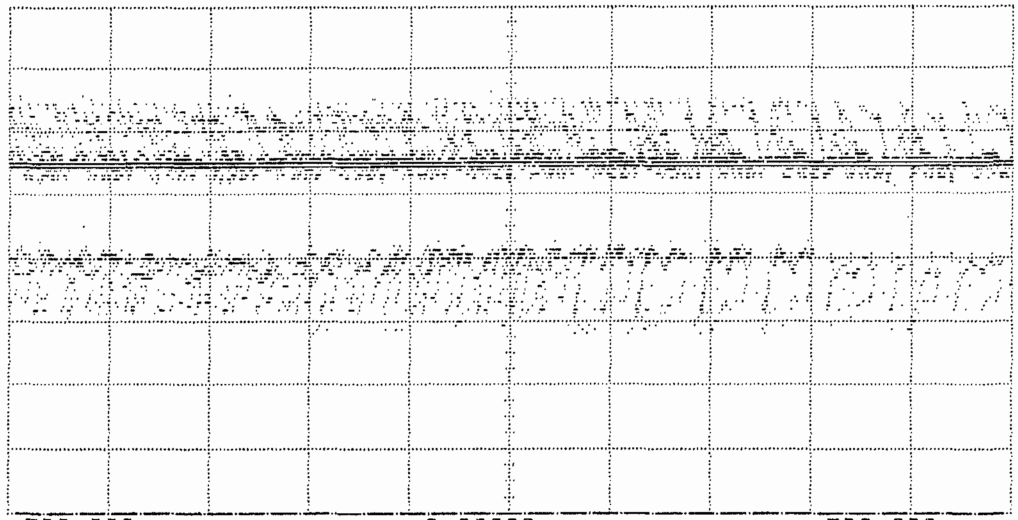
Ch. 1 = 10.00 volts/div
Timebase = 10.0 msec/div
Offset = 0.000 volts
Delay = 0.00000 sec

CRT Analog Waveform 11 (A1Q704 - Collector)



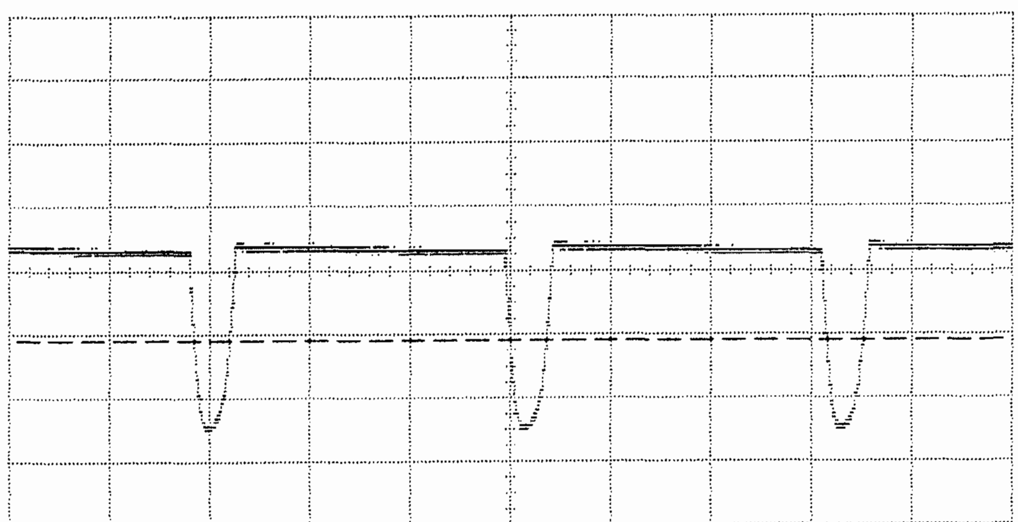
Ch. 1 = 2.000 volts/div
Timebase = 200 nsec/div
Ch. 1 Parameters
Offset = 4.940 volts
Delay = 0.00000 sec
Freq. = 1.23996 MHz

CRT Analog Waveform 12 (A1U805-9)



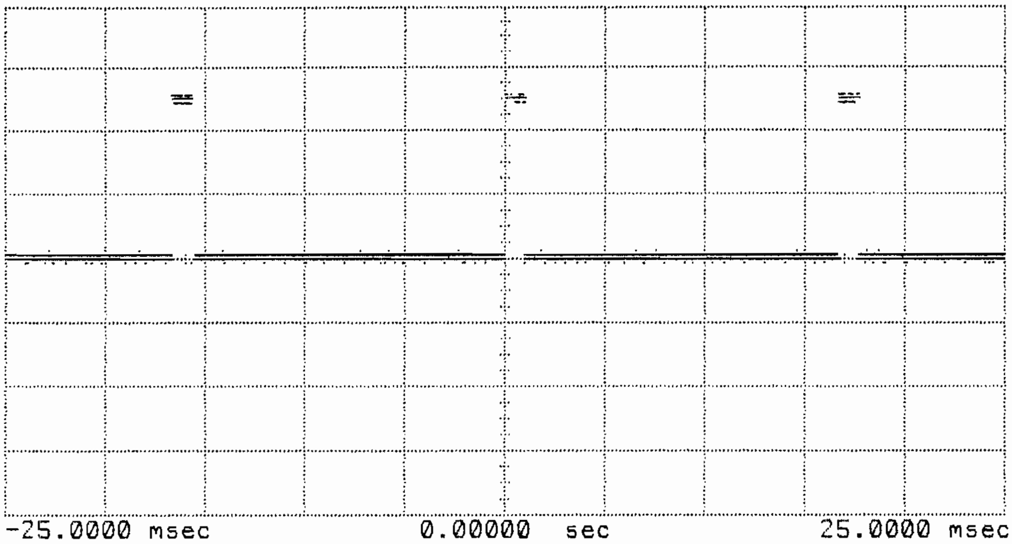
Ch. 1 = 10.00 volts/div
Timebase = 100 usec/div
Delta V = 0.000 volts
Vmarker1 = -55.00 volts
Offset = 0.000 volts
Delay = 0.00000 sec
Vmarker2 = -55.00 volts

CRT Analog Waveform 13 (A1Q702 - Collector)



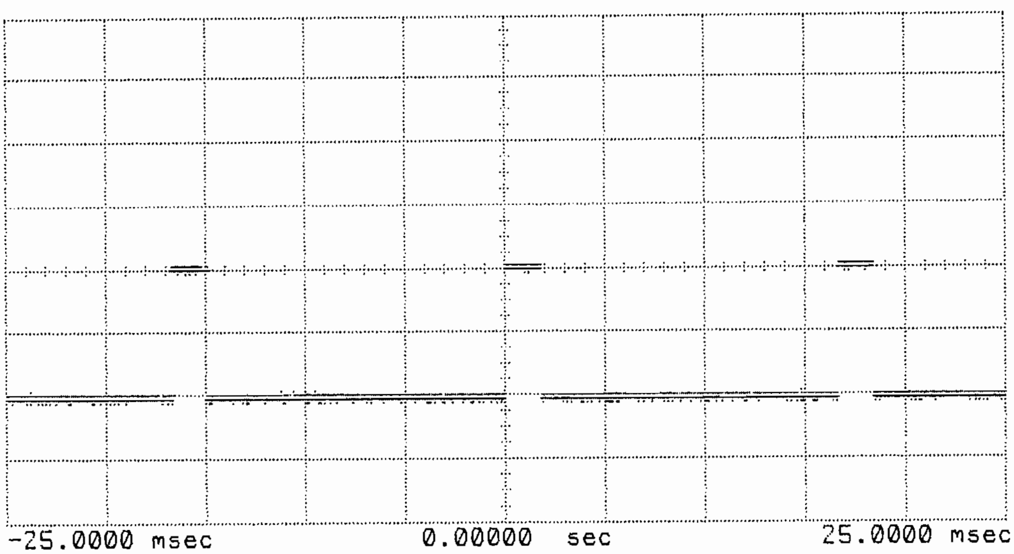
Ch. 1 = 50.00 volts/div
Timebase = 20.0 usec/div
Ch. 1 Parameters
Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 15.8461 KHz

CRT Analog Waveform 14 (A1CR25 - Anode)



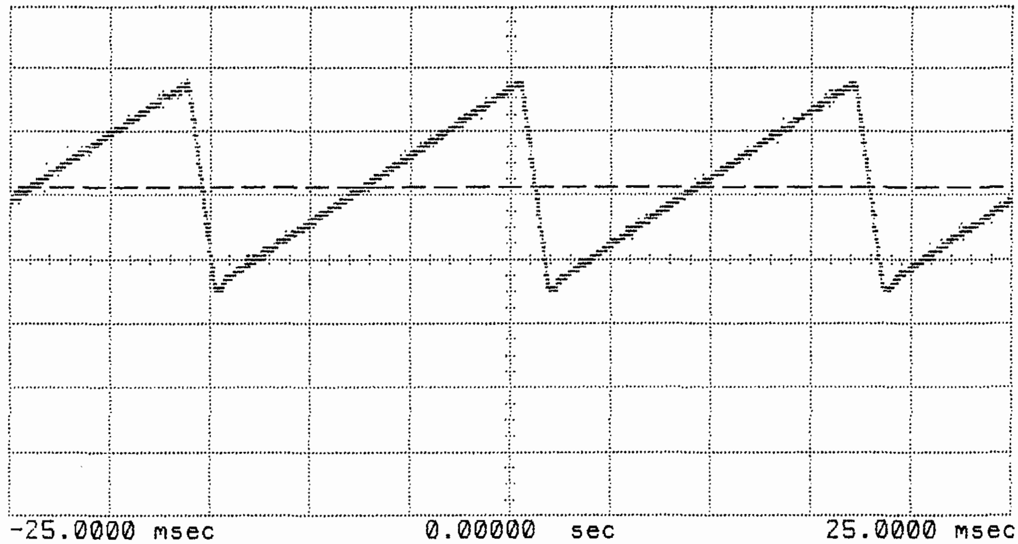
Ch. 1 = 2.000 volts/div Offset = 0.000 volts
Timebase = 5.00 msec/div Delay = 0.00000 sec

CRT Analog Waveform 15 (A1U507-2)



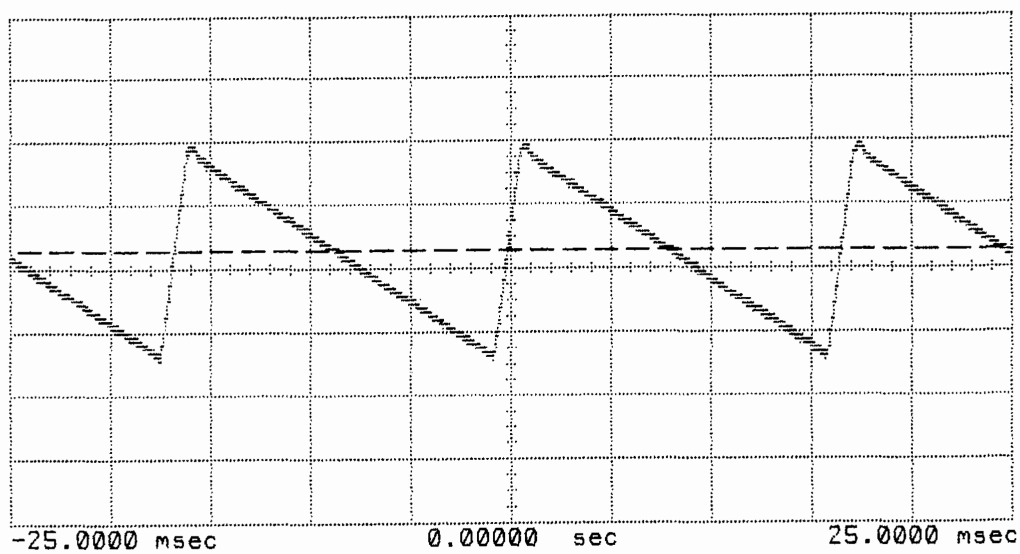
Ch. 1 = 1.000 volts/div Offset = 0.000 volts
Timebase = 5.00 msec/div Delay = 0.00000 sec

CRT Analog Waveform 16 (A1U608-1)



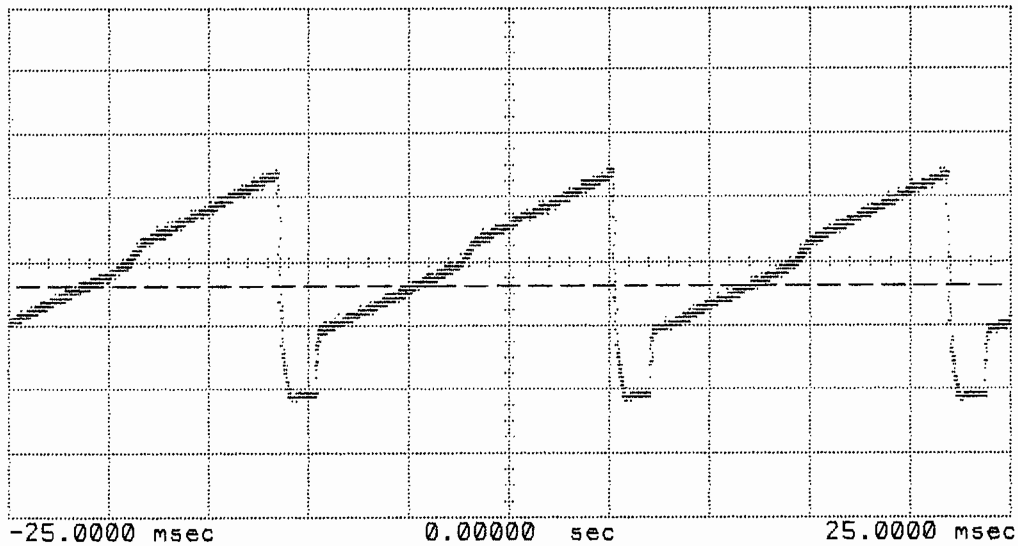
Ch. 1	=	1.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 msec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	60.1166 Hz

CRT Analog Waveform 17 (A1U608-7)



Ch. 1	=	5.000 volts/div	Offset	=	0.000 volts
Timebase	=	5.00 msec/div	Delay	=	0.00000 sec
Ch. 1 Parameters			Freq.	=	60.0305 Hz

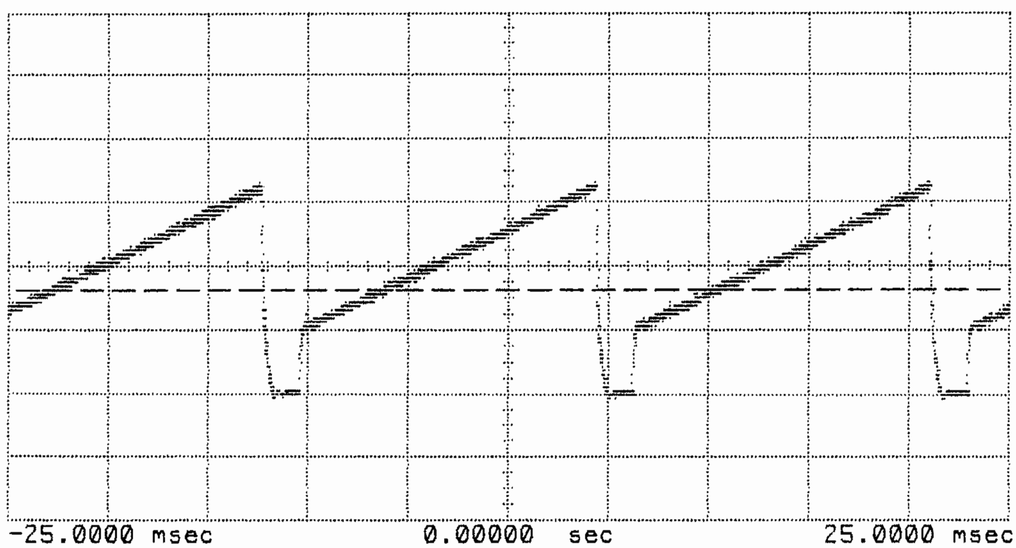
CRT Analog Waveform 18 (A1U608-8)



Ch. 1 = 5.000 volts/div
Timebase = 5.00 msec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 59.9890 Hz

CRT Analog Waveform 19 (A1U608-14)



Ch. 1 = 5.000 volts/div
Timebase = 5.00 msec/div
Ch. 1 Parameters

Offset = 0.000 volts
Delay = 0.00000 sec
Freq. = 59.9366 Hz

CRT Analog Waveform 20 (A1TP708 - A1Q606 & A1Q607 Emitter)

8-38. ARBITER TROUBLESHOOTING

A failure of the Arbiter Controller can cause several symptoms depending on the type of failure that exists. Failures will be noted as occurring early on in the beep sequence of the Performance Verification Tests. A continuous beep, one beep or two beeps can be caused by a failure in the Arbiter Controller. These types of failures can occur due to the fact that the arbiter is responsible for controlling a large amount of functional circuitry that exists in the kernel of the system.

Sequence of Events

During this test the Arbiter Controller (part of A1U510) is put into a free run test mode. This is accomplished by removing A1E408 (~RD) and A1E409 (~WR) which will tie the ~RD and ~WR inputs either high or low. There are three different modes of test used to check the operation of the Arbiter Controller. Each part manually drives the inputs to A1U510 and output conditions are established in each set up.

Circuitry Tested

This routine is used to verify the operation of the Arbiter Controller (A1U510). Trace continuity can be tested at the receiving nodes from the Arbiter controller outputs. The following nodes can be tested when there is activity on the output nodes of the Arbiter controller:

> Input and output conditions can be noted on the Arbiter Truth Table. When ~G (A1U510pin4) is active, you can check the transceiver enable on A1U613. When ~WCR (A1U510pin6) is active, you can test the CRT RAM write enable on A1U711. When ~WDR (A1U510pin34) is active, you can test the write direction and enables for A1U613 and A1U411. When ~EN (A1U510pin36) is active, you can test the CPU Bus Grant logic (A1U115 and A1U214) and the enables through A1U710 to A1U512, A1U713, A1U612, A1U711 and A1U411. When WAIT (A1U510pin37) is active, you can test its path to the CPU (A1U415). A1U510-35 (DE) is not active during this routine.

8-39. ARBITER TRUTH TABLE SETUP

The Arbiter Circuit has several ways to test it. Testing is comprised of putting the control lines into specific modes. There are three different modes of test. Each setup mode is explained with each table. With a given setup mode, output results are expected. The following tables document the setup mode, input values, and the expected output results.

When checking the functions of A1U510, use the "Key Modes" within the tables first. These modes are highlighted. If any of the output results are incorrect, A1U510 should be suspect as being bad.

Table #1 -

E408 (~RD) installed
E409 (~WR) installed

Set the input values on A1U510 pins 5, 3, and 38 to the values desired in Table 8-3, and then power the instrument up. Measure the output values on A1U510 pins 4, 6, 34, 35, 36, and 37.

A2 and A3 boards must be disconnected.
Remove XE815 to disable beeper.

Table #2 -

E408 (~RD) removed
E409 (~WR) removed

A1U510 pins 39 and 40 pulled low to circuit ground

Set the input values on A1U510 pins 5, 3, and 38 to the values desired in Table 8-3, and then power the instrument up. Measure the output values on A1U510 pins 4, 6, 34, 35, 36, and 37.

A2 and A3 boards must be disconnected.
Remove XE815 to disable beeper.

Table #3 -

E408 (~RD) removed
E409 (~WR) removed

A1U510 pins 39 and 40 pulled high to +5 volts DC.

Set the input values on A1U510 pins 5, 3, and 38 to the values desired in Table 8-3, and then power the instrument up. Measure the output values on A1U510 pins 4, 6, 34, 35, 36, and 37.

A2 and A3 boards must be disconnected.
Remove XE815 to disable beeper.

Table 8-3. Arbiter Truth Table

Signal PIN #	M4 (5)	HLD (3)	INT (38)	~G (4)	~WCR (6)	~WDR (34)	DE (35)	~EN (36)	~WAIT (37)
	0	0	0	H	H	H	L	H	L
#1	0	1	0	H	H	H	L	H	L
	1	0	0	H	H	H	L	H	L
	1	1	0	H	H	H	L	H	L
E408 & E409	0	0	1	X	H	H	L	H	L
ON	0	1	1	X	H	H	L	H	L
	1	0	1	H	H	H	L	H	L
	1	1	1	H	X	H	L	L	L
	0	0	0	H	H	H	L	H	L
#2	0	1	0	H	H	H	L	H	L
	1	0	0	H	H	H	L	H	L
	1	1	0	H	H	H	L	H	L
E408 & E409	0	0	1	X	X	X	L	X	X
OFF	0	1	1	X	X	X	L	X	X
	1	0	1	X	X	X	L	X	X
PINS 39&40=GND	1	1	1	X	X	X	L	X	X
	0	0	0	H	H	H	L	H	L
#3	0	1	0	H	H	H	L	H	L
	1	0	0	H	H	H	L	H	L
	1	1	0	H	H	H	L	H	L
E408 & E409	0	0	1	H	H	H	L	H	L
OFF	0	1	1	H	X	H	L	X	X
	1	0	1	H	H	H	L	H	L
PINS 39&40= +5	1	1	1	H	X	H	L	L	L

Legend:
- 0, L = zero volts dc
- 1, H = +5 volts dc
- X = Active Signal, Toggle states
- (shaded) = Key Modes

* - If incorrect results are seen at pin 35 (DE), cycle the instrument power and measure the node again.

8-40. TIC CLOCK GENERATOR TROUBLESHOOTING

The Tick Clock circuitry is not tested by the power up Performance Verification routine. Tick Clock failures will only be evident during run time operations or during post processing of data. Tick Marks are not visible to the user in any form. They are inserted with the data during run time and do not appear on the data screen. The Tick Mark failure is most evident when making timing measurements and getting incorrect or unexpected results.

Set Up Routine

During this diagnostics routine the instrument is in the "Top Level" display mode. The Tick Clock Counter (A1U114) is in a free run mode.

Circuitry Tested

This routine checks the operation of the Tick Clock Counter. When Tick Mark errors are evident and the counter checks out, the Tick Clock Latch (A1U712) could be suspected.

LOOP: TIC Clock Generator

PCA: A1 Main Board

SETUP: Instrument at top level
No Jumpers

* - Totalized Signature
(+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/+	A1U114- 9 (RSTA)
QUAL		
CLOCK	+	A1U415- 9 (SYS CLK)
GROUND		A1U114- 7 (GND)

VHIGH = 48CF

U114-	1-	0A3C
A1-3	2-	UN
	3-	513C
	4-	CH89
	5-	745P
	6-	8PA4
	8-	L
	9-	UN
	10-	7103
	11-	C2A1
	12-	UN
	13-	8PA4

8-41. REMOTE/PRINTER INTERFACE TROUBLESHOOTING

The Remote/Printer Interface troubleshooting procedure can be used to isolate the failure when the Remote test in the Self Test Loop has detected a failure. The procedure may also be used when no failure has been detected by the Remote Self Test but a remote or printer operation fails to operate properly. The Remote Self Test is not capable of verifying the operation of the input or output driver stages.

Sequence of Events

This diagnostics procedure is used to manually check the Remote/Printer interface of the A2 board. Most failures in the Remote/Printer Interface can be detected with the use of the Remote test, contained within the Self Test Loop. Failures in the TTL to RS232 level converter circuitry A2U102 and A2U103 will not be noted in the Self Test Loop. The HP 4951C should be in the Top Level Menu while the procedure is performed. Node and frequency checks are performed while the circuitry is manually enabled by the person doing the troubleshooting.

Circuitry Tested

During the Quick Test procedure some key checks are made. The clock input to the ACIA (A2U209) device is first checked. This measurement verifies the default operation of the Program Latch, Clock Generator, and Speed Multiplexer (A2U206, A2U207 & A2U106). Next, the outputs of the Loop Back Multiplexer (A2U107) are checked. This verifies partial operation of the multiplexer.

During the Detailed Troubleshooting Procedure more measurements are made to isolate the failure to a discrete component. The divide by 16 and 64 functions of the Clock Generator (A2U207) are checked first. Then the operation of the Speed Multiplexer (A2U106) is verified.

Several circuit areas are checked during the ACIA, Multiplexers, and the output section of the Remote/Printer Interface Troubleshooting. First, the ACIA is checked by running the instrument in the Continuous Self Test Loop and making node measurements associated with the ACIA. Next the output and input driver reverence levels are verified. Lastly, the operation of the output and input driver circuits are verified by providing a sinewave to each input stage and measuring the output of each stage.

8-42. REMOTE/PRINTER INTERFACE TROUBLESHOOTING

Quick Test Procedure

1. Get to the Top Level Menu on the HP 4951C.

The frequency at A2U209 pin 3 should be 76.8 kHz.

Pass- See step 3
Fail- Proceed to step 2

2. Put the HP 4951C into the continuous Self Test Loop.

The frequency at A2U209 pin 3 should change.

Pass- The problem is in the ACIA, Multiplexer (A2U209, A2U204), or the output stage.
Fail- The problem is in the baud rate generator circuit of the Remote/Printer board (A2U206, A2U207, or A2U106).

3. Put the HP 4951C into the continuous self test loop. A2U209 pin 6 and A2U107 pin 2 should have pulsing waveforms during the Remote Test execution.

Pass- Troubleshoot the output stages.
Fail- Troubleshoot A2U209 and A2U107.

Detailed Troubleshooting Procedure

If the Remote Interface test passes in the Performance Verification Self Test, but the Remote/Printer Interface does not work, the output stages are probably defective. To troubleshoot the Remote/Printer board, use the following procedures:

1. Get to the Top Level Menu on the HP 4951C.

The following conditions must be present and A2U207:

pin 22 is high
pin 23 is low
pin 10 is high

2. Check the divide by 16 capability of the divider. The frequencies listed below should be present at A2U207:

pin 2 -	76.8 kHz
pin 3 -	38.4 kHz
pin 4 -	19.2 kHz
pin 5 -	9.6 kHz
pin 6 -	3.2 kHz
pin 7 -	4.8 kHz
pin 8 -	2.4 kHz
pin 9 -	1.2 kHz
pin 20 -	1843.2 kHz
pin 21 -	1843.2 kHz

3. Verify the divide by 64 function.

Set Up

Disable A2U206 by pulling pin 1 to 5 vdc.
Pull pin 22 and 23 of A2U207 to 5 vdc.

Verification

Verify the following frequencies on A2U207:

pin 2 -	307.2 kHz
pin 3 -	153.6 kHz
pin 4 -	76.8 kHz
pin 5 -	38.4 kHz
pin 6 -	12.8 kHz
pin 7 -	19.2 kHz
pin 8 -	9.6 kHz
pin 9 -	4.8 kHz

4. Verify the operation of A2U106.

Set Up

Disable A2U206 by pulling pin 1 to 5 vdc.
Pull pin 23 of A2U207 to 5 vdc.
A2U106 pins 9, 10, and 11 should be high tristated due to A2U206 being disabled.

Verification

Connect the jumpers on A2U106 in the sequence listed below.
Verify that the correct frequency is at pin 5.

pin 9	pin 10	pin 11	pin 5 (frequency)
L	L	L	12.8 kHz
L	L	H	4.8 kHz
L	H	L	9.6 kHz
L	H	H	19.2 kHz
H	L	L	38.4 kHz
H	L	H	76.8 kHz
H	H	L	153.6 kHz
H	H	H	307.2 kHz

8-43. ACIA, MULTIPLEXERS, AND OUTPUT TROUBLESHOOTING

1. Get to the Top Level Menu.

   A2U209 pins 3 and 4 should have a square wave with a frequency of 76.8 kHz.

2. Put the HP 4951C into the continuous Self Test Loop.

   Press the softkeys <More>, <   >(f6, hidden 'Continuous Loop' function).

3. Verify that the following conditions exist on A2U209:

pin 2	High until remote test starts, then shows negative pulses.
pin 5	Low until remote test starts, then shows positive pulses. Set sweep rate to 1 sec on the scope.
pin 6	High until remote test starts, then shows negative pulses.
pin 7	High
pin 8	High
pin 9	High until remote test starts, then shows negative pulses.
pin 10	Pulses
pin 11	Pulses
pin 13	Negative Pulses
pin 14	High
pins 15 thru 22	Continuous address and data activity
pin 23	Low until remote test starts, then shows positive pulses.
pin 24	Low until remote test starts, then shows positive pulses. Set sweep rate to 1 sec on the scope.

4. Troubleshoot the output stage.

Set Up

Disable A2U206 by pulling pin 1 to 5 volts dc. Get the Top Level Menu.

Verification

Verify the following approximate voltage levels:

A2U102	A2U103
pin 5 - 2 vdc	pin 5 - 4 vdc
pin 10 - 2 vdc	pin 7 - 4 vdc
pin 12 - 2 vdc	pin 9 - 4 vdc

5. Troubleshoot A2U204 and A2U102.

Set Up

Pull pin 1 of A2U206 to 5 volts dc through a 100 ohm resistor.
Pull pins 9 and 12 of A2U204 low through a 100 ohm resistor.

Set up the external Signal Generator to a 1 KHz sinewave at 5 volts. Connect the Signal Generator to pins 10 and 13 of A2U204, to check TXD and RTS signal levels.

Verification

Check the following inputs and outputs of A2U102:

pin 6	5 volt squarewave
pin 7 (J4 pin 15)	+/- 12 volt squarewave
pin 8 (J4 pin 13)	+/- 12 volt squarewave
pin 9	5 volt squarewave

6. Test the DTR output.

Set Up

A2U206 should NOT be disabled. Put the HP 4951C into a continuous Self Test Loop.

Verification

A2U204 pin 14 and J4 pin 7 should have signal activity at levels of +/- 12 vdc.

7. Troubleshoot the input stages of RXD, CTS and DCD (A2U102).

Set Up

Input a sinewave of 12 volts peak to peak at 1 KHz on input pins 3, 5 and 8 of the A2J4 Remote Port.

Verification

Check for the following squarewaves at the inputs and outputs of A2U103:

pin 4	5 volt squarewave
pin 6	5 volt squarewave
pin 8	5 volt squarewave
pin 1	5 volt squarewave
pin 2	5 volt squarewave
pin 14	5 volt squarewave

8-44. POD INTERFACE TROUBLESHOOTING (Buffer and Relay)

This procedure should be used after an External DLC failure has been verified within the Self Test Menu.

Sequence of Events

During this procedure the instrument is in the Top Level Menu and any Pod Interface is connected. You can then make several manual measurements of discrete nodes within the circuitry. You can also manually enable and disable the pod interface relay circuitry for functional verification.

Circuitry Tested

Several discrete components are functionally checked during this procedure. The first part addresses the Pod Interface Buffer (A1U113). The procedure shows how to manually check the buffer. The second section of the procedure addresses the Pod Relay circuitry which is responsible for detecting the presence of a Pod Interface. This circuit block also supplies the necessary supply voltages to the Pod Interface Assembly that are needed for proper operation via the Pod Interface Relay (A1K208).

8-45. POD INTERFACE TROUBLESHOOTING

Interface Buffer

Set Up

Interface pod detached.
Instrument in Top Level Menu.

Verification

With the use of an IC clip and a jumper wire, manually toggle the outputs of A1U113 by driving the inputs to 5 vdc or system ground. Verify the output levels with a scope or digital voltmeter.

POD Interface Relay and Activation Circuitry

Set Up

Interface Pod detached.
Instrument in Top Level Menu.

A1U515 (And Gate) :	pins 3,4,5 and 6 should be high.
A1U213 (Inverter) :	pin 12 low and pin 13 high.
A1U311 (D Flip/Flop) :	pin 1 should be low.
	pin 3 should be low.
	pin 4 should be high.
	pin 5 should be low.

Verification

Verify the circuit and relay operation by enabling or disabling the circuit. To turn the relay on, touch 5 vdc to A1U311 pin 3. To turn the relay off, touch ground to A1U311 pin 3. Check the circuit operation. Additional checks of the Interface Cable to the rear panel can be performed by checking the voltage levels on the corresponding pins of the pod interface connector.

8-46. DISC CONTROLLER TROUBLESHOOTING

Testing of the A3 Disc Controller assembly is comprised of several firmware programs residing within the ROM A3U606. The concept is similar to that used for the main system during power up conditions. The specifics of the power up test are quite different from those used in the main system.

"Loop on failure" is a concept that is used in the algorithm of the self test routine (refer to the flow chart, Section VIII). The Self Test checks the hardware in an iterative fashion, building from the kernel (CPU, A3U500), outward to the disc drive (FDC) interface. The NSC800 Interface is not checked by the 8088, but by the NSC800 as it interrupts the Disc Controller for it's self test status.

There are several ways to initiate the Disc Controller Self Test:

A. Power up the HP 4951C. The disc test will run twice (once at initial power up and once when the NSC800 calls the Disc Self Test from the Self Test Loop). Any failure information is reported within the Mass Store Menu.

B. Call the Disc Self Test from the instrument Self Test Menu (refer to the Softkey Menu Guide, Section IV). The test will execute once and pass/fail information will be reported to the display.

C. Call the Disc Self Test from the instrument Self Test Menu using "Loop" for a continuous Self Test mode.

Portions of the Disc Controller Self Test can be forced to loop immediately (PIC test, DMAC test & FDC test). These conditions can be obtained by configuring two jumpers, E1 & E2 (refer to the following and the Disc Test Flow Chart).

PIC test	remove E2
DMAC test	remove E1
FDC test	remove E1 & E2

Disc System Service Assembly

The Disc System Service Assembly (p/n 5060-7184) is required to properly service the Disc Controller assembly. Because of space restrictions on the Disc Controller assembly, diagnostics circuitry could not be designed onto the pc board. The primary use of the assembly is to obtain an electrical configuration to allow the 8088 CPU to run in a NO-OP mode. This mode of operation is obtained with the use of the E201 bus jumper, E101 AND E102 control signal jumpers, and E103 the input buffer enable. Note that the CPU NO-OPs mode is also used to free run the system CPU (NSC800). The other main use of the Disc System Service assembly is for mode and error status display. This information is visible from CR202 located on the Disc System Service assembly. Refer to the reference designator information and the Disc Service Assembly schematic for electrical information. the Disc Controller LED Display Table shows the variety of display codes and VHigh signatures throughout the testing spectrum of the Disc Controller assembly.

Troubleshooting Overview

The first thing to do when troubleshooting the Disc Controller assembly is to verify a failure of some type. There are several indicators to use in verifying a failure:

A. During power up, if the Disc Controller test nears completion, the disc drive led will become active for a short period of time. The first occurrence of the LED flash should happen nearly at the same time that the HP 4951C executes the third beep of its power up self test sequence. The second flash of the disc drive LED should occur after the HP 4951C calls the disc self test during the power up sequence. You will see in the upper right hand corner of the display, the name of the test that is being executed by the main system. Failure information will be present and visible within the Mass Store Menu. A pass/fail indication will be evident. Absence of the disc drive LED activity also denotes a probable failure of the Disc Controller System.

B. From the Self Test Menu, the Disc Test can be called from the keyboard. The disc drive led will become active upon completion of the test routine. Specific error information will be presented on the display. One of several error messages may be displayed.

C. From the Mass Store Menu, there are several disc operations which are accessible. Most types of operational errors will be detected and reported accordingly during execution of some chosen operation. Error information will be reported on the display. These error messages are listed in Table 8-3 near the end of this section.

D. With the use of the Disc System Service assembly, two more error indicators are made available. With the diagnostics board properly installed, status information is displayed on the LED bank (CR202). With a Signature Analyzer properly connected and configured, unique VHigh signatures which provide status information of the test being executed will be presented. Refer to the LED Display Code Table for this information.

With the use of the indicators, you can derive some information about the failure related to the Disc Controller System. There are some general statements that can be made about analyzing the Disc Controller System.

A. The disc test occurs twice during power up of the instrument. Once when power is applied and once when the NSC800 system initiates it during the power up sequence.

   1. The Disc Controller Interface is exercised only when it is called on by the NSC800 CPU. Knowing this is helpful in determining if the interface is bad. If the disc drive LED flashes once (with the third beep of the instrument) during powerup, chances are the disc drive self test is passing and the interface is causing a failure. If there is no flash of the disc drive LED, then chances are that the failure mechanism is not associated with the interface circuitry.

B. If the disc Self Test fails when manually called by the operator, the disc diagnostics board will provide the best means of problem isolation. The next level of isolation is provided by the error code given by the LED display bank followed by the indication given by the VHigh signatures. The VHigh indicates which firmware routine is being repetitively executed. Refer to the LED Display Code Table to see which routine is not operating properly.

   1. The ROM, RAM & PIC tests are designed to loop on failure and are not individually accessible.

   2. The PIC1, PIC2, DMAC & FDC tests are not designed to loop on failure, but to report an error code to the system. The system then displays the proper error message. These tests can be manually activated. The E1 & E2 jumpers are used to enable this function.

C. When the Disc Controller causes operational failures from the Mass Store Menu and the Disc Self Test passes, several things can be suspected as being the failure mechanism.

1. The Disc Controller adjustments may not be properly adjusted. These are the first things to check when failures occur while performing an operation in the Mass Store Menu. Refer to Section V for the adjustment procedure.

2. The Disc Drive assembly itself could be bad. Many of its operations are not checked in the Disc Test. Failures related to reading or writing data to the disc will be evident from within the Mass Store Menu.

3. The failure mechanism could be located on the Disc Controller assembly itself. It most likely would be associated with the interface circuitry or the FDC itself.

The following are error messages associated with the Mass Store Menu and its operation.

Table 8-4. Mass Store Menu Errors

ERROR	EXPLANATION
Disc Out	Disc is not inserted into the drive.
Checksum Error	CRC error occurred during read or write.
Seek Error	Disc Drive unable to seek to track.
Drive Error	Drive is not working right (not ready).
Write Protected	Disc is write protected (tab on disc).
Media Wear Protected	Disc is write protected due to media wear.
Bad Disc	Disc will not format (too many bad tracks).
Disc Full	Disc is full of data, no more will fit.
Disc Not Formatted	Disc is not formatted.
Non LIF Format	Non LIF format in the disc.
Bad Sector Size	Formatted with 512 or 1024 byte sectors.
EOF Error	Tried to read past end of file.
Record Not Found	Record not found during a read or write.
Single Sided Disc	Disc is formatted single sided.
Controller Error	Controller is not working correctly (lost data).
Directory Full	Directory is full, no more entries exist.
Directory Too Large	Disc formatted with directory too big.
Improper Format	Disc formatted wrong for runtime Write_Open_LIF.

8-47. DISC CONTROLLER DIAGNOSTICS ROUTINES

8088 Microprocessor NO-OPS, Mode 1

This diagnostics routine is used to verify the operation of the diagnostics board and the 8088 CPU. When using the diagnostics board, remove the 8088 CPU (A3 U505) from the A3 Disc Controller assembly and install it onto the diagnostics board. The connector on the cable of the diagnostics board plugs into the CPU socket (A3U505) on the A3 board. Note the polarity of each device as you plug them in. The Disc Controller System should function properly with the diagnostics board attached and all of the jumpers in the "normal" position. Refer to the individual SA tables for the specific set up information.

8088 Microprocessor NO-OPS, Mode 2

This diagnostics routine is used to test the circuitry residing on the A3 board. It checks the kernel of the system. This test should be used to verify a ROM or RAM test failure. The operator can check the address, data and control lines to the ROM and RAM by using this routine. The contents of the ROM can be checked as well.

A3 Interface Buffers 8088 -> 800

This diagnostics routine is designed to check the interface buffers going from the 8088 system to the NSC800 system. The 8088 Microprocessor No-ops, Mode 2, is used to execute this routine.

A3 Interface Transceiver 800 -> 8088

This test routine checks the operation of the interface transceiver (A2U608) as it sends data from the NSC800 data bus to the 8088 data bus. This routine is based on the NSC800 Microprocessor No-ops routine.

ROM Test

This test is used only by the system. To verify the operation of the ROM, the operator must use the 8088 Microprocessor No-ops routine.

RAM Test

This test is used only by the system. To verify the operation of the RAM, the operator must use the 8088 Microprocessor No-ops routine. If address, data and control lines verify good, the RAM should be suspected as being defective.

PIC Test

This test consists of two main sections. Pic 1 tests the 8088 system interface to the PIC. Pic 2 tests the interrupt inputs to the PIC device. This test is active during the Disc Self Test or when the operator removes the E2 jumper. Four different VHigh conditions are possible during this test loop. Pic 2 failures can be caused by either the PIC device itself or the circuitry which generates the interrupt inputs to the PIC.

DMAC Test

This test is used to exercise the DMA Controller operation. The test is designed to do a 100 hex block move from one address block in the Disc Controller RAM to another address block within the Disc Controller RAM (A3U304). The operation of the DMA Controller (A3U400) is the focus of the test. Operation of the bus arbitration circuitry (A3U203, A3U704, and A3U706) and the upper byte address latch (A3U403) are checked as well. One restriction within the DMAC test is the full address range of the DMA Controller and upper byte address latch cannot be fully tested. In most failure modes, the upper byte address latch should be suspected as the failure mechanism. Following are the steps for problem isolation of a DMAC test failure:

A. Verify a DMAC failure by viewing the error message reported to the screen after manually initiating the disc test or verify the failing Vhigh signature while the DMAC test is looping by removing the A3E1 jumper.

B. Using the signature analyzer, verify the proper activity in the bus arbitration circuitry (A3U203, A3U704, and A3U706). If good, go to step 3.

C. Verify signal activity on the inputs and outputs of the upper byte address latch (3U403). When there is a DMAC test failure, this part should be replaced prior to any others in the associated circuitry. This part is not fully tested, is the easiest to remove, and is the least costly. If a DMAC test failure still exists after replacing the upper byte address latch, the DMA Controller can then be suspect.

D. After the above steps have been done, operation of the DMAC can be verified with the use of the signature analysis table.

FDC Test

The FDC test is used to test the operation of the FDC (floppy disc controller) and partial operation of the Disc Drive. It is important to know that a failure of the disc drive will cause a failure of the FDC test. There are several things to check before suspecting the FDC as the failure mechanism:

A. Check the output control signals from the FDC, through the buffering device (A3U703 & A3U803), to the disc drive.

B. Check the input signals from the disc drive, through the buffering device (A3U603 & A3U703), to the FDC. Refer to tables the Disc Controller Flowchart and the Disc Controller LED Display.

If the above signals check out good, the FDC can become a higher suspect as being the failure mechanism. This test is active during the Disc Self Test or when the operator removes E1 or E2.

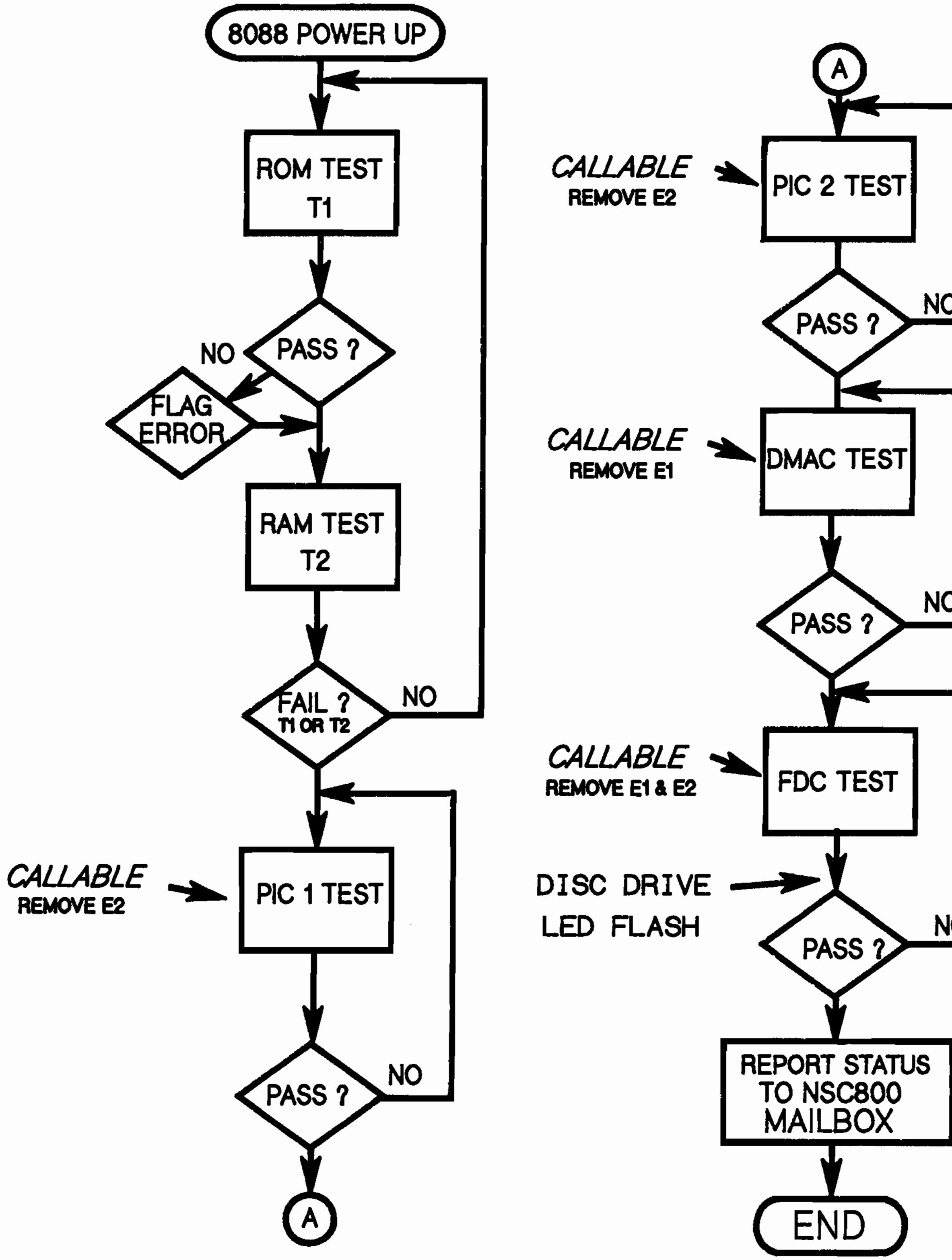


Figure 8-6. Disc Controller Flowchart

Table 8-5. Disc Controller LED Display

DISC CONTROLLER LED DISPLAY CODE TABLE		
TEST ROUTINE RUNNING	LED DISPLAY	SA, VHIGH
8088 MICROPROCESSOR NO-OPS, MODE 1	●○○○○○	0001
8088 MICROPROCESSOR NO-OPS, MODE 2	●○○○○○	0001
A3 INTERFACE BUFFERS 8088 -> 800	●○○○○○	0001
A3 INTERFACE TRANSCEIVER 800 -> 8088	○○○○○○	0001
ROM (TEST FAILING)	●●●○○○	NONE
RAM (TEST FAILING)	●●○●○○	NONE
PIC (TEST PASSING)	●●○○○○	P196
PIC (ERROR 1)	●●○○●○	FP67
PIC (ERROR 1.1)	●●○○●○	9515
PIC (ERROR 2)	●●○○○●	2538
DMAC (TEST PASSING)	●●○○○○	479P
DMAC (ERROR 1)	●●○○○○	16FF
FDC (TEST PASSING)	●●○○●●	90A3
FDC (ERROR 1)	●●○○●●	4P5U
FDC (ERROR 2)	●●○○●●	HF8H
FDC (ERROR 3)	●●○○●●	APOF
ALL TESTS PASSING	●●●○●●	NONE

LOOP: 8088 NO-OPS (Mode 1)

PCA: A3 Disc Diagnostics Board

SETUP: Test board installed. Remove E201 (AD0-AD7 bus jumper). Place E101, E102 and E103 to the 'T' position

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

	EDGE:	NODE:
SA MODE: Norm		
START/STOP	+/+	Test Board CPU(U100)pin39
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 0001

● ○ ○ ○ ○ ○

U100-
A30

1-	L	21-	L
2-	3827 (A14)	22-	H
3-	3C96 (A13)	23-	L
4-	HAP7 (A12)	24-	H
5-	1293 (A11)	25-	65536*
6-	HPP0 (A10)	26-	65536*
7-	2H70 (A9)	27-	L
8-	HC89 (A8)	28-	L
9-	52F8 (AD7)	29-	H
10-	UPFH (AD6)	30-	L
11-	0AFA (AD5)	31-	L
12-	5H21 (AD4)	32-	65536*
13-	7F7F (AD3)	33-	H
14-	CCCC (AD2)	34-	L
15-	5555 (AD1)	35-	16* (A19)
16-	UUUU (AD0)	36-	16* (A18)
17-	L	37-	65520* (A17)
18-	L	38-	16* (A16)
19-	0FL0*	39-	755P (A15)
20-	L	40-	H

LOOP: 8088 NO-OPS (Mode 2)

PCA: A3 Disc Controller Board

SETUP: Test board installed. Remove A3U606. E201 installed. Place E101, E102 and E103 to the 'T' position

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/+	Test Board CPU(U100)pin39
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)
VHIGH = 0001		● ○ ○ ○ ○ ○

XU606- A3-1	1-	755P
	2-	HAP7
	3-	52F8
	4-	UPFH
	5-	0AFA
	6-	5H21
	7-	7F7F
	8-	CCCC
	9-	5555
	10-	UUUU
	11-	UUUU
	12-	5555
	13-	CCCC
	14-	L
	15-	7F7F
	16-	5H21
	17-	0AFA
	18-	UPFH
	19-	52F8
	20-	CA7C
	21-	HPP0
	22-	0001
	23-	1293
	24-	2H70
	25-	HC89
	26-	3C96
	27-	3827
	28-	H

U304- A3-1	20-	65536*
	22-	CA7A
U500- A3-1	9-	UUUU
	10-	UUUU
	12-	5555
	13-	5555
U708- A3-1	1-	0016*
	2-	0016*
	4-	65536*
	12-	CA7C
	15-	CA7A
U105- A3-1	3-	65536*
U704- A3-1	5-	65536*
	6-	65536*
	8-	CA7A
	9-	CA7C
	12-	0FL0*
	13-	0FL0*

LOOP: 8088 NO-OPS (Mode 2)

PCA: A3 Disc Controller Board

SETUP: Test board installed. Remove A3U606. E201 installed. Place E101, E102 and E103 to the 'T' position

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/+	Test Board CPU(U100)pin39
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 0001 ● ○ ○ ○ ○ ○

U403-	1-	H	U508-	1-	L
A3-2	2-	HC89	A3-1	2-	UUUU
	3-	UUUU		3-	UUUU
	4-	5555		4-	5555
	5-	2H70		5-	5555
	6-	HPP0		6-	CCCC
	7-	CCCC		7-	CCCC
	8-	7F7F		8-	7F7F
	9-	1293		9-	7F7F
	11-	L		11-	65537*
	12-	HAP7		12-	5H21
	13-	5H21		13-	5H21
	14-	0AFA		14-	0AFA
	15-	3C96		15-	0AFA
	16-	3827		16-	UPFH
	17-	UPFH		17-	UPFH
	18-	52F8		18-	52F8
	19-	755P		19-	52F8

U803-	3-	UUUU
A3-2	4-	5555
	7-	CCCC
	8-	7F7F
	13-	5H21
	14-	0AFA
	17-	UPFH
	18-	52F8

LOOP: 8088 NO-OPS (Mode 2)

PCA: A3 Disc Controller Board

SETUP: Test board installed. Remove A3U606. E201 installed. Place E101, E102 and E103 to the 'T' position

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/+	Test Board CPU(U100)pin39
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)
VHIGH = 0001		●○○○○○

Reinstall A3U606 into socket. Leave pins 1, 11-19, 20, and 22 out of socket. Tie pin 1 to +5 vdc. Tie pins 20 and 22 to ground. Pin 14 should be grounded. Measure the data output.

NOTE - Minimize bends on IC legs. Use only when Loop on Failure ROM test exists.

U606- A3-1	1-	H	15-	H9F1
	2-	HAP7	16-	FP56
	3-	52F8	17-	8F05
	4-	UPFH	18-	A8PF
	5-	0AFA	19-	04AP
	6-	5H21	20-	L
	7-	7F7F	21-	HPP0
	8-	CCCC	22-	L
	9-	5555	23-	1293
	10-	UUUU	24-	2H70
	11-	96U5	25-	HC89
	12-	6585	26-	3C96
	13-	FC25	27-	3827
	14-	L	28-	H

LOOP: A3 Interface Buffers (8088->800)

PCA: A3 Disc Controller Board

SETUP: Test board installed. Remove A3U606. E201 installed. Place E101, E102, & E102 to the T position. Unplug A3 board from system bus cable. Jump power & ground from A2 board to A3 board.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/+	Test Board CPU(U100)pin39
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 0001

● ○ ○ ○ ○ ○

Pull U408 pin 1 LOW to enable Latch

U408- A3-1		
	1-	L
	2-	HC89
	3-	HC89
	4-	2H70
	5-	2H70
	6-	HPP0
	7-	HPP0
	8-	1293
	9-	1293
	10-	L
	11-	H
	12-	HAP7
	13-	HAP7
	14-	3C96
	15-	3C96
	16-	3827
	17-	3827
	18-	755P
	19-	755P
	20-	H

Pull U308 pin 1 LOW to enable Latch

U308- A3-1		
	1-	L
	2-	UUUU
	3-	UUUU
	4-	5555
	5-	5555
	6-	CCCC
	7-	CCCC
	8-	7F7F
	9-	7F7F
	10-	L
	11-	H
	12-	5H21
	13-	5H21
	14-	0AFA
	15-	0AFA
	16-	UPFH
	17-	UPFH
	18-	52F8
	19-	52F8
	20-	H

Pull U608 pin 19 LOW to gate the device. Pull U608 pin 1 HIGH to enable the direction output.

U608- A3-1		
	1-	H
	2-	UUUU
	3-	5555
	4-	CCCC
	5-	7F7F
	6-	5H21
	7-	0AFA
	8-	UPFA
	9-	52F8
	10-	L
	11-	52F8
	12-	UPFH
	13-	0AFA
	14-	5H21
	15-	7F7F
	16-	CCCC
	17-	5555
	18-	UUUU
	19-	L
	20-	H

LOOP: A3 Interface Transceiver (800->8088)

PCA: A3 Disc Controller Board

SETUP: Move A1E314 to 'T' position. A2 board disconnected. Remove A1E815 to disable the beeper. Remove CPU (A3U505) on A3 board.

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A1U415-8 (A15)
QUAL			
CLOCK		-	A1U415-32 (~RD)
GROUND			A1U415-20 (GND)
VHIGH =	0001		O O O O O O

Pull A3U608 pin 19 LOW and
pull A3U608 pin 1 LOW

U608-	1-	L
A3-1	2-	UUUU
	3-	5555
	4-	CCCC
	5-	7F7F
	6-	5H21
	7-	0AFA
	8-	UPFH
	9-	52F8
	10-	L
	11-	52F8
	12-	UPFH
	13-	0AFA
	14-	5H21
	15-	7F7F
	16-	CCCC
	17-	5555
	18-	UUUU
	19-	L
	20-	H

LOOP: PIC (Test Passing)

PCA: A3 Disc Controller Board

SETUP: With A3 Diagnostics board installed. Remove A3 E2. Disc out of drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:
START/STOP		+/-	Test Board TP4 (S/S)
QUAL			
CLOCK		-	Test Board TP3 (LRD)
GROUND			Test Board TP2 (GND)

VHIGH = P196

●●○○○○

U306-	1-	643F
A3-1	2-	0004*
	3-	0005*
	4-	AP66
	5-	UHF0
	6-	4UFP
	7-	8P65
	8-	2354
	9-	F640
	10-	17U3
	11-	85C2
	12-	L
	13-	L
	14-	L
	15-	L
	16-	H
	17-	0001*
	18-	L
	19-	H
	20-	L
	21-	L
	22-	H
	23-	H
	24-	L
	25-	H
	26-	H
	27-	A5P0
	28-	H

LOOP: PIC 1 (Error 1)

PCA: A3 Disc Controller Board

SETUP: With A3 Diagnostics board installed.
Remove A3 E2 or Loop on Failure
Condition. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)
VHIGH = FP67		●●○○●○

U306- A3-1	1-	FA6H
	2-	0004*
	3-	0001*
	4-	003U
	5-	F0H2
	6-	FP59
	7-	0ACU
	8-	1CU4
	9-	PFU3
	10-	7H2H
	11-	8482
	12-	L
	13-	L
	14-	L
	15-	L
	16-	H
	17-	H
	18-	L
	19-	H
	20-	L
	21-	L
	22-	H
	23-	L
	24-	L
	25-	H
	26-	H
	27-	8483
	28-	H

LOOP: PIC 1 (Error 1.1)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed. Remove A3 E2 or Loop on Failure Condition. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)
VHIGH = 9515		●●○○●○

U306-	1-	CC88
A3-1	2-	0005*
	3-	0002*
	4-	003U
	5-	41P1
	6-	952C
	7-	0H11
	8-	P895
	9-	FU68
	10-	72FA
	11-	5037
	12-	L
	13-	L
	14-	L
	15-	L
	16-	H
	17-	0001*
	18-	L
	19-	H
	20-	L
	21-	L
	22-	H
	23-	L
	24-	L
	25-	H
	26-	H
	27-	5036
	28-	H

LOOP: PIC (Error 2)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed. Remove A3 E2 or Loop on Failure Condition. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 2538

●●○○○●

U306-	1-	93HH
A3-1	2-	0005*
	3-	0004*
	4-	U1A7
	5-	4H3P
	6-	H49F
	7-	U65U
	8-	5UF6
	9-	88U6
	10-	H90C
	11-	55P5
	12-	L
	13-	L
	14-	L
	15-	L
	16-	H
	17-	0001*
	18-	L
	19-	H
	20-	L
	21-	High or low, must be opposite of each other
	22-	
	23-	L
	24-	L
	25-	H
	26-	H
	27-	55P4
	28-	H

LOOP: DMAC (Test Passing)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/-	Test Board TP4 (S/S)
QUAL			
CLOCK		..	Test Board TP3 (LRD)
GROUND			Test Board TP2 (GND)
VHIGH =	479P		●●OOOO

U400- A3-2	1-	0003*		30-	46C6	U403- A3-2	1-	0001*
	2-	0014*		31-	H		2-	47C6
	3-	5358*		32-	FUF0		3-	46C6
	4-	0268*		33-	H819		4-	FPCP
	5-	H		34-	8A43		5-	FHF0
	6-	H		35-	8H9U		6-	565F
	7-	0000		36-	479P		7-	AA83
	8-	0000		37-	49HC		8-	563H
	9-	0000		38-	796H		9-	994A
	10-	AAC7		39-	7HP8		10-	L
	11-	FFHP		40-	41PP		11-	0514*
	12-	479P					12-	13P1
	13-	L					13-	AA71
	14-	H	U706- A3-1	1-	0001*		14-	754U
	15-	H		2-	0001*		15-	994A
	16-	L					16-	994A
	17-	L					17-	1A0P
	18-	L	U203- A3-1	11-	0284*		18-	1897
	19-	L		12-	0283*		19-	8AAC
	20-	L		13-	0001*		20-	H
	21-	1897						
	22-	1A0P						
	23-	754U	U704- A3-1	8-	0284*			
	24-	H		9-	0284*			
	25-	H						
	26-	AA71						
	27-	563H						
	28-	AA83						
	29-	FPCP						

LOOP: DMAC (Error)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1. Disc out of Drive.

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK		Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 16FF

●●○○○○

U400-	1-	0003*		28-	PF80
A3-2	2-	0014*		29-	H115
	3-	1301*		30-	9FA0
	4-	0270*		31-	H
	5-	H		32-	5306
	6-	H		33-	0UUA
	7-	0000		34-	58P1
	8-	0000		35-	U9U4
	9-	0000		36-	16FF
	10-	C7P6		37-	3476
	11-	3246		38-	8FUC
	12-	16FF		39-	7C2C
	13-	L		40-	91U7
	14-	H			
	15-	H			
	16-	L	U706-	1-	0001*
	17-	L	A3-1	2-	0001*
	18-	L			
	19-	L			
	20-	L	U203-	11-	0032*
	21-	U0HP	A3-1	12-	0031*
	22-	F62H		13-	0001*
	23-	7100			
	24-	H			
	25-	H	U704-	8-	0032*
	26-	3554	A3-2	9-	0033*
	27-	25C2			

LOOP: FDC (Test Passing)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1 & E2. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE:	Norm	EDGE:	NODE:
START/STOP		+/-	Test Board TP4 (S/S)
QUAL			
CLOCK		-	Test Board TP3 (LRD)
GROUND			Test Board TP2 (GND)
VHIGH =	90A3		●●○○●●

U600- A3-2

1-	UN
2-	0008*
3-	0007*
4-	0005*
5-	22U8
6-	993P
7-	CHCP
8-	U7H8
9-	1FC8
10-	677U
11-	P526
12-	3C30
13-	3931
14-	1C70
15-	0002*
16-	0002*
17-	UU92
18-	H
19-	C749
20-	L
21-	H
22-	UU92
23-	UN
24-	2 Mhz
25-	UU92
26-	0FLO*
27-	H
28-	0001*
29-	0006*
30-	L
31-	0005*
32-	L
33-	H
34-	UN
35-	H
36-	6U31
37-	L
38-	L
39-	0002*
40-	0001*

U803- A3-2

2-	6U31
5-	0002*
6-	L
9-	L
12-	UU92
15-	UU92
16-	C749
19-	UU92

U703- A3-2

3-	0002*
5-	0002*
6-	H
7-	H
9-	0005/0006*
12-	0001*
14-	L
18-	UU92

U603- A3-2

3-	6U31
5-	H
7-	6U31
8-	H
9-	UN
11-	UN
12-	H
13-	6U31
15-	H
17-	6U31

LOOP: FDC (Failure 1)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1 & E2. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = 4P5U

●●○○●●

U600- A3-2			
1-	UN	30-	L
2-	0007*	31-	UN
3-	0004*	32-	L
4-	0003*	33-	H
5-	0HAC	34-	H
6-	5AHC	35-	H
7-	11C3	36-	83C6
8-	7828	37-	L
9-	716A	38-	L
10-	4P37	39-	L
11-	7325	40-	L
12-	8C58		
13-	U1P6		
14-	74P4		
15-	0010*		
16-	0000*		
17-	FHP9		
18-	H		
19-	8F07		
20-	L		
21-	H		
22-	FHP9		
23-	UN		
24-	2 Mhz		
25-	FHP9		
26-	0FL0*		
27-	H		
28-	L		
29-	UN		

U803- A3-2	
2-	83C6
5-	0001*
6-	L
9-	L
12-	FHP9
15-	FHP9
16-	8F07
19-	FHP9

U703- A3-2	
3-	0010*
5-	H
6-	H
7-	H
9-	UN
12-	H
14-	L
18-	FHP9

U603- A3-2	
3-	83C6
5-	H
7-	83C6
8-	H
9-	H
11-	83C6
12-	H
13-	83C6
15-	H
17-	83C6

LOOP: FDC (Failure 2)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1 & E2. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/-	Test Board TP4 (S/S)
QUAL			
CLOCK		-	Test Board TP3 (LRD)
GROUND			Test Board TP2 (GND)
VHIGH =	HF8H		●●○○●●

U600- A3-1	1-	UN
	2-	0008*
	3-	0007*
	4-	0005*
	5-	CU67
	6-	PPP1
	7-	76HA
	8-	8FC3
	9-	CHAH
	10-	0754
	11-	78AF
	12-	9PFH
	13-	8U36
	14-	4110
	15-	0001*
	16-	0002*
	17-	851C
	18-	H
	19-	42AH
	20-	H
	21-	H
	22-	851C
	23-	UN
	24-	2 Mhz
	25-	851C
	26-	0FL0*
	27-	H
	28-	0001*
	29-	UN
	30-	L
	31-	UN
	32-	L
	33-	H
	34-	L
	35-	H
	36-	5996
	37-	L
	38-	L
	39-	0002*
	40-	0001*

U803- A3-2	2-	5996
	5-	0001/0002*
	6-	L
	9-	L
	12-	851C
	15-	851C
	16-	42AH
	19-	851C

U703- A3-1	3-	0001*
	5-	0002*
	6-	H
	7-	H
	9-	0004/0005/0006*
	12-	0001*
	14-	L
	18-	851C

U603- A3-2	3-	5996
	5-	H
	7-	5996
	8-	H
	9-	L
	11-	H
	12-	H
	13-	5996
	15-	H
	17-	5996

LOOP: FDC (Failure 3)

PCA: A3 Disc Controller Board

SETUP: A3 Diagnostics board installed.
Remove A3 E1 & E2. Disc out of Drive.

* - Totalized Signature (+/- 1 count)
- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	Test Board TP4 (S/S)
QUAL		
CLOCK	-	Test Board TP3 (LRD)
GROUND		Test Board TP2 (GND)

VHIGH = APOF

●●○○●●

U600- A3-2	1-	UN
	2-	0008*
	3-	0014*
	4-	0012*
	5-	U761
	6-	36P9
	7-	P9A2
	8-	715F
	9-	C4C6
	10-	HCUP
	11-	UA7U
	12-	8711
	13-	8A75
	14-	5PUH
	15-	L
	16-	L
	17-	1A55
	18-	H
	19-	L
	20-	L
	21-	H
	22-	1A55
	23-	UN
	24-	2 Mhz
	25-	1A55
	26-	OFLO
	27-	H
	28-	L
	29-	UN
	30-	L
	31-	UN
	32-	L
	33-	H
	34-	C459
	35-	H
	36-	C459
	37-	L
	38-	L
	39-	L
	40-	L

U803- A3-2	2-	C459
	5-	0001
	6-	L
	9-	L
	12-	1A55
	15-	1A55
	16-	XXXX
	19-	1A55

U703- A3-2	3-	H
	5-	H
	6-	H
	7-	H
	9-	UN
	12-	H
	14-	L
	18-	1A55

U603- A3-2	3-	C459
	5-	H
	7-	C459
	8-	H
	9-	C459
	11-	C459
	12-	H
	13-	C459
	15-	H
	17-	C459

8-48. INSTRUMENT OPERATION VERIFICATION

After performing a repair on an HP 4951C complete the following test procedure. This test turns lines on and off as well as simulates various triggers. Any protocol may be used, however HDLC was selected for this procedure.

NOTE

Complete the proper setup when using a different protocol.

Two HP 4951Cs must be used for this test. Use the same set up for both HP 4951Cs. The HP 4951C that was repaired is the Unit Under Test and the other one is the Standard or Control Unit. After performing the test procedure, reverse the roles of the instruments and perform the test again to verify that all operations are functioning correctly. Operate the Unit Under Test in the monitor line mode.

Set Up:

Protocol	HDLC
Ext Adrr	OFF
Ext Ctrl	OFF
Code	ASCII8
DTE Clock	DCE
Bits/Sec	19200
Disp Mode	2 LINE

Procedure:

Enter the following program for the standard or control HP 4951C.

	Simulate	DCE
Block 1		
	Set Lead	CTS ON
	and then	
	Send	THIS IS A FINAL TEST
	and then	
	Start Timer	1
	and then	
	Increment Counter	1
	and then	
	Wait	100
	and then	
	Stop Timer	1
	and then	
	Set lead	CTS OFF
Block 2		
	Set lead	DSR ON
	and then	

	Send	SO FAR I'M GOOD
	and then	
	Start Timer	2
	and then	
	Increment counter	2
	and then	
	Wait	200
	and then	
	Set lead	DSR OFF
Block 3		
	Set lead	CD ON
	and then	
	Send	TEST COMPLETE AND I PASSED!
	and then	
	Start timer	3
	and then	
	Increment counter	3
	and then	
	Wait	300
	and then	
	Stop timer	3
	and then	
	Set lead	CD OFF
	If counter	3>3
	then goto block	5
Block 4		
	Goto block	1
	Goto block 1 or	STOP TEST

NOTE

Block 5 can cause the test to run continuously or stop the test after 3 passes.

Set Up:

Protocol	HDLC
Ext Adrr	OFF
Ext Ctrl	OFF
Code	ASCII8
DTE Clock	DCE
Bits/Sec	19200
Disp Line	2 LINE

Procedure:

Enter the following monitor program for the Unit to be tested.

Block 1		
	When lead	CTS GOES ON
	Then goto block	2
Block 2		
	Start timer	1
	and then	
	Increment counter	1
	When lead	CTS GOES OFF
	Then goto block	3
Block 3		
	Stop timer	1
	When lead	DSR GOES ON
	Then goto block	4
Block 4		
	Start timer	2
	and then	
	Increment counter	2
	When lead	DSR GOES OFF
	Then goto block	5
Block 5		
	Stop timer	2
	When lead	CD GOES ON
	Then goto block	6
Block 6		
	Start timer	3
	and then	
	Increment counter	3
	When lead	CD GOES OFF
	Then goto block	7
Block 7		
	If counter	3>3
	Then goto block	9
Block 8		
	Goto block	1
Block 9		
	Got block 1 or	STOP TESTS

NOTE

Block 9 can cause the test to run continuously or stop the test after 3 passes.

Test Procedure:

1. Press <Exam Data>.

2. The appropriate messages from the programs should appear on the CRT.

3. Press <Timer> and <Cntr>.

   Compare the numbers for the standard and the unit under test. They should be the same.

8-49. DISC READ/WRITE TEST

After performing a repair on an HP 4951C, complete the following test procedure. This test assures the read and write functions of the HP 4951C are working properly.

Set Up: To create a data file for this test start with a blank 92192A flexible disc that has been formatted. If the disc has not been formatted, you can do this by going into the 'Mass Store Menu'. Execute the following program by first going to the Set Up Menu and changing the appropriate fields to the Following:

Set Up Menu:	Default Configuration
Bits/Sec:	19200
Disp Mode:	DCE

Now enter the following program in the Simulate Menu:

Simulate: DCE

Block 1
  Start Display
    And Then
  Start Disc

Block 2
  Send "Disc Test"
    And Then
  Goto Block 2

Now press <Run Menu> and <Simulate>. You will be asked for a file name to give to the data, enter "DTEST", and then press <Execute>. The test will now begin executing. Notice that information is now being stored to the disc. This test will run for about 2.5 minutes. Once the test is complete the message "DISC FULL"should be displayed. If no errors have been reported, the 'write' phase of the test has been completed. The data file has now been created and data has been written to the entire area of the disc.

Procedure: To read the data that has been written to the flexible disc do the following procedure:

Using the disc that the data file has been created on, go to the Mass Store Menu and load the "Menu & Data" file. Exit the Mass Store Menu and go to the Examine Data Menu (Note: The typical size of the file should be 2449 sectors as indicated in the Mass Store Directory).

Using the <More> key find the <Spec Block> key and press. The current block should be #16. Manually enter 999. After you press the last '9' the display should default to '308'. This is the maximum block number allowed by the HP 4951C. Press <Return>. The message "Searching" should appear and you should see occasional activity of the disc drive as the system searches through the file to find block #308.

When this test is complete, the message "End of Disc File: Last Part of Disc Data in Buffer" should appear. If no errors have occurred, the Disc Drive and Disc Controller Board are writing and reading data correctly.

NOTE

If this test is to be repeated, the data file must be deleted and the disc must be packed. Otherwise the HP 4951C will reject the disc as having the same file name or being full of data.

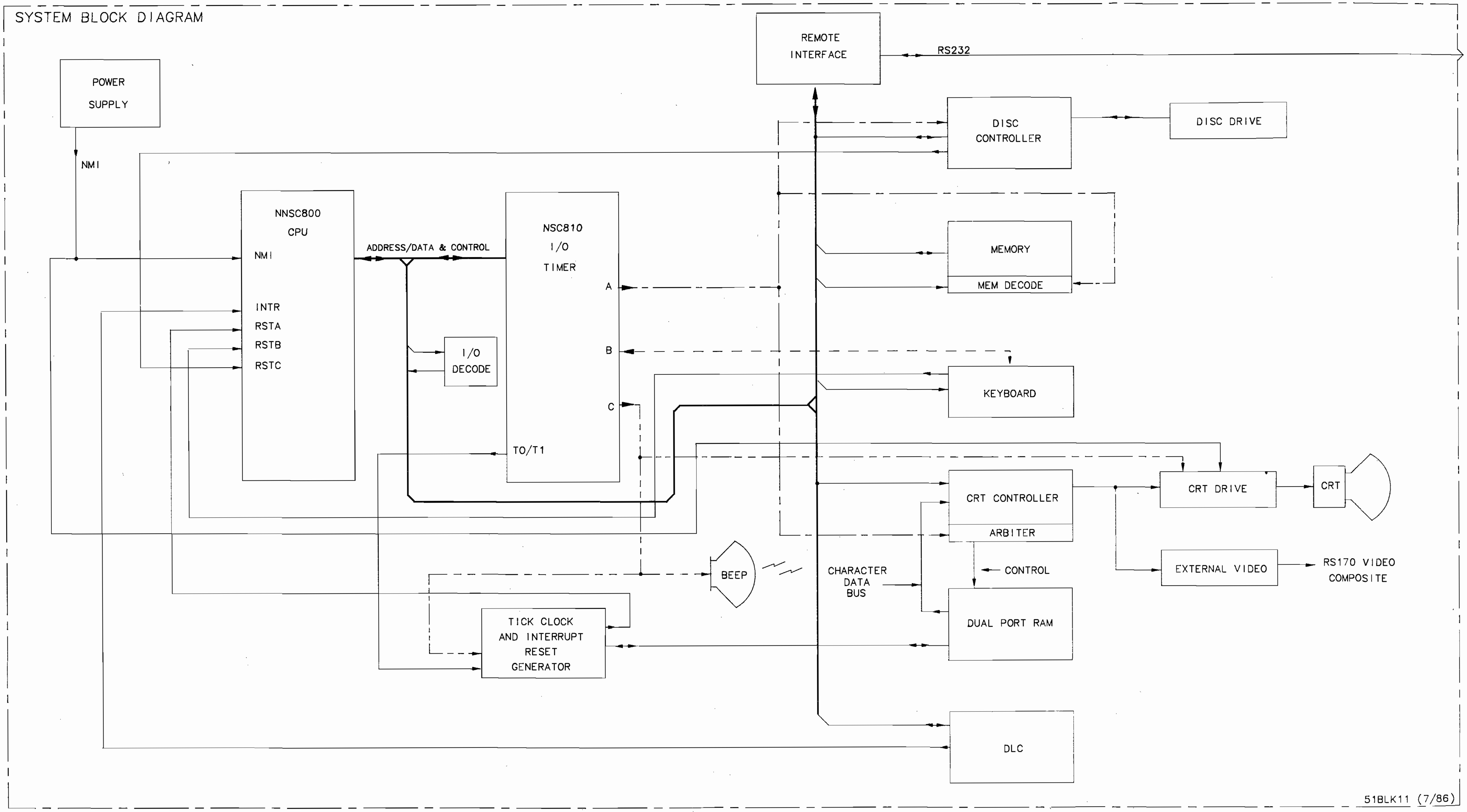


Figure 8-7. System Block Diagram

A1	1	A8
A1	2	A9
A1	3	+12
A1	4	GND
A1	5	+12
A1	6	A10
A1	7	-12
A1	8	A11
A1	9	-12
A1	10	+5
A1	11	GND
A1	12	A12
A1	13	A13
A1	14	A14
A1	15	A15
A1	16	GND
A1	17	+5
A3	18	BREQ
A1	19	~BGRANT
	20	UNDEFINED
A1	21	~WR
A1	22	GND
A1	23	ALE
A2	24	~M4
	25	M16
A1	26	RE
A1	27	+5
A1	28	GND
A1	29	~RD
A1	30	GND
A1	31	UNDEFINED
A1	32	GND
A1	33	+5
A1	34	AD7
A1	35	AD6
A1	36	GND
A1	37	AD5
A1	38	AD4
A1	39	GND
A1	40	+5
A1	41	AD3
A1	42	AD2
A1	43	GND
A1	44	AD1
A1	45	AD0
A1	46	+5
A2	47	VCCF (BATT)
A1	48	IO/M
A1	49	~NMI
A3	50	A3->A1 ~FLP_INT
A1	51	A1->A3 ~INTFLP
A1	52	GND
A1	53	PA6
A1	54	PA4
A1	55	PA2
A1	56	PA1
A1	57	GND
A1	58	PA0
A1	59	~REM_EN
A2	60	~IRQ

↑ THESE TELL FROM WHICH BOARD THE SIGNAL ORIGINATES

J1 Connector - Line Identifiers

	4952A	4951A,B,C	
1	RC	RTXCB	<--
2	~DTRB		-->
3	RTS	PD0 (CTSB)	<--
4	GND		-->
5	CD	DCDB (PD5)	<--
6	~RTSA		-->
7	TXCLK	TRXCA	-->
8	+12V		-->
9	-12		-->
10	+5		-->
11	~30HZ		-->
12	~2HZ		-->
13	ID2	PD4	<--
14	GND		-->
15	ID0	PD6	<--
16	ID1	PD7	<--
17	~RTXCA	TXCLK	-->
18	MONITOR		-->
19	DTESIM		-->
20	RD_DCE	RBB	<--
21	RD_DTE	RAB	<--
22	TD		-->
23	DTE_TC	TXDTE	<--
24	DCE_TC	TXDCE	<--
25	CTS	CTSA	<--

26	~DTRA		-->
27	+12V		-->
28	-12V		-->
29	+5V		-->
30	30HZ		-->
31	2HZ		-->
32	DTR	PD2	<--
33	DSR	PD3	<--
34	KEYPLUG		
35	RTS	PD0 (CTSB)	<--
36	GND		-->
37	DCESIM		-->

--> = FROM 4951 TO THE POD

<-- = FROM POD TO THE 4951

J2 Connector - Line Identifiers

Figure 8-8. J1 & J2 Connector Signals

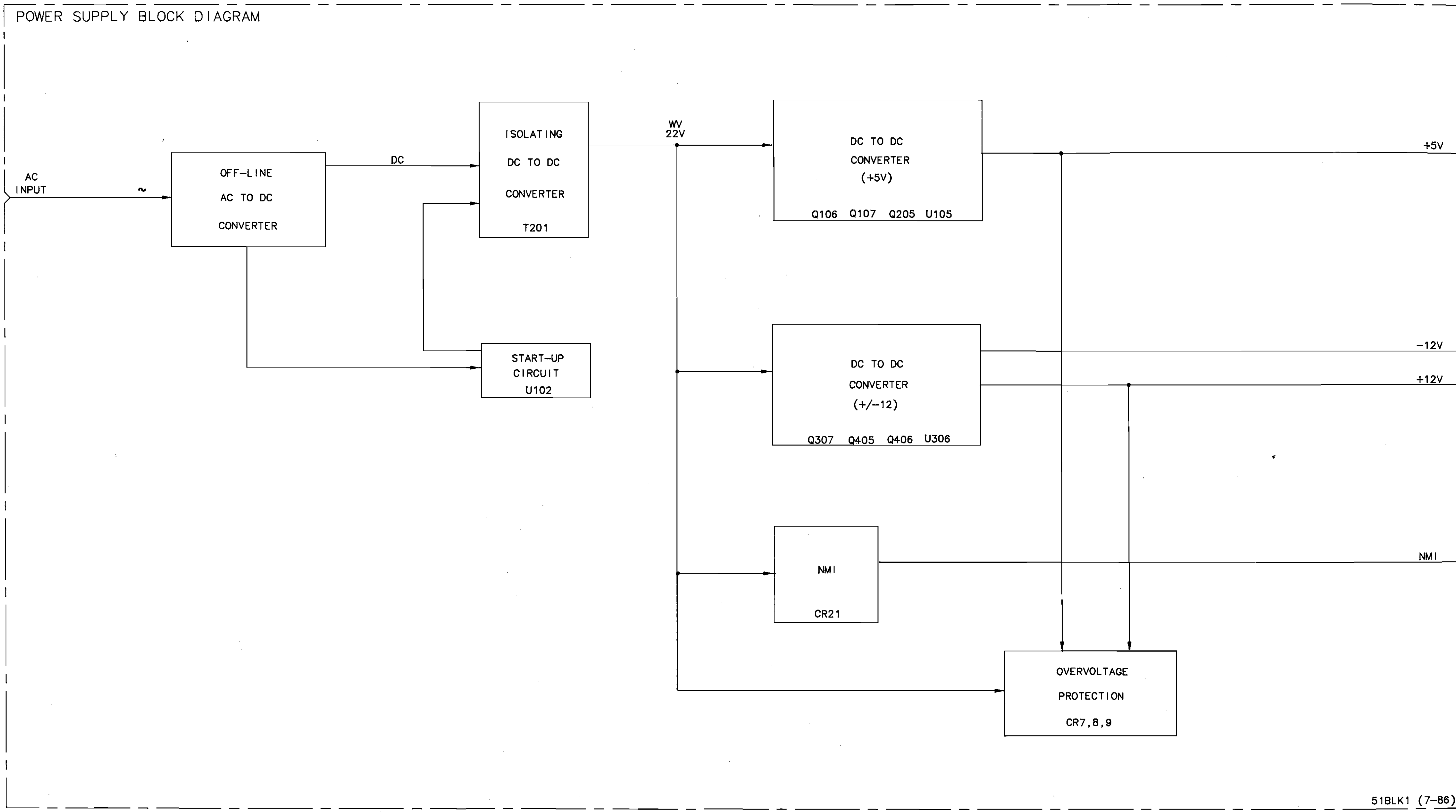


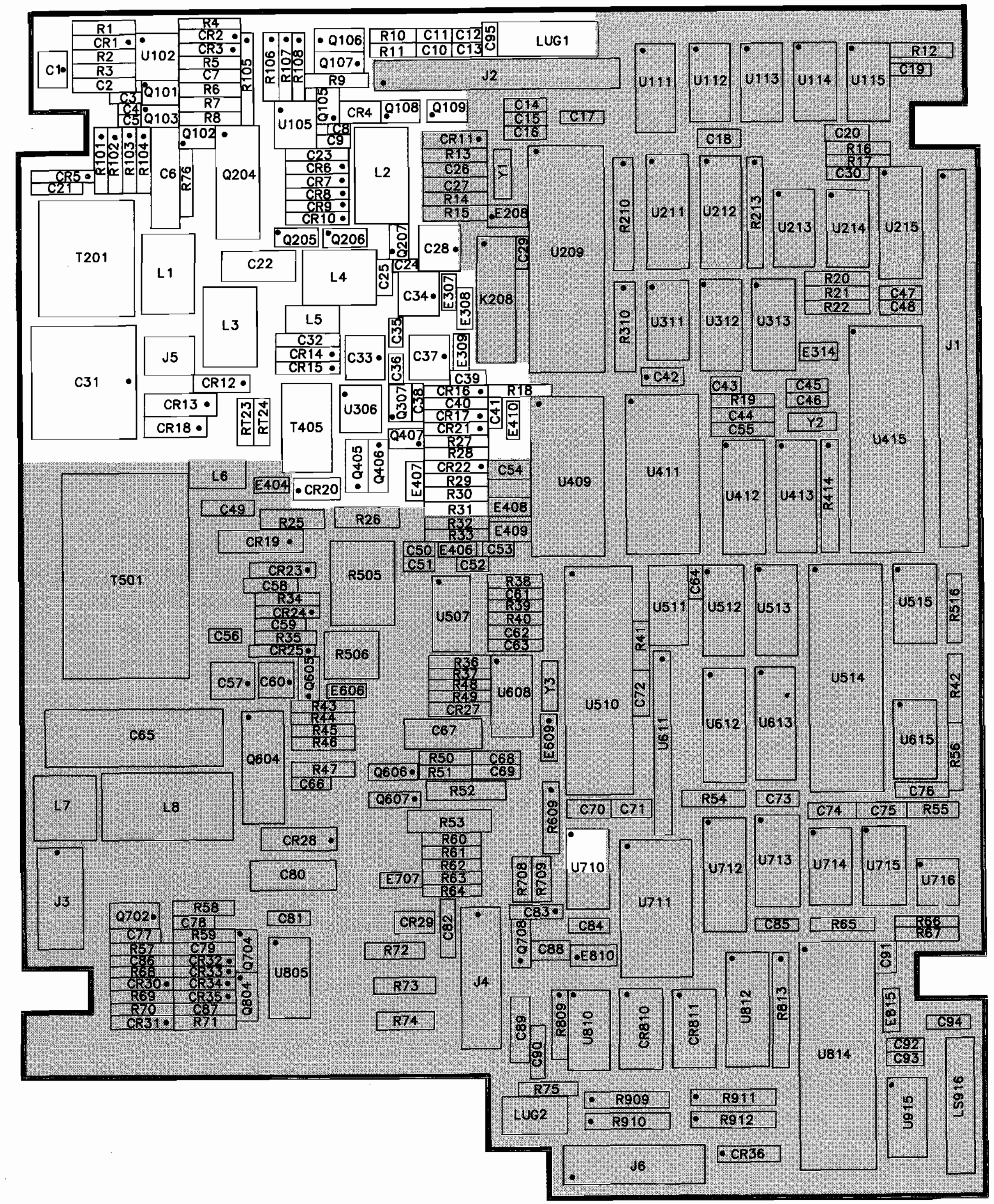
Figure 8-9. A1-1 Power Supply Block Diagram

Power & Ground

Part #	+5	Gnd
U102	9	18
U105	6	4
U306	6	4
U710	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3



04951-60701
51COMLC4 (7-86)

Figure 8-10. A1-1 Power Supply Component Locator

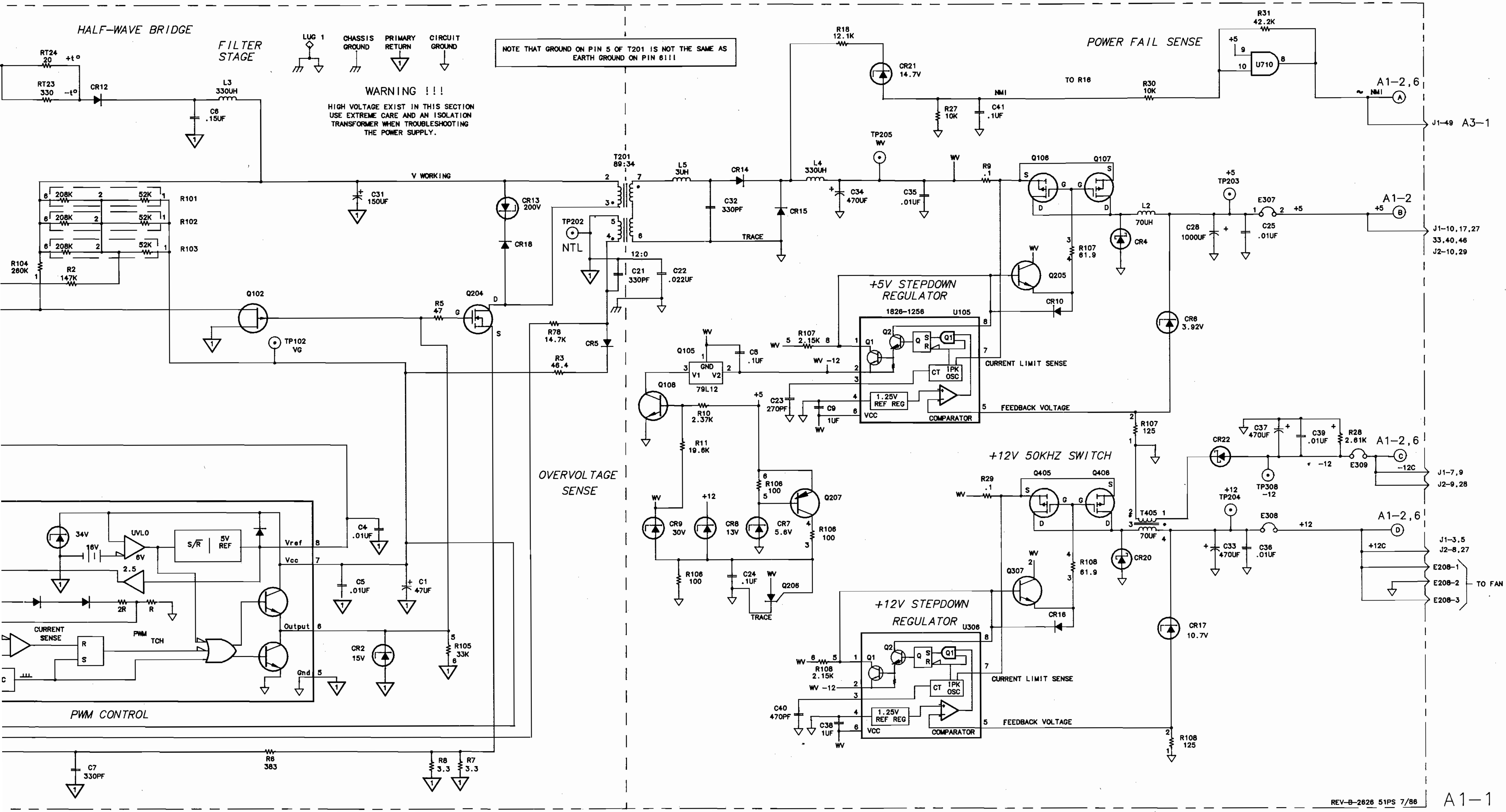
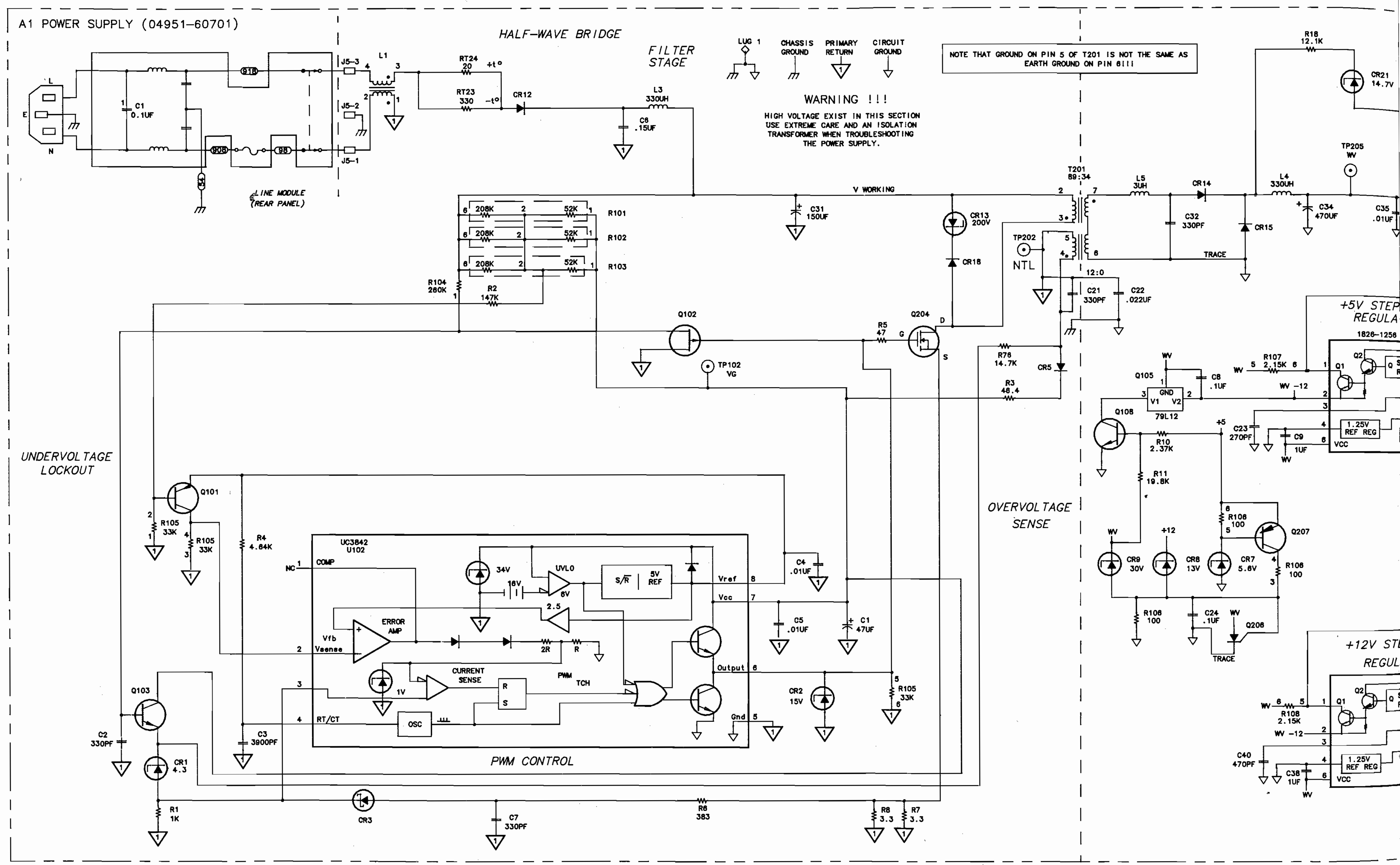


Figure 8-11. A1-1 Power Supply Schematic Diagram


A1 POWER SUPPLY (04951-60701)
HALF-WAVE BRIDGE
FILTER STAGE
LINE MODULE (REAR PANEL)
LUG 1
CHASSIS GROUND
PRIMARY RETURN
CIRCUIT GROUND
NOTE THAT GROUND ON PIN 5 OF T201 IS NOT THE SAME AS EARTH GROUND ON PIN 6!!!
WARNING !!!
HIGH VOLTAGE EXIST IN THIS SECTION USE EXTREME CARE AND AN ISOLATION TRANSFORMER WHEN TROUBLESHOOTING THE POWER SUPPLY.
V WORKING
UNDERVOLTAGE LOCKOUT
OVERVOLTAGE SENSE
PWM CONTROL
UC3842 U102
ERROR AMP
CURRENT SENSE
UVLO
5V REF
OSC
+5V STEP REGULA
+12V ST REGUL
1.25V REF REG
TRACE
NTL

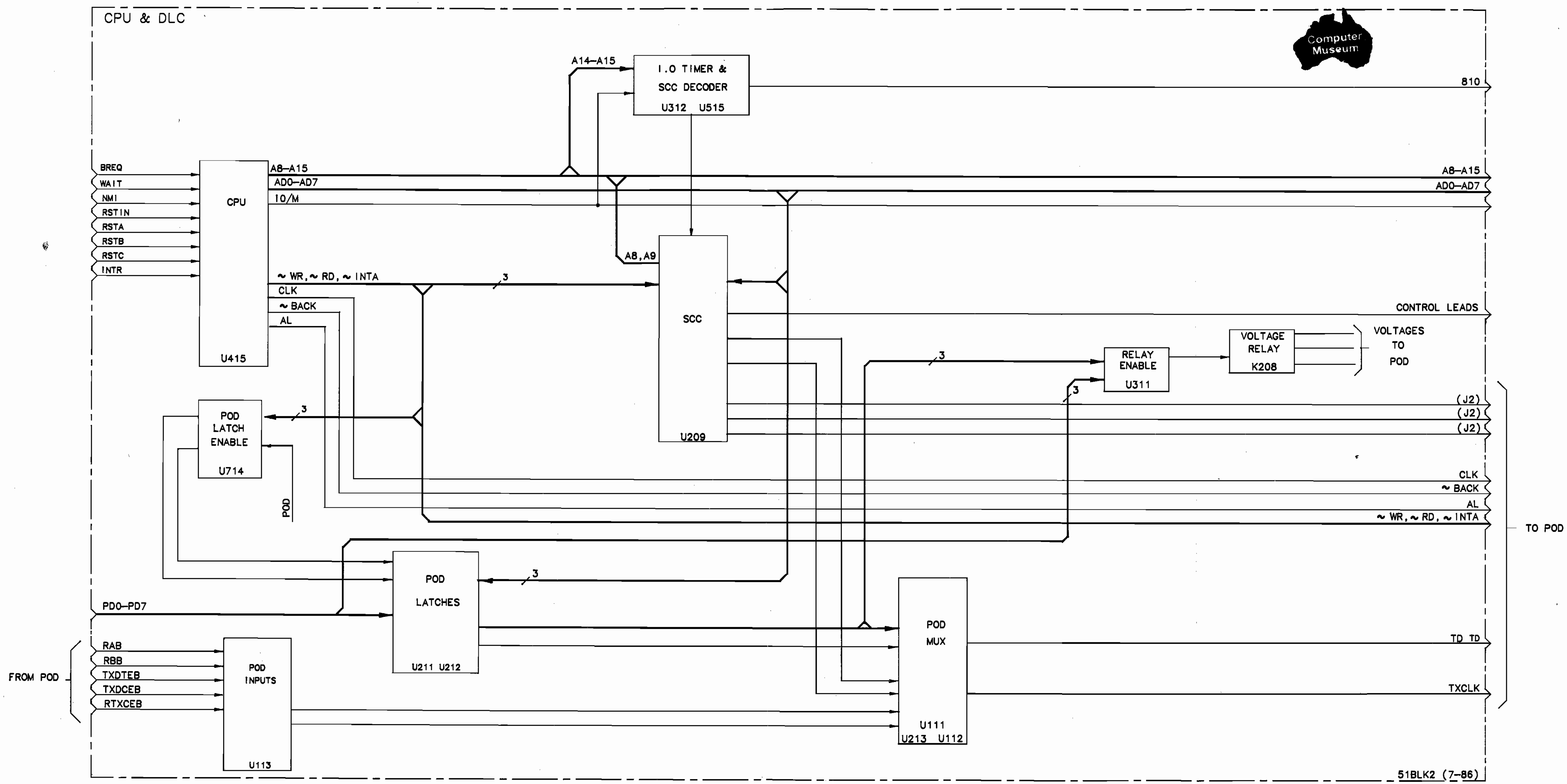


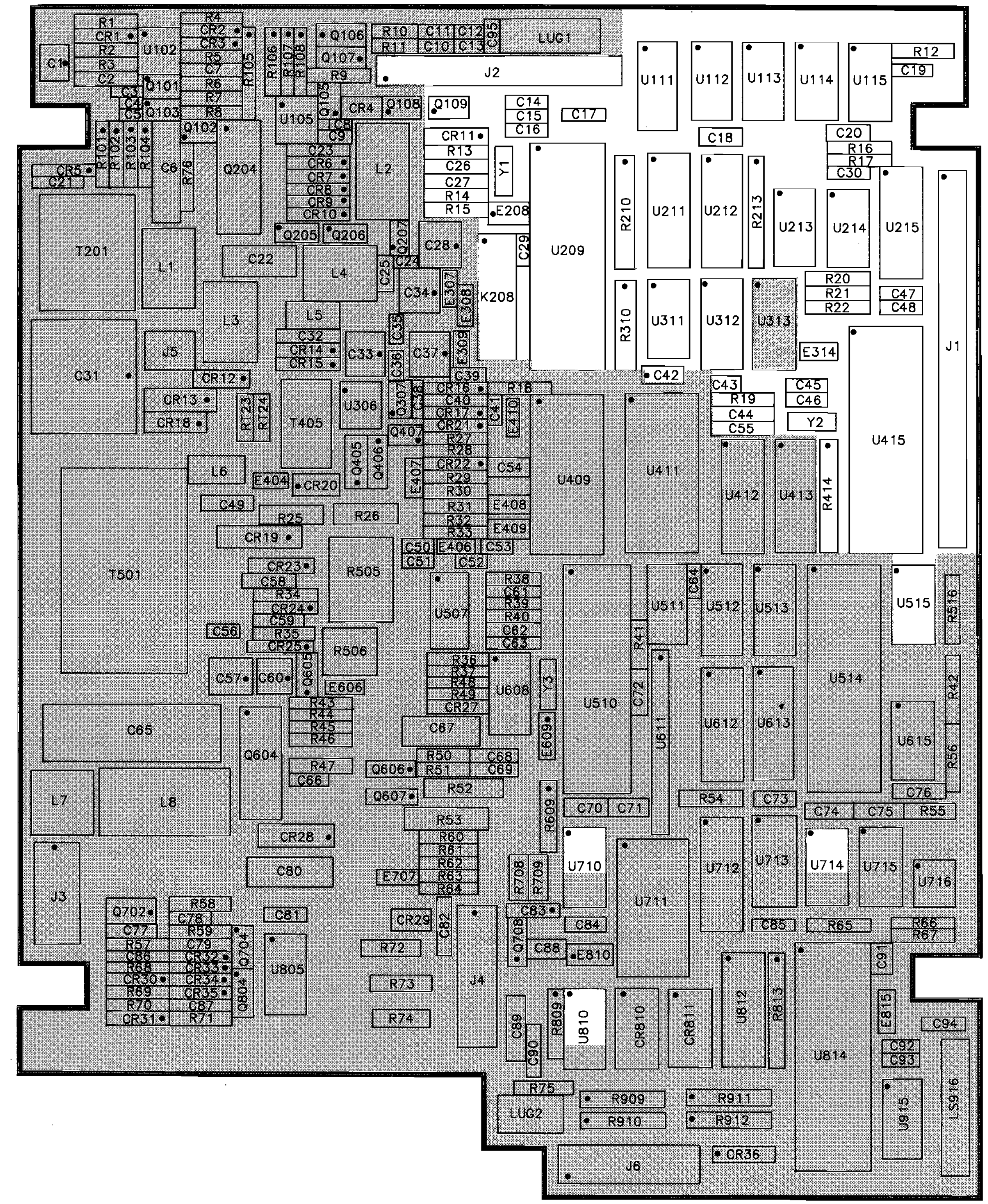
Figure 8-12. A1-2 CPU and DLC Block Diagram

Power & Ground

Part #	+5	Gnd
U111	16	8
U112	20	10
U113	14	7
U115	14	7
U209	9	31
U211	20	10
U212	20	10
U213	14	7
U214	14	7
U215	20	10
U311	14	7
U312	16	8
U415	40	20
U511	14	7
U515	14	7
U710	14	7
U714	14	7
U810	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3



04951-60701
51COMLC4 (7-86)

Figure 8-13. A1-2 CPU and DLC Component Locator

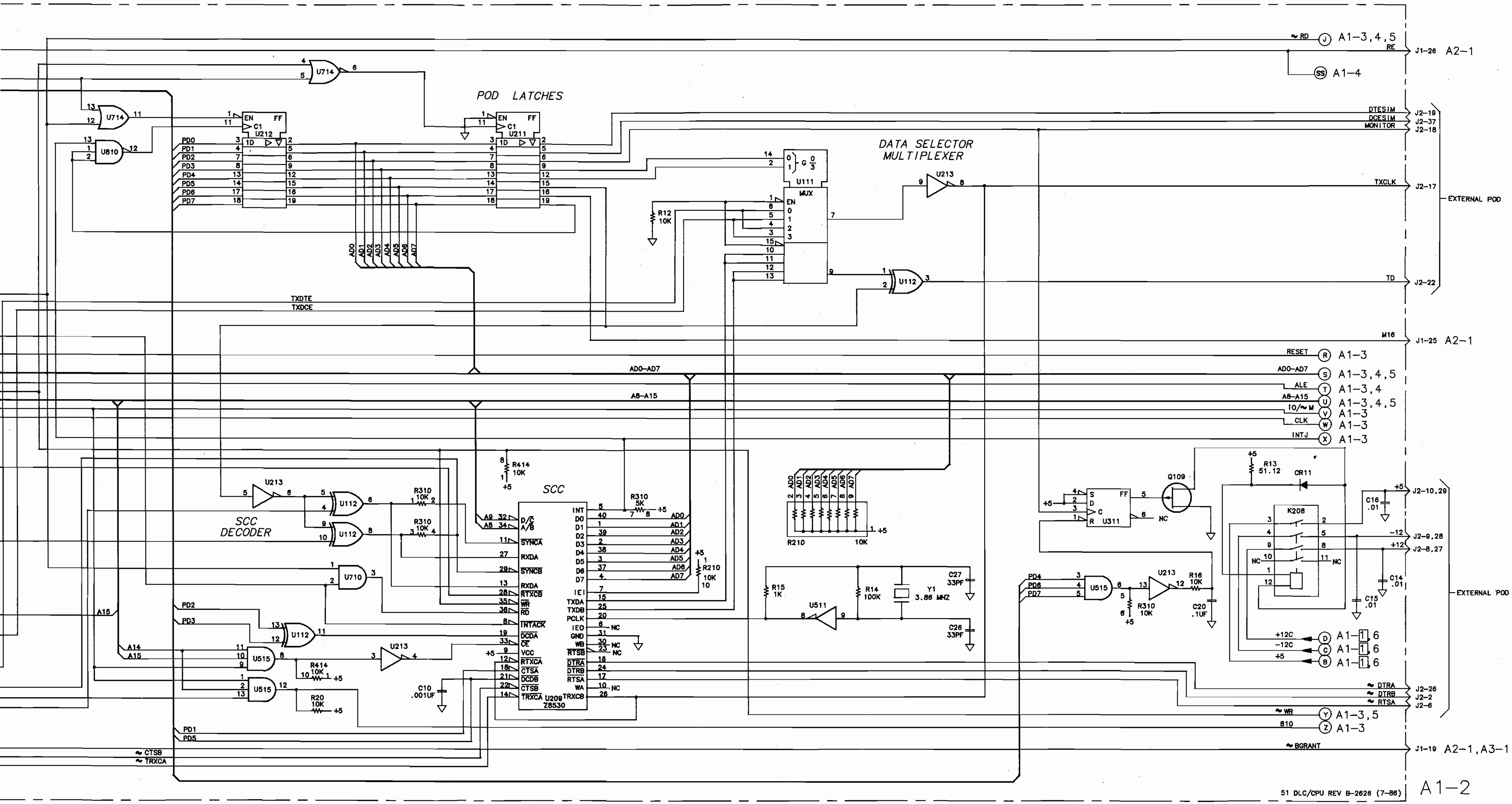
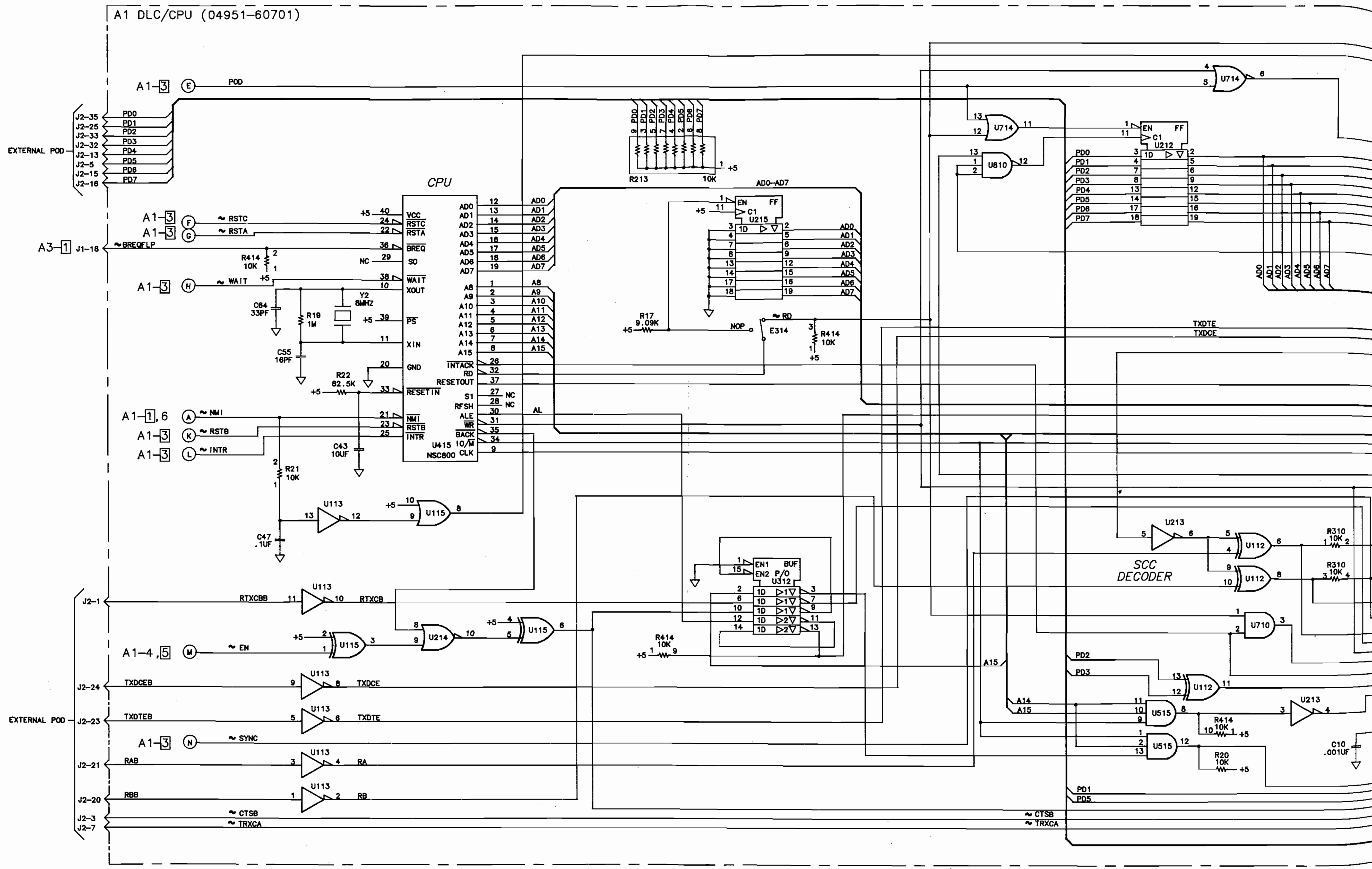


Figure 8-14. A1-2 CPU and DLC Schematic Diagram


A1 DLC/CPU (04951-60701)
CPU
U415
NSC800
EXTERNAL POD
SCC
DECODER
AD0-AD7

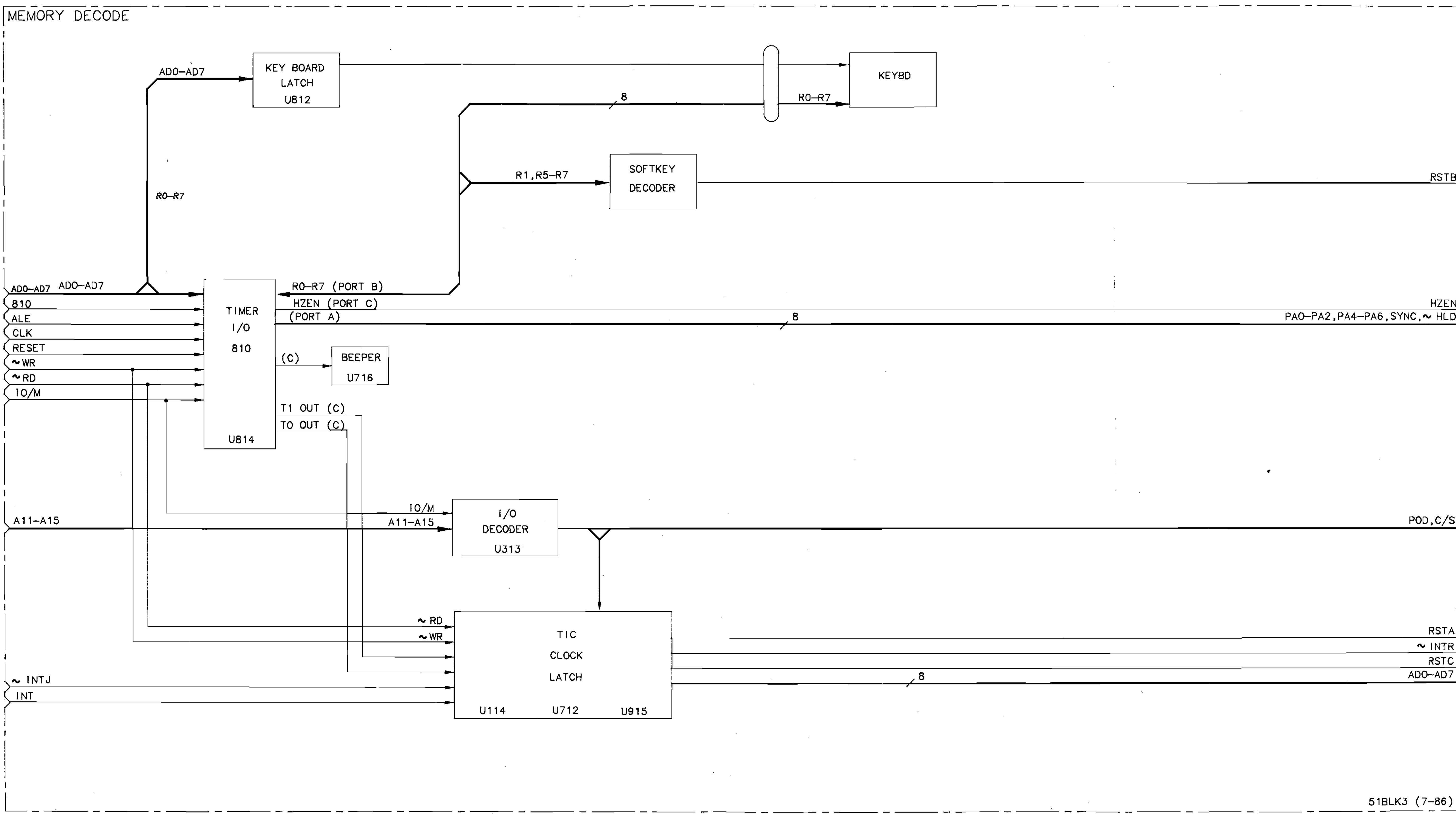


Figure 8-15. A1-3 Memory Decode Block Diagram

Power & Ground

Part #	+5	Gnd
U114	14	7
U213	16	8
U214	14	7
U311	14	7
U312	16	8
U313	16	8
U511	14	7
U615	14	7
U712	20	10
U714	14	7
U715	14	7
U716	8	1
U812	20	10
U814	40	20
U915	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3

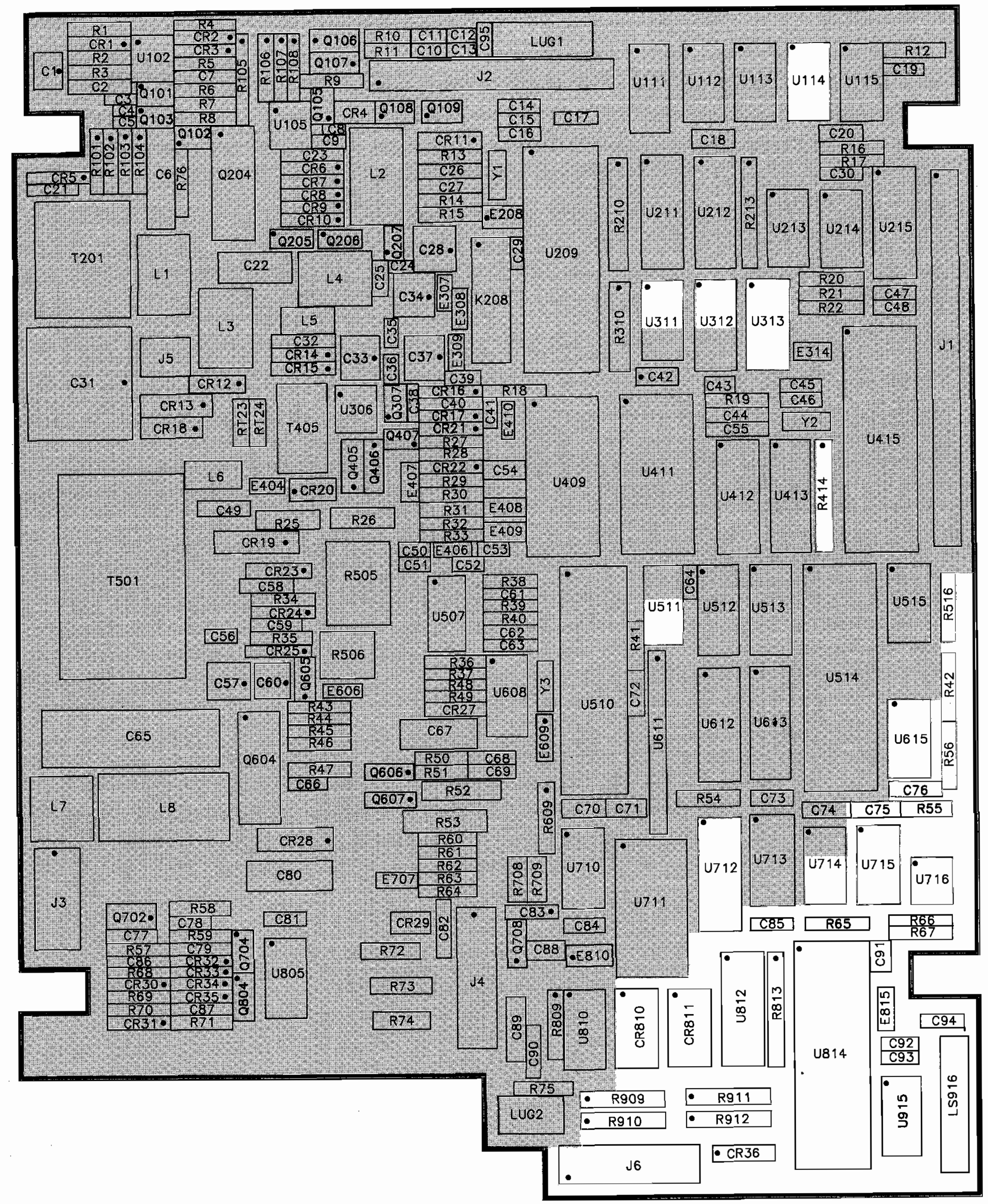
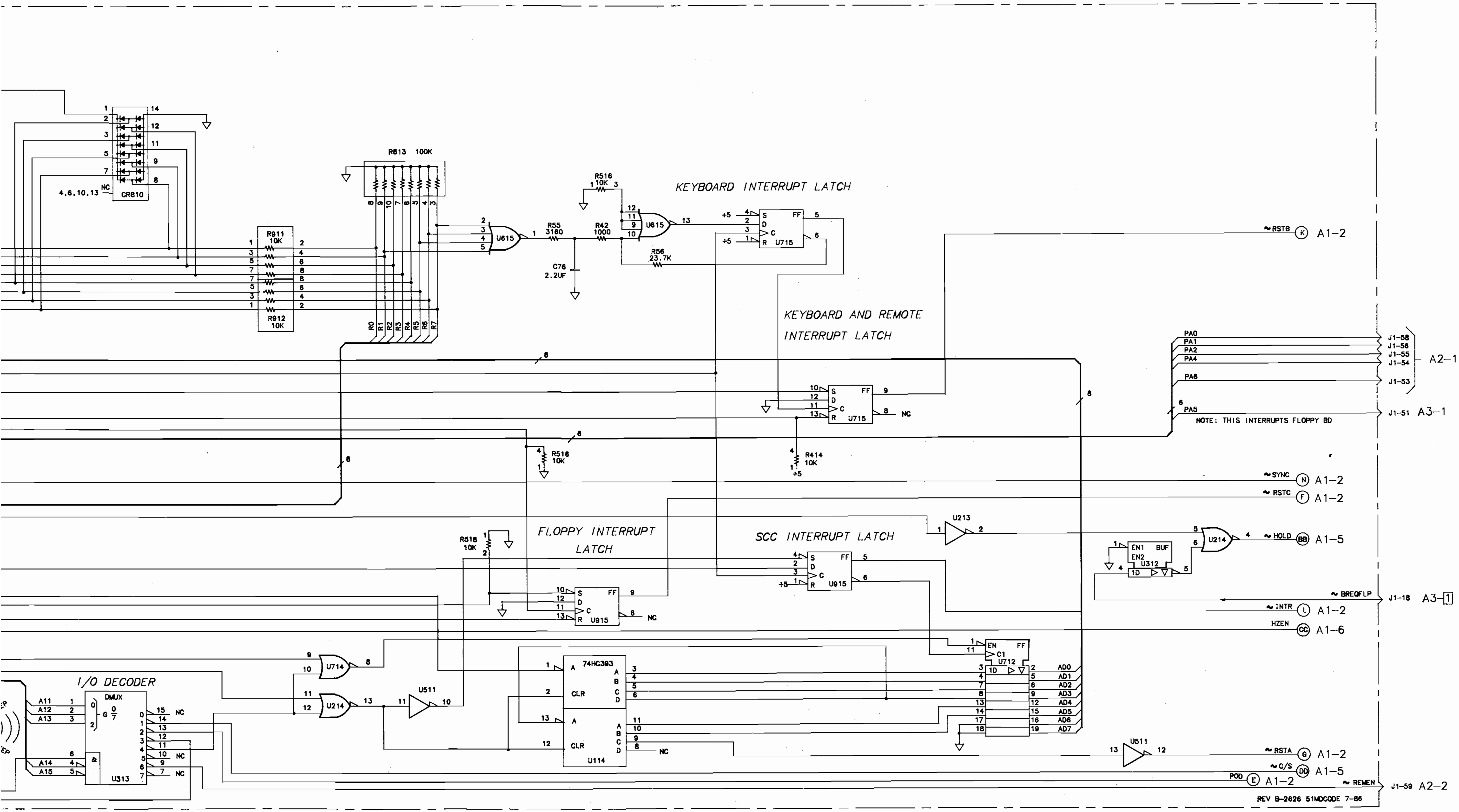
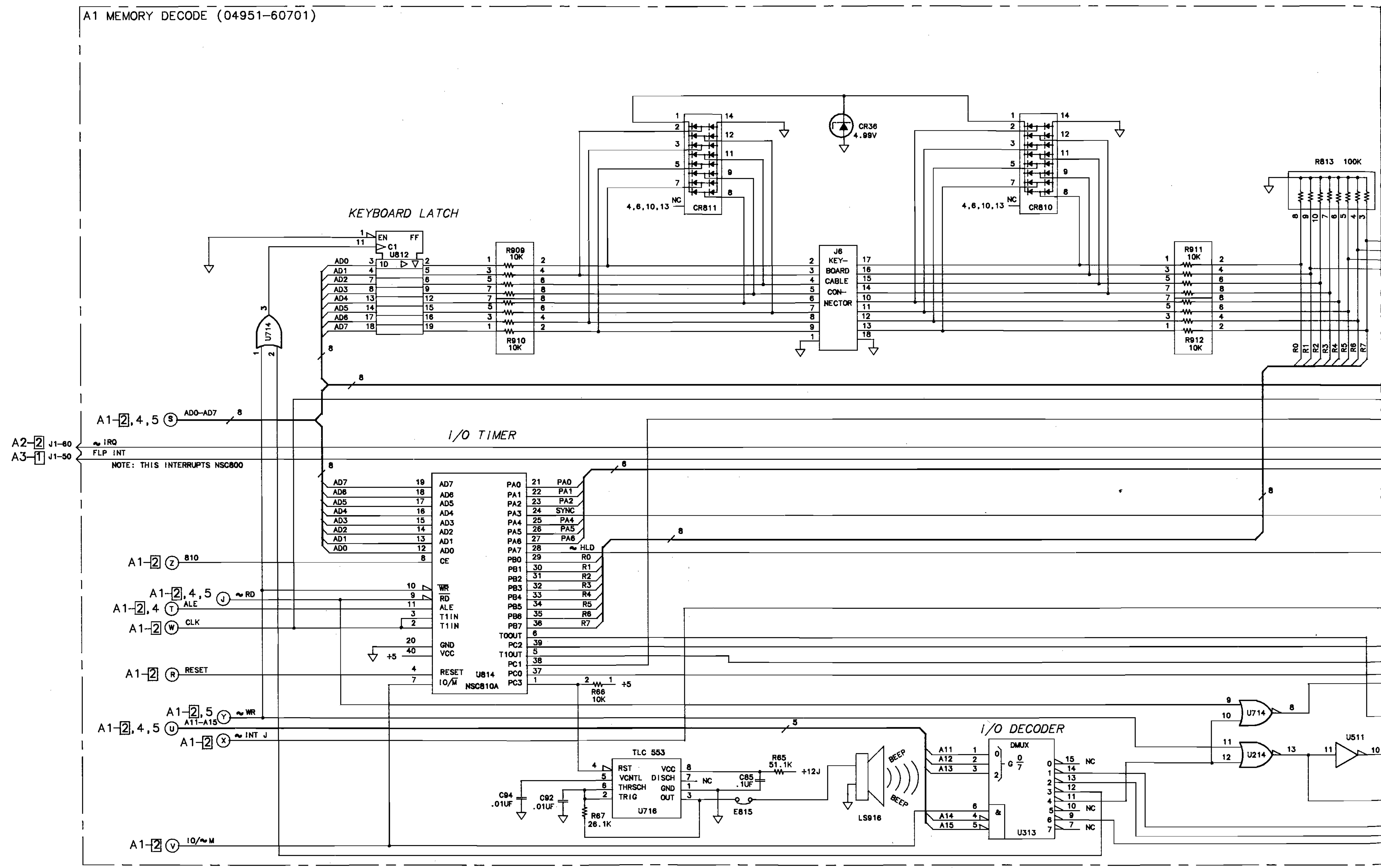


Figure 8-16. A1-3 Memory Decode Component Locator



A1-3

Figure 8-17. A1-3 Memory Decode Schematic Diagram



A1 MEMORY DECODE (04951-60701)
KEYBOARD LATCH
U812
R909 10K
R910 10K
CR811
CR36 4.99V
J8 KEY-BOARD CABLE CON-NECTOR
CR810
R911 10K
R912 10K
R813 100K
U714
A1-2,4,5 S AD0-AD7
A2-2 J1-60 ~IRQ
A3-1 J1-50 FLP INT
NOTE: THIS INTERRUPTS NSC800
I/O TIMER
A1-2 Z 810
A1-2,4,5 J ~RD
A1-2,4 T ALE
A1-2 W CLK
A1-2 R RESET
U814 NSC810A
R66 10K
A1-2,5 Y ~WR
A1-2,4,5 U A11-A15
A1-2 X ~INT J
TLC 553
U716
R65 51.1K
C85 .1UF
C94 .01UF
C92 .01UF
R67 26.1K
E815
LS916
BEEP
I/O DECODER
DMUX
U313
U214
U511
A1-2 V IO/~M

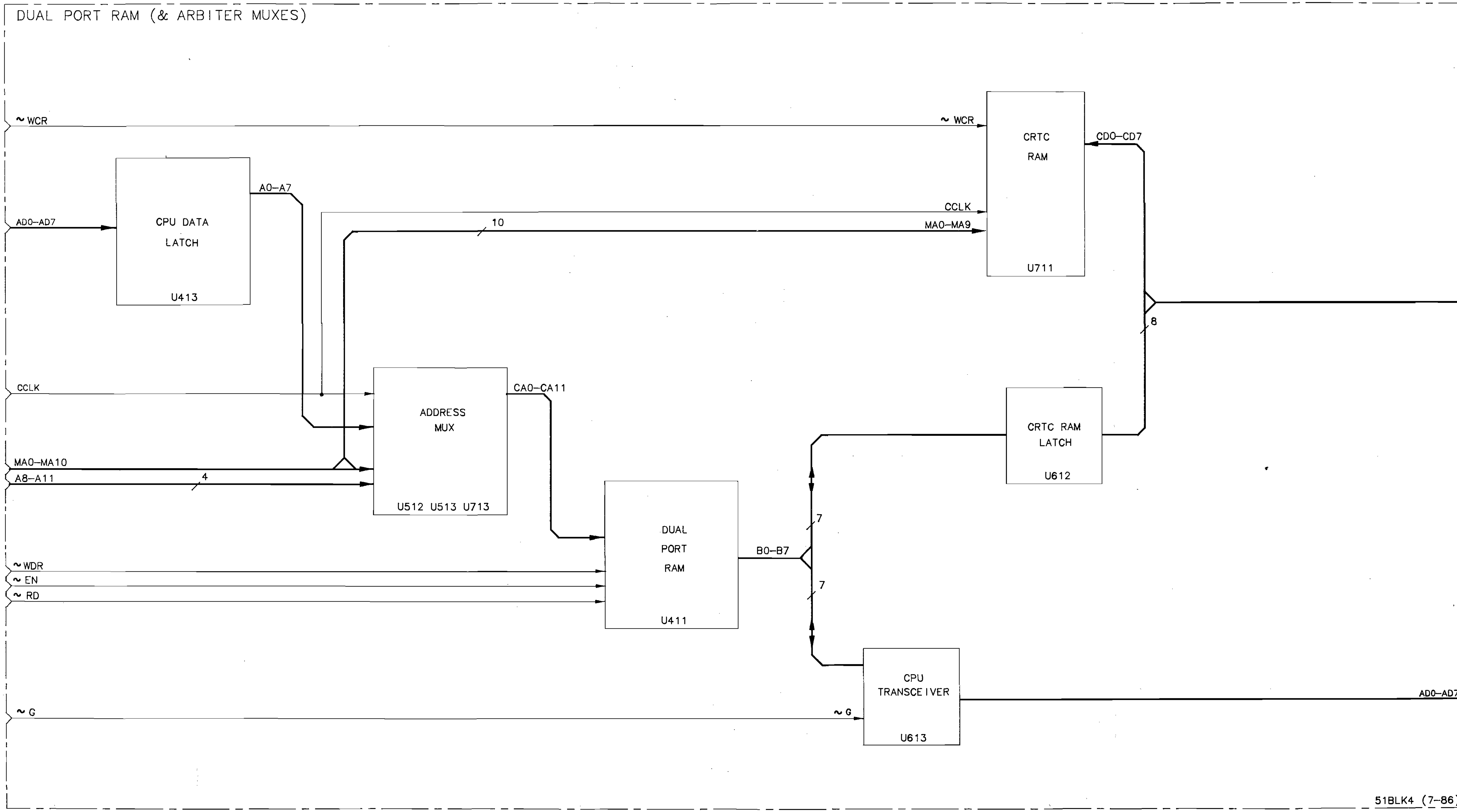


Figure 8-18. A1-4 Dual Port RAM Block Diagram

Power & Ground

PART #	+5	GND
U213	16	8
U411	28/B	14
U413	20	10
U512	16	8
U513	16	8
U612	20	10
U613	20	10
U710	14	7
U711	24	12
U713	16	8

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3

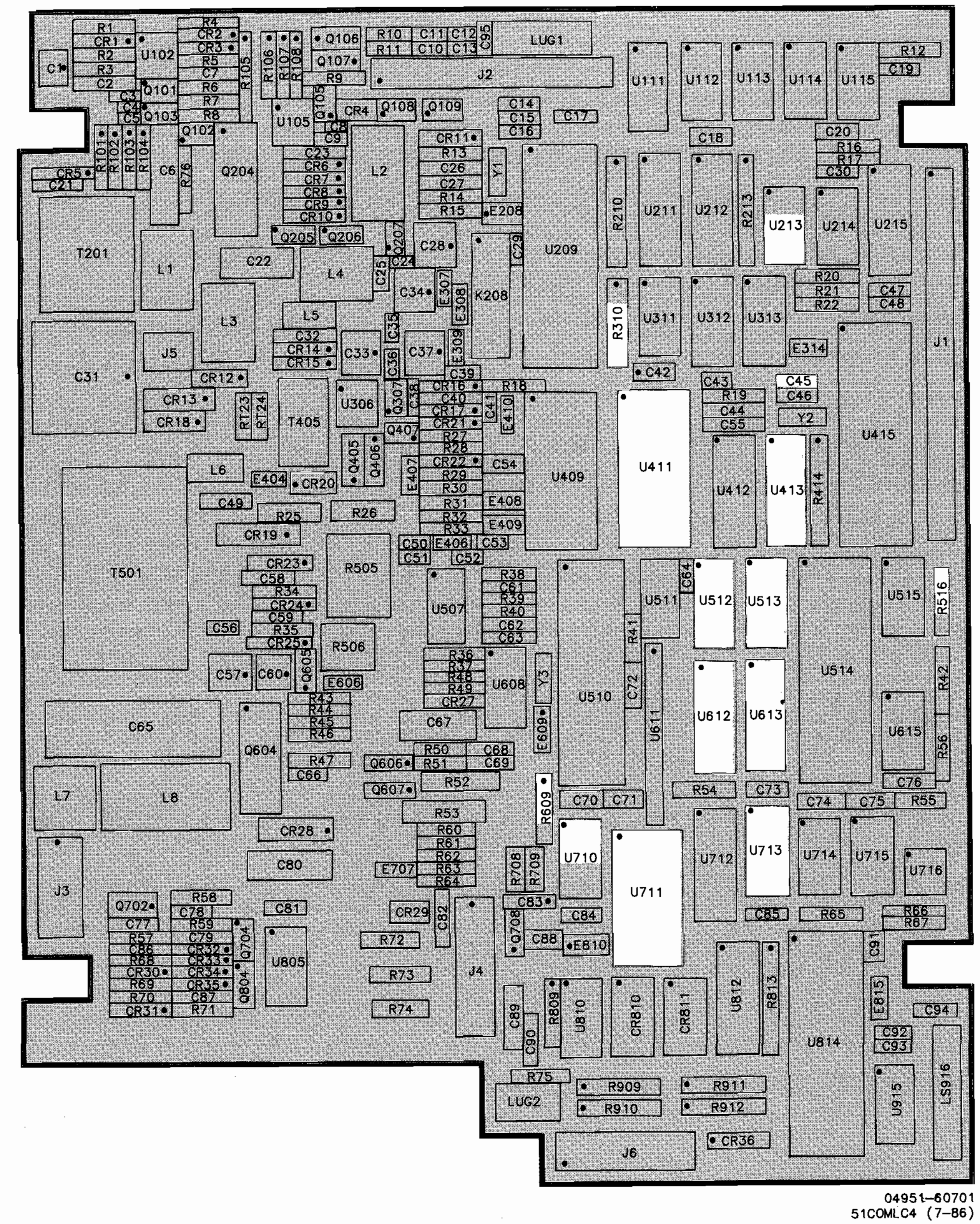


Figure 8-19. A1-4 Dual Port RAM Component Locator

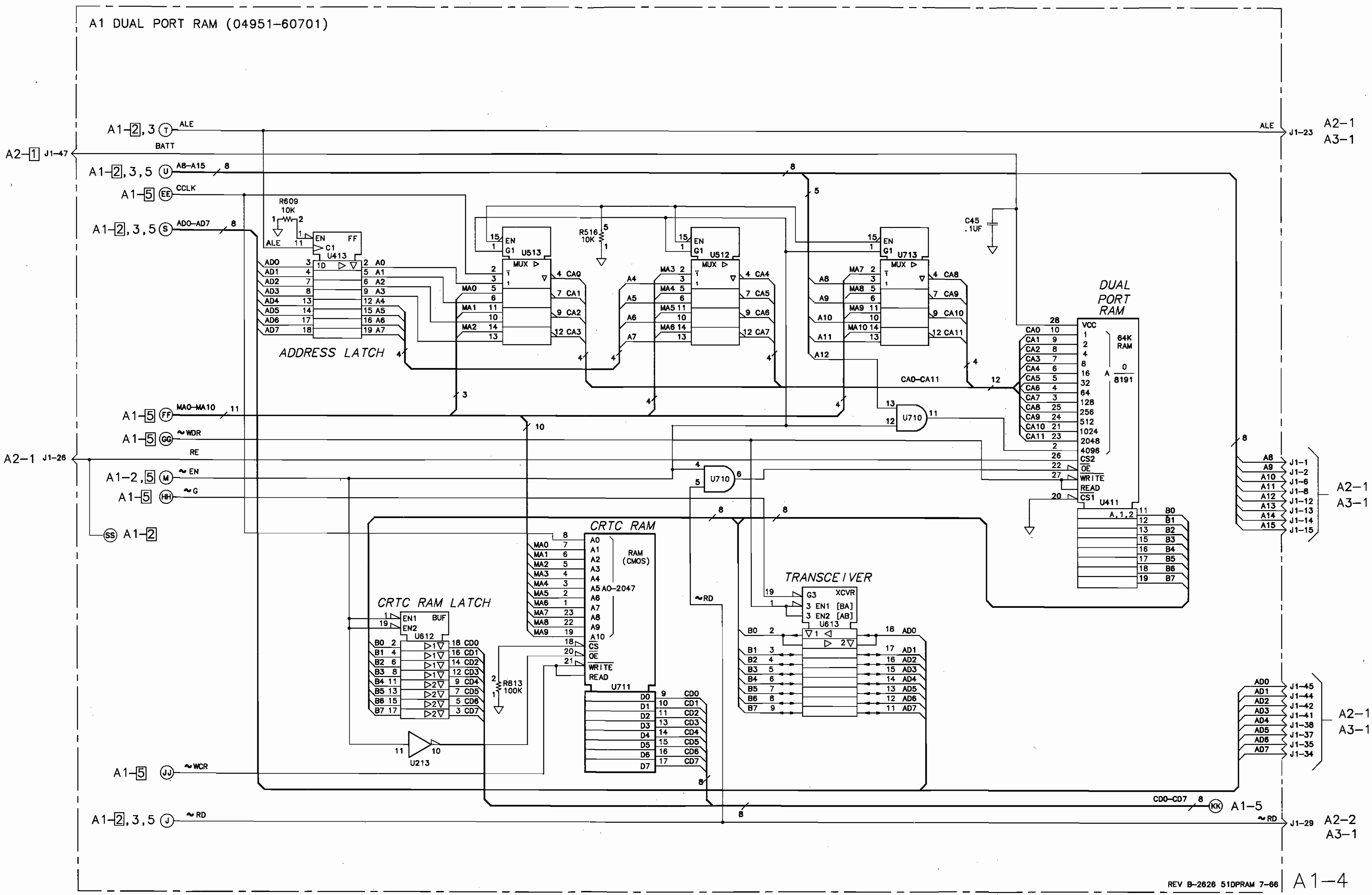


Figure 8-20. A1-4 Dual Port RAM Schematic Diagram

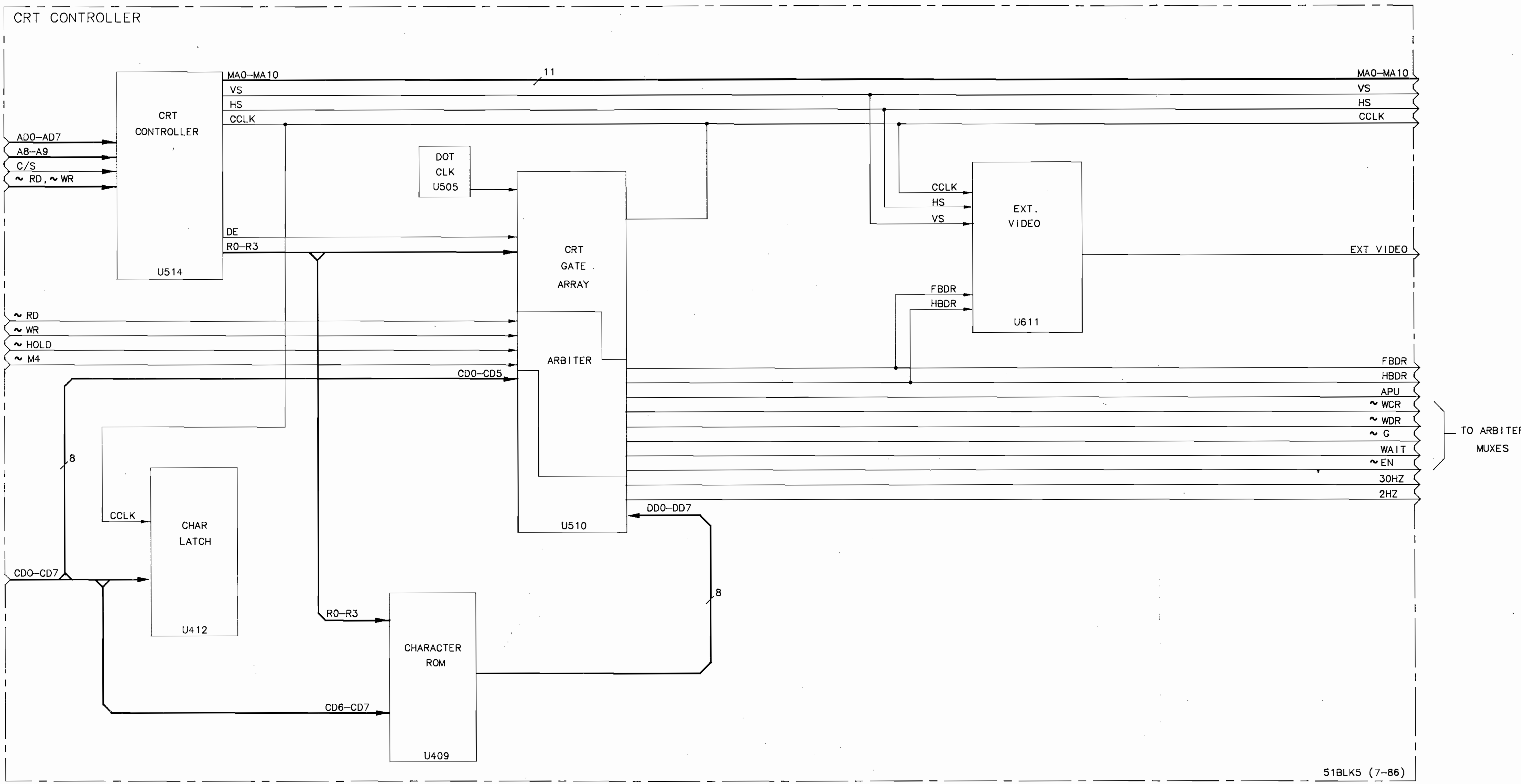


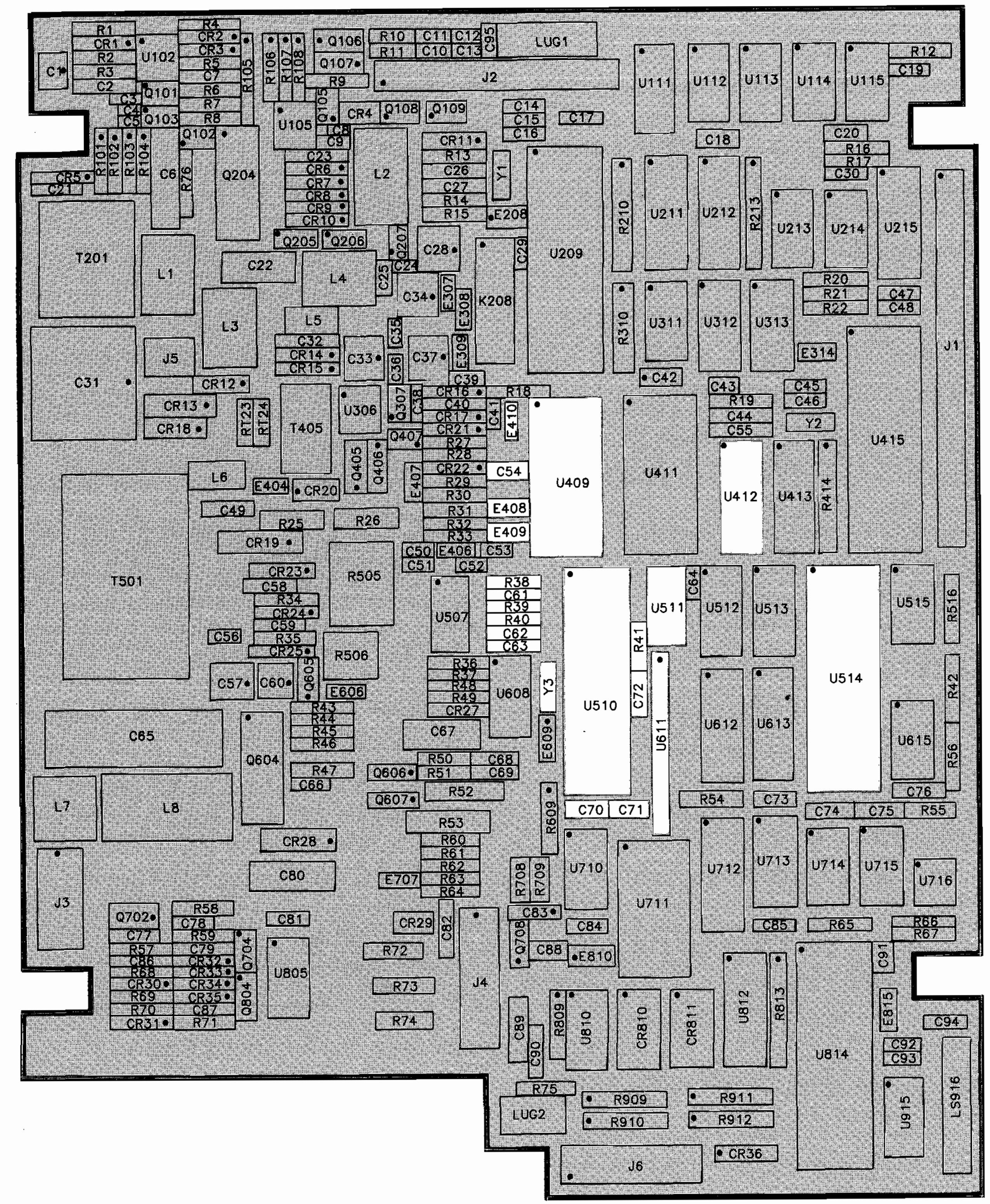
Figure 8-21. A1-5 CRT Controller Block Diagram

Power & Ground

PART #	+5	GND
U214	14	7
U409	28	14
U412	20	10
U510	30	10
U511	14	7
U514	28	1
U611	7	3
U810	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3



04951-60701
51COMLC4 (7-86)

Figure 8-22. A1-5 CRT Controller Component Locator

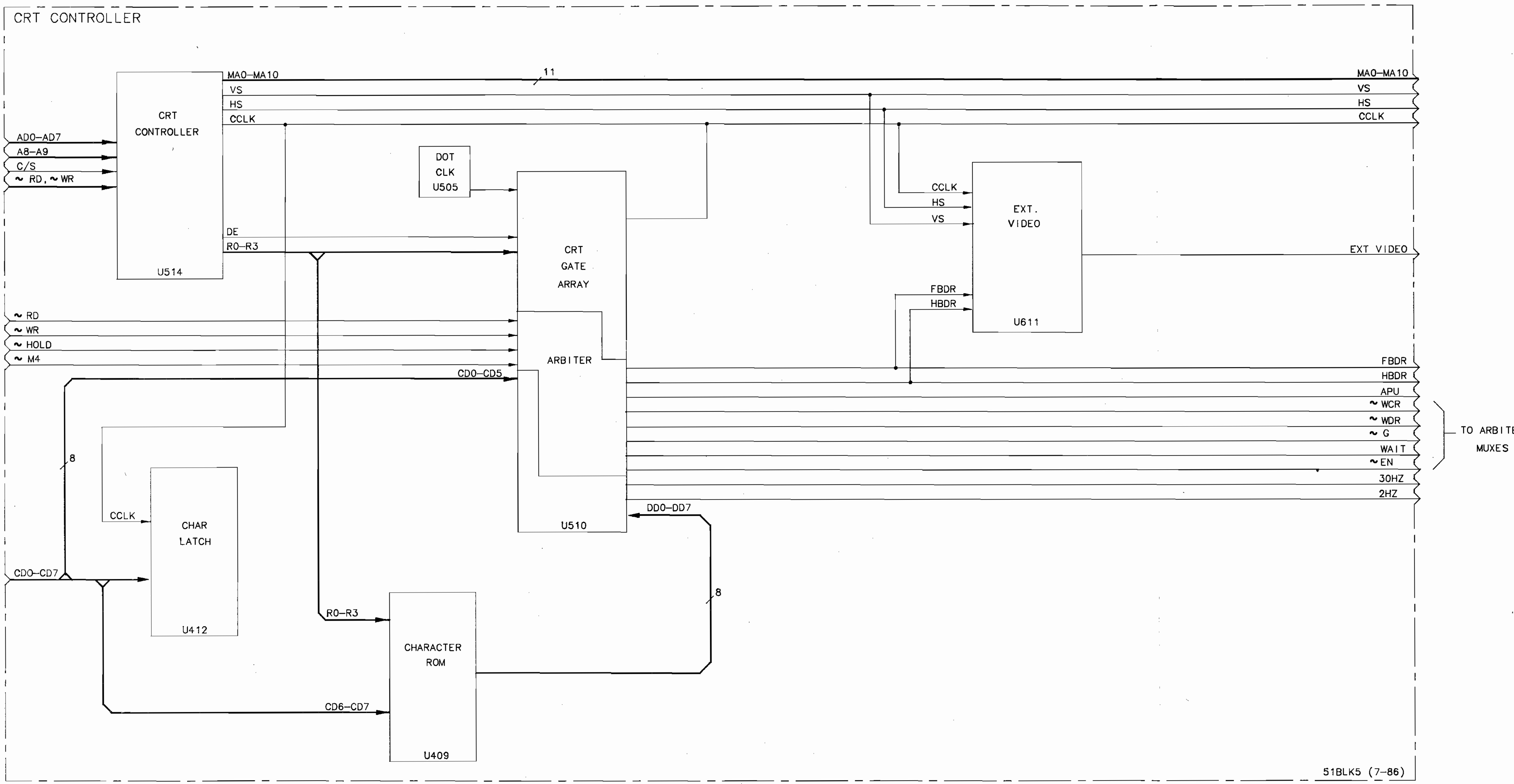


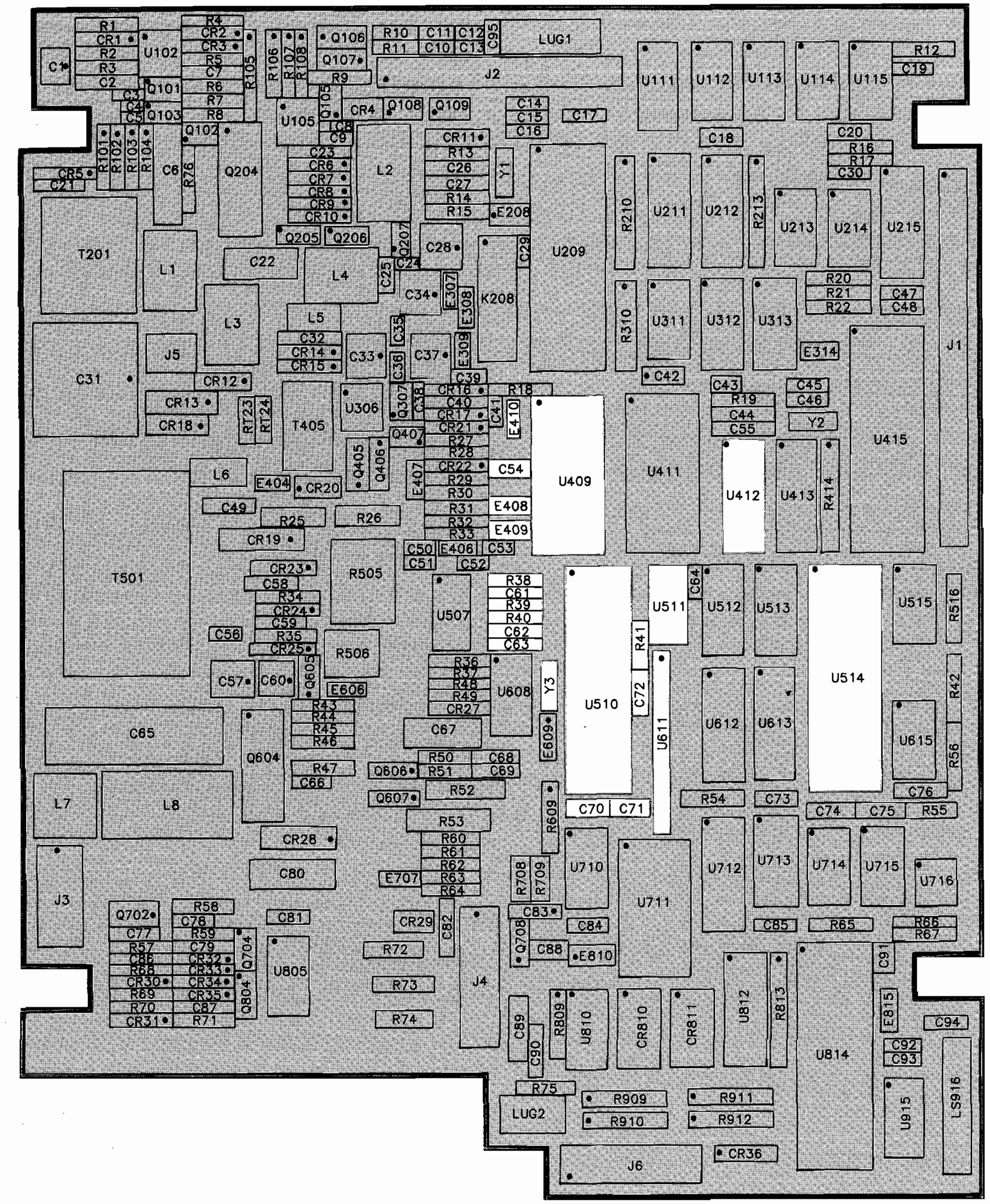
Figure 8-21. A1-5 CRT Controller Block Diagram

Power & Ground

PART #	+5	GND
U214	14	7
U409	28	14
U412	20	10
U510	30	10
U511	14	7
U514	28	1
U611	7	3
U810	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3



04951-60701
51COMLC4 (7-86)

Figure 8-22. A1-5 CRT Controller Component Locator

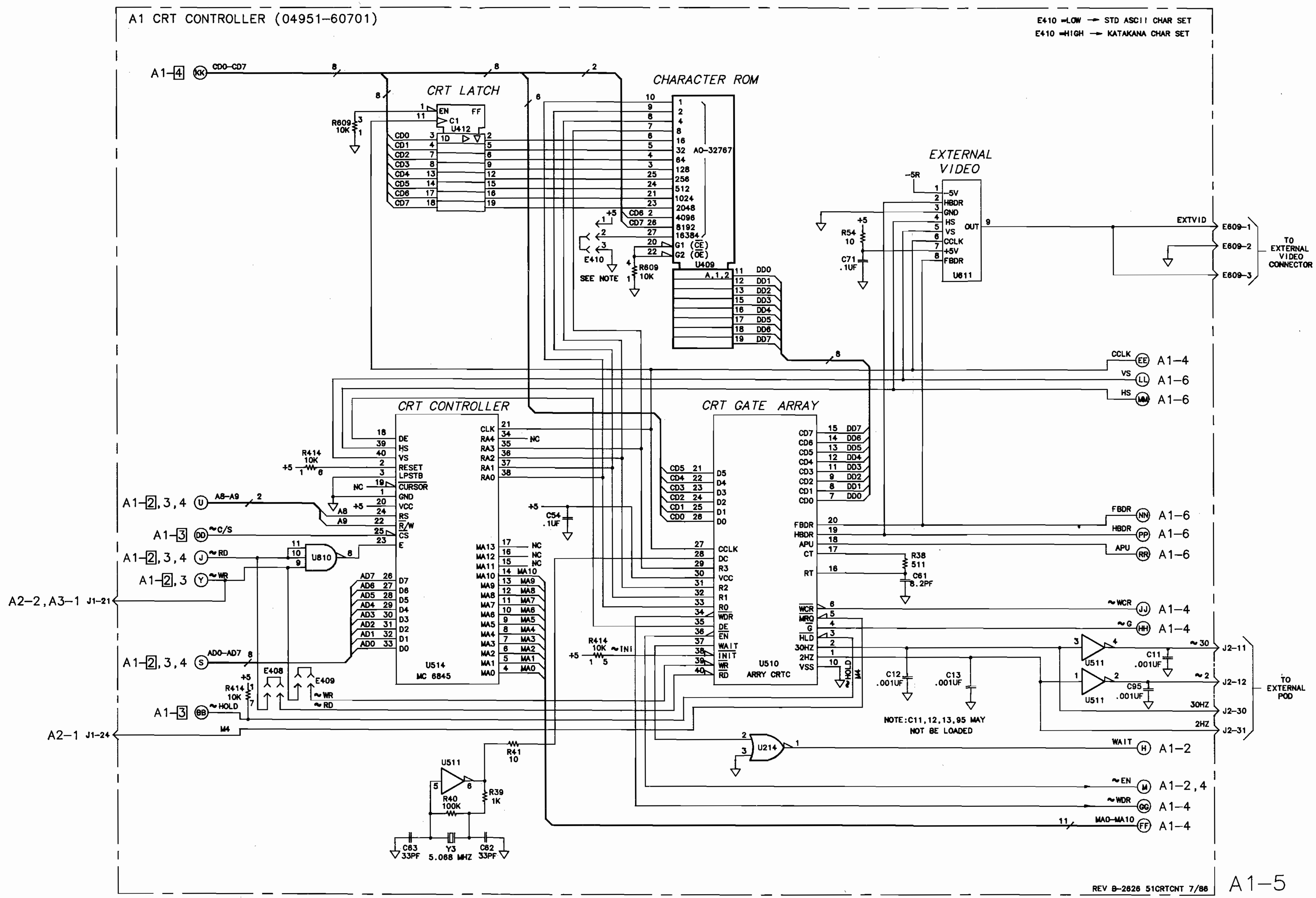


Figure 8-23. A1-5 CRT Controller Schematic Diagram

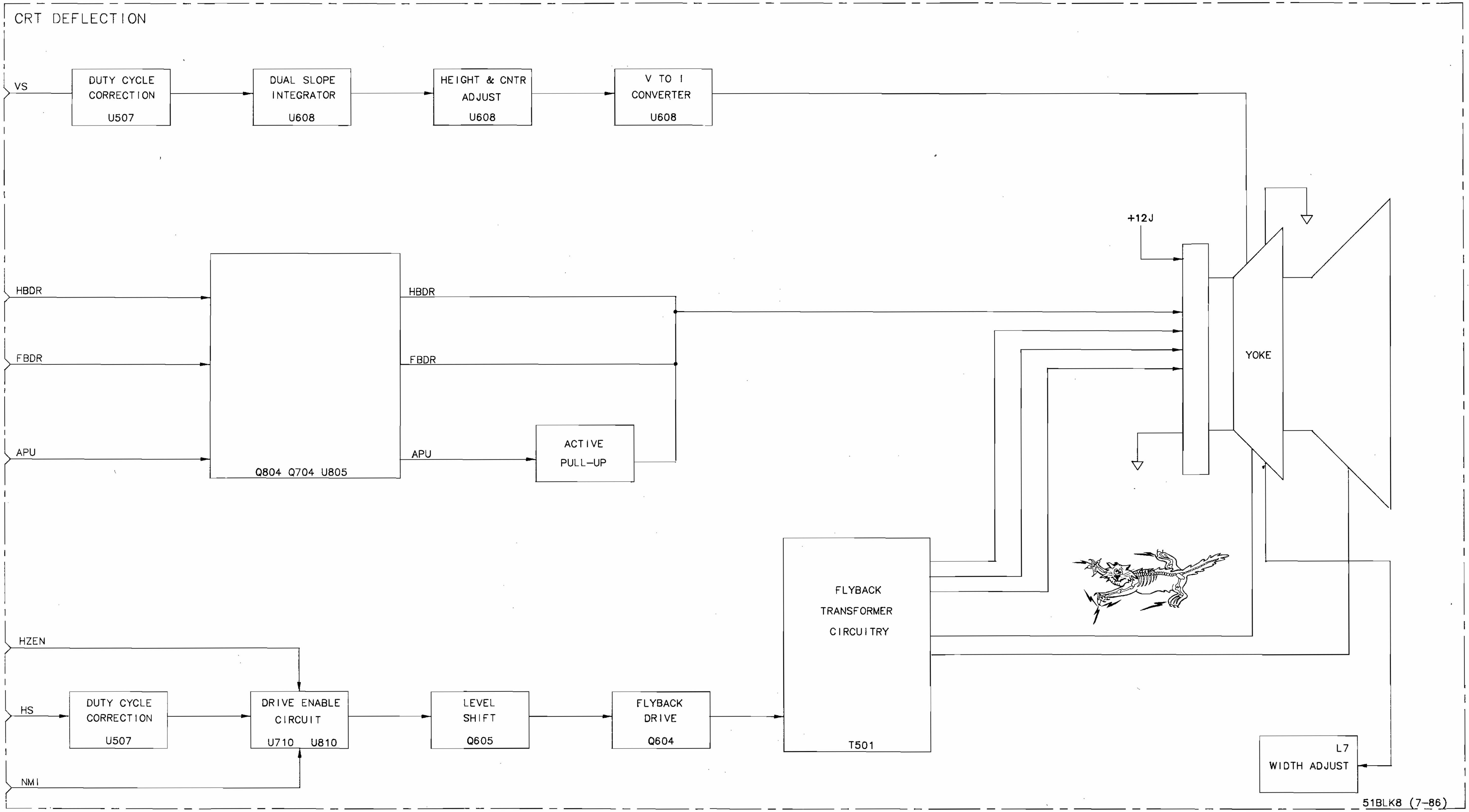


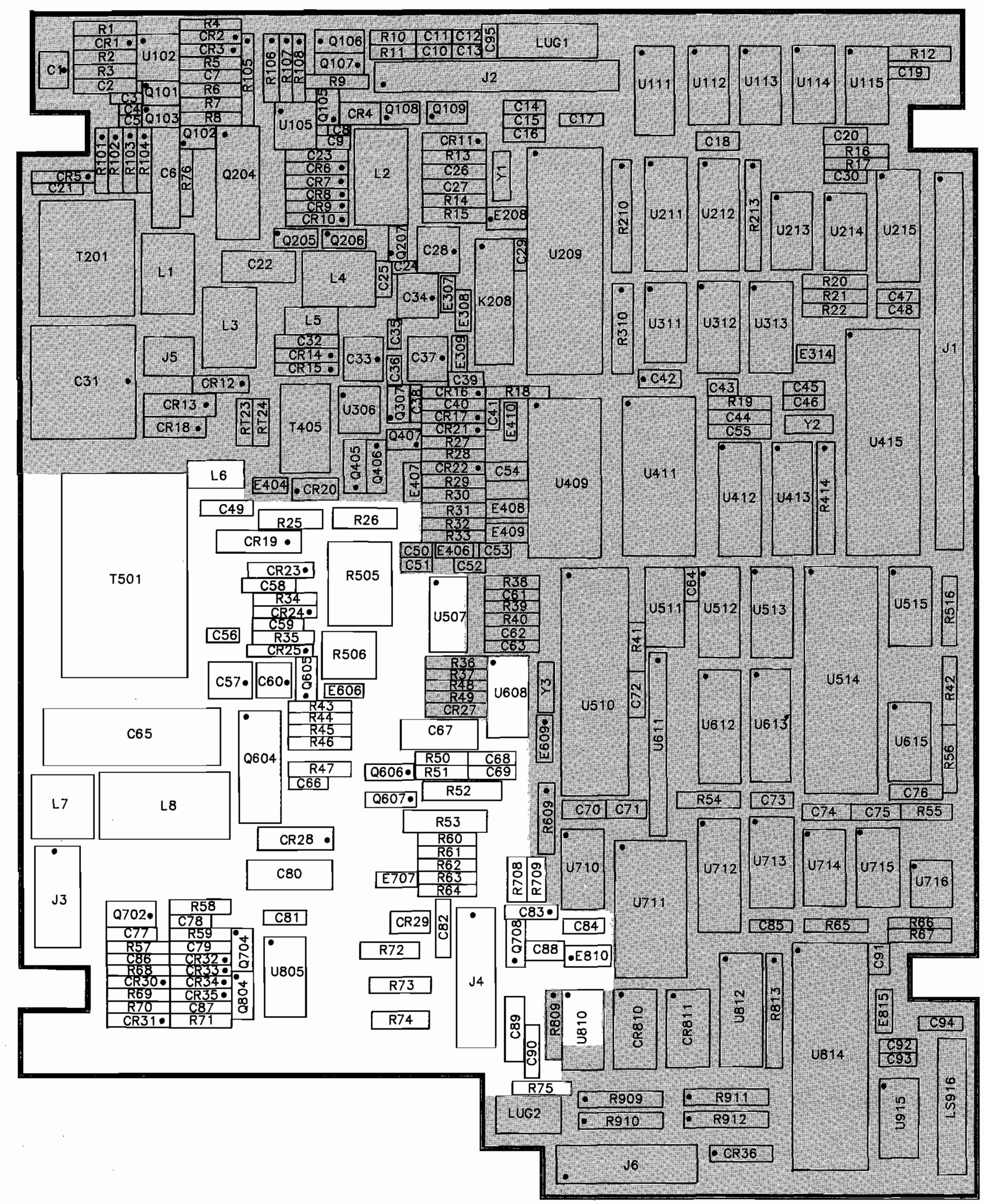
Figure 8-24. A1-6 CRT Deflection Block Diagram

Power & Ground

Part #	+5	Gnd
U507	16	8
U608	4	11
U805	14	7
U810	14	7

CROSS - REFERENCED PARTS

U102	A1-1	U312	A1-2,3	U611	A1-5
U105	A1-1	U313	A1-3	U612	A1-4
U111	A1-2	U409	A1-5	U613	A1-4
U112	A1-2	U411	A1-4	U615	A1-3
U113	A1-2	U412	A1-5	U710	A1-1,2,4
U114	A1-3	U413	A1-4	U711	A1-4
U115	A1-2	U415	A1-2	U712	A1-3
U209	A1-2	U507	A1-6	U713	A1-4
U211	A1-2	U510	A1-5	U714	A1-2,3
U212	A1-2	U511	A1-2,3,5	U715	A1-3
U213	A1-2,3,4	U512	A1-4	U716	A1-3
U214	A1-2,3,5	U513	A1-4	U810	A1-2,5,6
U215	A1-2	U514	A1-5	U812	A1-3
U306	A1-1	U515	A1-2	U814	A1-3
U311	A1-2,3	U608	A1-6	U915	A1-3



04951-60701
51COMLC4 (7-86)

Figure 8-25. A1-6 CRT Deflection Component Locator

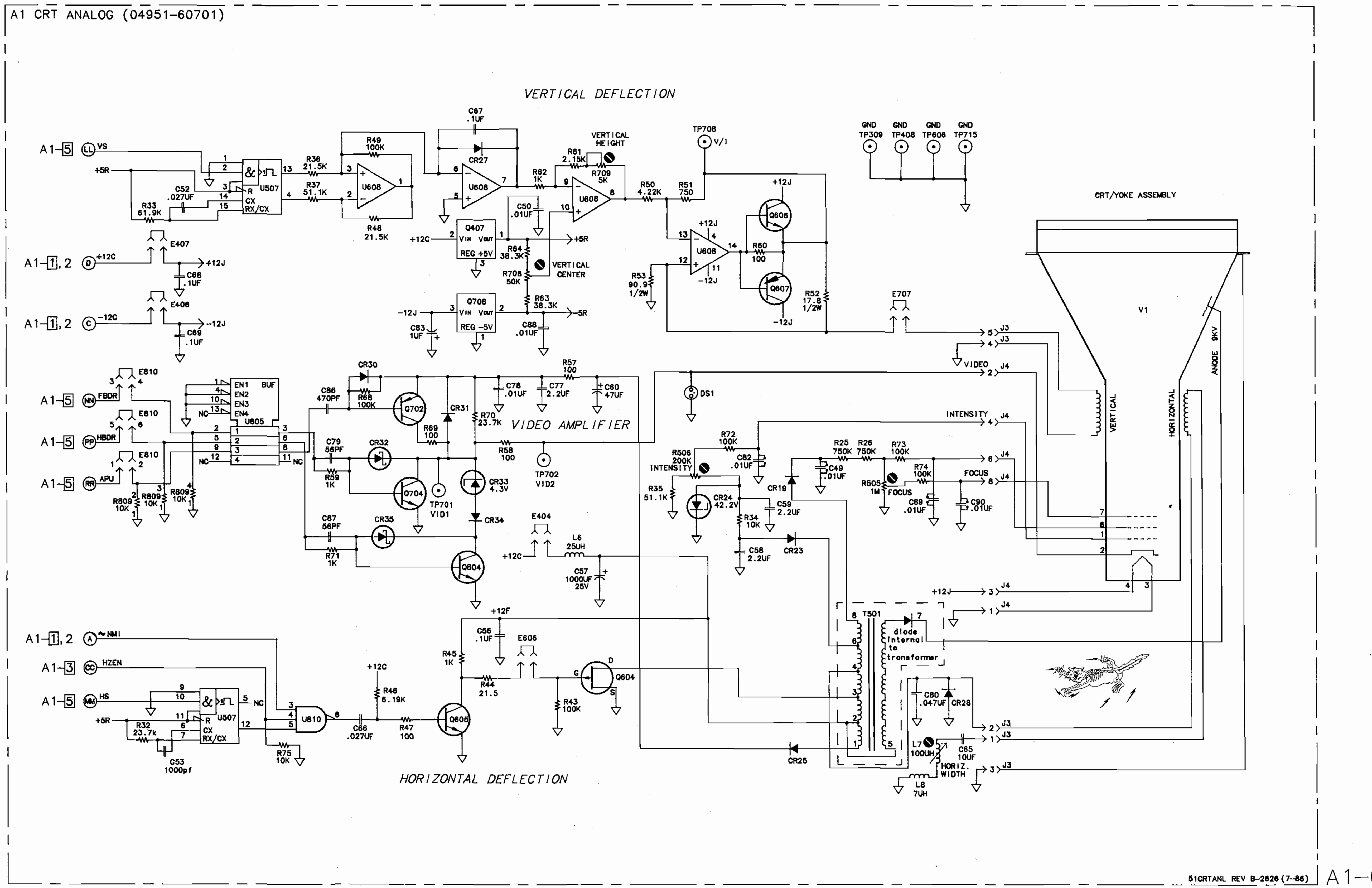


Figure 8-26. A1-6 CRT Deflection Schematic Diagram

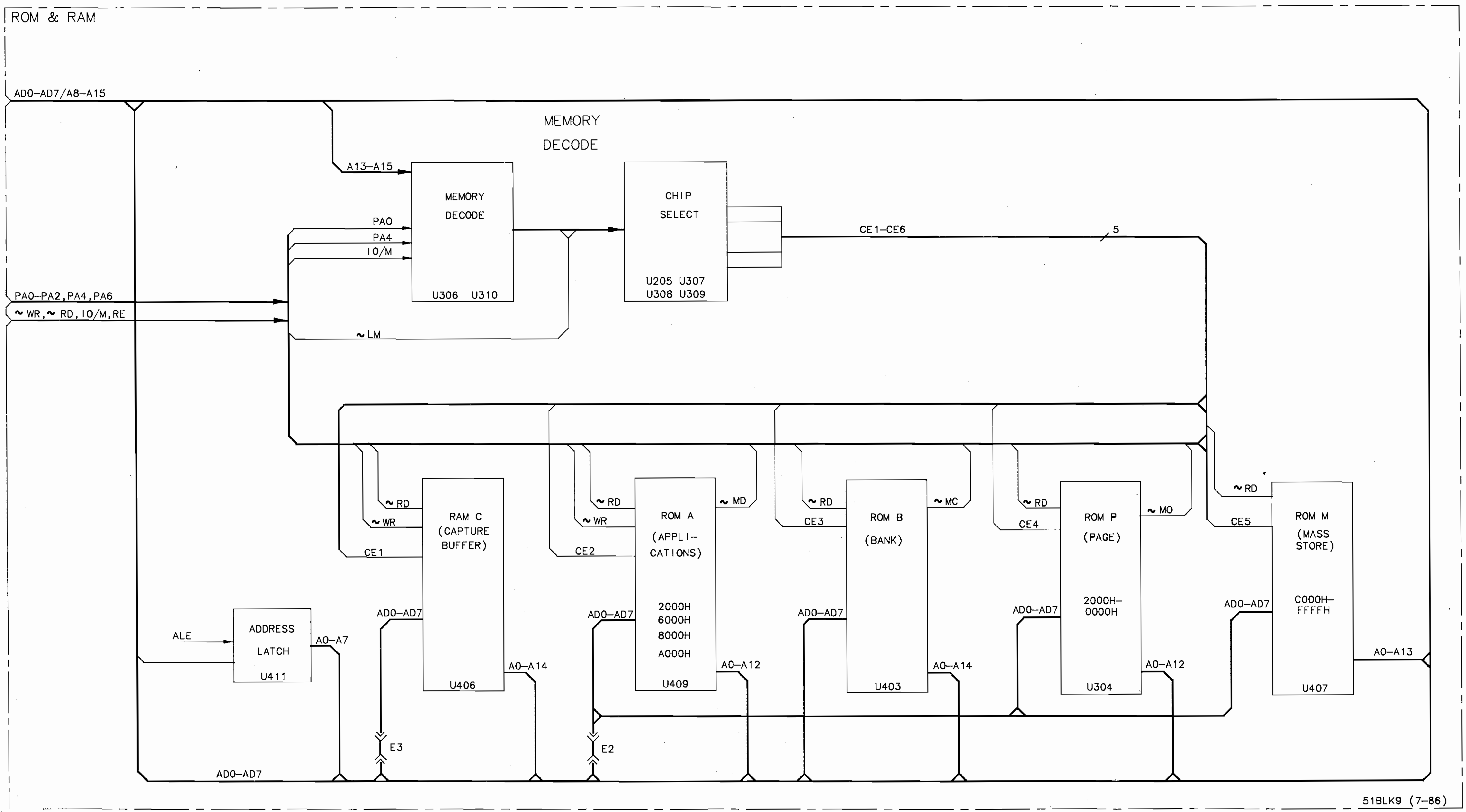
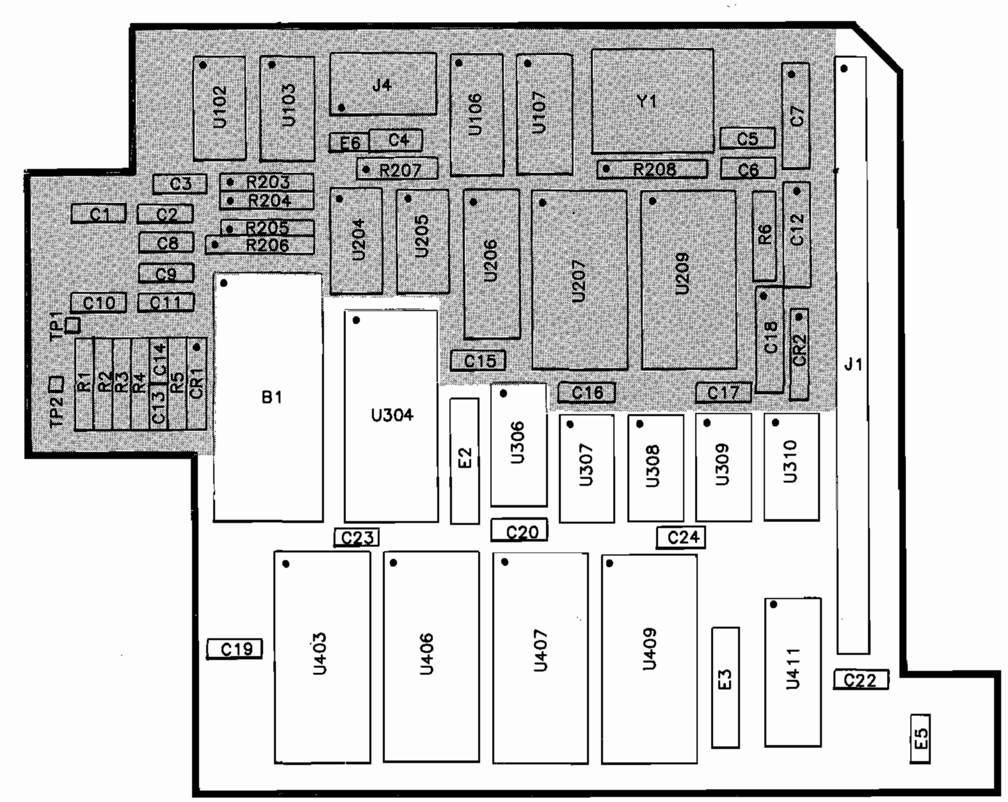


Figure 8-27. A2-1 ROM and RAM Block Diagram

Power & Ground

Part #	+5	Gnd	Battery
U205	14	7	14
U304	28	14	
U306	16	8	
U307	14	7	
U308	14	7	
U309	14	7	14
U310	14	7	
U403	28	14	
U406	28	14	28
U407	28	14	
U409	28	14	28
U411	20	10	



04951-60702
51COMLC2 (7-86)

Figure 8-28. A2-1 ROM and RAM Component Locator

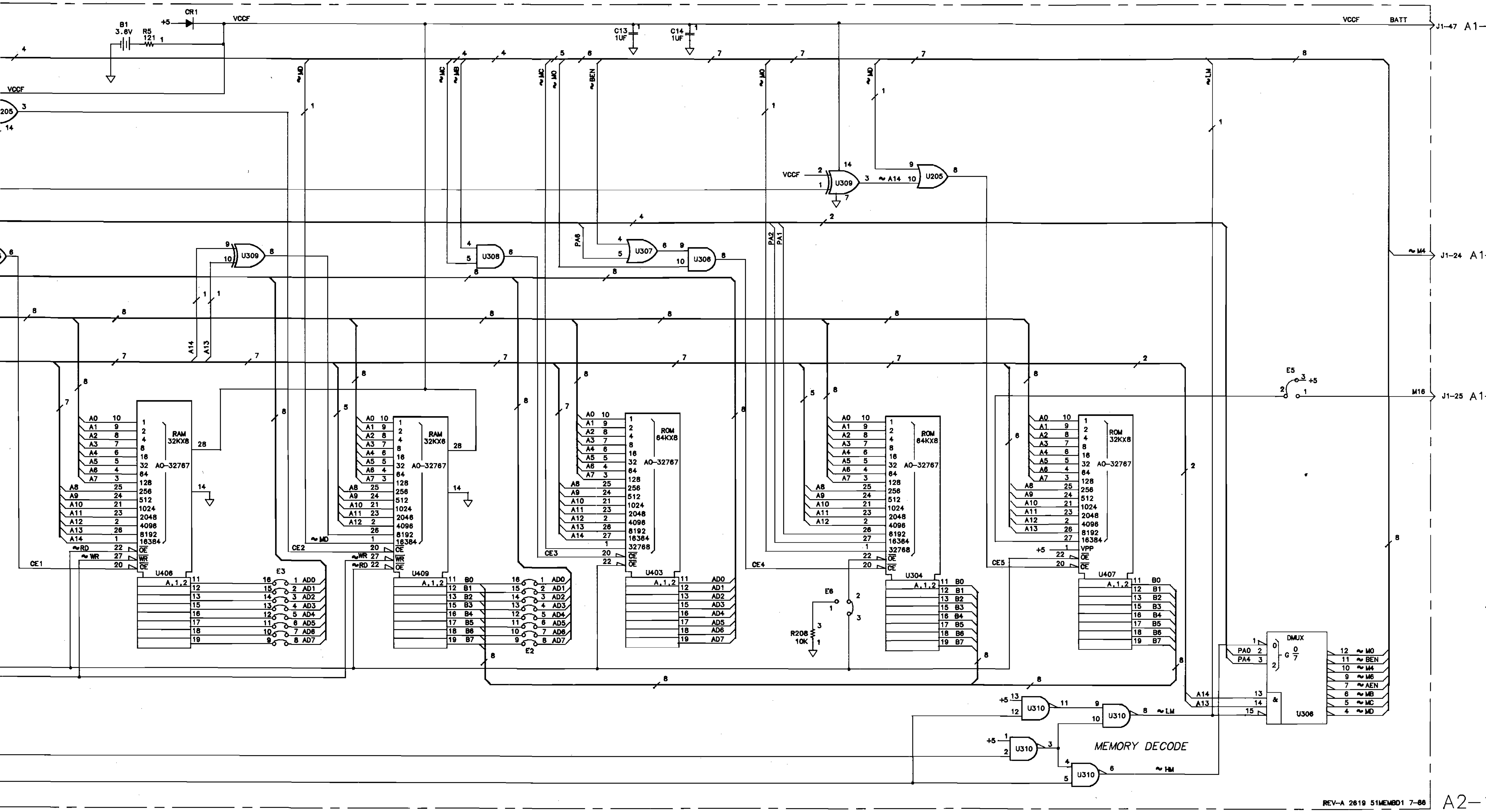
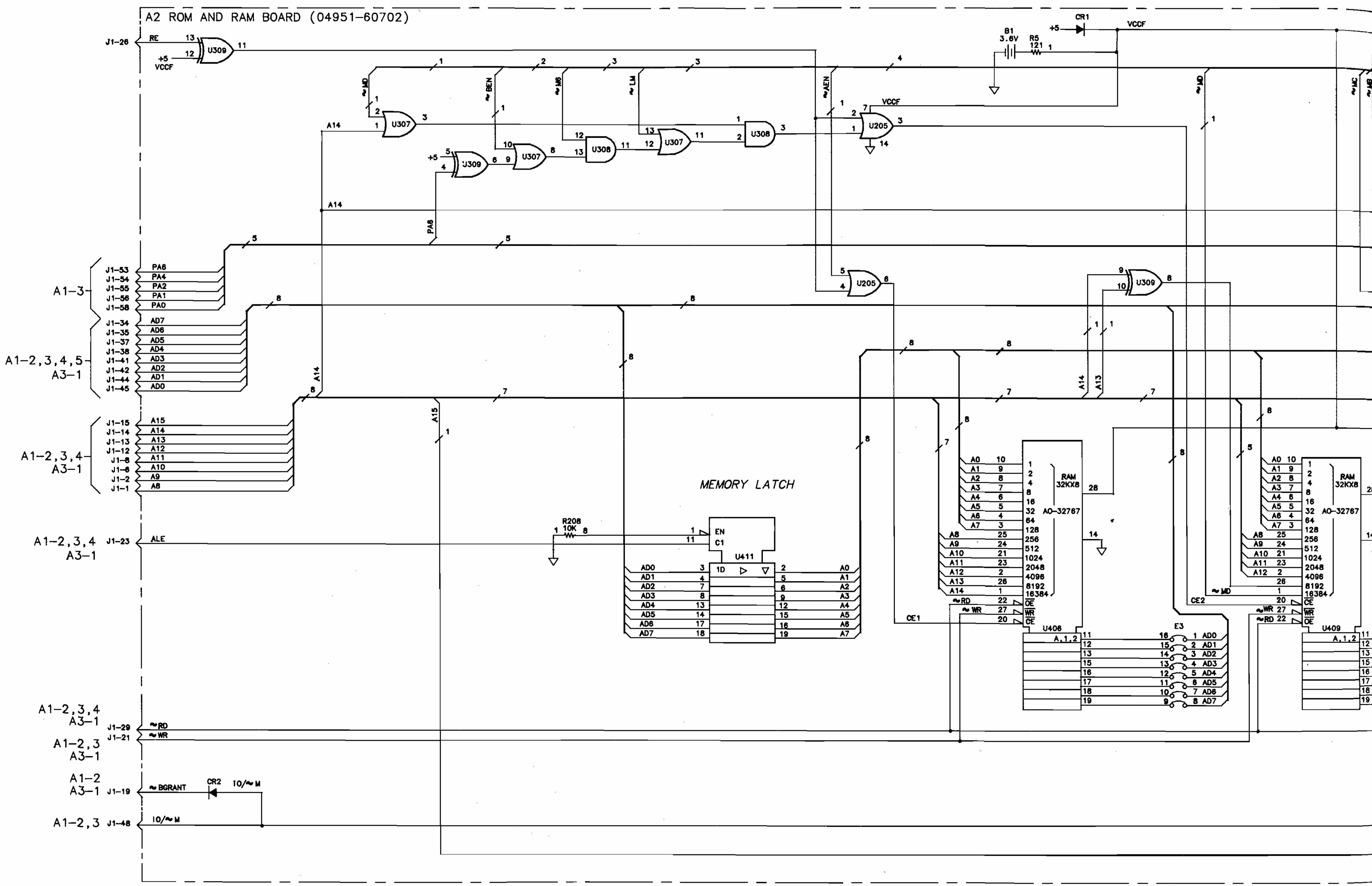


Figure 8-29. A2-1 ROM and RAM Schematic Diagram



A2 ROM AND RAM BOARD (04951-60702)
MEMORY LATCH
A1-3
A1-2,3,4,5
A3-1
A1-2,3,4
A3-1
A1-2,3,4
A3-1
A1-2,3,4
A3-1
A1-2,3
A3-1
A1-2
A3-1
A1-2,3
RAM 32KX8
U411
U406
U409

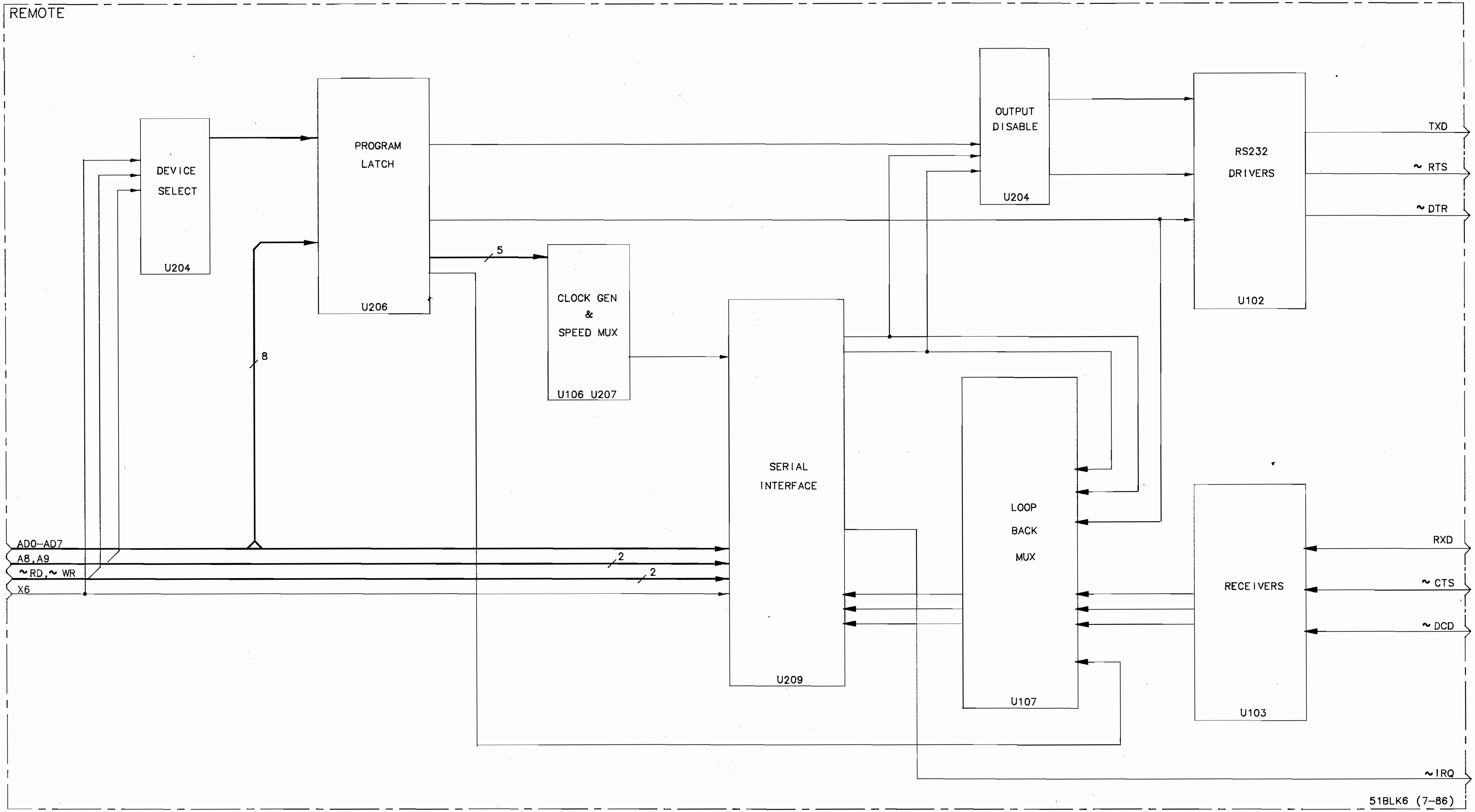


Figure 8-30. A2-2 Remote Block Diagram

Power & Ground

Part #	+5	Gnd
U102	4	11
U103	3	12
U106	16	8
U107	16	8
U204	14	7
U205	14	7
U206	20	10
U207	24	12
U209	12	1

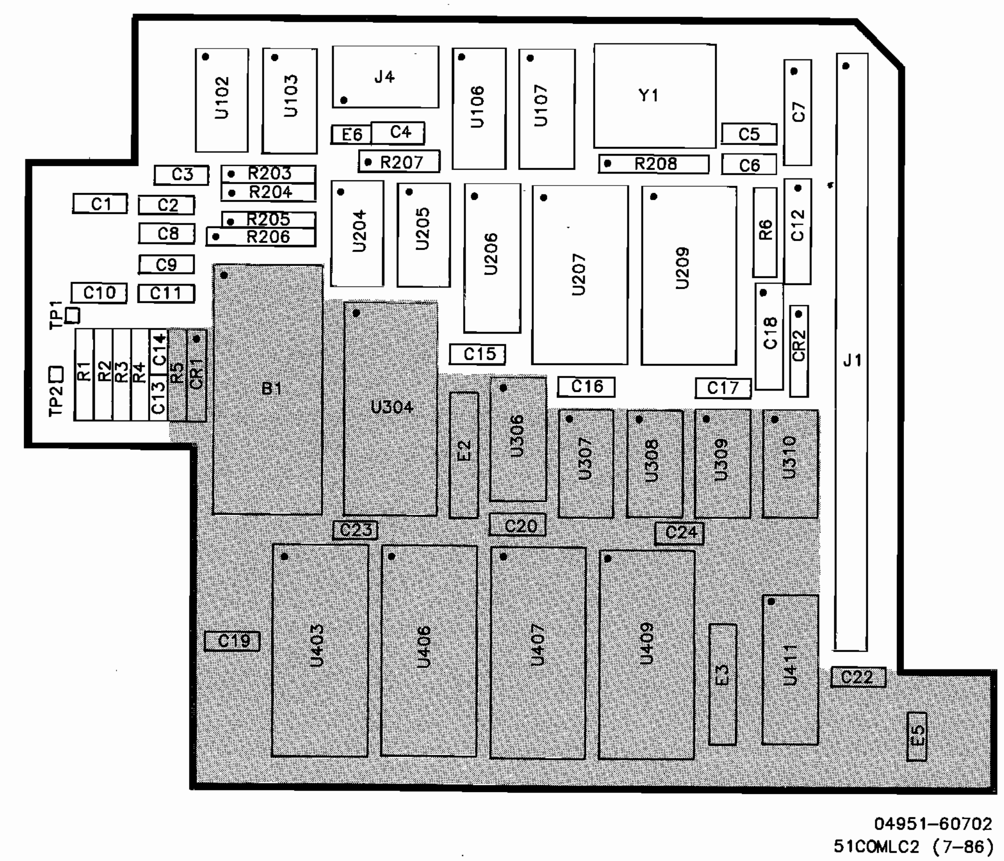


Figure 8-31. A2-2 Remote Component Locator

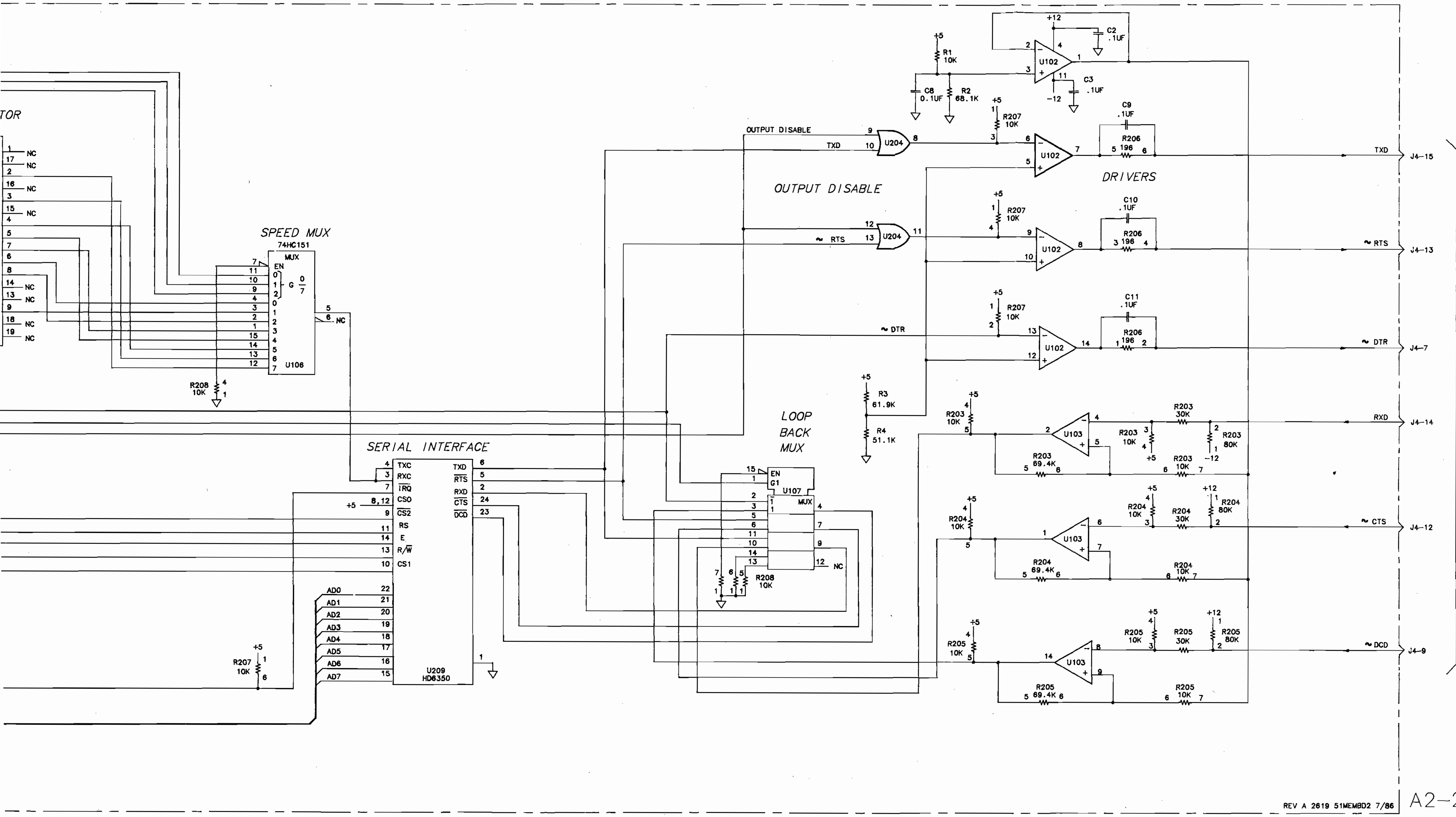
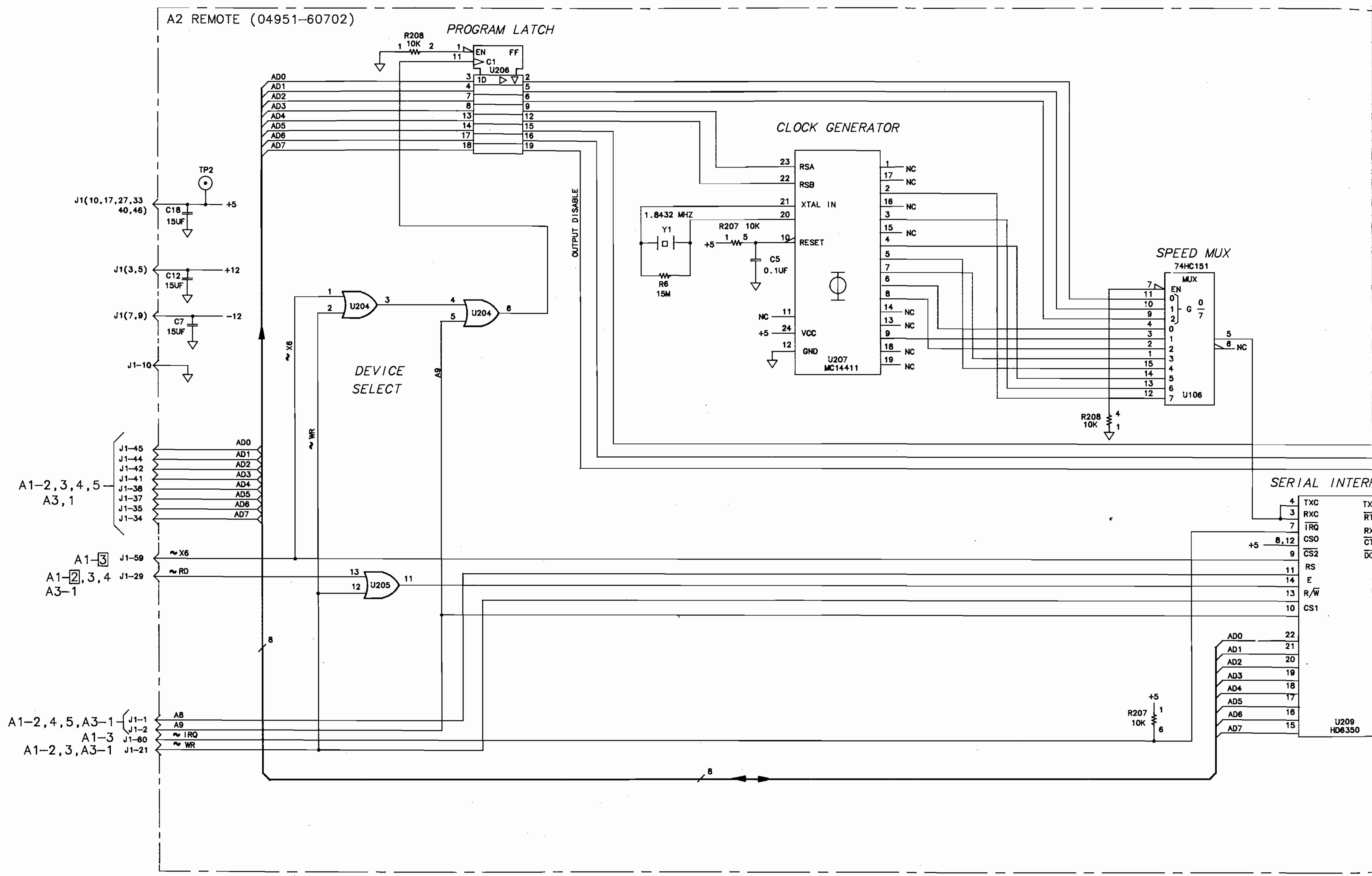


Figure 8-32. A2-1 Remote Schematic Diagram


A2 REMOTE (04951-60702)
PROGRAM LATCH
CLOCK GENERATOR
SPEED MUX
74HC151
DEVICE SELECT
SERIAL INTER
OUTPUT DISABLE
U206
U207
MC14411
U106
U204
U205
U209
HD6350
1.8432 MHZ
R208 10K
R207 10K
R6 15M
C5 0.1UF
C18 15UF
C12 15UF
C7 15UF
TP2
J1(10,17,27,33 40,46)
J1(3,5)
J1(7,9)
J1-10
A1-2,3,4,5-A3,1
A1-3
A1-2,3,4 A3-1
A1-2,4,5,A3-1
A1-3
A1-2,3,A3-1

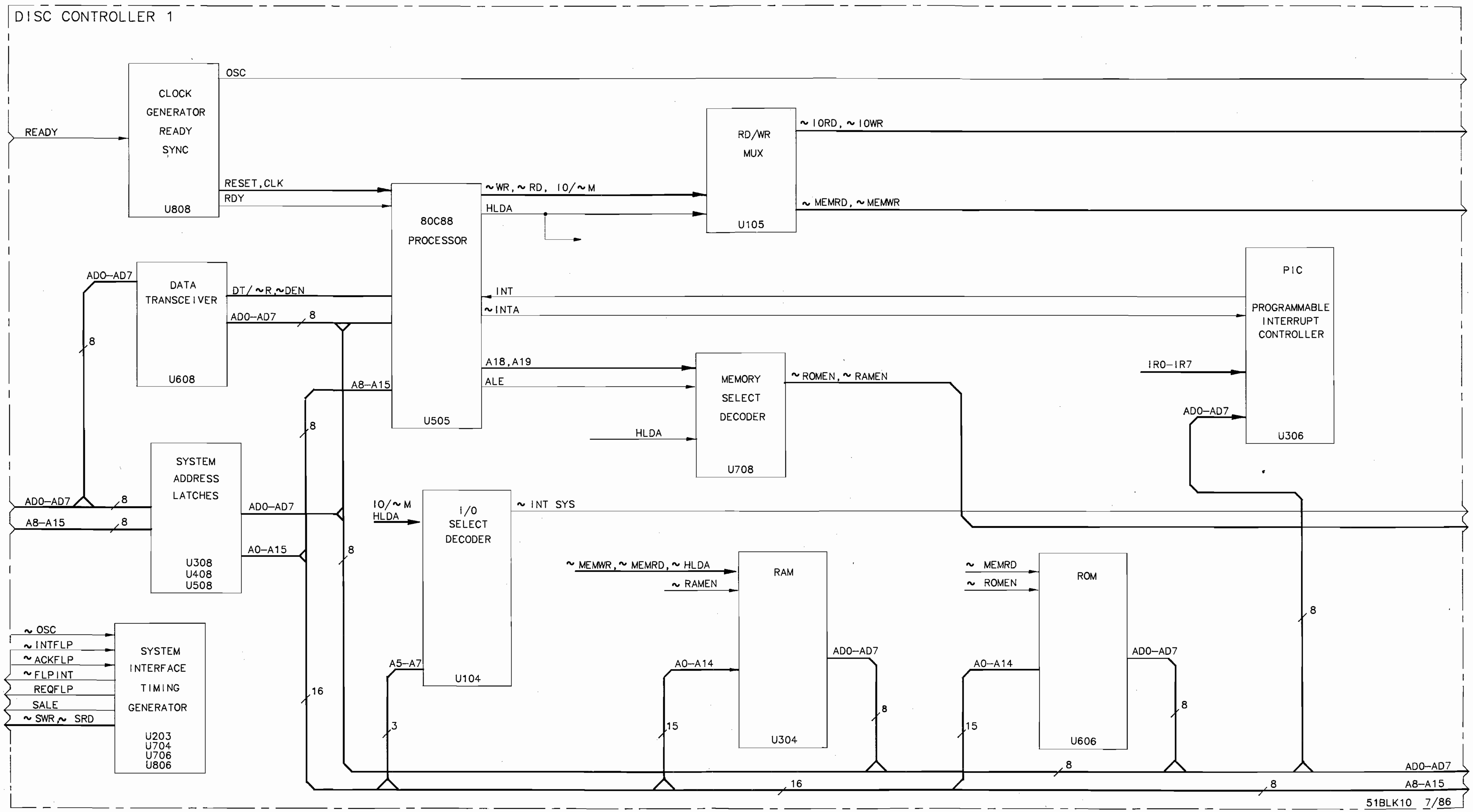
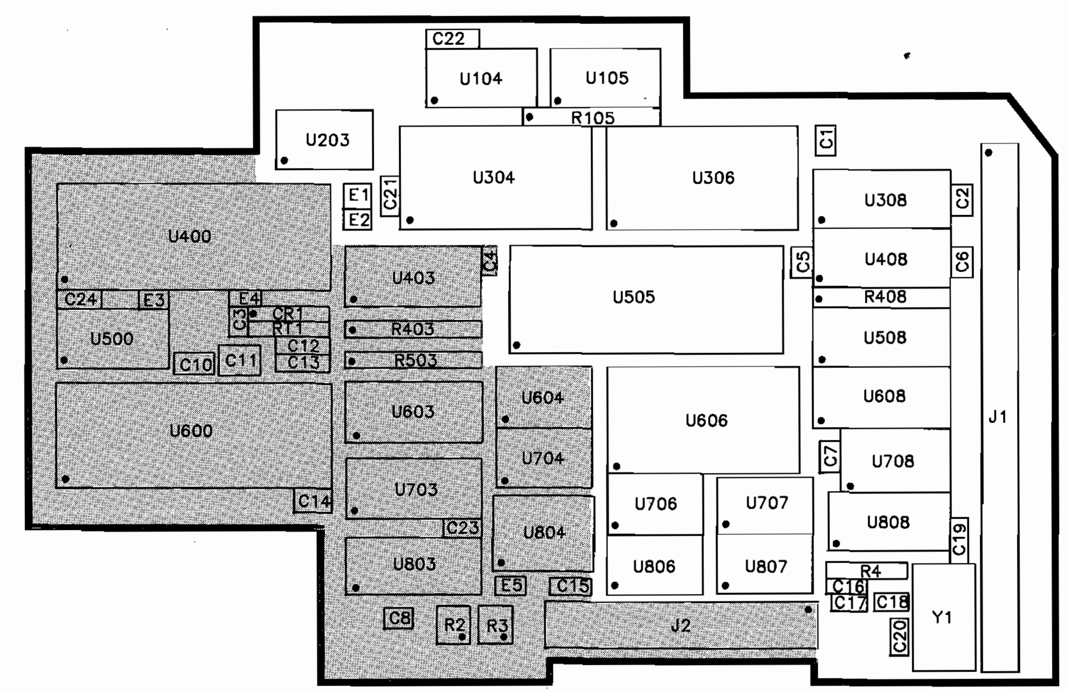


Figure 8-33. A3-1 Disc Controller Block Diagram

Power & Ground

Part #	+5	Gnd
U104	16	8
U105	16	8
U203	14	7
U304	28	14
U306	28	14
U308	20	10
U408	20	10
U505	40	20
U508	20	10
U604	14	7
U606	28	14
U608	20	10
U704	14	7
U706	14	7
U707	13	12
U708	16	8
U806	14	7
U807	14	7
U808	18	9



04951-60703
51COMLC3 (7-86)

Figure 8-34. A3-1 Disc Controller Component Locator

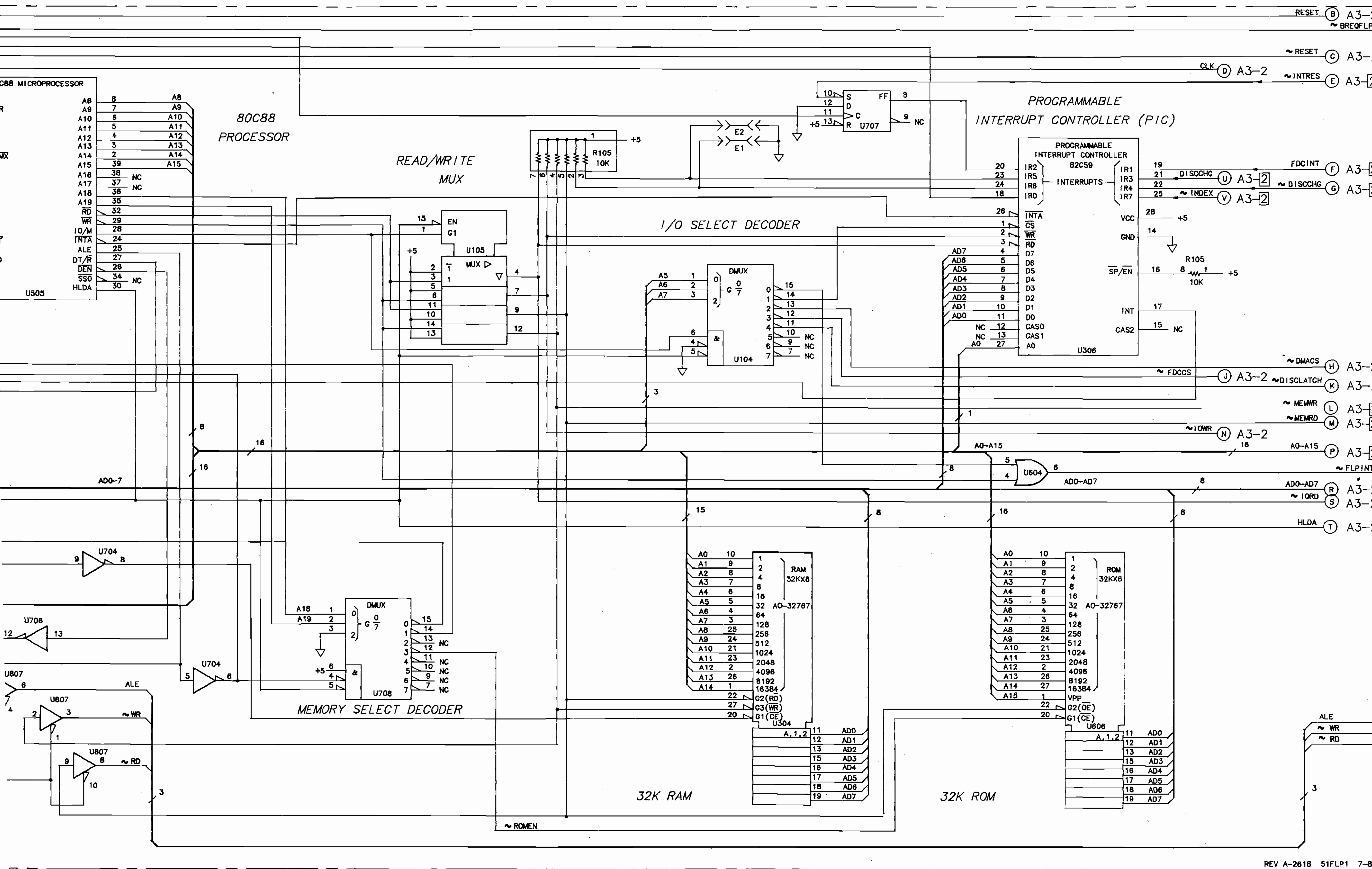
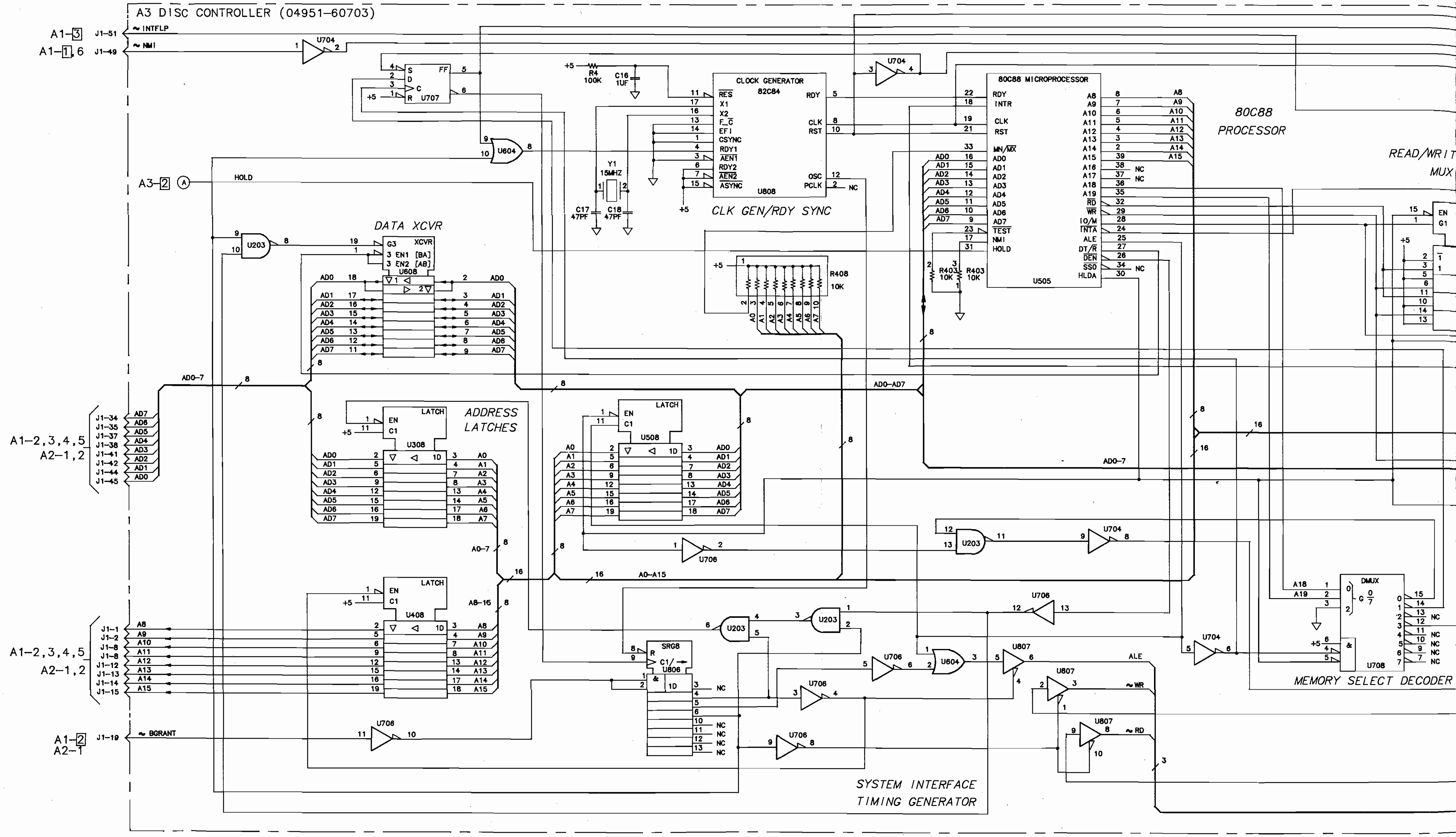


Figure 8-35. A3-1 Disc Controller Schematic Diagram


A3 DISC CONTROLLER (04951-60703)
80C88 PROCESSOR
80C88 MICROPROCESSOR
CLOCK GENERATOR
82C84
CLK GEN/RDY SYNC
DATA XCVR
ADDRESS LATCHES
READ/WRIT
MUX
SYSTEM INTERFACE
TIMING GENERATOR
MEMORY SELECT DECODER
~ INTFLP
~ NMI
HOLD
~ BGRANT
ALE
~ WR
~ RD
AD0-AD7
A0-A15
A8-16
A1-3
A1-1, 6
A3-2
A1-2,3,4,5
A2-1,2
A1-2
A2-1

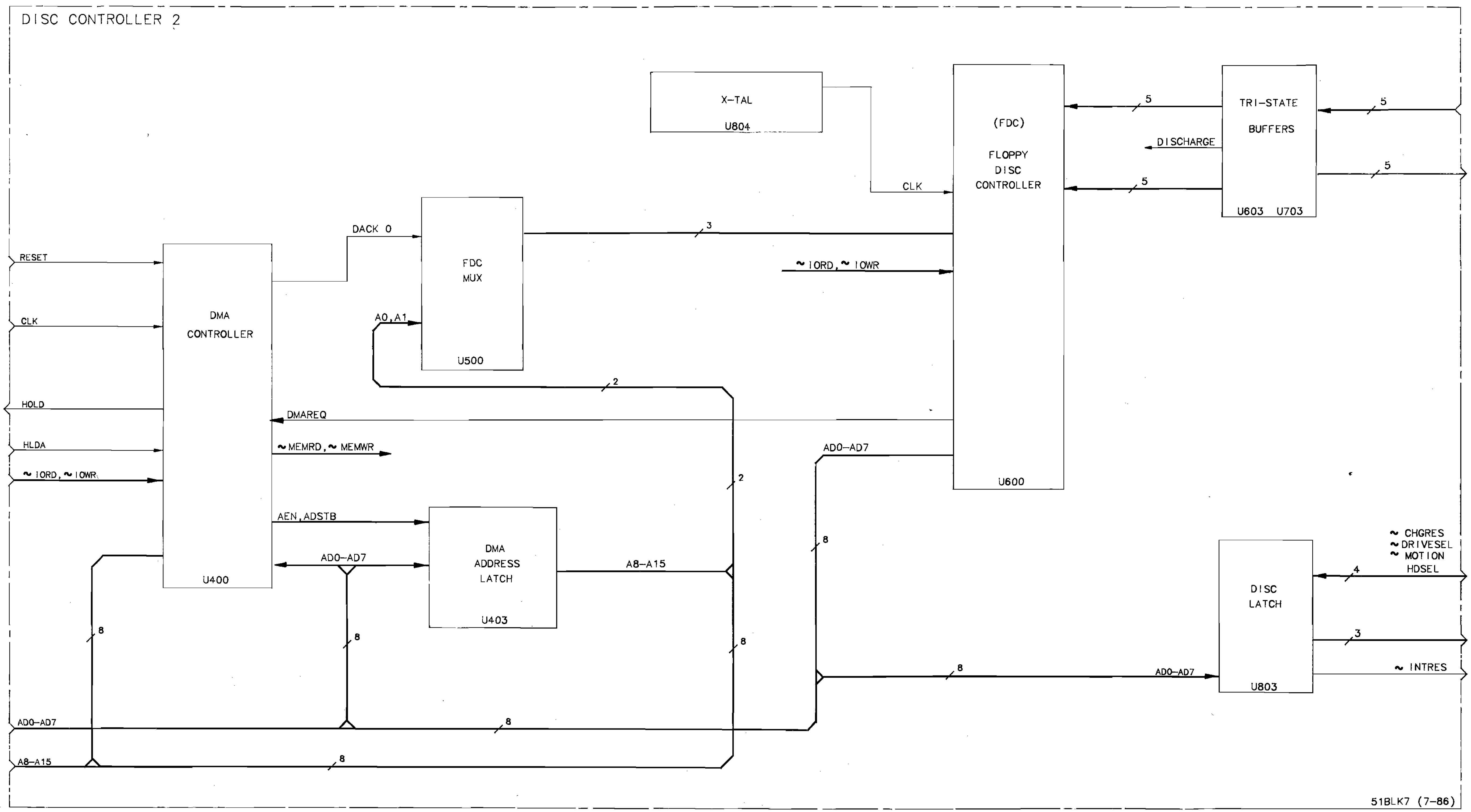


Figure 8-36. A3-2 Disc Controller Block Diagram

Power & Ground

Part #	+5	Gnd
U400	31	20
U403	20	10
U500	16	8
U600	21	20
U603	20	10
U703	20	10
U803	20	10
U804	14	7

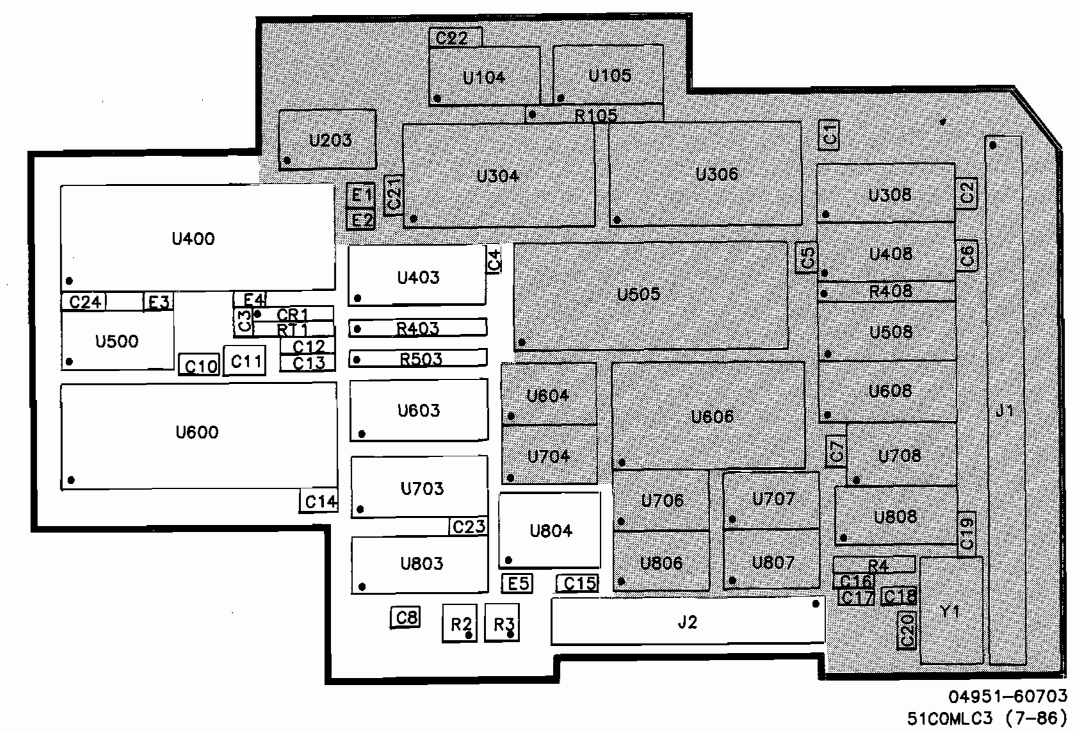


Figure 8-37. A3-2 Disc Controller Component Locator

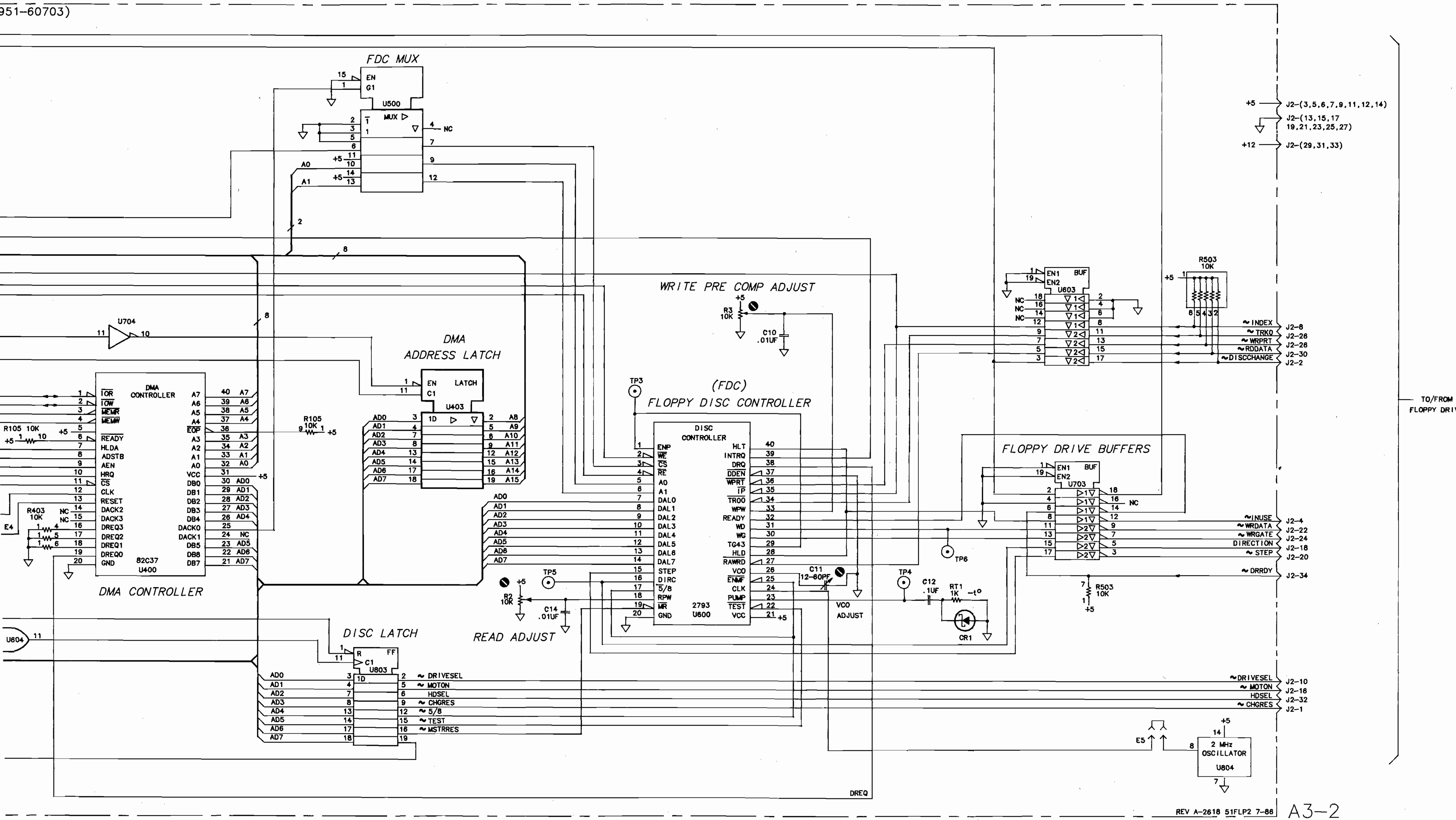
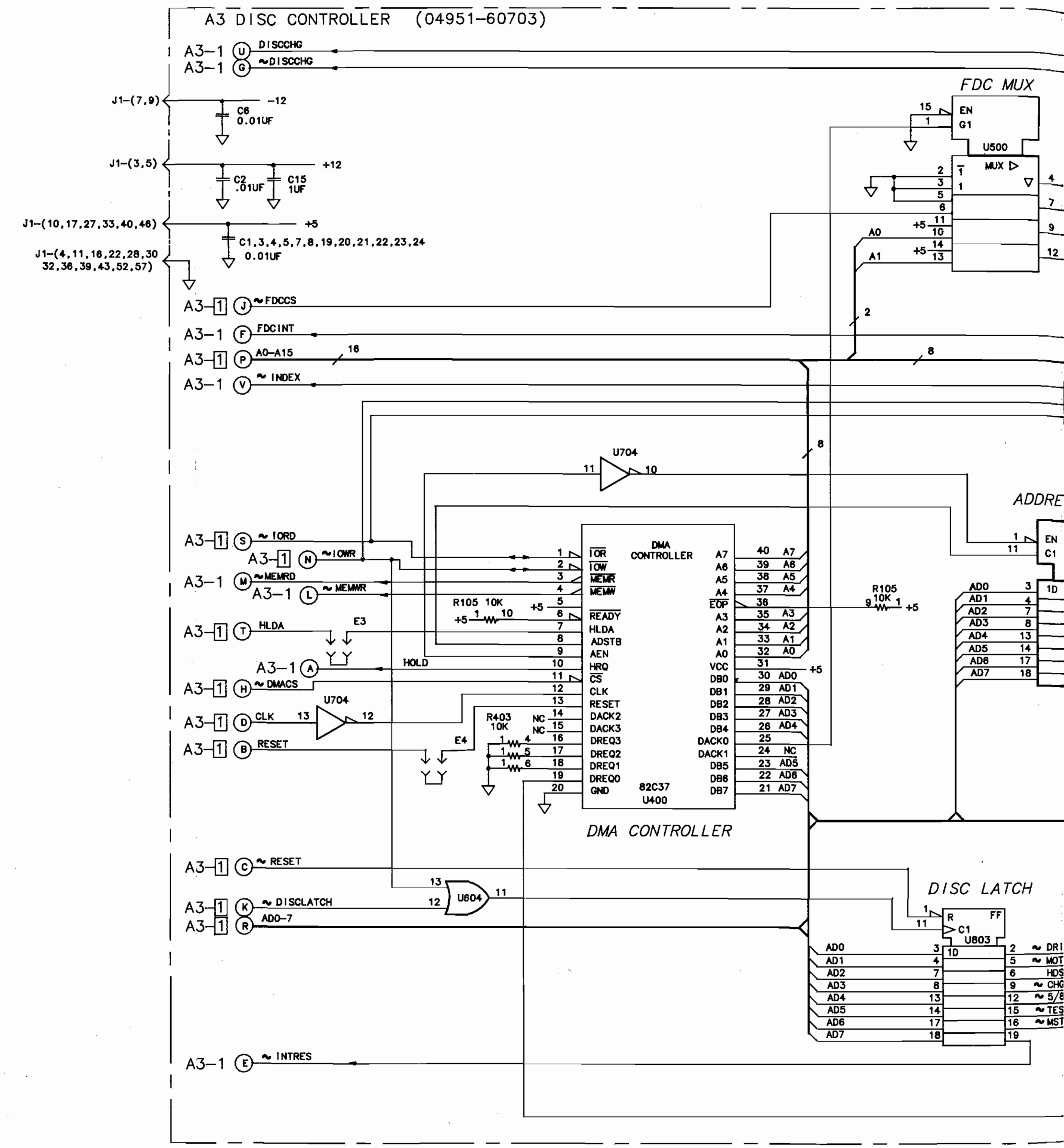


Figure 8-38. A3-2 Disc Controller Schematic Diagram


A3 DISC CONTROLLER (04951-60703)
FDC MUX
U500
MUX
DMA CONTROLLER
82C37
U400
U704
U604
ADDRE
DISC LATCH
U803
R105 10K
R403 10K
E3
E4
C6 0.01UF
C2 .01UF
C15 1UF
C1,3,4,5,7,8,19,20,21,22,23,24 0.01UF
J1-(7,9)
J1-(3,5)
J1-(10,17,27,33,40,46)
J1-(4,11,16,22,28,30 32,36,39,43,52,57)
DISCCHG
~DISCCHG
~FDCCS
FDCINT
A0-A15
~ INDEX
~ IORD
~IOWR
~MEMRD
~ MEMWR
HLDA
HOLD
~ DMACS
CLK
RESET
~ RESET
~ DISCLATCH
AD0-7
~ INTRES

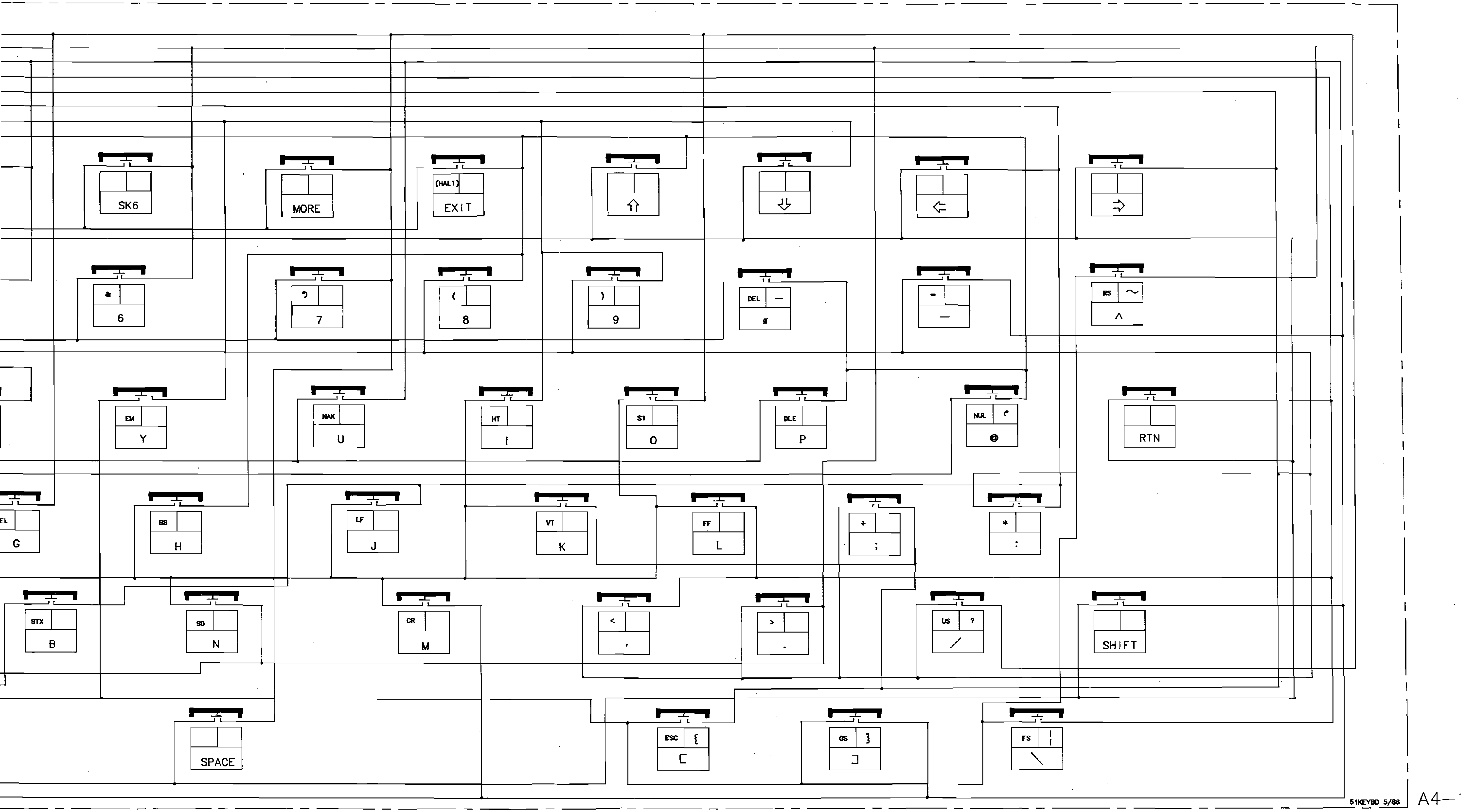
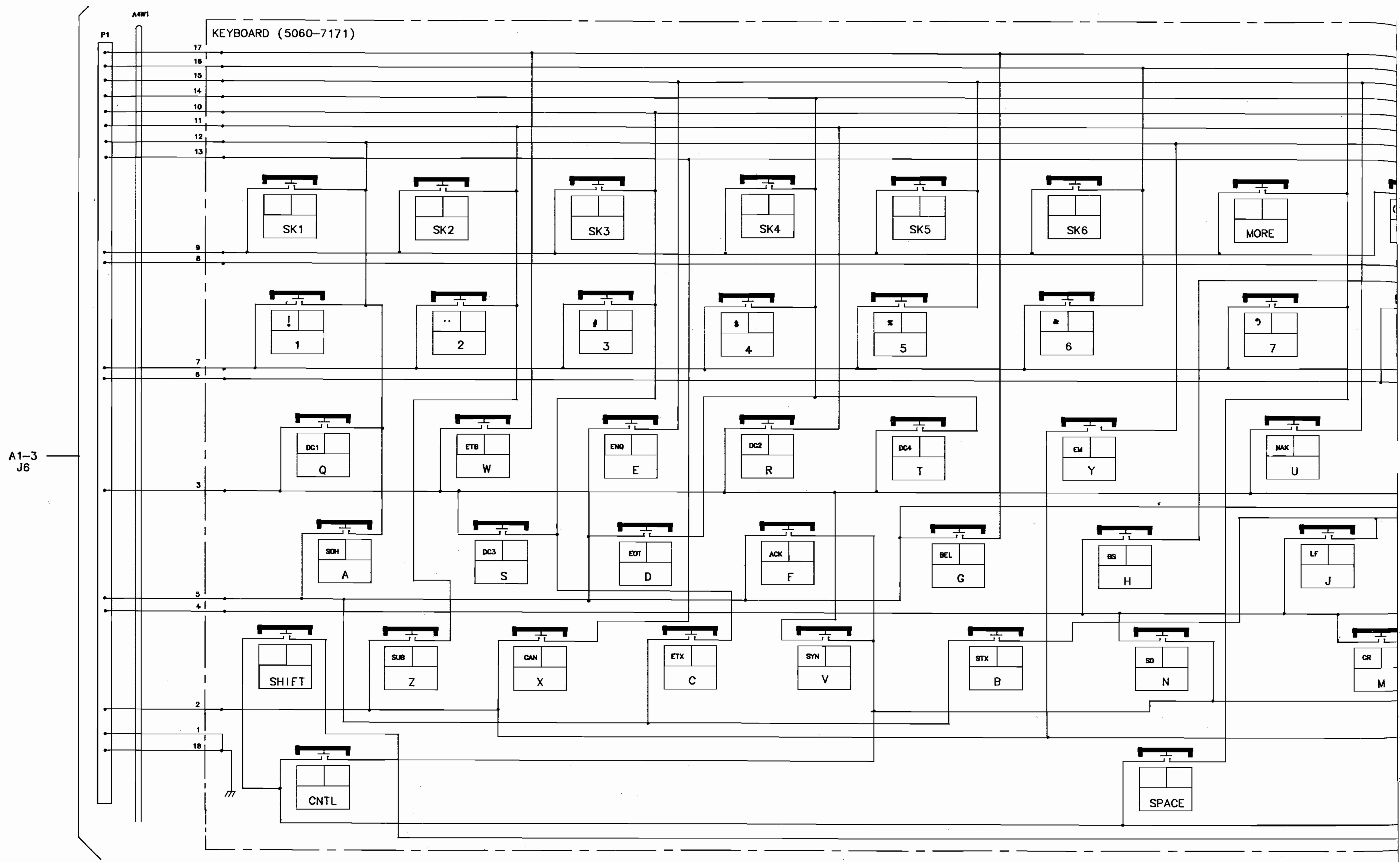


Figure 8-39. A4-1 Keyboard Schematic Diagram



A1–3
J6
P1
A4W1
KEYBOARD (5060–7171)
SK1
SK2
SK3
SK4
SK5
SK6
MORE
1
2
3
4
5
6
7
DC1
Q
ETB
W
ENQ
E
DC2
R
DC4
T
EM
Y
NAK
U
SOH
A
DC3
S
EOT
D
ACK
F
BEL
G
BS
H
LF
J
SHIFT
SUB
Z
CAN
X
ETX
C
SYN
V
STX
B
SO
N
CR
M
CNTL
SPACE

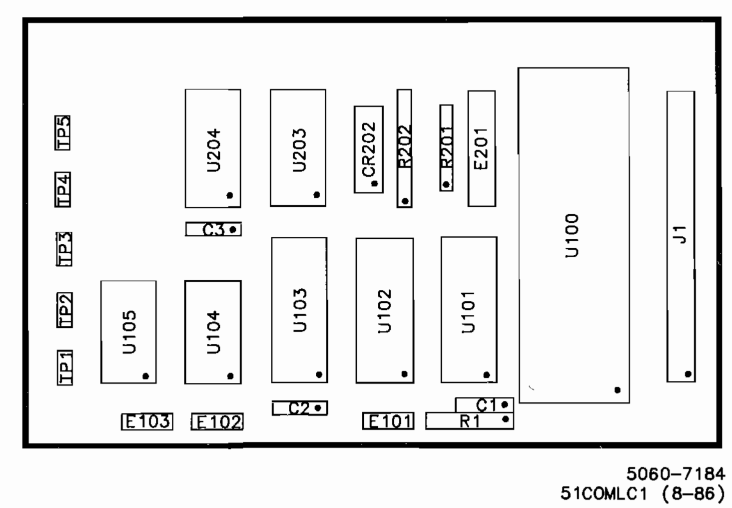


Figure 8-40. A30 Disc Controller Service Board Component Locator

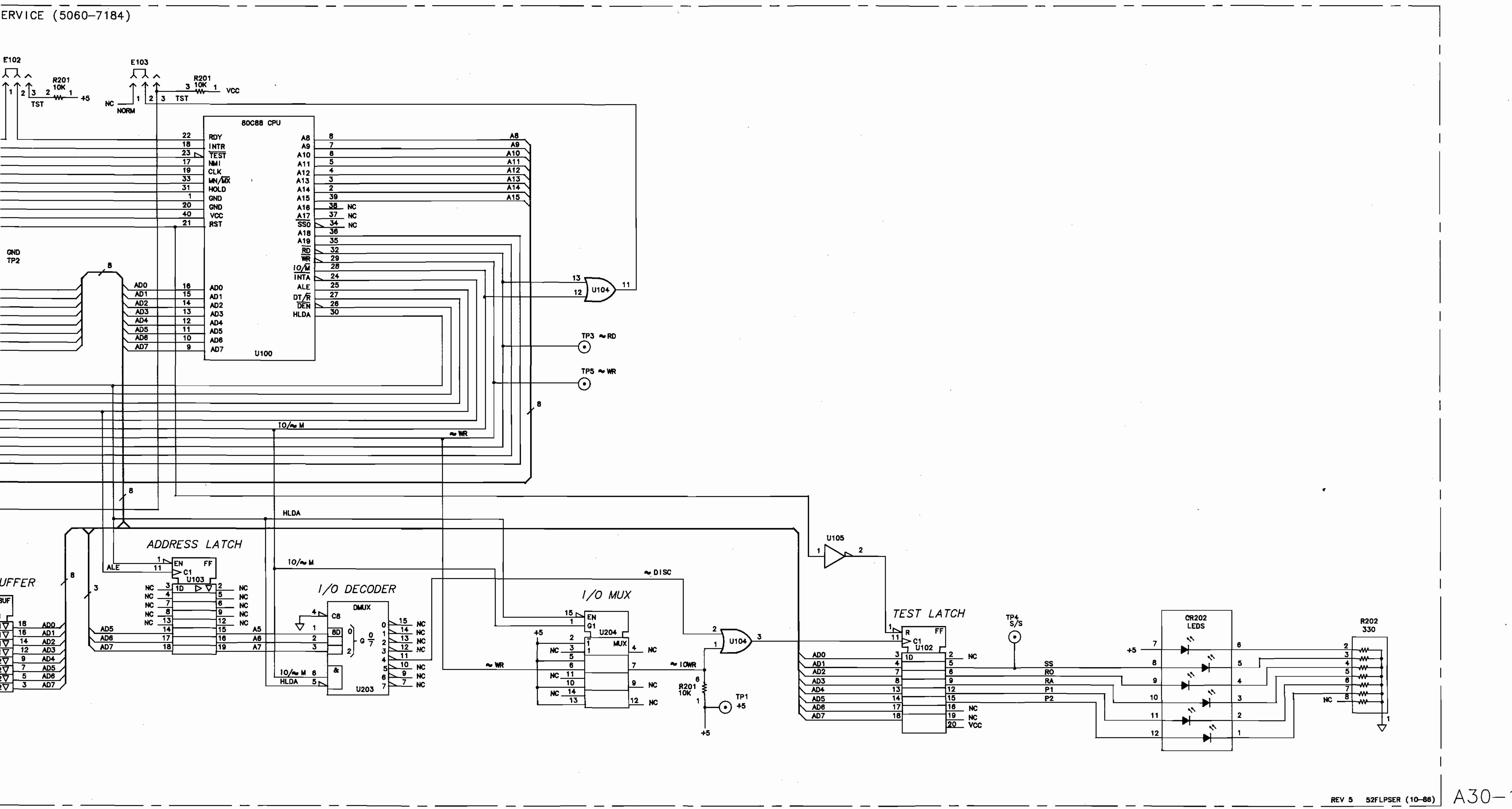


Figure 8-41. A30 Disc Controller Service Board Schematic Diagram

A30 DISC CONTROLLER SERVICE (5060-7184)

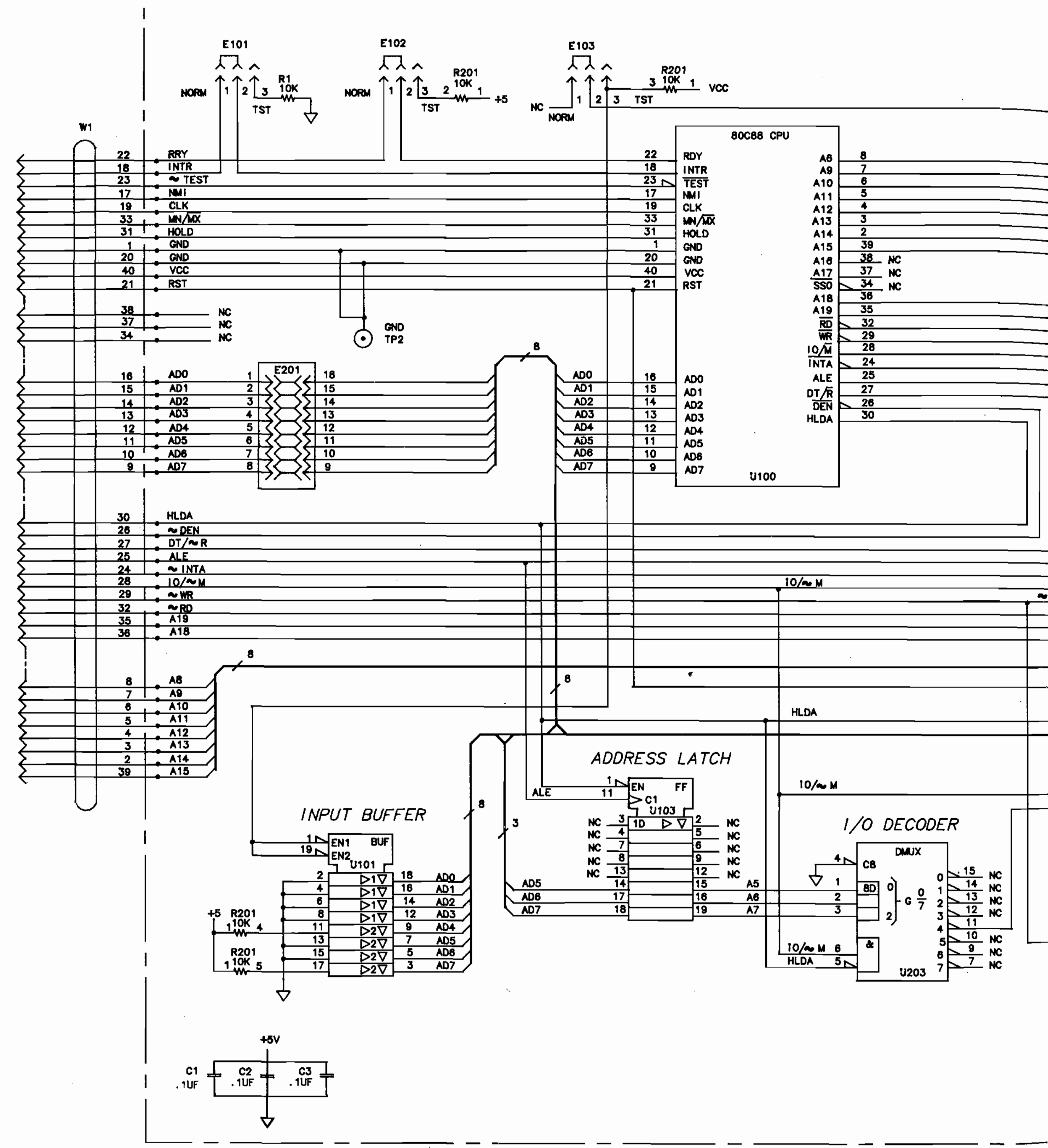


Table 8-6. A30 Disc Service Board Part Numbers

REF. DES.	HP PART NUMBER	QTY	DESCRIPTION
C1,C2,C3	0160-5332	3	CAP .1UF 20% 50V
PCB Legs	0380-0772	4	SPCR-RVT-ON
R1	0757-0442	1	RF 10K 1% .125W
XW1	1200-0682	1	SKT-IC 40 CONT
XU100	1200-0998	1	ZIF SKT-IC 40 CONT
XE101,XE102,XE103	1251-4670	3	CONN-POST-3PIN
TP1,2,3,4,5	1251-5380	5	CONN-POST-2PIN
XE201	1251-8702	1	CONN-POST 2 X 8
E101,E102,E103	1258-0209	3	JUMPER 1 X 2
E201	1258-0218	1	JUMPER 2 X 8
R201	1810-0368	1	NET 10.0KOHM X 5
R202	1810-0747	1	NET-RES 330.0 X 7
U105	1820-2921	1	IC MM74HC04N
U103	1820-2998	1	IC MC74HC373N
U204	1820-3191	1	IC 74HC257
U104	1820-3298	1	IC 74HC32N
U102	1820-3399	1	IC MC74HC273N
U101	1820-3456	1	IC MM74HCT244N
U203	1820-4084	1	IC 74HC137N
U100	1820-4100	1	IC 80C88
CR202	1990-1157	1	LAMP MINATURE
RAW PCB	5020-5263	1	DISC SYS SER BD
W1	5060-7182	1	DISC SYS SER CBL

8-50. TROUBLESHOOTING THE DISC SYSTEM SERVICE ASSEMBLY

In the event that the Disc System Service Assembly fails, the following SA loops can be used to determine the fault with the assembly. A known good HP 4951C should be used for testing.

Reasons for suspecting the Disc System Service Assembly as being faulty:

A. Disc System will not function with the Disc System Service Assembly installed into the system.
B. Improper Vhigh signatures or no Vhigh signatures are obtainable. Several or all of the SA loops within the Disc Controller troubleshooting part of Section VIII are incorrect or not functioning properly.

Loop #1 -

This loop checks the no-op function of the Disc System Service Assembly. Cable continuity, CPU operation and no-ops generation circuitry can be verified.

Loop #2 -

This loop checks the Disc System Service Assembly circuitry used to generate the SA start/stop interval and the LED readout values.

Summation:

In both of the SA procedures mentioned above, the SA meter control signals are generated within a known good environment that resides on the A3 Disc Controller board. Fault mechanisms can then be located on the Disc System Service Assembly.

LOOP: #1 NO-OPS Check

PCA: Disc System Service Assembly

SETUP: Disc System Service Assembly installed. E201 on or off, E101 and E102 to T position, and E103 to N position. GND , E103 pin 3, T, to enable U101 NO-OP buffer. Use known good HP 4951C.

* - Totalized Signature (+/- 1 count)
A30 - Key Data

(Rev. 4.0)

		EDGE:	NODE:
SA MODE:	Norm		
START/STOP		+/+	A3U403-19 (A15)
QUAL			
CLOCK		-	A3U105-3 (~RD)
GROUND			A3 TP GND
VHIGH =	0001		● ○ ○ ○ ○ ○

U100-	1-	L		30-	L	U104-	11-	65536*
A30	2-	3827(A14)		31-	L	A30	12-	L
	3-	3C96(A13)		32-	65536*		13-	65536*
	4-	HAP7(A12)		33-	H			
	5-	1293(A11)		34-	L			
	6-	HPP0(A10)		35-	16* (A19)			
	7-	2H70(A9)		36-	16* (A18)			
	8-	HC89(A8)		37-	65520*(A17)			
	9-	H (A7)		38-	16* (A16)			
	10-	L (AD1)		39-	755P(A15)			
	11-	L (AD2)		40-	H	E103-	1-	65536*
	12-	H (AD3)				A30	2-	65536*
	13-	L (AD4)					3-	L (GND)
	14-	L (AD5)	U101-	1-	L			
	15-	L (AD6)	A30	3-	H			
	16-	L (AD7)		5-	L			
	17-	L		7-	L			
	18-	L		9-	H			
	19-	0FL0*		12-	L			
	20-	L		14-	L			
	21-	L		16-	L			
	22-	H		18-	L			
	23-	L		19-	L			
	24-	H						
	25-	65536*						
	26-	65536*						
	27-	L						
	28-	L						
	29-	H						

LOOP: #2 FDC Check

PCA: Disc System Service Assembly

SETUP: Using known good HP 4951C, set up FDC Loop. All jumpers on Service Assembly in N position. Remove A3E1 and A3E2.

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	A3U803-5
QUAL		
CLOCK	-	A3U105-3
GROUND		A3 TP GND
VHIGH = 90A3		●●○○●●

U100- A30	1-	L
	2-	P0H0
	3-	960P
	4-	60C3
	5-	P0H0
	6-	5H99
	7-	7F31
	8-	5711
	9-	1C70
	10-	3931
	11-	3C30
	12-	P526
	13-	677U
	14-	1FC8
	15-	U7H8
	16-	CHCP
	17-	L
	18-	90A3
	19-	0FL0*
	20-	L
	21-	L
	22-	H
	23-	L
	24-	H
	25-	0FL0*
	26-	0FL0*
	27-	910H
	28-	90F4
	29-	8034*
	30-	L
	31-	L
	32-	0FL0*
	33-	H
	34-	P119
	35-	0FL0*
	36-	0FL0*
	37-	7073
	38-	P0H0
	39-	P0C7
	40-	H
U203- A30	1-	8655
	2-	9H09
	3-	U8AF
	4-	L
	5-	L
	6-	90F4
	7-	0005*
	9-	0003*
	10-	H
	11-	0005*
	12-	0007*
	13-	H
	14-	9AU6
	15-	0003*
U204- A30	1-	90F4
	6-	8034*
	7-	0008*
	15-	L
U105- A30	1-	L
	2-	H

LOOP: #2 FDC Check (cont)

PCA: Disc System Service Assembly

SETUP: Using known good HP 4951C, set up FDC Loop. All jumpers on Service Assembly in N position. Remove A3E1 and A3E2.

* - Totalized Signature (+/- 1 count)

- Key Data

(Rev. 4.0)

SA MODE: Norm	EDGE:	NODE:
START/STOP	+/-	A3U803-5
QUAL		
CLOCK		A3U105-3
GROUND		A3 TP GND

VHIGH = 90A3

●●○○●●

U102-	1-	H	U103-	1-	L
A30	2-	6U31	A30	11-	0FL0*
	3-	CHCP		14-	3C30
	4-	U7H8		15-	8655
	5-	0001*		16-	9H09
	6-	L		17-	3931
	7-	1FC8		18-	1C70
	8-	677U		19-	U8AF
	9-	L			
	11-	0005*			
	12-	UU92	U104-	1-	0008*
	13-	P526	A30	2-	0005*
	14-	3C30		3-	0005*
	15-	UU92		11-	0FL0*
	16-	C749		12-	90F4
	17-	3931		13-	0FL0*
	18-	1C70			
	19-	UU92			

APPENDIX A
FUNCTIONAL PART DESCRIPTIONS

A-1. INTRODUCTION

The following pages in Appendix A describe some of the major parts that are used in the HP 4951C. They are intended to be used in conjunction with the Troubleshooting Diagnostics and Theory sections of the HP 4951C Service Manual.

A-2. CENTRAL PROCESSING UNIT (CPU)

INPUTS:	OUTPUTS:
XIN	XOUT
NMI	~BACK
RSTA	RSTOUT
RSTB	ALE
RSTC	~RD
~INTR	~WR
RSTIN	IO/~M
~BREQ	CLK
~WAIT	~INTA

BIDIRECTIONAL:

AD0-AD7
A8-A15

VCC = pin 40
GND = pin 20

Interrupt Lines - ~INTR, ~INTA, ~RSTA, ~RSTB, ~RSTC, and NMI
Control Lines - ~RD, ~WR, and ALE
DMA Lines - ~BREQ, ~BACK
Timing and Control Lines - IO/~M, ~RSTIN, RSTOUT

FUNCTIONAL DESCRIPTION:

The CPU is an 8-bit microprocessor. The 16-bit address bus is divided into a high-order 8-bit address bus that handles bits 8-15 of the address, and a low-order 8-bit multiplexed address/data bus that handles bits 0-7 of the address and bits 0-7 of the data. Outputs from the CPU (ALE, ~RD, and ~WR) indicate when a valid address or data is present on the bus. IO/~M indicates whether the ensuing cycle accesses memory or input/output.

The interrupt lines (NMI, ~INTR, ~RSTA, ~RSTB, ~RSTC) which are generated from peripheral devices cause the CPU to go to a restart setup. During an input or output instruction the CPU duplicates the lower half of the address (AD0-AD7) onto the upper half (A8-A15). The eight bits of address will stay on A8-A15 for the entire machine cycle.

FUNCTIONAL PIN DESCRIPTIONS:

~BREQ - Bus Request (Input, active Low) - The ~BREQ request is used when another device is requesting the system bus. When the ~BREQ is recognized, the request is acknowledged by the ~BACK output signal.

~NMI - Non-Maskable Interrupt (Input, active Low) - This non-maskable interrupt is the highest priority interrupt request line in the CPU system. NMI is generated from the power supply section of the 4951C and is used when a major interrupt is requiring immediate attention.

~RSTA, ~RSTB, ~RSTC - Restart Interrupts A,B,C (Input, active Low, level sensitive) - These interrupt lines are generated from the Memory Decode areas of the instrument and cause different interrupt routines in the system.

~INTR - Interrupt Request (Input, active Low, level sensitive) - This interrupt signal is generated from the 'SCC' area of the Memory Decode section.

~WAIT - Wait (Input, active Low) - The ~WAIT input will be accepted only during ~RD, ~WR, or ~INTA cycles, or immediately after an interrupt has been accepted by the CPU. The ~WAIT cycle continues until the ~WAIT input returns high.

~BACK - Bus Acknowledge (Output, active Low) - ~BACK indicates to the bus requesting device that the CPU bus and it's control signals are in the tri-state mode. The requesting device may then take control of the bus and it's control signals.

RSTOUT - Reset Out (Output, active High) - When RSTOUT is high it indicates that the CPU is being reset. This signal is normally used to reset the peripheral devices.

IO/~M - Input/Output/Memory (Output) - An active high on the IO/~M output signifies that the current cycle is relative to an input/output device. An active low on the IO/~M output signifies that the current cycle is relative to memory.

ALE - Address Latch Enable (Output) - The high to low transition of ALE indicates that a valid memory/IO address is available on the AD0-AD7 lines.

~RD - Read Strobe (Output, active Low) - On the trailing edge of the ~RD strobe, data is input to the CPU through the AD0-AD7 lines. The ~RD line is in the tri-state mode during ~BREQ/~BACK cycles.

~WR - Write Strobe (Output, active Low) - While the ~WR line is low, valid data is output by the CPU on the AD0-AD7 lines.

~INTA - Interrupt Acknowledge (Output, active Low) - The interrupt acknowledge output is activated immediately following the state in which the ~INTR input is recognized. The output is normally used to gate the interrupt response vector from the peripheral controller onto the AD0-AD7 lines.

CLK - Clock (Output) - CLK is an output provided for use as a system clock. The CLK output is a square wave at one half the input frequency.

~RSTIN - Reset Input (Input, active Low) - The ~RSTIN input is used with an R-C network to ensure proper power-up conditions for the CPU.

XIN, XOUT - These two pins are used to create necessary timing signals.

A8-A15 - Address/Data Bits (Bidirectional, active High) - A8-A15 are the most significant 8 bits of the memory address during a memory instruction. During an I/O instruction, the port address on the lower 8 bits of address get duplicated onto these 8 bits.

AD0-AD7 - Address/Data Bits (Bidirectional, active High) - At ~RD cycles these lines input data to the CPU. During ~WR cycles, they output data from the CPU.

A-3. SERIAL COMMUNICATIONS CONTROLLER (SCC)

INPUTS:

PCLK
IEI
~CE
~RD
~WR
D/~C
A/~B
~INTACK
RXDA,RXDB
~RTXCA,~RTXCB
~CTSA,CTSB
~DCDA,DCDB

OUTPUTS:

~INT
TXDA
TXDB
~RSTA
~DTRA
~DTRB

BIDIRECTIONNAL:

AD0-AD7
SYNCA,SYNCB
TRXCA,TRXCB

VCC = pin 9
GND = pin 31

FUNCTIONAL DESCRIPTION:

The SCC is programmed by the CPU as an I/O device. It is capable of supporting full duplex transmit and receive operations. It can also drive and/or monitor various physical interface leads. The SCC generates an interrupt to the CPU whenever the status of the interface changes or when it requires servicing. Upon receiving an interrupt acknowledge, the SCC will generate one of eight vectors that describes the nature of the interrupt by pointing to the appropriate service routine. The SCC has an on-board baud rate generator (BRG) which uses a 4.032 MHz clock and a 16-bit programmable divider to generate common baud rates to +/- .003% of nominal. The BRG can be used for asynchronous or synchronous clock generation. Transmit and receive clock sources for the SCC must be programmed to reflect the test to be performed. This information is also obtained from the Set-up Menu.

FUNCTIONAL PIN DESCRIPTIONS:

A/~B - Channel A/Channel B Select (Input). This signal selects the channel in which the read or write operation occurs.

~CE - Chip Enable (Input, active low). This signal selects the SCC for a read or write operation.

~CTSA, ~CTSB - Clear to Send (Inputs, active low). A low on these inputs enables their respective transmitters.

D/~C - Data/Control Select (Input). This signal defines the type of information transferred to or from the SCC. A high means data is transferred, a low indicates a command.

~DCDA,~DCDB - Data Carrier Detect (Inputs, active low). These pins function as receiver enables.

D0-D7 - Data Bus (bidirectional, 3-state). These lines carry data and commands to and from the SCC.

~DTRA,~DTRB - Data Terminal Ready/Request (Outputs, active low). These outputs follow the state programmed into the DTR bit. They can also be used as general-purpose outputs or as request lines for a DMA controller.

IEI - Interrupt Enable In (input, active high). A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

~INT - Interrupt Request (output, active low). This signal is activated when the SCC requests an interrupt.

~INTACK - Interrupt Acknowledge (Input, active low). This signal indicates an active interrupt acknowledge cycle. During this cycle, the SCC interrupt settles. When ~RD becomes active, the SCC places an interrupt vector on the data bus (if IEI is high). ~INTACK is latched by the rising edge of PCLK.

PCLK - Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal.

~RD - Read (input, active low). This signal indicates a read operation and when the SCC is selected, enables the SCC's bus drivers. During the interrupt acknowledge cycle, this signal gates the interrupt vector onto the bus if the SCC is the highest priority device requesting an interrupt.

RXDA, RXDB - Receive Data (Inputs, active high). These input signals receive serial data at standard TTL levels.

~RTXCA, ~RTXCB - Receive/Transmit Clocks (Inputs, active low). These pins can be programmed in several different modes of operation. In each channel, RTXC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in Asynchronous modes.

~RTSA, ~RTSB - Request to Send (outputs, active low). When the request to send bit in the write register 5 is set, the ~RTS signal goes low. When the RTS bit is reset in the asynchronous mode and Auto Enable is on, the signal goes high after the transmitter is empty. In synchronous mode or in asynchronous mode with Auto Enable off, the RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

~SYNCA, ~SYNCB - Synchronization (Inputs, active low). These pins can act either as inputs or outputs. In the asynchronous receive mode these pins are inputs similar to ~CTS and ~DCD. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in the Read Register 0 but have no other function. In external synchronous mode these lines also act as inputs. In this mode, ~SYNC must be driven low for two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of ~SYNC.

TXDA, TXDB - Transmit Data (Outputs, active high). These output signals transmit serial data at standard TTL levels.

~TRXCA, ~TRXCB - Transmit/Receive Clocks (Inputs or outputs, active low). These pins can be programmed in several different modes of operation. ~TRXC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

<u>**~WR**</u> - Write (Input, active low). When the SCC is selected, this signal indicates a write operation. The coincidence of ~RD and ~WR is interpreted as a reset.

<u>**AD0-AD7**</u> - Address/Data Bus (Bidirectional) - These lines carry register addresses to the SCC as well as data or control information to and from the SCC.

A-4. CRT CONTROLLER (CRTC)

INPUTS:	OUTPUTS:
~RESET	VS
RS	HS
R/W	DE
~CS	MA0-MA10
E	RA0-RA3
CLK	

BIDIRECTIONAL:

AD0 - AD7

VCC = 20
GND = 1

FUNCTIONAL DESCRIPTION:

The CRT Controller generates the signals necessary to interface a digital system to a raster scan CRT display. The processor communicates with the CRT Controller through a 8-bit data bus by reading or writing into the registers. All timing in the CRT Controller is derived from the CLK input. Internal CRTC registers are programmed by the processor through the data bus (AD0-AD7) and the control signals (R/~W, ~CS, RS, and E). The CRT Controller generates the refresh address (MA0-MA10), row address (RA0-RA3), and the video timing (VS, HS, and DE).

FUNCTIONAL PIN DESCRIPTIONS:

AD0-AD7 - Data Bus (Bidirectional) - These lines allow data transfers between the internal CRTC register file and the processor.

E - Enable (Input) - The enable signal is an input which enables the data bus input/output buffers and clocks data to and from the CRTC.

~CS - Chip Select (Input, active Low) - The Chip Select line is the input which selects the CRTC to read or write to the internal register file. This signal should be active only when there is a valid address being decoded from the processor.

RS - Register Select (Input) - The Register Select line is an input which selects the address register, one of the data registers, or the internal register file.

R/~W - Read/Write (Input) - The Read/Write line is the input which determines whether the internal register file is written or read. A write signal is defined as a low level, a read signal is defined as a high level.

VS, HS - Vertical Sync and Horizontal Sync (outputs, active High) - These outputs are active high signals which go to the video processing circuitry to generate a composite video signal. The VS signal determines the vertical position of the displayed text while the HS signal determines the horizontal position of the displayed text.

DE - Display Enable (Output, active High) - The Display Enable output is an active high signal which indicates the CRTC is providing addressing in the active display area.

MA0-MA10 - Refresh Memory Address (Outputs) - These outputs are used to refresh the CRT screen with pages of data located within a block of refresh memory.

RA0-RA3 - Row Address (Outputs) - These outputs from the internal row address counter are used to address the character Rom.

CLK - Clock (Input) - The Clock input is used to synchronize all CRT functions except for the processor interface.

A-5. DIRECT MEMORY ACCESS CONTROLLER (DMAC)

INPUTS:	OUTPUTS:
~READY	~MEMR
HLDA	~MEMW
~CS	ADSTB
CLK	AEN
RESET	HRQ
DREQ0	~EOP
	DACK0
	A4-A7

BIDIRECTIONAL:

A0-A3
DB0-DB7
~IOR
~IOW

VCC = 31
GND = 20

FUNCTIONAL DESCRIPTION:

The Direct Memory Access Controller is a peripheral interface circuit designed to allow external devices to directly transfer information to or from the system memory. The DMA Controller operates in two major cycles. They are called Idle and Active. When no channel is requesting service, the DMA Controller will enter the idle cycle. In this mode, the DMA Controller will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample the Chip Select line, looking for an attempt by the microprocessor to write or read the internal registers of the DMA Controller. ~IOR and ~IOW lines are used to select and time read or write operations. When the DMA Controller is in the idle cycle and a channel requests a DMA service, the device will output a Hold Request (HRQ) to the microprocessor and enter the active cycle. It is in this cycle that the DMA service will take place. Write transfers move data from and I/O device to the memory by activation ~MEMW and ~IOR. Read transfers move data from memory to an I/O device by activating ~MEMR and ~IOW. To perform block moves of data from one memory address to another with a minimum of program effort and time, the DMA Controller is capable of a memory to memory transfer.

FUNCTIONAL PIN DESCRIPTION:

CLK - Clock (Input) - This input controls the internal operations of the DMA Controller.

~CS - Chip Select (Input, active Low) - The Chip Select line is an input used to select the DMA Controller as an I/O device during the idle cycle. This allows CPU communication on the data bus.

RESET - Reset (Input, active High) - Reset is an input which clears the Command, Status, Request, and Temporary Registers. Following a Reset the device is in an idle cycle.

~READY - Ready (Input) - Ready is an input used to extend the memory read and write pulses from the DMA Controller to accommodate slow memories or input/output devices.

HLDA - Hold Acknowledge (Input, active High) - The Hold Acknowledge signal from the CPU indicates that control of the system buses has been relinquished.

DREQ0-DREQ3 - DMA Request (Inputs) - The DMA Request lines channel request inputs to obtain DMA service. A request is generated by activating the DREQ line. DACK will acknowledge the recognition of a DREQ signal. RESET initializes the DREQ lines to active high. DREQ must be maintained until the DACK line goes active.

DB0-DB7 - Data Bus (Bidirectional) - The data bus lines are connected to the system data bus. The outputs are enabled in the program condition during the I/O Read cycle to output the contents of a register to the CPU. The inputs are read during an I/O write cycle when the CPU is programming the DMA control registers. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB.

~IOR - I/O Read (Bidirectional, active Low) - I/O Read, in the idle cycle, is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the DMA Controller to access data from a peripheral device during a DMA write transfer.

~IOW - I/O Write (Bidirectional, active Low) - In the idle cycle, I/O Write is an input control signal used by th CPU to load information into the DMA Controller. In the active cycle, it is an output control signal used by the DMA controller to load data to the peripheral device during a DMA Read transfer.

~EOP - End of Process (Bidirectional, active Low) - The DMA Controller allows an external signal to terminate an active DMA service. This is accomplished by pulling the ~EOP input low with an external signal.

A0-A3 - Address (Bidirectional) - In the idle cycle these lines are inputs and are us by the DMA Controller to address the control register to be loaded or read. In the active cycle, they are outputs and provide the lower 4 bits of the output address.

A4-A7 - Address (Outputs) - A4 through A7 are the most significant bits of the output address. These lines are enabled only during the DMA service.

HRQ - Hold Request (Output) - This line is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of a valid DREQ causes the DMA Controller to issue the Hold Request.

DACK0-DACK3 - DMA Acknowledge (Output) - DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. Reset initializes the DACK lines to active low.

AEN - Address Enable (Output, active High) - This output enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers.

ADSTB - Address Strobe (Output, active High) - The Address Strobe is used to strobe the upper address byte into an external latch.

~MEMR - Memory Read (Output, active Low) - The Memory Read signal is an output used to access data from the selected memory location during a DMA Read or a memory to memory transfer.

~MEMW - Memory Write (Output, active Low) - The Memory Write signal is an output used to write data to the selected memory location during a DMA Write or a memory to memory transfer.

A-6. I/O-TIMER (NSC810)

INPUTS:

CE
IO/~M
~WR
~RD
ALE
T0IN
T1IN
RESET

OUTPUTS:

T0OUT
T1OUT

BIDIRECTIONAL:

AD0-AD7
PA0-PA7
PB0-PB7
PC0-PC3

VCC = 40
GND = 20

FUNCTIONAL DESCRIPTION:

The NSC810 is an I/O-Timer device that interfaces with the CPU. The NSC810 contains address/data bus latches that latch the address input/output at the falling edge of the ALE input signal when CE is high. Data is then directed according to the other control signals: IO/~M, ~RD, or ~WR. Six control signals, furnished by the CPU, effect the functions of the NSC810. The memory is comprised of 1024 bits of Static Ram organized as 128 x 8. The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or an output. The port bits can be set or cleared individually and can be written or read in bytes. The memory portion of the NSC810 is accessed by a 7-bit address input to pins AD0-AD6. The IO/~M input must be low and the CE input must be high at the falling edge of ALE to address the RAM.

FUNCTIONAL PIN DESCRIPTIONS:

RESET - Reset (Input) - Reset is an active high input that resets all registers to a low state.

IO/~M - Input/output Timer or Ram Select (Input) - IO/~M is an input/output memory select line. A high input selects the I/O Timer portion of the chip; a low input selects the RAM portion of the chip. IO/~M is latched at the falling edge of ALE.

CE - Chip Enable (Input) - CE is an active high input that allows access to the NSC810. CE is latched at the falling edge of ALE.

~RD - Read (Input) - ~RD is an active low input that enables a read operation of the RAM or I/O Timer locations.

~WR - Write (Input) - ~WR is an active low input that enables a write operation to RAM or I/O Timer locations.

ALE - Address Latch Enable (Input) - The falling edge of the ALE input latches AD0-AD7, CE, and IO/~M inputs to form the address for the RAM, I/O, or Timer.

T0IN, T1IN - Timer 0,1 Input (Inputs) - T0IN and T1IN are the clock inputs for Timer 0 and Timer 1.

T0OUT, T1OUT - Timer 0,1 Output (Outputs - T0OUT and T1OUT are the programmable outputs of Timers 0 and 1.

AD0-AD7 - Address/Data Bus (Bidirectional) - AD0-AD7 will latch address inputs at the falling edge of ALE. A ~WR input enables the 8-bit data to be written into the addressed location. The ~RD input enables the 8-bit data to be read from the addressed location. The ~RD or ~WR inputs occur while ALE is low.

PA0-PA7 - Port A, 0-7 (Bidirectional) - Port A is an 8-bit basic mode input/output port.

PB0-PB7 - Port B, 0-7 (Bidirectional) - Port B is an 8-bit basic mode input/output port.

PC0-PC3 - Port C, 0-3 (Bidirectional) - Port C is a 4-bit basic mode input/output port. Each pin has a programmable second function as follows:

PC0 - Port C/Interrupt - PC0 is an active low strobed mode interrupt request to the CPU.
PC1 - Port C/BF - PC1 is an active high buffer full output to peripheral devices.
PC2 - Port C/~STB - PC2 is an active low strobe input from peripheral devices.
PC3 - Port C/TG - PC3 is the timer gating signal.

A-7. ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

INPUTS:	OUTPUTS:
E	~IRQ
R/~W	TxDATA
CS0	~RTS
CS1	
~CS2	
RS	
TxCLK	
RxCLK	
RxDATA	
~CTS	
~DCD	

BIDIRECTIONAL:

D0-D7

VCC = 12
GND = 1

FUNCTIONAL DESCRIPTION:

The Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to a bus organized system. The bus interface of the ACIA includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface with proper formatting and error checking. A programmable control register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided.

FUNCTIONAL PIN DESCRIPTION:

D0-D7 - Data Bus (Bidirectional) - D0-D7 is the data bus that allows the transfer of data between the ACIA and the CPU.

E - Enable (Input) - Enable is the input that enables the input/output data buffers and clocks data to and from the ACIA.

R/~W - Read/Write (Input) - The R/~W line is an input used to control the direction of data through the ACIA's I/O data bus interface. When R/~W is high, the output drivers are turned on and a selected register is read. When R/~W is low, the output drivers are turned off and data is written into a selected register.

CS0, CS1, ~CS2 - Chip Select 0-2 (Inputs) - The CS lines are used to address the ACIA. It is selected when CS0 and CS1 are high and CS2 is low. Transfers of data to and from the ACIA are then performed under the control of E, R/~W, and RS.

RS - Register Select (Input) - The RS line is used to select one of four internal registers. A high is used to select the Transmit/Receive Data Registers and a low selects the Control/Status Registers. The R/~W line is used with the Register Select line to select the read-only or write-only register in each register pair.

IRQ - Interrupt Request (Output) - The Interrupt Request line is used to interrupt the main processor unit. A low on this line will remain as long as the cause of the interrupt is present.

TxCLK - Transmit Clock (Input) - The TxCLK input is used for the clocking of transmitted data. The TxCLK initiates data on the negative transition of the clock.

RxCLK - Receive Clock (Input) - The RxCLK input is used for synchronization of received data. The RxCLK samples the data on the positive transition of the clock.

RxData - Receive Data (input) - The RxData line is an input through which data is received on a serial format.

TxData - Transmit Data (Output) - The TxData line transfers serial data to a modem or other peripheral device.

~CTS - Clear to Send (Input) - The Clear to Send input provides automatic control of the transmitting end of a communications link when a low input is detected from the modem or other peripheral.

~RTS - Request to Send (Output) - The ~RTS output enables the main processor to control a peripheral or modem via the data bus.

~DCD - Data Carrier Detect (Input) - The ~DCD signal is used to control the receiving operation . When ~DCD goes high, the ACIA stops all receiving operations. When ~DCD goes low, the receiving part is allowed to receive data.

A-8. 80C88 MICROPROCESSOR

INPUTS:	OUTPUTS:
RDY	HLDA
INTR	A8-A15,A18,A19
~TEST	~RD
NMI	~WR
CLK	IO/~M
RST	~INTA
MN/~MX	ALE
HOLD	DT/~R
	~DEN

BIDIRECTIONAL:

AD0-AD7

VCC = 40
GND = 1,20

FUNCTIONAL DESCRIPTION:

The 80C88 Microprocessor is an eight bit microprocessor which can operate in two modes: minimum mode or maximum mode. The 80C88 has a twenty bit address bus with the lower eight bits of the address bus multiplexed with the eight bit data bus. The upper four address bits are also time multiplexed. The HOLD input is used to request access of the 80C88 buses. Control outputs from the microprocessor indicate read and write memory or I/O cycles. There is also an interrupt acknowledge, and a signal which indicates that the 80C88 has relinquished control of it's address and data buses.

FUNCTIONAL PIN DESCRIPTION:

AD0-AD7 - Address Data Bus (Inputs/Outputs) - The Address/Data Bus makes up the Memory/IO address and data bus. These lines are active high.

A8-A15 - Address Bus (Outputs) - These lines provide address bits 8 through 15 for the entire bus cycle. These lines are active high and do not have to be latched by ALE to remain valid.

A18, A19 - Address/Status (Outputs) - A18 and A19 are the most significant address lines for memory operations. During I/O operations, these lines are low. During memory and I/O operations, status information is available on these lines.

~RD - Read (Output) - This signal is used to read devices which are connected to the 80C88 bus. ~RD is active low and indicates that the processor is performing an I/O or Memory Read cycle, depending on the state of IO/~M.

~WR - Write (Output) - The Write line is an active low signal which indicates the processor is performing a write memory or a write I/O, depending on the state of IO/~M.

RDY - Ready (Input) - The Ready line is an active high signal that is the acknowledgment from the addressed memory or an I/O device that it will complete the data transfer.

INTR - Interrupt Request (Input) - The Interrupt Request line is an active high signal which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation.

~TEST - Test (Input) - ~Test is an active low input. When the ~Test line is low, execution of the processor continues.

NMI - Non-Maskable Interrupt (Input) - The NMI line is an active high signal that initiates an interrupt at the end of the current instruction.

RST - Reset (Input) - Reset is an active high input that causes the processor to immediately terminate it's present activity.

CLK - Clock (Input) - The clock input provides the basic timing for the processor and the bus controller. It functions with a 33% duty cycle to provide optimized internal timing.

MN/~MX - Minimum/Maximum (Input) - MN/MX indicates what mode the processor is to operate in. If the MN/MX line is high (VCC), it is operating in the minimum mode. If the MN/MX line is low (GND), the processor is operating in the maximum mode.

IO/~M - Input-Output/Memory (Output) - The IO/~M is used to distinguish a memory access from an I/O address. If the IO/~M input is high, an I/O cycle is selected. If IO/~M is low, a Memory cycle is selected.

~INTA - Interrupt Acknowledge (Output) - Interrupt Acknowledge is an active low output that is used as a read strobe with Interrupt Request.

ALE - Address Latch Enable (Output) - The ALE line is an active high signal that is used to latch the address into an address latch.

DT/~R - Data Transmit/Receive (Output) - The DT/~R line is used to control the direction of the data flow through the transceiver. If DT/~R is high, the data is being transmitted. If DT/~R is low, the data is being received.

~DEN - Data Enable (Output) - The ~DEN line is an active low signal that is used for an output enable for the transceiver.

HOLD, HLDA - Hold (Input,Output) - Hold is an active high signal which indicates that a bus "HOLD" is being requested. The processor receiving the HOLD request will issue a "HLDA" (hold acknowledge). After HOLD is detected as being low, the processor lowers HLDA, and then the processor will again drive the bus and control lines.

A-9. FLOPPY DISC CONTROLLER

INPUTS:	OUTPUTS:
ENP	STEP
~WE	DIRC
~CS	INTRQ
A0	DRQ
A1	WD
~5/8	WG
RPW	TG43
~MR	HLD
~DDEN	PUMP
~WPRT	
~IP	
~TR00	
WPW	
READY	
~RAW RD	
VCO	
~ENMF	
CLK	
~TEST	

BIDIRECTIONAL:

AD0-AD7

VCC = 21
GND = 20

FUNCTIONAL DESCRIPTION:

The Floppy Disc Controller handles commands for data transfer to and from the floppy disc. It controls the head move commands required for the operation of the floppy drive. The Floppy Disc Controller has two modes of operation: single density or double density. When operating in double density mode, Write precompensation is automatically engaged to a selected value from an external potentiometer. The FDC interface consists of an 8-bit bidirectional bus for data, status, and control word transfers.

FUNCTIONAL PIN DESCRIPTION:

ENP - Enable Precompensation (Input) - Then the ENP signal is high, this input enables the write precompensation to be performed on the Write Data output.

~MR - Master Reset (Input) - When the ~MR line is low it resets the device. When the ~MR line is high a Restore command is executed.

~WE - Write Enable (Input) - The Write Enable line is an input that when low gates data on the address/data bus if the Chip Select line is low.

~CS - Chip Select (Input) - The Chip Select line is an active low signal that selects the chip and enables communication with the device.

~RE - Read Enable (Input) - The Read Enable line is an active low input that controls the placement of data from a selected register on the address/data bus when ~CS is low.

A0, A1 - Register Select Lines (Inputs) - These inputs select the register to receive or transmit data on the address/data lines in conjunction with ~RE and ~WE.

AD0-AD7 - Address/Data Bus (Bidirectional) - AD0-AD7 are the address/data lines used in the Disc Controller. These bidirectional active high signals are used for the transfer of commands, status, and data.

CLK - Clock (Input) - This input requires a free running 50% duty cycle square wave clock for internal timing reference.

DRQ - Data Request (Output) - This active high output indicates that the Data Register contains assembled data in Read operations, or the Data Register is empty in Write operations.

INTRQ - Interrupt Request (Output) - This output is set at the completion of any command when the Status Register is read from, or the Command Register is written to.

STEP - Step (Output) - The Step output contains a pulse for each step.

DIRC - Direction (Output) - The Direction signal is an output which when high causes the disc to step in, and when low, step out.

~5/8 - 5 1/4", 8" Select (Input) - This input selects the internal VCO frequency for use with 5 1/4" or 8" drives.

RPW - Read Pulse Width (Input) - An external potentiometer tied to this input controls the phase comparator within the data separator.

~TEST - Test (input) - The ~Test input is an active low signal that allows adjustment of external resistors by enabling internal signals to appear on selected pins.

PUMP - Pump (Output) - The Pump output is a signal which is forced high or low to increase or decrease the VCO frequency.

~ENMF - Enable Mini-Floppy (Input) - A logic low on this input enables an internal ÷2 of the Master Clock when ~5/8 is also at a logic 0. This allows both 5 1/4" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a high level.

VCO - Voltage-Controlled oscillator (Input) - An external capacitor tied to this pin adjusts the VCO center frequency.

~RAW RD - Raw Read (Input) - This input is a negative pulse for each recorded flux transition.

HLD - Head Load (Output) - The HLD output controls the loading of the Read/Write head against the media.

TG43 - Track Greater Than 43 (Output) - This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write commands.

WG - Write Gate (Output) - This output is made valid before writing is to be performed on the disc.

WD - Write Data (Output) - a 250ns (MFM) or 500ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.

READY - Ready (Input) - This input indicates disc readiness and is sampled for a high level before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type 1 operations are performed regardless of the state of Ready.

WPW - Write Precomp Width (Input) - An external potentiometer tied to this input controls the amount of delay in Write Precompensation mode.

~TR00 - Track 00 (Input) - This input informs the Floppy Disc Controller that the Read/Write head is positioned over Track 00.

~IP - Index Pulse (Input) - This input informs the Floppy Disc Controller when the index hole is encountered on the disc.

~WPRT - Write Protect (Input) - This input is sampled whenever a Write command is received. A low input terminates the command and sets the Write Protect Status Bit.

~DDEN - Double Density (Input) - This input pin selects either single or double density operation. When ~DDEN is low, Double Density is selected. When ~DDEN is high, single density is selected.

HLT - Head Load Timing (High) - When a logic high is found on the HLT input the head is assumed to be engaged.

A-10. CLOCK GENERATOR

INPUTS:	OUTPUTS:
~RES	RESET
X1	OSC
X2	PCLK
F/~C	CLK
EFI	READY
CSYNC	
RDY1	
~AEN1	
RDY2	
~AEN2	
~ASYNC	

VCC = 18
GND = 9

FUNCTIONAL DESCRIPTION:

The Clock Generator-Driver is designed to service the 80C88 Microprocessor. It contains a crystal controlled oscillator, a divide-by-three counter, and complete 'Ready' synchronization and reset logic.

FUNCTIONAL PIN DESCRIPTIONS:

~AEN1, ~AEN2 - Address Enable (Inputs) - ~AEN1 and ~AEN2 are active low signals that are used to qualify their respective Bus Ready signals (RDY1 and RDY2).

RDY1, RDY2 - Bus ready (Inputs) - Bus Ready is an active high signal which is an input from a device located on the system bus that data has been received or is available.

~ASYNC - Ready Synchronization Select (Input) - ~ASYNC is an input which defines the synchronization of the READY logic. When ~ASYNC is low, two stages of READY synchronization are provided. When ~ASYNC is high, a single stage of READY synchronization is provided.

READY - Ready (Output) - Ready is an active high signal which is synchronized by the RDY signal input.

X1, X2 - Crystal in (Inputs) - X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.

F/~C - Frequency/Crystal Select (Input) - When F/~C is tied low, it permits the processor's clock to be generated by the crystal. When F/~C is tied high, CLK is generated from the EFI input.

EFI - External Frequency (Input) - When F/~C is tied high, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired clock output. When F/~C is tied low, EFI should be tied high or low.

CLK - Processor Clock (Output) - CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is one-third of the crystal or EFI input frequency and a one-third duty cycle.

PCLK - Peripheral Clock (Output) - PCLK is a peripheral clock whose output frequency is one-half that of the processor clock and has a 50% duty cycle.

OSC - Oscillator (Output) - OSC is the output of the internal oscillator circuitry. It's frequency is equal to that of the crystal.

~RES - Reset In (Input) - An active low on this signal is used to generate the RESET output signal.

RESET - Reset (Output) - Reset is an active high output which is used to reset the 80C88 microprocessor. It's timing characteristics are determined by ~RES.

CSYNC - Clock Synchronization (Input) - When CSYNC is high, the internal counters are set. When CSYNC goes low, the internal counters are allowed to resume counting.

A-11. PROGRAMMABLE INTERRUPT CONTROLLER (PIC)

INPUTS:	OUTPUTS:
~RD	INT
~WR	
A0	
~CS	
~SP/~EN	
~INTA	
IR0-IR7	

BIDIRECTIONAL:

AD0-AD7

VCC = 28
GND = 14

FUNCTIONAL DESCRIPTION:

The Programmable Interrupt Controller functions as the controller for the interrupt system. It accepts requests from the peripheral devices, determines which of the incoming requests has the highest priority, decides whether the incoming request has a higher priority value than the level currently being serviced, and then issues an interrupt to the microprocessor based on this information. The Programmable Interrupt Controller has eight requests and is programmed by the microprocessor as an input/output device.

FUNCTIONAL PIN DESCRIPTIONS:

~CS - Chip Select (Input) - A low on the Chip Select line enables ~RD and ~WR communication between the Microprocessor and the Programmable Interrupt Controller.

~WR - Write (Input) - When the ~WR line is low and the ~CS line is low, the PIC is enabled to accept command words from the Microprocessor.

~RD - Read (Input) - A low on the ~RD line when the ~CS line is low enables the PIC to release information onto the data bus for the microprocessor.

AD0-AD7 - Data Bus (Bidirectional) - Control, status, and interrupt information is transferred using the AD0-AD7 data lines.

~SP/~EN - Slave Program/Enable Buffer (Bidirectional) - This is a dual function pin. In the buffered mode it can be used as an output. When not in the buffered mode, it is used as an input to designate a master (high input) or a slave (low input).

INT - Interrupt (Output) - The INT line goes high whenever a valid interrupt request is asserted. It is used to interrupt the Microprocessor, thus it is connected to the Microprocessor's interrupt pin.

IR0-IR7 - Interrupt Request (Inputs) - The IR lines are inputs that when high, tell the PIC that an interrupt to the system is being requested.

~INTA - Interrupt Acknowledge (Input) - This pin is used to enable the interrupt data onto the data bus by the Microprocessor.

A0 - A0 Address Line (Input) - This pin acts in conjunction with the ~CS, ~WR, and the ~RD inputs. It is used by the PIC to decipher commands the Microprocessor writes and status that the Microprocessor wants to read.

APPENDIX B
HP 18174A
RS-449 INTERFACE POD

Figure B-1. HP 18174A Interface Pod

B-1. INTRODUCTION

The HP 18174A is an RS-449 Interface Pod designed to provide the connection between the HP 4951C Protocol Analyzer and Data Terminal Equipment (DTE) and/or Data Circuit-Terminating Equipment (DCE). The HP 18174A is compatible with EIA RS-449/422A/423A electrical, mechanical, functional, and procedural specifications.

This appendix includes information to install, operate, and service the HP 18174A.

B-2. INSTALLATION

To connect the Interface Pod to the HP 4951C Protocol Analyzer, turn the power off and attach the 37 pin connector to the port on the back of the Protocol Analyzer as shown in Figure B-2. Tighten the screws to ensure that the cable will not pull off during operation.

CAUTION

Turn off the Protocol Analyzer before connecting or disconnecting any Interface Pod.

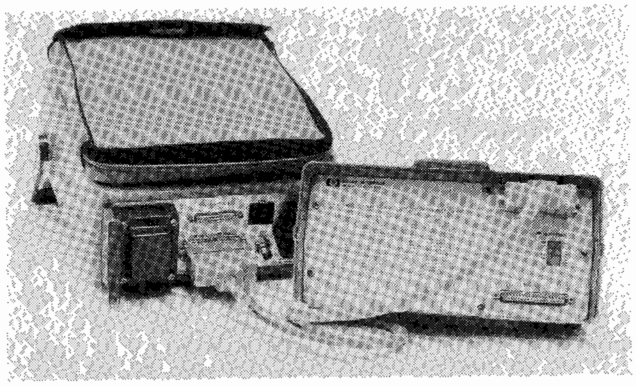


Figure B-2. Interface Pod Connections

B-3. OPERATION

Once the Interface Pod is installed, all operations are performed from the keyboard. See the Operating Manual for procedures.

B-4. PERFORMANCE VERIFICATION

The Performance Verification test is performed by the operator. Follow the procedure described below.

HP 18174A Self Test -

Description

This test checks that there is an Interface Pod connected to the Protocol Analyzer and verifies that the lines work.

Set Up

1. Turn on the HP 4951C.
2. Press MORE.
3. Select <SELFTEST>.
4. Select <EXT DLC>.

Procedure

1. When the <EXT DLC> softkey is pressed, the Interface Pod test is automatically performed.
2. If there are no failures DLC TEST PASSED will be displayed.

B-5. ADJUSTMENTS

There are no adjustments for the HP 18174A.

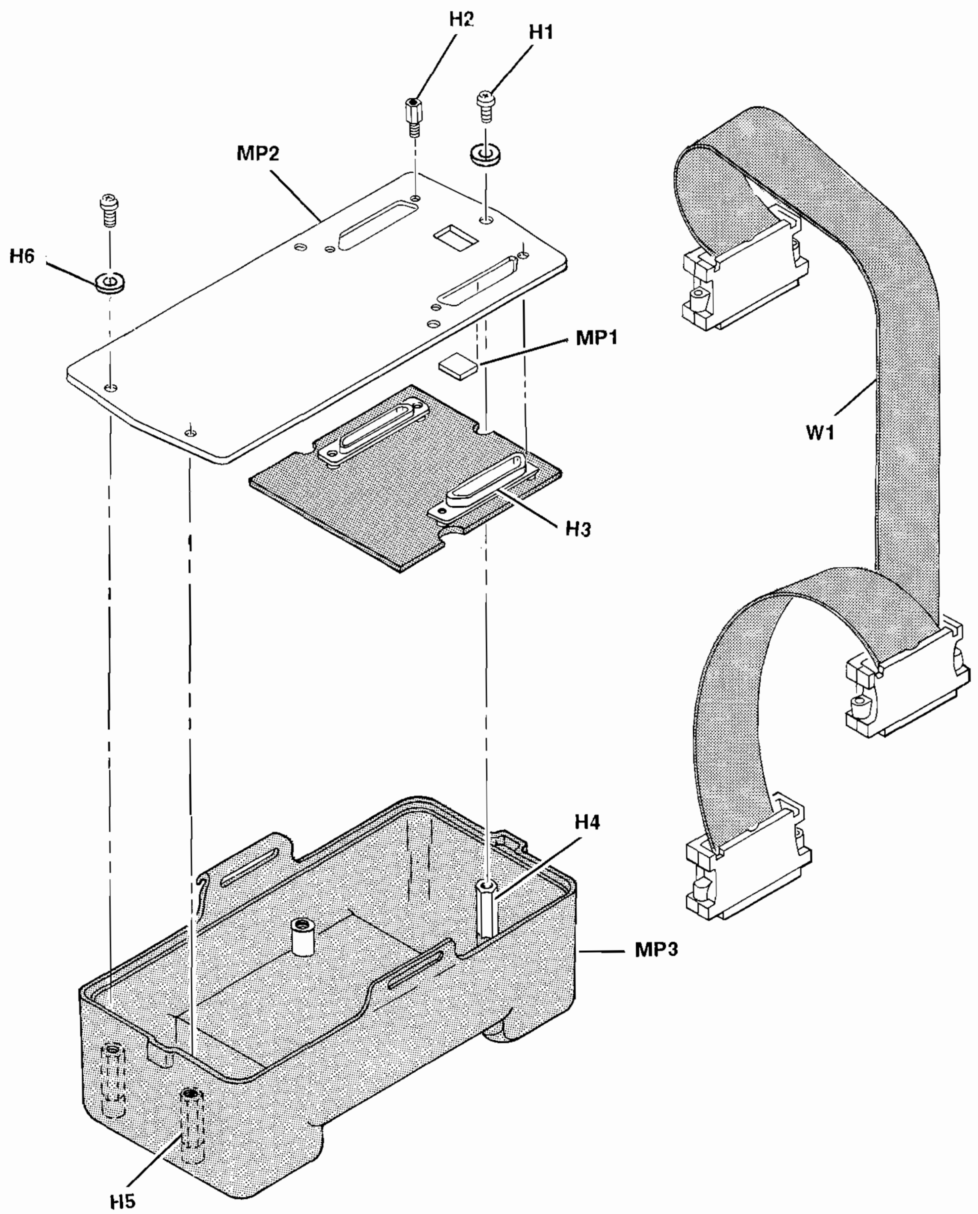
B-6. REPLACEABLE PARTS

The following tables and figure give information for ordering replacement parts. Table B-1 is the Manufacturer's Code List. Table B-2 lists the replaceable parts in Reference Designator order. Information is given for the description, Quantity, HP Part Number, and Manufacturers Part Number. Chassis and mechanical parts are listed in Figure B-2. To order a listed part, include the HP Part Number, indicate the quantity needed, and send the order to the nearest Hewlett-Packard office.

When ordering a part not listed, include the instrument model number, serial number, and a physical and functional description of the part. Send the order to the nearest Hewlett-Packard office.

Table B-1. HP 18174A Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
11236	CTS OF BERNE INC	BERNE	IN	46711
13606	SPRAGUE ELECT CO SEMICONDUCTOR DIV	CONCORD	NH	03301
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247



Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H1	2360-0195	3	5	SCR, MCH, 6-32-312	04771	ORDER BY DESCRIPTION
H2	1251-2942	4	4	SCR POST LOCK	01380	206509-1
H3	1251-6074	4	2	CONNECTOR-37 PIN	04486	DC375V
H4	0380-1719	6	1	STANDOFF	28480	0380-1719
H5	0380-1720	9	2	STANDOFFS	28480	0380-1720
H6	2190-0876	3	5	WASHER, FLAT, #6	00000	ORDER BY DESCRIPTION
MP1	5040-4478	5	1	LENS	28480	5040-4478
MP2	18174-00001	5	1	RS-449 PANEL	28480	18174-00001
MP3	5041-6749	4	1	HOUSING, COATED	28480	5041-6749
W1	18174-61601	8	1	CABLE, RS-449	28480	18174-61601
J1	8120-4218	4	4	CABLE JUMPER	28480	8120-4218
J2	8120-4219	5	2	CABLE JUMPER	28480	8120-4219

Figure B-3. HP 18174A Exploded View

Table B-2. HP 18174A Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	18174-60003	1	1	RS-449 POD	28480	18174-60003
A1C1	0180-1846	6	2	CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A1C2	0180-1846	6		CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A1C3	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C4	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C5	0160-0576	5	3	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C6	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C7	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1DS1	1990-0883	7	1	DISPLAY-LIQ-XTAL	28480	1990-0883
A1J1	1251-6074	4	2	CONNECTOR 37-PIN F D SUBMINIATURE	28480	1251-6074
A1J2	1251-6074	4		CONNECTOR 37-PIN F D SUBMINIATURE	28480	1251-6074
A1R1	0698-3266	5	2	RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A1R2	0698-3266	5		RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A1R3	0699-0556	2	2	RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A1R4	0699-0556	2		RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A1R5	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R6	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R201	1810-0680	2	10	RES NETWK SIP 2	28480	1810-0680
A1R202	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R203	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R204	1810-0732	5	1	NETWORK-RES 10.0K OHM X 5	28480	1810-0732
A1R301	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R302	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R303	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R304	1810-0369	4	2	NETWORK-RES 6-SIP100.0K OHM X 5	11236	750-61-R100K
A1R401	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R402	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R403	1810-0780	3	2	RES NETWK SIP 2	28480	1810-0780
A1R404	1810-0680	2		RES NETWK SIP 2	28480	1810-0680
A1R405	1810-0780	3	2	RES NETWK SIP 2	28480	1810-0780
A1U100	1820-3373	7	1	IC MV CMOS/74HC MONOSTBL CLEAR DUAL	28480	1820-3373
A1U101	1820-3396	4	1	IC GATE CMOS/74HC AND-OR-INV DUAL 2-INP	28480	1820-3396
A1U103	1820-3081	4	1	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	28480	1820-3081
A1U104	1820-3007	4	3	IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A1U200	1826-0759	9	3	IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U202	1820-2831	0	3	ICD 75174 DRIVER	28480	1820-2831
A1U300	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U302	1820-2831	0		ICD 75174 DRIVER	28480	1820-2831
A1U400	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U402	1820-2831	0		ICD 75174 DRIVER	28480	1820-2831
A1U403	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A1U404	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
	0380-0332	7	4	STANDOFF-RVT-ON .187-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
	1251-7642	4	1	KEYING PLUG	28480	1251-7642

B-7. SERVICE

The following paragraphs contain service information for the HP 18174A. Included is the Theory of Operation, RS-449 Signal Mnemonics, Troubleshooting, Component Locators, and Schematics.

B-8. THEORY OF OPERATION

The HP 4951C operates in three modes.

1. Monitor mode: The HP 4951C monitors traffic on a communication line.
2. DTE simulate: The HP 4951C drives the data lines and acts as a terminal.
3. DCE simulate: The HP 4951C drives the data lines and acts as the digital side of a modem or another piece of Data Circuit-Terminating Equipment.

The Interface Pod is configured for the correct mode of operation by the DTESIM and DCESIM output signals from the protocol analyzer.

The RS-449 Interface Pod has the following capabilities.

1. Translates voltages to and from RS-449 and HP 4951C logic levels.
2. Displays EIA line signal status (of selected lines only).
3. Programmable for monitoring and DTE or DCE simulation.
4. Supports differentially driven category I circuits.

Drivers

U202, U302, and U402 convert the HP 4951C signals from single-ended logic levels to differential voltage waveforms. These drivers are tristate devices and are disabled when the pod is in the monitor mode to isolate them from the RS-449 interface.

Receivers

Receivers U200, U300, and U400 operate over a common mode voltage range from -7 to +7 volts and require a minimum differential off 200 millivolts to change states. They maintain operation over a differential voltage range from 200 millivolts to 6 volts; however, the positive common mode signal voltage cannot exceed the RS-449 specification of 10 volts. The receivers are protected by divider resistors from signals up to 12 volts.

The EIA status of the selected interface lines is displayed on a bargraph LCD. Clock and data indicators are flashed at a 2Hz rate when line state transitions are detected. Table B-3 lists these RS-449 lines.

Table B-3. HP 18174A Front Panel LCD Display

CS	Clear to Send
DM	Data Mode
RD	Receive Data
RR	Receiver Ready
RS	Request to Send
RT	Receive Timing
SD	Send Data
ST	Send Timing
TR	Terminal Ready

Table B-4. RS-449 Signal Mnemonics

	RS449 PIN #	CIRCUIT	DESCRIPTION
	1	Shield	
	2	SI	Signaling-rate Indicator
	3	Space	
*	4	SDa	Send Data (a)
	5	STa	Send Timing (a)
*	6	RDa	Receive Data (a)
*	7	RSa	Request to Send (a)
	8	RTa	Receive Timing (a)
*	9	CSa	Clear to Send (a)
	10	LL	Local Loopback
*	11	DM	Data Mode (a)
	12	TR	Terminal Ready (a)
*	13	RR	Receiver Ready (a)
	14	RL	Remote Loopback
	15	IC	Incoming Call
	16	SF	Select Frequency/ Signaling-rate Selector
	17	TT	Terminal Timing (a)
	18	TM	Test Mode
	19		Signal Ground
	20		Receive Common
	21	Spare	
	22	DTE	Send Data (b)
	23	ST	Send Timing (b)
	24	DCE	Receive Data (b)
	25	RS	Request to Send (b)
	26	RT	Receive Timing (b)
	27	CS	Clear to Send (b)
	28	IS	Terminal in Service
	29	DM	Data Mode (b)
	30	TR	Terminal Ready (b)
	31	RR	Receiver Ready (b)
	32	SS	Select Standby
	33	SQ	Signal Quality
	34	NS	New Signal
	35	TT	Terminal Timing (b)
	36	SB	Standby Indicator
	37		Send Common

*Indicates lines for which parameters can be selected from HP 4951C display.

B-9. TROUBLESHOOTING

Troubleshoot the portion of the Interface Pod that has failed (DTE or DCE). When entering the test programs below, "Press" indicates a hardkey and "Select" indicates a softkey.

DCE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod.

1. Enter the following DCE test program.

Table B-5. DCE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DCE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed.		
Select	Simulate	
	DCE	
Press	MORE	
Select	Set Lead	
	CS	
	Off	
	and then	
Press	MORE	
Select	Set Lead	
	DM	
	Off	
	and then	
Press	MORE	
Select	Set Lead	
	RR	
	Off	
	and then	
	Send	
Type in	CS OFF	
Press	RTN (return)	

Table B-5. DCE Test Program (continued)

Select	Next Block
Press	MORE
	Set Lead
	CS
	On
	and then
Press	MORE
Select	Set Lead
	DM
	On
	and then
Press	MORE
Select	Set Lead
	RR
	On
	and then
	Send
Type in	CS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	CS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

2. Run the program entered in Table B-5.

Select Run Menu
Simulate

a. All lines on the HP 4951C display should be active except DTE and RS.

b. Segments RD, ST, and RT should be flashing. Segments CS, DM, and RR should be on, and segments SD, RS, and TR should be off.

3. If any of the above conditions fail, troubleshoot that part of the circuit.

DTE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod.

1. Enter the following DTE test program.

Table B-6. DTE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DTE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed.		
Select	Simulate	
	DTE	
Press	MORE	
Select	Set Lead	
	RS	
	Off	
	and then	
	MORE	
	Set Lead	
	TR	
	Off	
	and then	
	Send	
Type in	RS OFF	
Press	RTN (return)	
Select	Next Block	
Press	MORE	
Select	Set Lead	
	RS	
	On	
	and then	
Press	MORE	
Select	Set Lead	
	TR	
	On	
	and then	
	Send	
Type in	RS ON	
Press	RTN (return)	

Table B-6. DTE Test Program (continued)

Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	RS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

2. Run the program entered in Table B-6.

   Select RUN MENU
   SIMULATE

3. Segments SD and ST should be flashing, RS and TR should be on, and all of the other segments should be off (-- is never active).

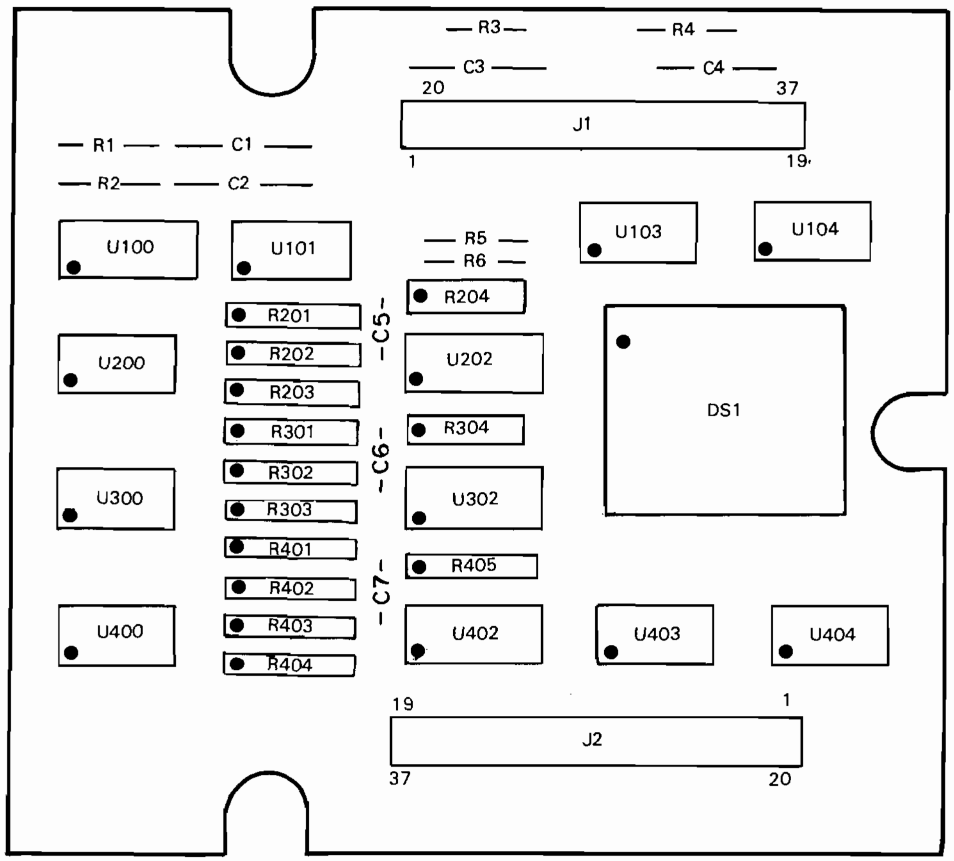
4. If any of the conditions in step 2 fail, check items a through c.

   a. The inputs to U202, U302, and U402 should be at TTL levels (between 0 and 5 volts).

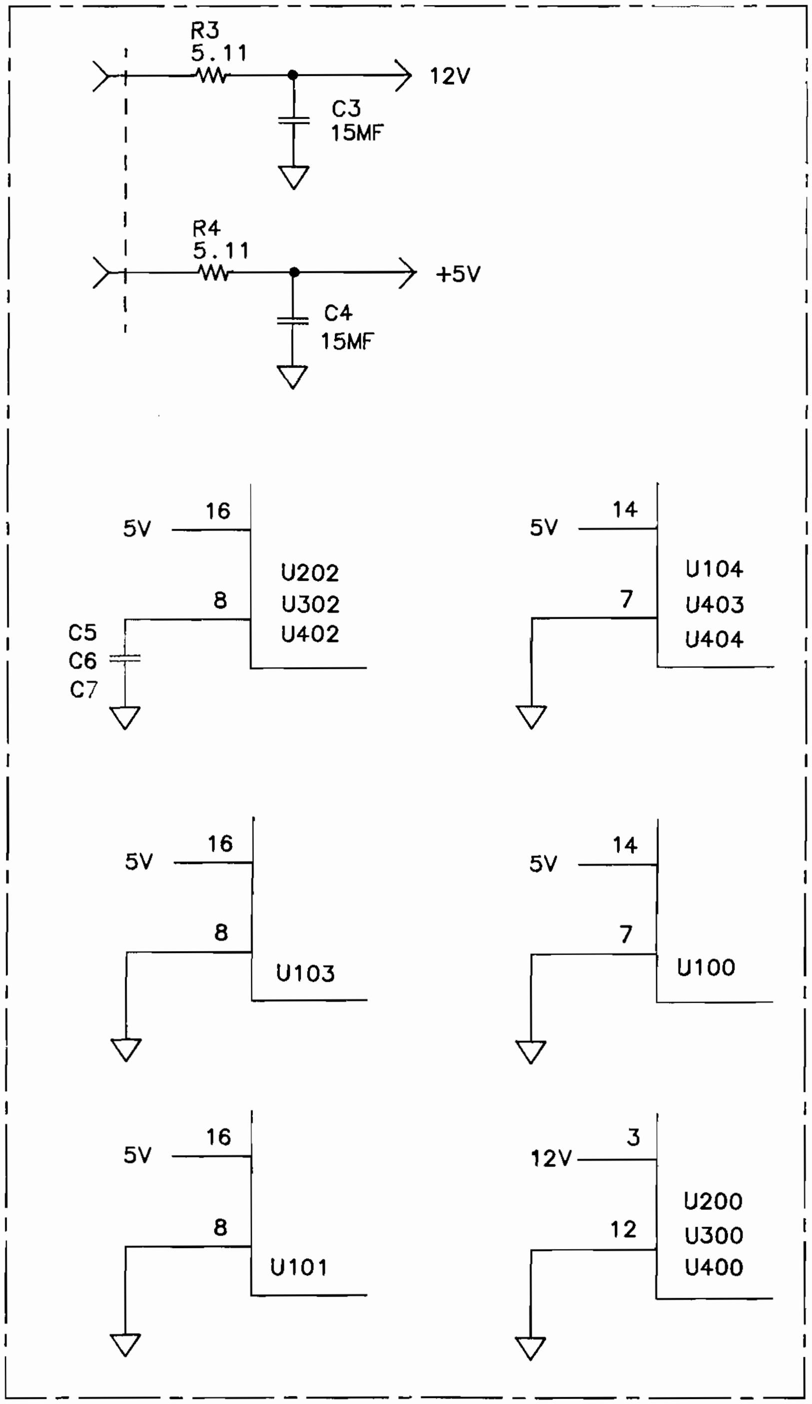
   b. The outputs of U202, U302, and U402 should be RS-449 levels (+- 12V).

   c. The inputs and outputs of all other circuits should be at TTL levels. Check for correct amplitudes and pulsing signals.

Figure B-4. HP 18174A Component Locator



18174-60001-0113-2-84



Power and Grounds

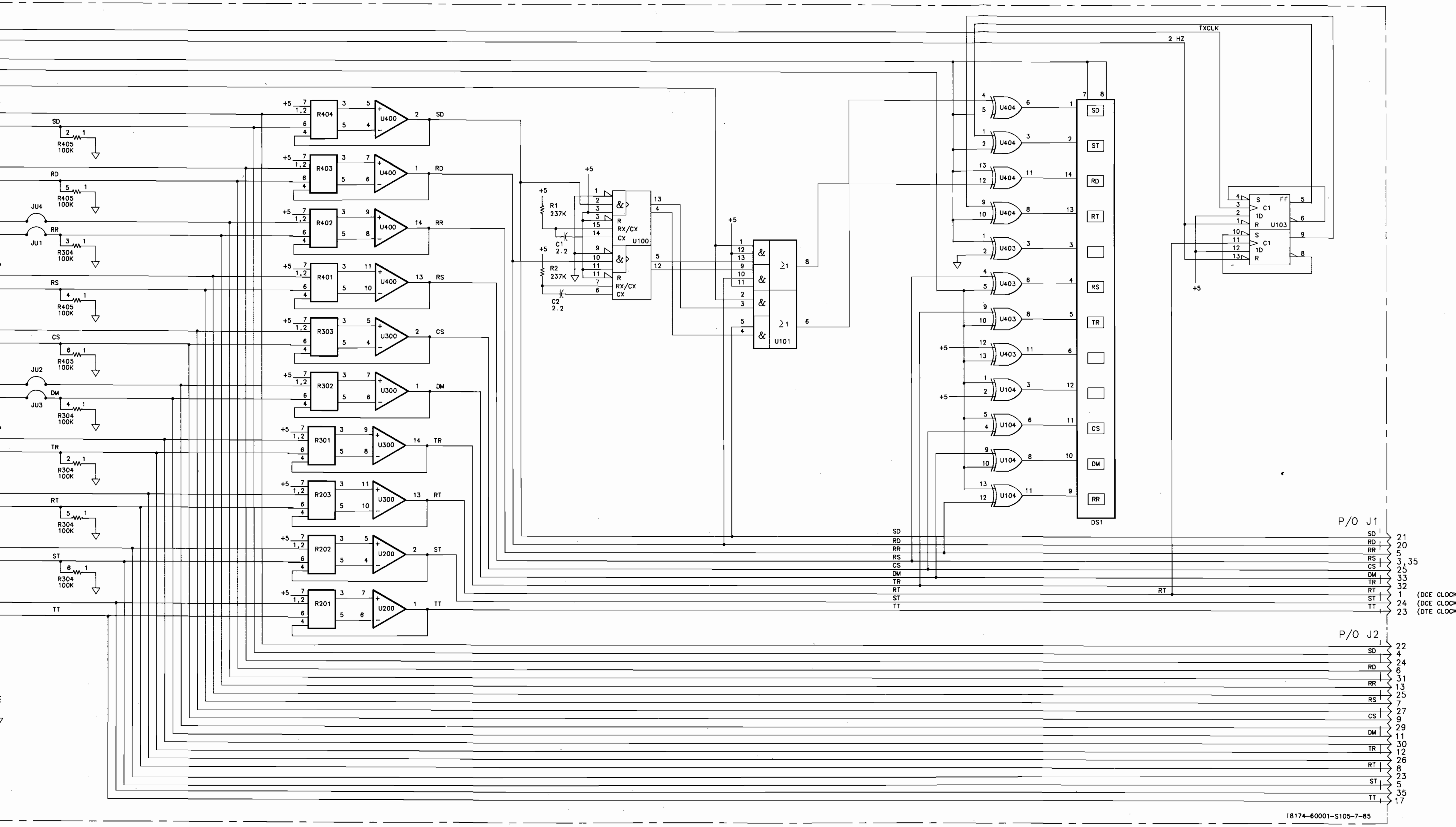
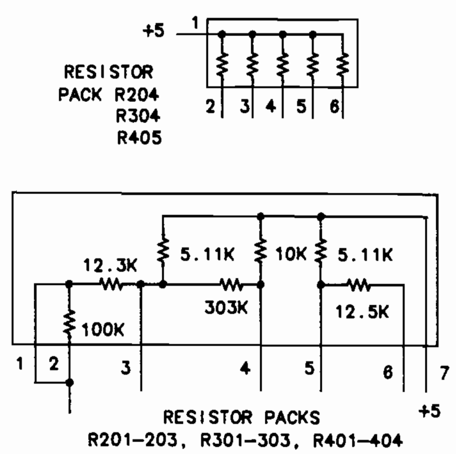
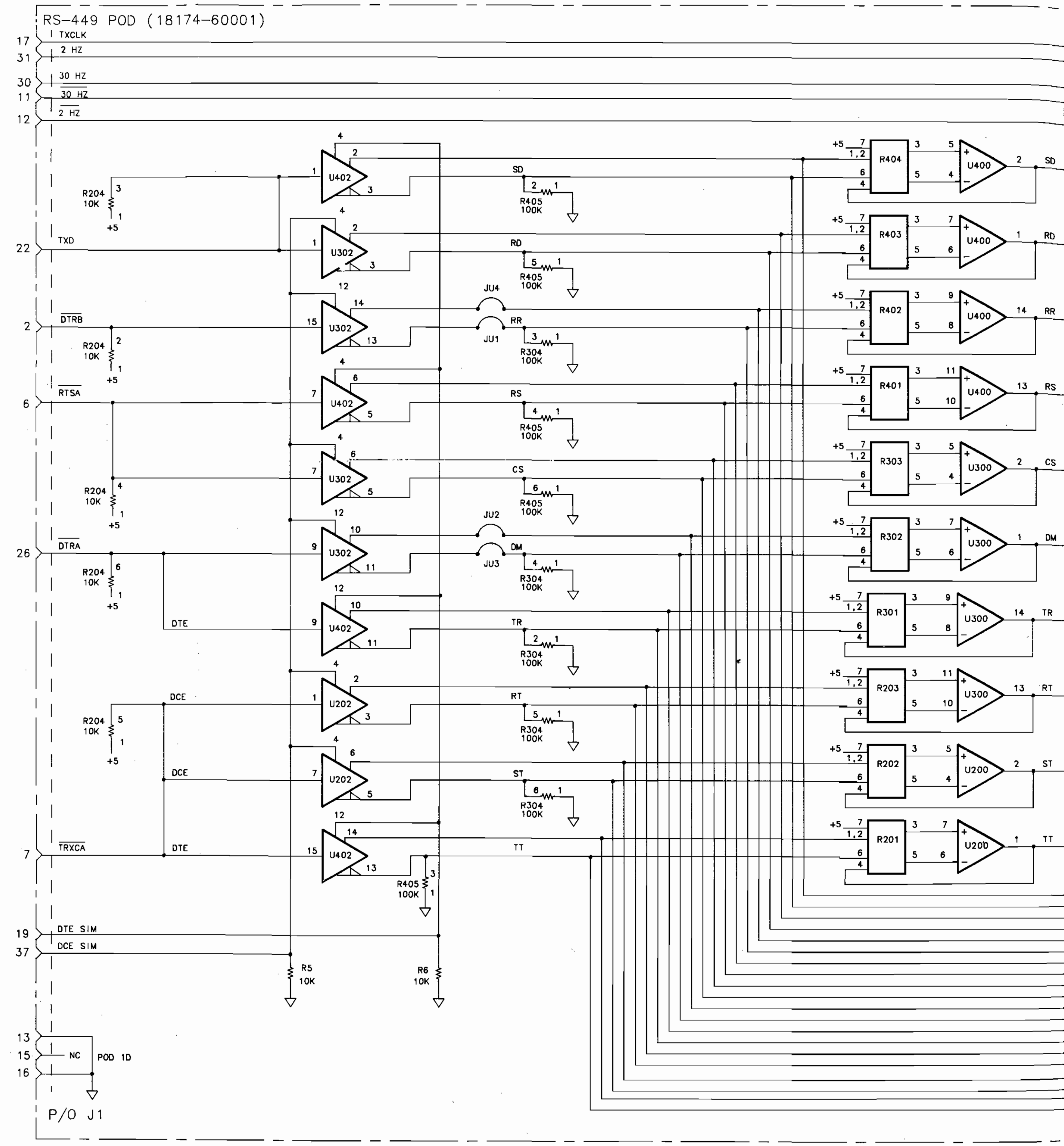


Figure B-5. HP 18174A Interface Pod Schematic


+5
RESISTOR
PACK R204
R304
R405
12.3K
5.11K
10K
5.11K
303K
12.5K
100K
+5
RESISTOR PACKS
R201-203, R301-303, R401-404


RS-449 POD (18174-60001)
TXCLK
2 HZ
30 HZ
30 HZ
2 HZ
TXD
DTRB
RTSA
DTRA
DTE
DCE
DCE
TRXCA
DTE
DTE SIM
DCE SIM
NC
POD ID
P/O J1
U402
U302
U202
R204
10K
R405
100K
R304
100K
JU1
JU2
JU3
JU4
SD
RD
RR
RS
CS
DM
TR
RT
ST
TT
R5
10K
R6
10K
R404
R403
R402
R401
R303
R302
R301
R203
R202
R201
U400
U300
U200

APPENDIX C
HP 18177A
V.35 INTERFACE POD

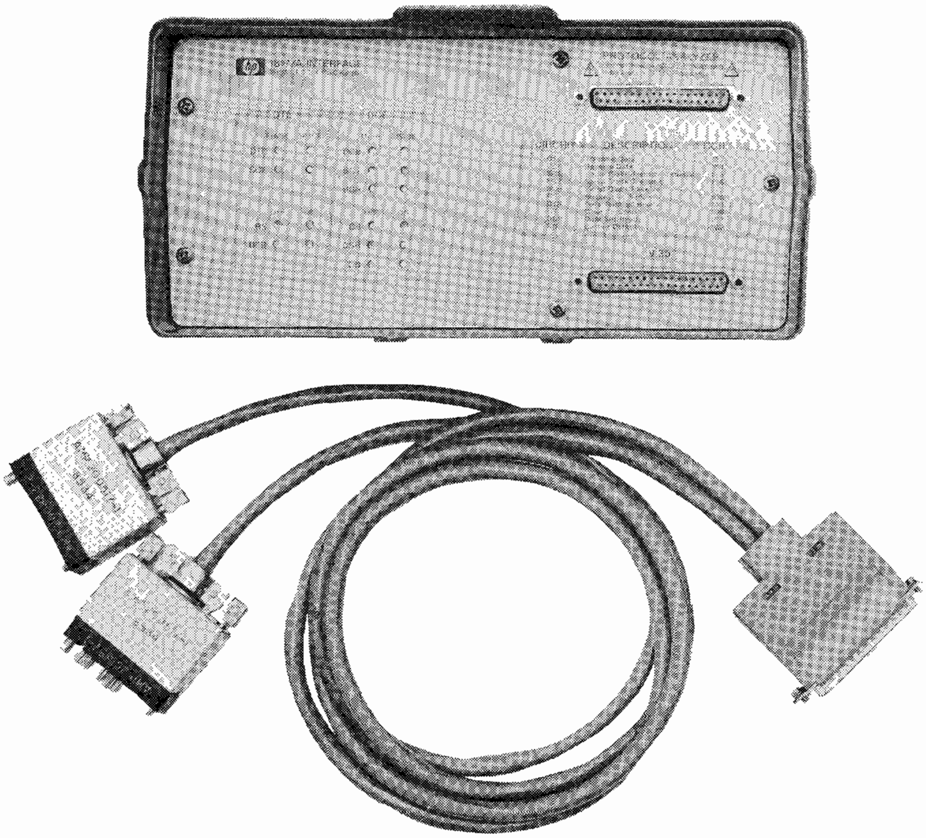


Figure C-1. HP 18177A Interface Pod and V.35 Cable

C-1. INTRODUCTION

The HP 18177A is a V.35 Interface Pod which provides the connection between the HP 4951 Protocol Analyzer and Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The HP 18177A follows V.28/V.35 electrical specifications, V.24 functional specifications, and ISO 2593 mechanical specifications.

This appendix includes information on how to install, operate, and service the HP 18177A.

C-2. INSTALLATION

CAUTION

Turn the HP 4951 Protocol Analyzer off before connecting or disconnecting the Interface Pod.

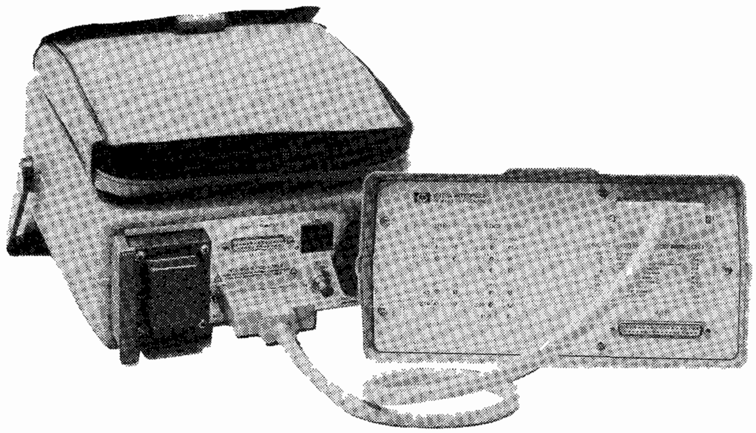


Figure C-2. Connecting the Interface Pod to the HP 4951

To connect the Interface Pod to the HP 4951, attach the Interface Pod Cable between the lower port on the back of the HP 4951 and the top right connector of the HP 18177A as shown in Figure C-2. Tighten the connector screws to ensure that the cable will not pull off during operation.

C-3. OPERATION

Once the Interface Pod is connected to the HP 4951, it effectively becomes a part of the HP 4951. Refer to the HP 4951 Operating Manual for specific operating instructions.

The Performance Verification test in paragraph C-4 can be used to check the Interface Pod functionally before it is used.

Theory of Operation

The HP 18177A V.35 Interface Pod connects the HP 4951 Protocol Analyzer to the DTE and DCE.

There are three modes of operation for the HP 18177A Interface Pod: monitor mode, DTE simulate mode, and DCE simulate mode. During the monitor mode the pod nonintrusively acquires signals from the DTE and DCE and sends them to the HP 4951 for analysis. During both of the simulate modes the HP 4951 drives the appropriate lines to either the DTE or DCE. In all three modes, the pod LEDs show activity on the lines.

Figures H-3 and C-4 show the typical monitor and simulate connections.

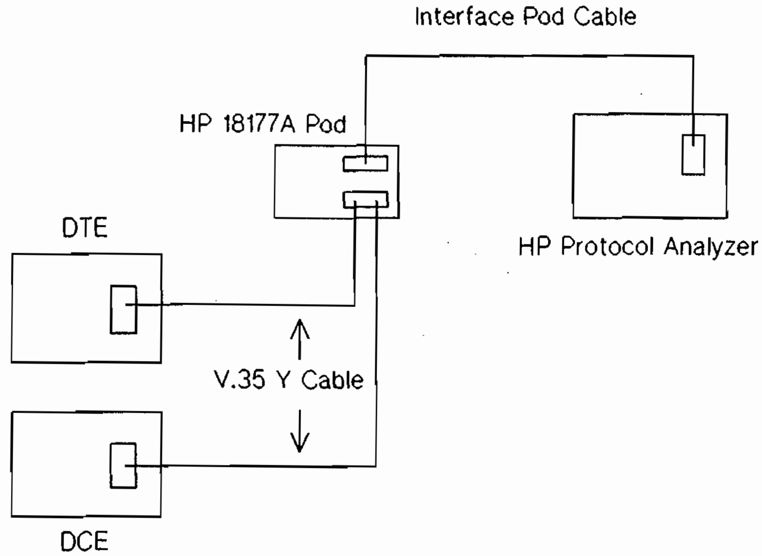


Figure C-3. Monitor Mode Set Up

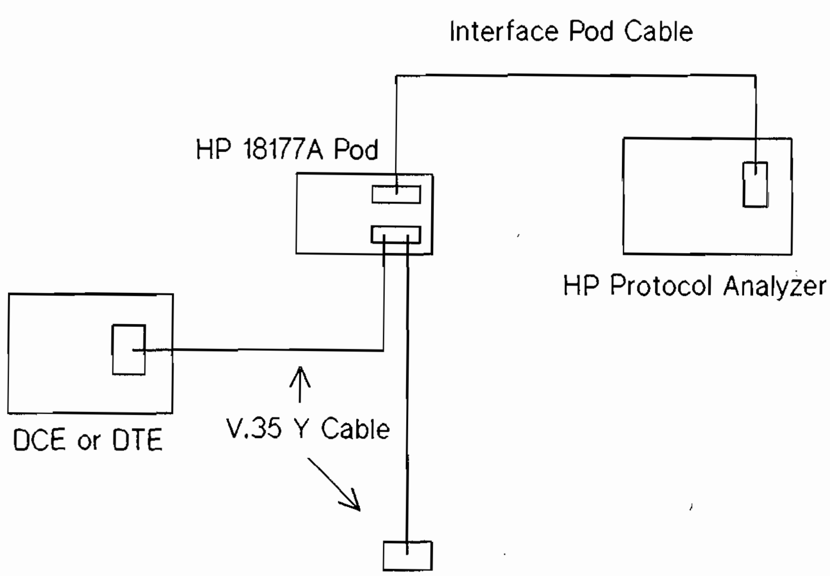


Figure C-4. Simulation Modes Set Up

MONITOR MODE

In the monitor mode, data, clock, and control signals from the DTE and DCE are routed through the pod receivers to the pod mark/space LEDs and to the HP 4951. The pod LEDs indicate whether the signals are on, off, or neither. The HP 4951 can be programmed to make decisions based on the states of the signals.

Figure C-5 and the following text describe the main signal flow during monitor mode. The grey-shaded arrows show how the DTE and DCE signals are routed to the pod LEDs and the HP 4951.

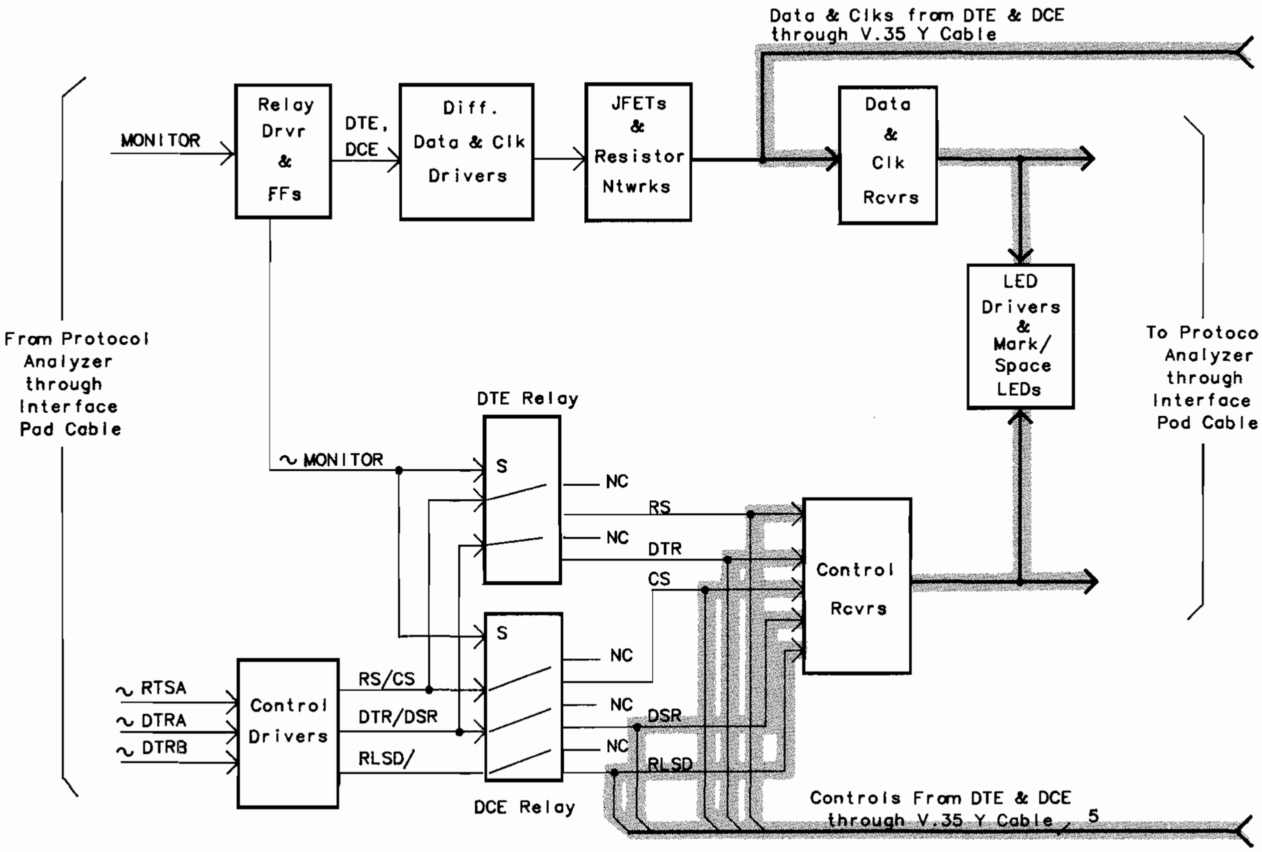


Figure C-5. Monitor Mode Signal Flow.

When the HP 4951 selects the monitor mode, it pulses the pod MONITOR line high and the following events occur:

- Relay Driver U201 output pin 12 (~MONITOR) goes low and sets both the DTE and the DCE Relays (K100 and K101). With the relays set, the control driver outputs are not connected to the V.35 interface.

- Relay Driver output pin 16 goes low and clears both the DTE and DCE Flip Flops (U300). The Flip Flop Q outputs (DTE and DCE) go low and inhibit all of the data and clock differential drivers. When the drivers are inhibited both outputs of each driver are tri-stated and are effectively disconnected from the V.35 interface.

- Relay Driver output pin 15 (SIM/~MON) goes low, causing SIM/~MONJFET to go low and switch JFETS Q3 through Q7 off. This creates the correct impedance on the data and clock lines.

With all the pod drivers effectively disconnected from the pod receivers, and the correct impedance on the data and clock lines, the signals from the DTE and DCE can be sent through the receivers to the mark/space LEDS and to the HP 4951.

SIMULATE MODES

DTE Simulation

In the DTE simulate mode, the HP 4951 acts like a DTE by sending DTE data, clock, and control signals through the pod DTE drivers to the DCE. These signals also go to the pod mark/space LEDs. Data, clock, and control signals from the DCE are routed through the pod receivers to the pod mark/space LEDs and to the HP 4951.

Figure C-6. and the following text describe the main signal flow during DTE simulation. The grey-shaded arrows show how the DTE signals are driven to the DCE, the pod LEDs, and the HP 4951.

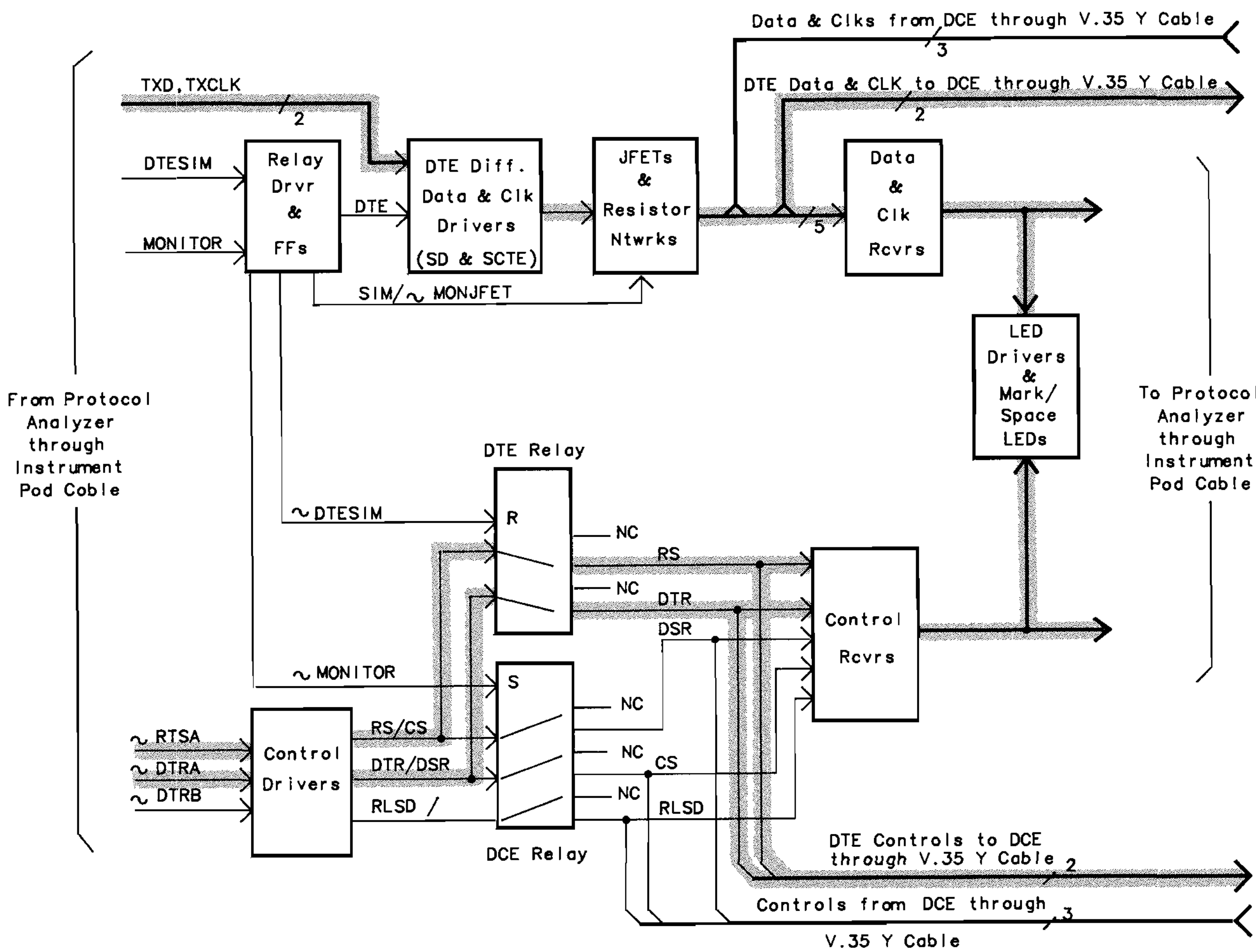


Figure C-6. DTE Simulation Mode Signal Flow

When the HP 4951 selects the DTE Simulation mode, it pulses the pod MONITOR line high to put the pod in a known state. Then it pulses the pod DTESIM line high and the following events occur:

- Relay Driver U201 output pin 11 (~DTESIM) goes low and resets the DTE Relay K101. This connects the DTE control lines from the pod control drivers to the DCE, and also through the control receivers to the pod mark/space LEDS. The DTE control lines (RS and DTR) are derived from the ~RTSA, ~DTRA, and ~DTRB signals from the HP 4951.

- The DTE Flip Flop (p/o U300) is clocked and its Q output pin 5 (DTE) goes high. This lets the TXD and TRXCA signals (from the HP 4951) drive the DTE data and clock differential drivers (SD and SCTE).

- SIM/~MONJFET is high, which turns JFETS Q3 through Q7 on. This creates the proper V.35 voltage levels on the outputs of the differential drivers.

DCE Simulation

In the DCE simulate mode, the HP 4951 acts like a DCE by sending DCE data, clock, and control signals through the pod DCE drivers to the DTE. These signals also go to the pod mark/space LEDs. Data, clock, and control signals from the DTE are routed through the pod receivers to the pod mark/space LEDs and to the HP 4951.

Figure C-7 and the following text describe the main signal flow during DCE simulation. The grey-shaded arrows show how the DCE siganls are driven to the DTE, the pod LEDs, and the HP 4951.

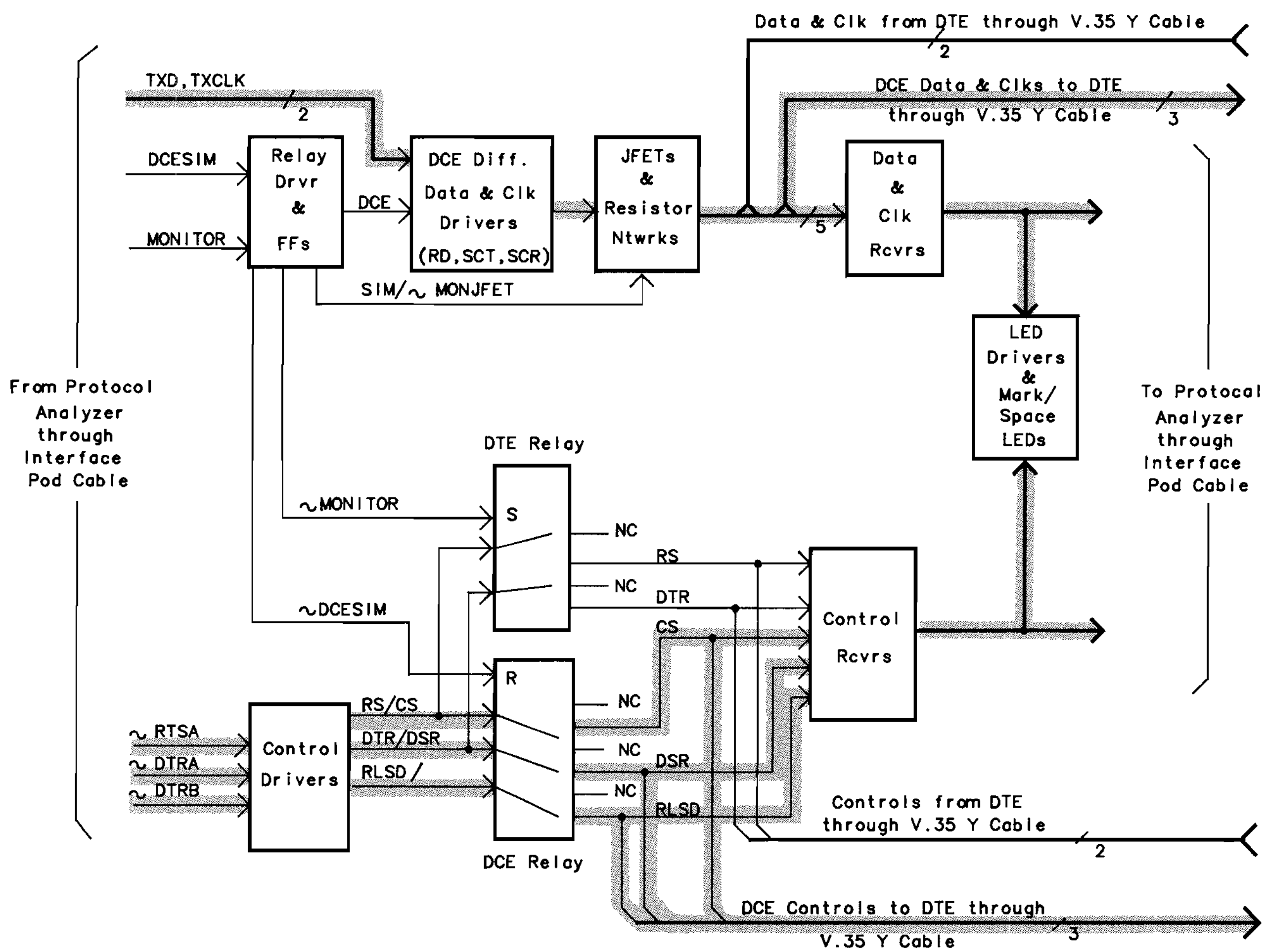


Figure C-7. DCE Simulation Mode Signal Flow

When the HP 4951 selects the DCE Simulation mode, it pulses the pod MONITOR line high to put the pod in a known state. Then it pulses the pod DCESIM line high and the following events occur:

- Relay Driver U201 output pin 10 (~DCESIM) goes low and resets the DCE Relay K100. This connects the DCE control lines from the pod control drivers to the DTE, and also through the control receivers to the pod mark/space LEDS. The DCE control lines (CS, DSR, and RLSD) are derived from the ~RTSA, ~DTRA, and ~DTRB signals from the HP 4951.

- The DCE Flip Flop (p/o U300) is clocked and its Q output pin 9 (DCE) goes high. This lets the TXD and TRXCA signals (from the HP 4951) drive the DCE data and clock differential drivers (RD, SCT, and SCR).

- SIM/~MONJFET is high, which turns JFETS Q3 through Q7 on. This creates the proper V.35 voltage levels on the outputs of the differential drivers.

C-4. PERFORMANCE VERIFICATION

This Performance Verification test can be used to check that the pod is functional once it is connected to the HP 4951. (See paragraph C-2 for connecting the pod to the HP 4951).

CAUTION

Do not perform the pod performance verification test while the pod is connected to a network device. To do so may cause damage to the network device or the pod.

Description

This test checks if there is an Interface Pod connected to the HP 4951, and verifies the DTE and DCE lines.

Procedure

1. Turn on the HP 4951.
2. Press MORE.
3. Select <SELFTEST>.
4. Select <EXT DLC>.

Once the <EXT DLC> softkey is pressed, the Interface Pod Performance Test is run.

If there are no failures, the HP 4951 displays DLC TEST PASSED.

There are several error messages that may be displayed if the test fails:

No pod attached

DTE TEST FAILED and DCE TEST FAILED

DTE TEST FAILED

DCE TEST FAILED

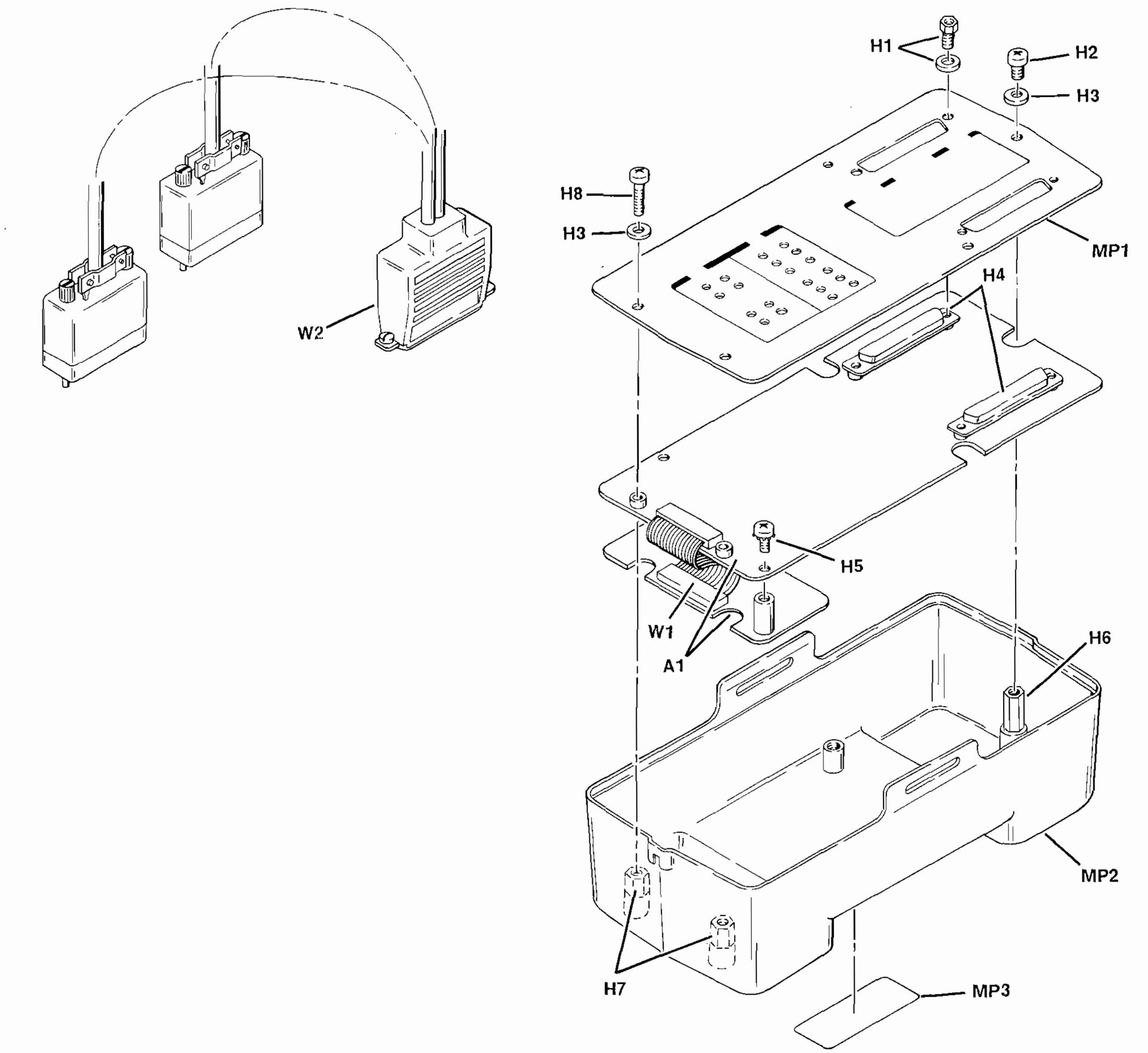
If any of these error messages are displayed, refer to paragraph C-8 for service information.

C-5. ADJUSTMENTS

There are no adjustments for the HP 18177A.

C-6. REPLACEABLE PARTS

This section contains information for ordering parts for the HP 1877A V.35 Interface Pod. Table C-1 is a list of the HP 18177A Replaceable Parts, and Table C-2 is a Manufacturer's Code List. Figure C-8 is an exploded view of the Interface Pod along with a list of the chassis and mechanical parts.



Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	**18177-60001**	**2**	**1**	**V.35 INTERFACE BOARD**	**28480**	**18177-60001**
H1	1251-2942	7	4	SCREW POST LOCK, INC WASHER	28480	1251-2942
H2	2360-0195	0	3	SCR MCH 6-32.312	28480	2360-0195
H3	2190-0876	3	5	WASHER FLAT MET	28480	2190-0876
H4	1251-6074	4	2	CONN 37-PIN F	28480	1251-6074
H5	2360-0115	4	2	SCR MCH 6-32.312	28480	2360-0115
H6	0380-1719	6	1	STDF-HEX M&F	28480	0380-1719
H7	0380-1617	3	2	STDF-HEX .5-IN	28480	0380-1617
H8	2360-0205	3	2	SCR MCH 6-32.750	28480	2360-0205
MP1	18177-00001	6	1	V.35 PANEL	28480	18177-00001
MP2	5041-6749	7	1	POD HSG PAINTED	28480	5041-6749
MP3	18177-80001	4	1	LBL-HP18177A	28480	18177-80001
W1	18173-61601	6	1	BD INTERCONNECT CABLE	28480	18173-61601
W2	18177-61601	0	1	V.35 Y CBL ASSY	28480	18177-61601

Figure C-8. HP 18177A Exploded View

Table C-1. HP 18177A Replaceable Parts List

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	**18177-60001**	**2**	**1**	**V.35 INTERFACE**	**28480**	**18177-60001**
A1C1	0180-0291	3	4	CAPACITOR-FXD 1UF 35V	04200	150D105X9035A2-DYS
A1C2	0180-0291	3		CAPACITOR-FXD 1UF 35V	04200	150D105X9035A2-DYS
A1C3	0160-5298	8	12	CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C4	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C5	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C6	0180-0228	6	1	CAPACITOR-FXD 22UF 15V	04200	150D226X9015B2-DYS
A1C7	0180-0116	1	2	CAPACITOR-FXD 6.8UF 35V	04200	150D685X9035B2-DYS
A1C8	0180-0116	1		CAPACITOR-FXD 6.8UF 35V	04200	150D685X9035B2-DYS
A1C9	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C10	0160-5371	8	6	CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C11	0160-5332	1	6	CAPACITOR .1 UF 20% 50V	02010	MD015C104MAA
A1C12	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C13	0180-0291	3		CAPACITOR-FXD 1UF 35V	04200	150D105X9035A2-DYS
A1C14	0180-0291	3		CAPACITOR-FXD 1UF 35V	04200	150D105X9035A2-DYS
A1C15	0160-5371	8		CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C16	0160-5371	8		CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C17	0180-3641	3	1	CAPACITOR-FXD 1000UF 10V AL	00493	SME10B102M10X16LL
A1C18	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C20	0180-3763	0	1	CAPACITOR-FXD 100UF 10V	00493	SME10VB101M5X11LL
A1C21	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C22	0160-5371	8		CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C23	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C24	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C25	0160-5332	1		CAPACITOR .1 UF 20% 50V	02010	MD015C104MAA
A1C26	0160-5332	1		CAPACITOR .1 UF 20% 50V	02010	MD015C104MAA
A1C27	0160-5371	8		CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C28	0160-5371	8		CAPACITOR-FXD 1000PF 20%	02010	MD011C102MAA
A1C29	0160-5332	1		CAPACITOR .1 UF 20% 50V	02010	MD011C104MAA
A1C30	0160-5332	1		CAPACITOR .1 UF 20% 50V	02010	MD011C104MAA
A1C31	0160-5332	1		CAPACITOR .1 UF 20% 50V	02010	MD011C104MAA
A1C32	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C33	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1C34	0160-5298	8		CAPACITOR-FXD 0.01UF 20%100V	02010	MD011C103MAA
A1CR1	1901-0734	0	1	DIODE IN5818	02037	SBR5303
A1CR2	1990-0913	4	10	LED-LAMP	01542	HLMP-1340
A1CR3	1990-0914	5	10	LED-LAMP	01542	HLMP-1540
A1CR4	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR5	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR6	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR7	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR8	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR9	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR10	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR11	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR12	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR13	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR14	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR15	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR16	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR17	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR18	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR19	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR20	1990-0913	4		LED-LAMP	01542	HLMP-1340
A1CR21	1990-0914	5		LED-LAMP	01542	HLMP-1540
A1CR23	1902-0960	6	2	DIODE-ZNR 12V 5%	28480	1902-0960
A1CR24	1902-0960	6		DIODE-ZNR 12V 5%	28480	1902-0960
A1CR25	1902-0949	1	2	ZENER 4.3V	02037	SZ30035-007
A1CR26	1902-0949	1		ZENER 4.3V	02037	SZ30035-007
A1J1	1251-6074	4	2	CONN 37 - PIN F	04486	DC37SV
A1J2	1251-6074	4		CONN 37 - PIN F	04486	DC37SV
A1K100	0490-1383	3	1	RELAY	01850	DS4E-ML2-DC5V-H123
A1K101	0490-1354	8	1	RELAY-10 PIN PKG	01850	DS2E-ML2-DC5V-H36
A1L1	9140-1069	0	1	INDCTR-92100	01869	92100
A1L2	9140-1163	5	2	IND 27O UH .77A	28480	9140-1163
A1L3	9140-1163	5		IND 27O UH .77A	28480	9140-1163

Table C-1. HP 18177A Replaceable Parts List (continued)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1Q1	1826-0285	6	1	IC MC79L05ACP	02037	SC61916P1
A1Q2	1853-0512	9	1	PNP PD-50	01973	X45H589
A1Q3	1855-0078	6	5	N CHAN FET	28480	1855-0078
A1Q4	1855-0078	6		N CHAN FET	28480	1855-0078
A1Q5	1855-0078	6		N CHAN FET	28480	1855-0078
A1Q6	1855-0078	6		N CHAN FET	28480	1855-0078
A1Q7	1855-0078	6		N CHAN FET	28480	1855-0078
A1Q8	1826-0772	6	1	IC LM317LZ	02037	SC317L2
A1R1	0757-0442	9	1	RESISTOR 10K 1%.125W	02995	5033R
A1R2	0698-3450	9	1	RESISTOR 42.2 KOHM 1%	02995	5033R
A1R13	0698-3442	9	1	RESISTOR 237 1% .125W	02995	5033R
A1R14	0698-8812	7	2	RESISTOR 1 1% .125W	03292	L04D
A1R15	0757-0417	8	1	RESISTOR 562 1% .125W	02995	5033R
A1R16	0757-0317	7	1	RESISTOR 1.33K 1% .125W	02995	5033R
A1R17	0698-8812	7		RESISTOR 1 1% .125W	03292	L04D
A1R18	0757-0398	4	1	RESISTOR 75 .12MF 1%	02995	5033R
A1R19	0698-8820	7	2	RESISTOR 4.64 1% .125W	03292	L04D
A1R20	0698-8820	7		RESISTOR 4.64 1% .125W	03292	L04D
A1R21	0757-0416	7	2	RESISTOR 511 1% .125W	02995	5033R
A1R22	0757-0416	7		RESISTOR 511 1% .125W	02995	5033R
A1R101	1810-0273	9	1	NET 470 OHM X9	01607	210A471
A1R104	1810-0921	4	2	560 OHM SIP 6PIN	01607	206A561
A1R106	1810-0920	3	2	680 OHM SIP 6PIN	01607	106A681
A1R108	1810-0921	4		560 OHM SIP 6PIN	01607	206A561
A1R110	1810-0920	3		680 OHM SIP 6PIN	01607	106A681
A1R112	1810-0318	3	3	NET 1.0K OHM X5	02483	750-61-R1K
A1R113	1810-0966	2	2	330 OHM 6 PIN	28480	1810-0966
A1R114	1810-0966	2		330 OHM 6 PIN	28480	1810-0966
A1R115	1810-0780	3	1	RESISTOR NETWORK 100K	05524	CSC06A01
A1R116	1810-0318	3		NET 1.0K OHM X5	02483	750-61-R1K
A1R206	1810-0338	7	1	NET 100.0 OHM X8	01607	316B101
A1R207	1810-0924	7	10	CUST SIP NET RES	28480	1810-0924
A1R208	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R209	1810-0679	9	5	RES NETWK SIP 4	05524	CSC07A-00-S9
A1R210	1810-0679	9		RES NETWK SIP 4	05524	CSC07A-00-S9
A1R224	1810-0205	7	1	NET 4.7K OHM X7	02483	750-81-R4.7K
A1R225	1810-0318	3		NET 1.0K OHM X5	02483	750-61-R1K
A1R226	1810-0679	9		RES NETWK SIP 4	05524	CSC07A-00-S9
A1R227	1810-0280	8		NET 10.0K OHM X9	02483	750-101-R10K
A1R228	1810-0342	3	1	NTWK RES 100K X5	02483	750-103-R100K
A1R306	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R307	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R308	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R309	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R506	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R507	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R508	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R509	1810-0924	7		CUST SIP NET RES	28480	1810-0924
A1R510	1810-0280	8		NET 10.0K OHM X9	02483	750-101-R10K
A1R511	1810-0292	2	1	NETWORK-RES DIP	02483	760-3-R220
A1R512	1810-0679	9		RES NETWK SIP 4	05524	CSC07A-00-S9
A1R513	1810-0679	9		RES NETWK SIP 4	05524	CSC07A-00-S9
A1U103	1820-3297	4	3	IC 74HC244N	02037	MC74HC7244N
A1U104	1820-1826	1	3	IC 75112N	01698	SN98460N
A1U105	1820-1826	1		IC 75112N	01698	SN98460N
A1U201	1858-0047	5	1	XSTR ARY 16P-DIP	02634	ULN-2003A
A1U203	1820-3297	4		IC 74HC244N	02037	MC74HC7244N
A1U204	1820-1826	1		IC 75112N	01698	SN98460N
A1U205	1826-0138	8	6	IC 339	03406	LM339N
A1U208	1826-0138	8		IC 339	03406	LM339N
A1U209	1826-0138	8		IC 339	03406	LM339N
A1U300	1820-3081	4	1	IC MC74HC74N	02037	MC74HC74N
A1U301	1826-0138	8		IC 339	03406	LM339N
A1U403	1820-3297	4		IC 74HC244N	02037	MC74HC7244N
A1U406	1826-0753	3	1	IC 34004B	02037	MC7796BL1
A1U407	1906-0074	1	3	DIODE ARRAY	02037	MAD1103P
A1U408	1906-0074	1		DIODE ARRAY	02037	MAD1103P

Table C-1. HP 18177A Replaceable Parts List (continued)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U409	1906-0074	1		DIODE ARRAY	02037	MAD1103P
A1U500	1826-1256	9	1	IC MC34063P1	02037	MC34063U
A1U504	1826-0138	8		IC 339	03406	LM339N
A1U505	1826-0138	8		IC 339	03406	LM339N
A1W1	18173-61601	6	1	BD INTERCONNECT CABLE	28480	18173-61601
	1400-1025	2	20	MOUNT LED	03724	908-150
	0380-0059	5	2	SPCR.152.250	02121	MK6310-1/4-2-14
	0380-0162	5	2	SPCR 6-32 .750	02121	MK6910-3/4-2-14
	0380-0332	7	4	STDF 4-40	02121	MK6911-3/16-2-14

Table C-2. Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
01456	MICROWAVE DEVELOPMENT LABS INC	NEEDHAM HTS	MA	02194
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06383	PANDUIT CORP	TINLEY PARK	IL	60477
08806	GE CO MINIATURE LAMP PROD DEPT	CLEVELAND	OH	44112
1B546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
12969	UNITRODE CORP	WATERTOWN	MA	02172
17856	SILICONIX INC	SANTA CLARA	CA	95054
19209	GE CO ELEK CAP & BAT PROD DEPT	GAINSVILLE	FL	32601
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
32293	INTERSIL INC	CUPERTINO	CA	95014
32997	BOURNS INC TRIMPOT PROD DIV	RIVERSIDE	CA	92507
5L813	ASHLAND PRODUCTS CO	CHICAGO	IL	60628
51642	CENTRE ENGINEERING INC	STATE COLLEGE	PA	16801
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
71590	CENTRALAB ELEK DIV GLOBE-UNION INC	MILWAUKEE	WI	50501
72982	ERIE TECHNOLOGICAL PRODUCTS INC	ERIE	PA	16512
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108

C-7. APPENDIX CHANGES

The service information in this appendix is for 18177-60001 revision B boards. To adapt this information to revision A boards, note the following physical differences on revision A boards. Electrically revision A and revision B boards should operate the same.

R21 is soldered onto the circuit side of the main board between a feedthrough hole and J1 pin 18

R22 is soldered onto the circuit side of the main board between a feedthrough hole and J1 pin 19

C1 and C2 are loaded into the auxiliary board against the normal polarity convention and therefore appear to be backwards, but are not

U105 pin 1 is not tied to +5, but to U105 pin 2

U104 pin 1 is not tied to +5, but to U104 pin 2

U104 pin 5 is not tied to +5, but to U104 pin 6

U204 pin 1 is not tied to +5, but to U204 pin 2

U204 pin 5 is not tied to +5, but to U204 pin 6

C-8. SERVICE

The remainder of this appendix contains service information for the HP 18177A such as a block diagram, circuit theory, a V.35 Mnemonic Table, a component locator, schematics, and troubleshooting procedures.

Troubleshooting

Follow the troubleshooting procedures below which correspond to the error message (s) that are displayed after running the <EXT DLC> performance verification test described in paragraph C-4.

NO POD ATTACHED

When the <EXT DLC> test is run, the HP 4951C first checks to see if there is an interface pod attached by reading the pod ID lines.

	ID0 (J1-15)	ID1 (J1-16)	ID2 (J1-13)
No pod attached =	1	1	1
HP 18177A attached =	0	1	0

DCE TEST FAILED and DTE TEST FAILED

The second part of the <EXT DLC> test checks if the HP 4951C can drive the appropriate HP 18177A lines to simulate a DTE device and a DCE device. If both of these checks fail, the circuits that are common to both should be checked. These circuits are the power supplies, the mode control, and the control drivers.

Power Supplies

The pod uses +5 , +12, and -12 volts from the HP 4951C. The pod Pulse Width Modulator produces -5 volts. A +4.36 reference voltage and a +3.08 reference voltage are produced from the +12 volt supply by Q8 and part of U406.

If the -5 volt supply is bad, check the following points on the pod Auxiliary board.

Q1 pin 3	-5 volt reference
U500 pin 3	approximately 0 to +1 volt 35 kHz sawtooth
U500 pin 5	approximately 0 to +5 volt 35 kHz squarewave
CR1 cathode	approximately -5 to +5 volt 35 kHz squarewave

Mode Control

The mode control circuitry is located on the pod Auxiliary board and consists of the Relay Driver (U201), the DTE and DCE Relays (K100 and K101), the DTE and DCE Flip Flop (U300), and the Comparator (U301).

The HP 4951C drives the MONITOR, DTESIM, and DCESIM lines to select either the monitor mode, the DTE simulation mode, or the DCE simulation mode. MONITOR is pulsed when any of the three modes are selected to put the pod in a known state. If the DTE simulate or the DCE simulate mode is selected, then DTESIM or DCESIM is also pulsed.

When the <EXT DLC> test is run, MONITOR, DTESIM, and DCESIM should each pulse high once.

Control Drivers

The ~RSTA, ~DTRA, and ~DTRB lines from the HP 4951C are driven through the Control Drivers (part of U406) during both DTE simulation and DCE simulation. The outputs of the Control Drivers go to the Mode Control relays where they are demultiplexed depending on the selected mode.

When the <EXT DLC> test is run, ~RSTA, ~DTRA, and ~DTRB should toggle at TTL levels.

DTE TEST FAILED

If only the DTE portion of the <EXT DLC> test failed, enter and run the following DTE simulate program. This program will exercise the DTE lines so that the DTE signal paths and LEDs can be checked.

NOTE: "PRESS" indicates a hardkey, and "SELECT" indicates a softkey.

DTE Simulate Program

SELECT	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	DTE	(DTE clock)
	SYNC	(Mode)
	9600	(Bits/sec)
	D & S	(Disp mode)
PRESS	(HALT)EXIT	

(The Top Level Menu should be displayed.)

SELECT	Simulate
	DTE
	MORE
	Set Lead
	RTS
	On
	and then
	MORE
	WAIT
PRESS	1
	5
	0
	RTN
SELECT	Next Block
	MORE
	Set Lead
	RTS
	Off
	and then
	MORE
	Set Lead
	DTR
	On
	and then
	MORE
	WAIT

PRESS	1 5 0 RTN
SELECT	Next Block MORE Set Lead DTR Off and then MORE Goto Blk
PRESS	1 RTN (HALT)EXIT

(The Top Level Menu should now be displayed.)

SELECT	Run Menu Simulate

The DTE simulate program should be running now. Check the pod LEDs for the conditions listed below.

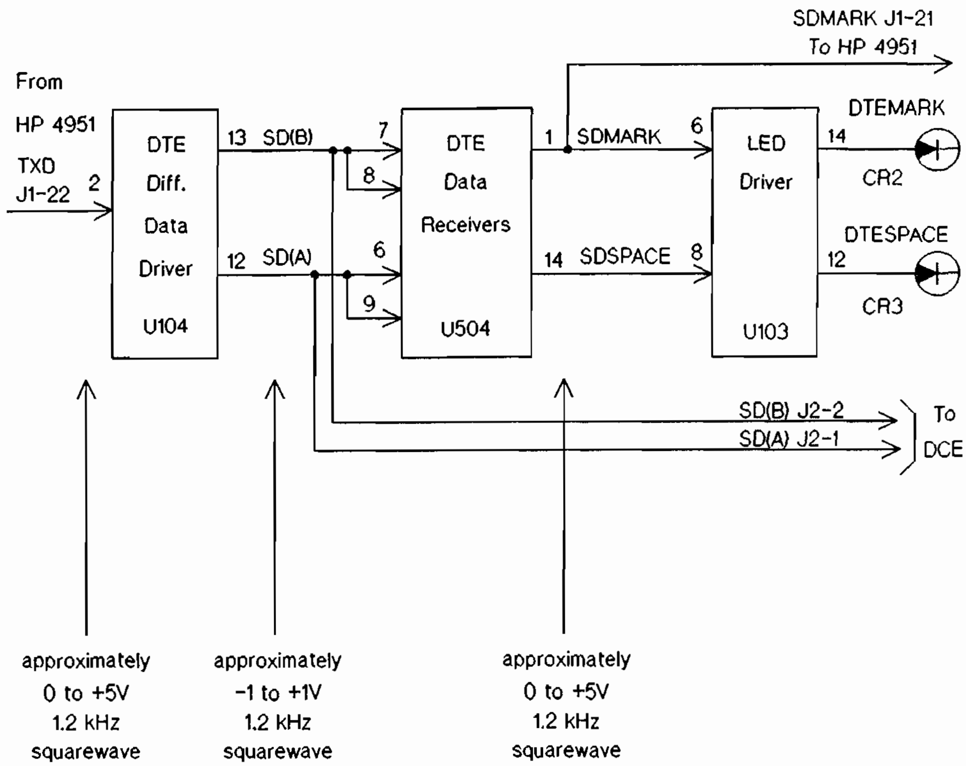
Pod LEDs

DTE			DCE		
	MARK	**SPACE**		**MARK**	**SPACE**
DTE	ON	ON	**DCE**	OFF	OFF
SCE	ON	ON	**SCT**	OFF	OFF
			SCR	OFF	OFF
	OFF	**ON**		**OFF**	**ON**
RS	B	B	**CS**	OFF	OFF
DTR	B	B	**DSR**	OFF	OFF
			CD	OFF	OFF

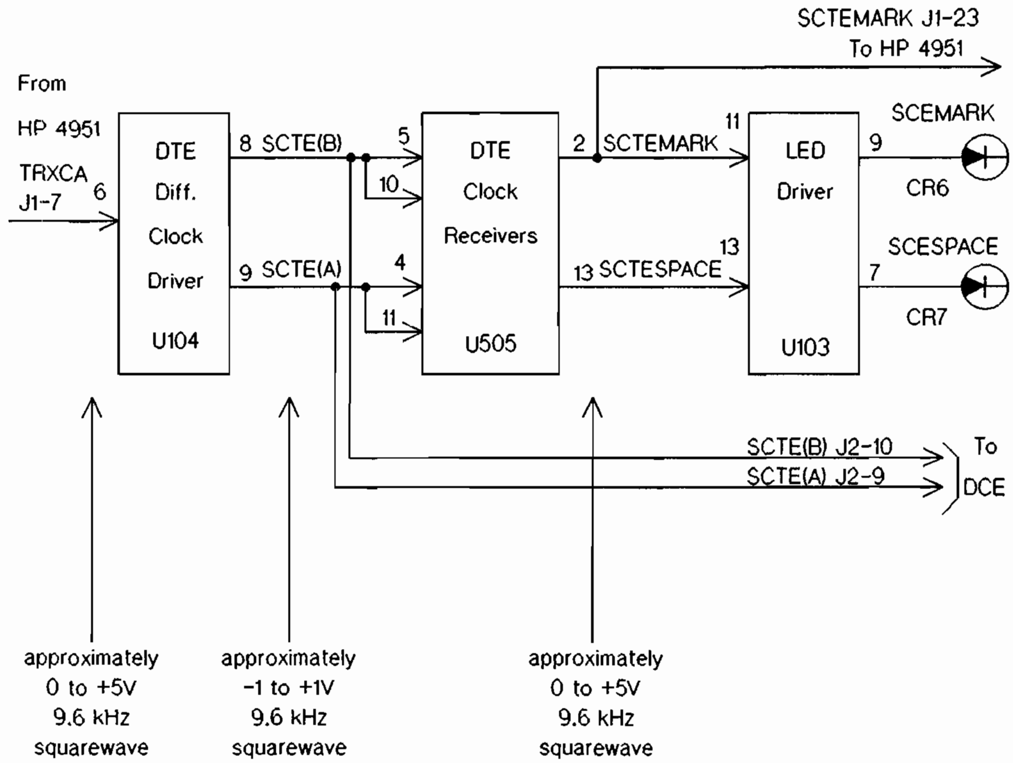
NOTE: B indicates blinking

If any of the DTE LEDs are incorrect, use an oscilloscope to check the DTE Data, Clock, and Control signal paths for the approximate voltages and frequencies listed in the block diagrams below.

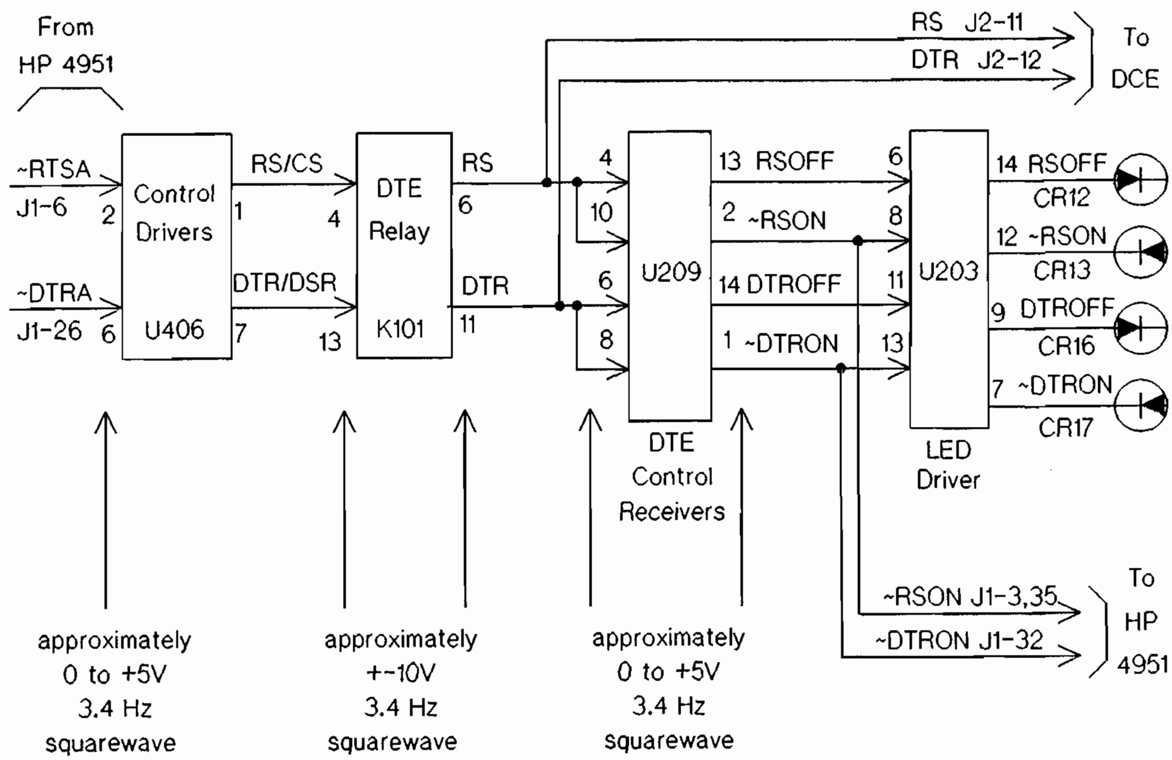
DTE Data Signal Path



DTE Clock Signal Path



DTE Control Signal Path



DCE TEST FAILED

If only the DCE portion of the <EXT DLC> test failed, enter and run the following DCE simulate program. This program will exercise the DCE lines so that the DCE signal paths and LEDs can be checked.

NOTE: "PRESS" indicates a hardkey, and "SELECT" indicates a softkey.

DCE Simulate Program

SELECT	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	DTE	(DTE clock)
	SYNC	(Mode)
	9600	(Bits/sec)
	D & S	(Disp mode)
PRESS	(HALT)EXIT	

(The Top Level Menu should be displayed.)

SELECT	Simulate
	DCE
	MORE
	Set Lead
	CTS
	On
	and then
	MORE
	WAIT
PRESS	1
	5
	0
	RTN
SELECT	and then
	MORE
	Set Lead
	DSR
	On
	and then
	MORE
	Set Lead
	CTS
	Off
	and then
	MORE
	WAIT

PRESS	1 5 0 RTN
SELECT	and then MORE Set Lead CD On and then MORE Set Lead DSR Off and then MORE WAIT
PRESS	1 5 0 RTN
SELECT	and then MORE Set Lead CD Off and then MORE WAIT
PRESS	1 5 0 RTN
SELECT	Next Block MORE Goto Blk
PRESS	1 RTN (HALT)EXIT

(The Top Level Menu should now be displayed.)

SELECT	Run Menu Simulate

The DCE simulate program should be running now. Check the pod LEDs for the conditions listed below.

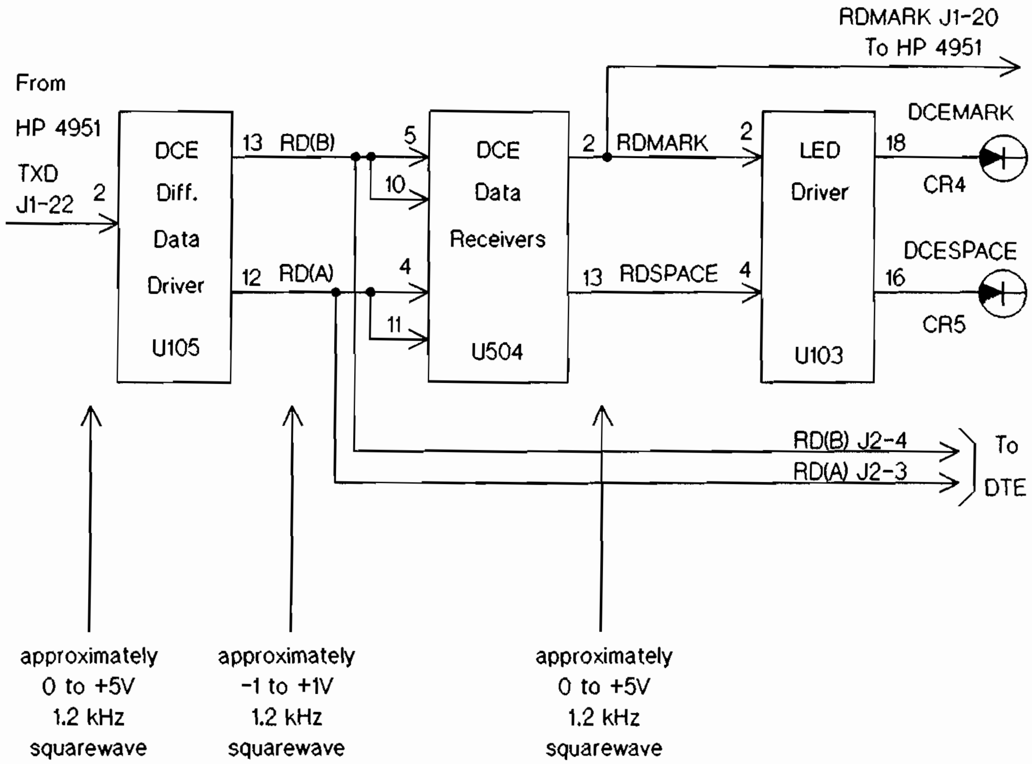
Pod LEDs

DTE			DCE		
	MARK	**SPACE**		**MARK**	**SPACE**
DTE	OFF	OFF	**DCE**	ON	ON
SCE	OFF	OFF	**SCT**	ON	ON
			SCR	ON	ON
	OFF	**ON**		**OFF**	**ON**
RS	OFF	OFF	**CS**	B	B
DTR	OFF	OFF	**DSR**	B	B
			CD	B	B

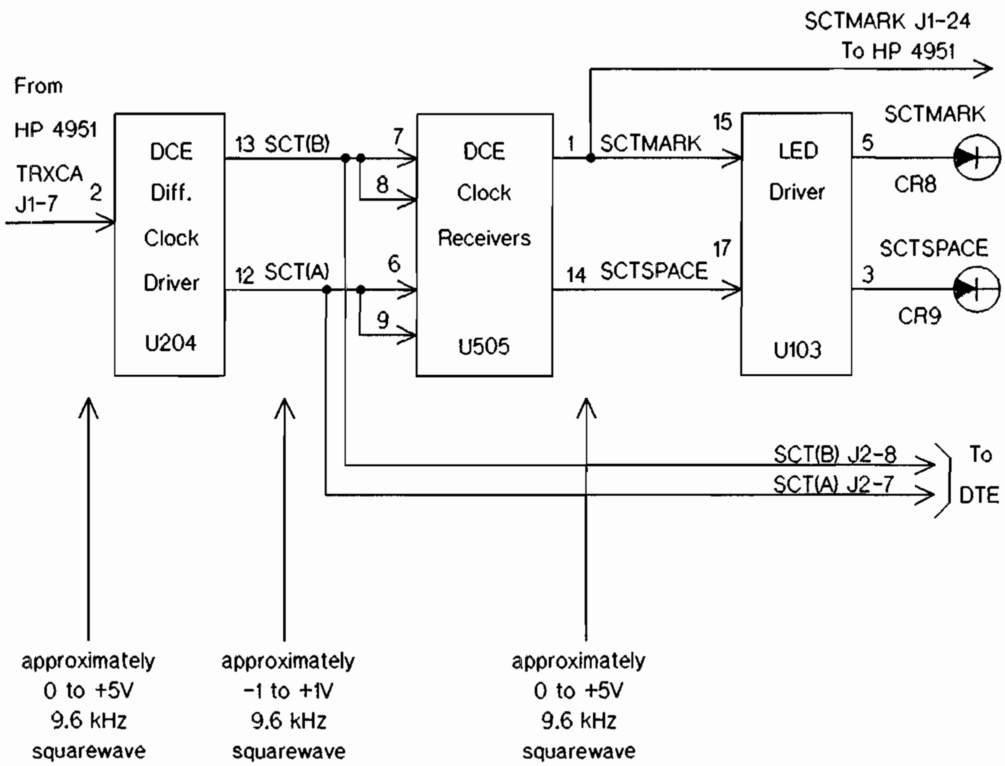
NOTE: B indicates blinking

If any of the DCE LEDs are incorrect, use an oscilloscope to check the DCE Data, Clock, and Control signal paths for the approximate voltages and frequencies listed in the block diagrams below.

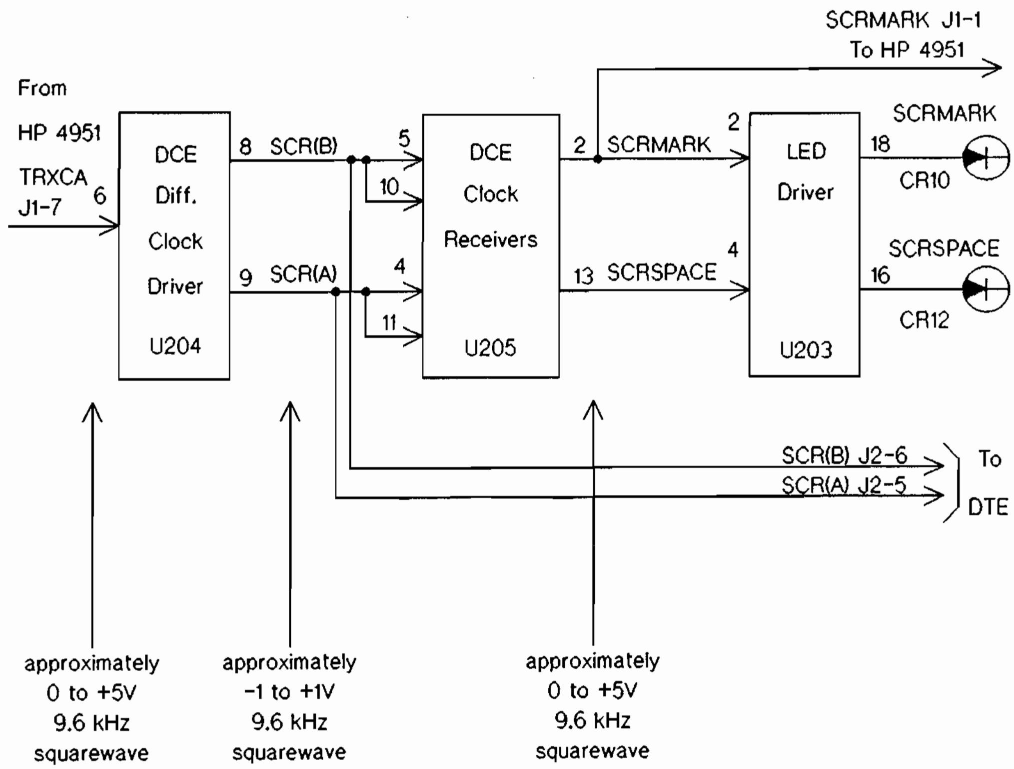
DCE Data Signal Path



DCE Clock Signal Paths



DCE Clock Signal Paths (cont.)



DCE Control Signal Path

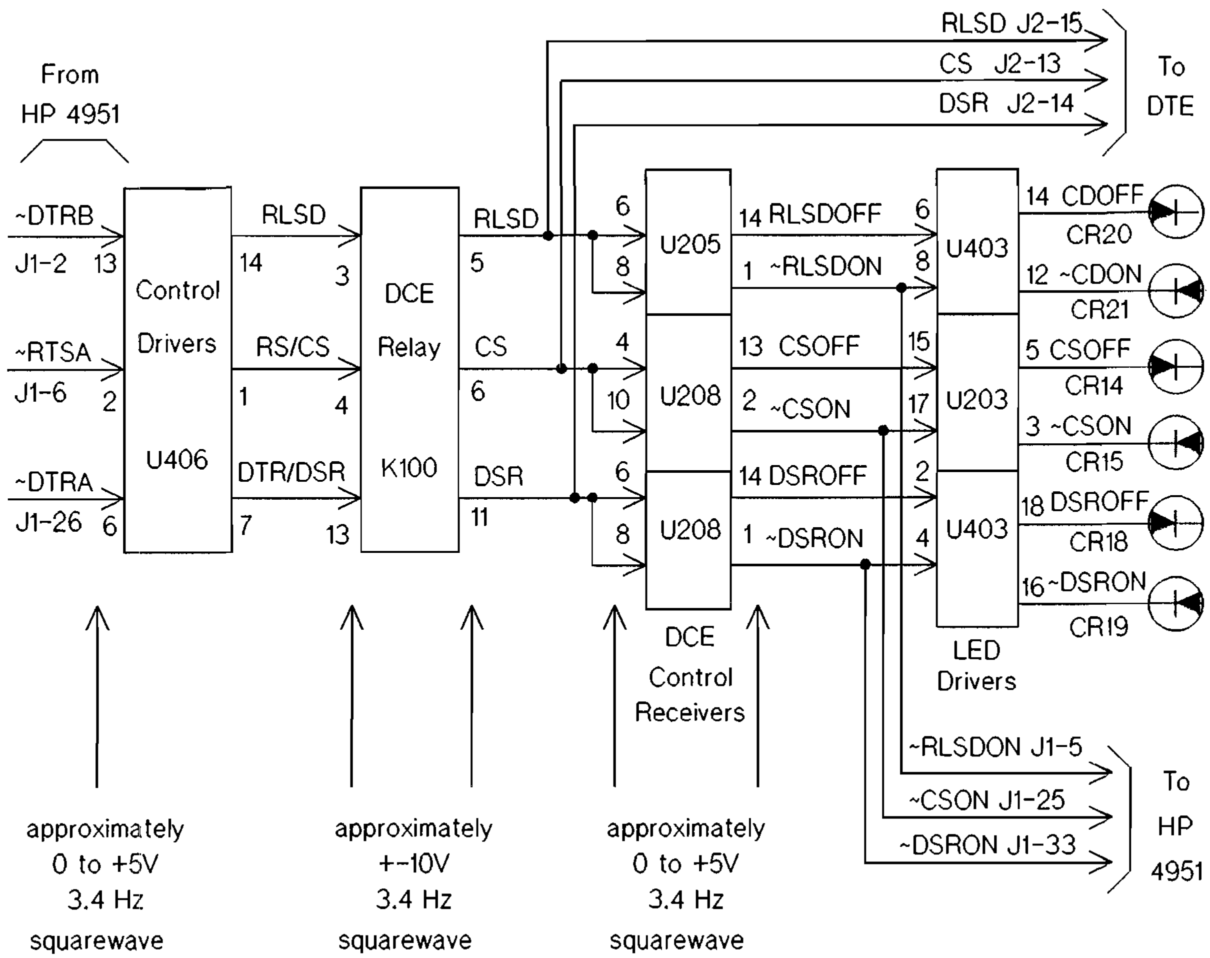


Table C-3. V.35 Cross Reference

POD MARK/ SPACE LEDS	POD SCHEM. MNEMON.	SIGNAL	CCITT	V.35 Y-CABLE PIN #		SIGNAL FROM	
				Y ENDS	POD END	DCE	DTE
Data Lines:							
DTE	SD (A) SD (B)	Transmit Data*	103	P S	1 2		x x
DCE	RD (A) RD (B)	Receive Data*	104	R T	3 4	x x	
Clock Lines:							
SCE	SCTE (A) SCTE (B)	Serial Clk Xmit Ext.*	113	U W	9 10		x x
SCT	SCT (A) SCT (B)	Serial Clk Xmit*	114	Y AA	7 8	x x	
SCR	SCR (A) SCR (B)	Serial Clk Rcv*	115	V X	5 6	x x	
Control Lines:							
RS	RS	Request To Send	105	C	11		x
DTR	DTR	Data Terminal Ready	108/2	H	12		x
CS	CS	Clear To Send	106	D	13	x	
DSR	DSR	Data Set Ready	107	E	14	x	
CD	RLSD	Rcv Line Sig. Detect (Carrier Detect)	109	F	15	x	
-	GND	Protective Ground	101	A	16	-	-
-	-	Not Used	-	-	17 - 37	-	-

* Differential Pairs

V.35 Signal Functions

DTE LINES:

Note: DTE lines are driven either by the DTE device during monitor mode, or by the HP 4951 during DTE simulation.

SD (DTE) TRANSMIT DATA - The SD signal is a balanced signal used by the DTE device to transmit serial data to the DCE device on the SD(A) and SD(B) leads. This signal is in phase with the SCTE signal. The relative timing of SD with respect to SCTE is explained in the SCTE description. The SD(A) lead should be negative with respect to the SD(B) lead for a mark or binary one condition.

SCTE (SCE) SERIAL CLOCK TRANSMIT EXTERNAL - The SCTE signal is a balanced clock transmitted by the DTE device to the DCE device over the SCTE(A) and SCTE(B) leads. SCTE is generated by the DTE device from the SCT signal provided by the DCE device. The SD signal should be sampled by the DCE device coincident with the negative edge zero crossing of SCTE(A) minus SCTE(B).

RS REQUEST TO SEND - The RS control lead must be in the ON condition before the DCE device will transmit data. This circuit conforms to CCITT V.28 electrical standards.

DTR DATA TERMINAL READY - The DTR control lead must be turned ON by the DTE device to enable the DCE device to answer a call. It must be turned OFF to terminate a call. This circuit conforms to CCITT V.28 electrical standards.

DCE LINES:

Note: DCE lines are driven either by the DCE device during monitor mode, or by the HP 4951 during DCE simulation.

RD (DCE) RECEIVE DATA - The RD signal is a balanced signal driving the RD(A) and RD(B) leads to the DTE device. This signal is in phase with SCR. The relative timing between the data on RD and SCR is explained in the SCR description.

SCR SERIAL CLOCK RECEIVE - The SCR circuit is a balanced signal driving the SCR(A) and SCR(B) leads to the DTE device. The data changes on the RD lead are coincident (within +-10% of a clock cycle) with the positive edge zero crossing of SCR(A) minus SCR(B).

SCT SERIAL CLOCK TRANSMIT - SCT is a 1.344 MHz balanced clock signal transmitted on the SCT(A) and SCT(B) leads. SCT is used by the DTE device to synchronize the clocking of data to the DCE, and to generate the SCTE clock.

CS CLEAR TO SEND - When the CS control lead is ON, then data transmission from the DTE device is permitted. This circuit conforms to CCITT V.28 electrical standards.

DSR DATA SET READY - When the DSR control lead is ON, the DCE device is ready to receive data from the DTE device provided the CS lead is ON. This circuit conforms to CCITT V.28 electrical standards.

RLSD (CD) RECEIVED LINE SIGNAL DETECTOR (CARRIER DETECT) - When the RLSD control lead is ON this indicates that the signals on the RD lead are reliable. This circuit conforms to CCITT V.28 electrical standards.

Interface Pod Circuit Theory

Refer to the 18177A Block Diagram Figure C-9 when reading the following description. For more information on the different modes of operation refer to the theory of operation located under paragraph C-3.

DATA AND CLOCK DIFFERENTIAL DRIVERS

There are five differential drivers, 2 for data lines (RD and SD) and 3 for clock lines (SCR, SCT, and SCTE). RD is the DCE data line and SD is the DTE data line. SCR and SCT are the DCE clock lines, and SCTE is the DTE clock line.

The TXD and TRXCA signals from the HP 4951 drive the differential drivers to create the data and clock signals during simulation modes. Each of the five drivers provide a differential output (A and B). When one output is sinking current, the other is in tri-state. Both outputs can be tri-stated simultaneously by a low on the inhibit input.

The differential drivers are powered by +5 volts and -5 volts. -5 volts is derived on the pod in the -5 volt Switching Power Supply block.

The following function table shows how the differential drivers operate.

Inputs	**Inhibit**	**Outputs**	
TXD or TRXCA	**DCE or DTE**	**(B)**	**(A)**
X	L	OFF	OFF
L	H	ON	OFF
H	H	OFF	ON

JFETS AND RESISTOR NETWORKS

The current outputs from the data and clock differential drivers are converted to the proper V.35 voltage levels by resistor networks. The resistor networks generate the proper V.35 differential source impedance as well as the short circuit impedance specifications:

Voltage levels	+-0.55 volts
Source Impedance	50 to 100 ohms
Short Circuit Impedance	127 to 172 ohms

JFETs in series with the resistor networks allow the differential loads to be switched out during monitor operation. This is done by the SIM/~MONJFET signal which controls the gates of the JFETs.

DATA AND CLOCK RECEIVERS

Ten receivers monitor the ten differential outputs from the data and clock drivers. The outputs of the receivers drive the LED Drivers. Two receivers monitor each differential pair so that both the Mark and the Space LEDs can be off at the same time to indicate that no signal is present on the line. The receiver outputs also go to the HP 4951 for analysis.

LED DRIVERS AND MARK/SPACE LEDS

The 10 outputs from the data and clock receivers and the 10 outputs from the control receivers drive the LED drivers to control the Mark (off) and Space (on) LEDs.

Data and Clock Differential Lines:

MARK LED is on when (B) > (A) + 0.39* volts

SPACE LED is on when (A) > (B) + 0.39* volts

Neither LED is on when |(A) - (B)| < 0.39* volts

*Note: CCITT V.35 specifications call for a differential voltage of .55 volts +- 20%. The HP 18177A is specified to .55 volts +- 30%.

Control Lines:

OFF LED on indicates < -2.8 volts on the line

ON LED on indicates > 0.25 volts on the line

Neither LED on indicates -2.8 < volts < .25 on the line

CONTROL DRIVERS

Three single-ended drivers are used to generate the 5 control lines (RS, DTR, CS, DSR, and RLSD). The RS and DTR control lines are DTE, while CS, DSR, and RLSD are DCE. Since either only the DTE control lines or the DCE control lines need to be driven at any one time (during DTE simulation and DCE simulation respectively) only three control drivers are needed. The inputs to the control drivers (~RTSA, ~DTRA, and ~DTRB) come from the HP 4951.

The outputs of the control drivers conform to the CCITT V.28 electrical standard (same as RS-232C) with -12 volts for a mark (1, off), and +12 volts for a space (0, on). Capacitors in series with the control driver outputs provide compensation for capacitive loads. Resistors in series with the control driver outputs provide current limiting. The control driver outputs go to the Mode Control circuits on the pod Auxiliary Board through the W1 Interconnect Cable.

MODE CONTROL

The mode control circuits configure the pod for the desired mode of operation: either monitor mode, DTE simulation mode, or DCE simulation mode. The mode control signals (MONITOR, DCESIM, and DTESIM) come from the HP 4951 to the J1 connector of the pod Main Board through the Interface Pod Cable. Then they routed through the W1 Interconnect Cable to the pod Auxiliary Board.

Relay Driver

The Relay Driver contains 8 darlington drivers. Three of the darlington outputs drive the DTE and DCE relays to either isolate the control driver outputs from the control receivers (by setting the relays during monitor mode) or to demultiplex the control driver outputs (by resetting the relays during either simulation mode).

The other five darlingtons are used as open collector inverters in conjunction with the DTE and DCE Flip Flops to create the DTE, DCE, and SIM/~MONJFET control signals for the data and clock differential drivers, and the JFETs and Resistor Networks.

DTE and DCE Flip Flops

The DTE and DCE Flip Flops create the DTE and DCE control signals. When either DTESIM or DCESIM from the HP 4951 pulses high, the corresponding Flip Flop is clocked and its Q output goes high. The Q outputs (DTE and DCE) perform two functions. They go to the inhibit inputs on the data and clock differential drivers to control which drivers are inhibited. They also are logically ORed by the Relay Driver to produce the SIM/~MON signal. SIM/~MON drives a comparator (U301) which creates SIM/~MONJFET. If either of the Q outputs are high, then SIM/~MONJFET is high to enable the gates of the JFETs on the outputs of the data and clock differential drivers.

DTE Q OUTPUT HIGH:	DCE Q OUTPUT HIGH:
SD data driver enabled	RD data driver enabled
SCTE clock driver enabled	SCR clock driver enabled
JFETs enabled	SCT clock driver enabled
	JFETs enabled

DTE and DCE Relays

The DTE and DCE Relays (K100 and K101) isolate the control driver outputs from the control receivers during monitor mode operation. During either of the simulation modes the relays demultiplex the control driver outputs to the correct control receivers.

The relays are 2 coil latching relays so that the coils only need to be pulsed to change states.

CONTROL RECEIVERS

There are 10 receivers used for the five control lines; 2 receivers per line. The outputs of the receivers drive the LED Drivers. Two receivers are used so that both the ON and OFF LEDs can be off at the same time to indicate that no signal is present on the line. The control receiver outputs also go to the HP 4951 for analysis.

- 5V SWITCHING POWER SUPPLY

The pod uses a switching power supply to create -5 volts for the data and clock differential drivers. U500 is used to control the frequency, duty cycle and current consumption of the power supply. +5 volts from the HP 4951 is used as VCC for U500. C22 sets the operating frequency at approximately 35 kHz. -12 volts from the HP 4951 is regulated by Q1 to produce a -5 volt reference (-5 REF). This reference is compared to the -5 volt output by comparator U301. The output of U301 drives pin 5 of U500 to control the duty cycle of output pin 8. Pin 8 controls Switching Transistor Q2. Pin 7 of U500 monitors the current through R14 and R17 to control the current limit operation of U500.

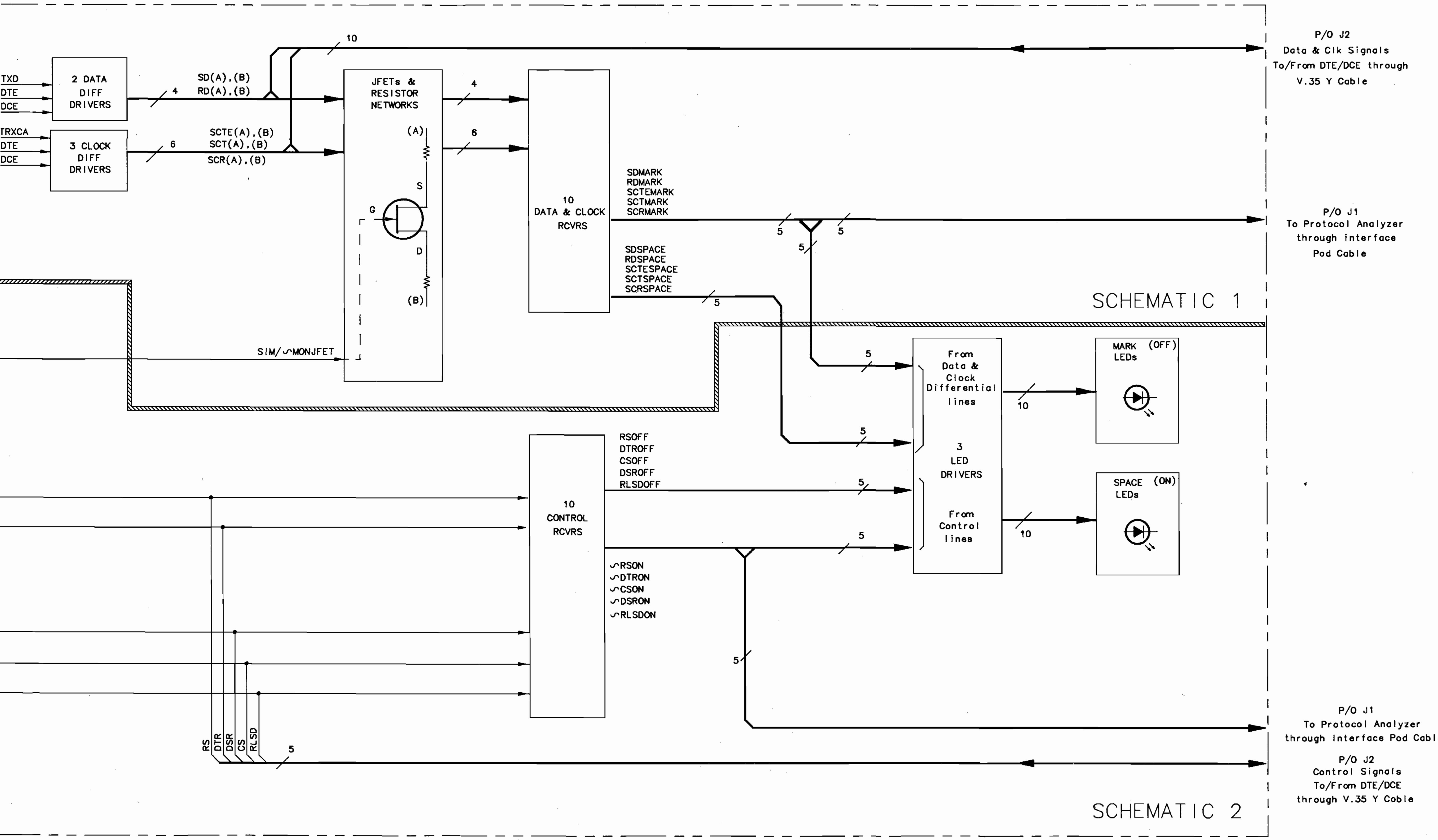
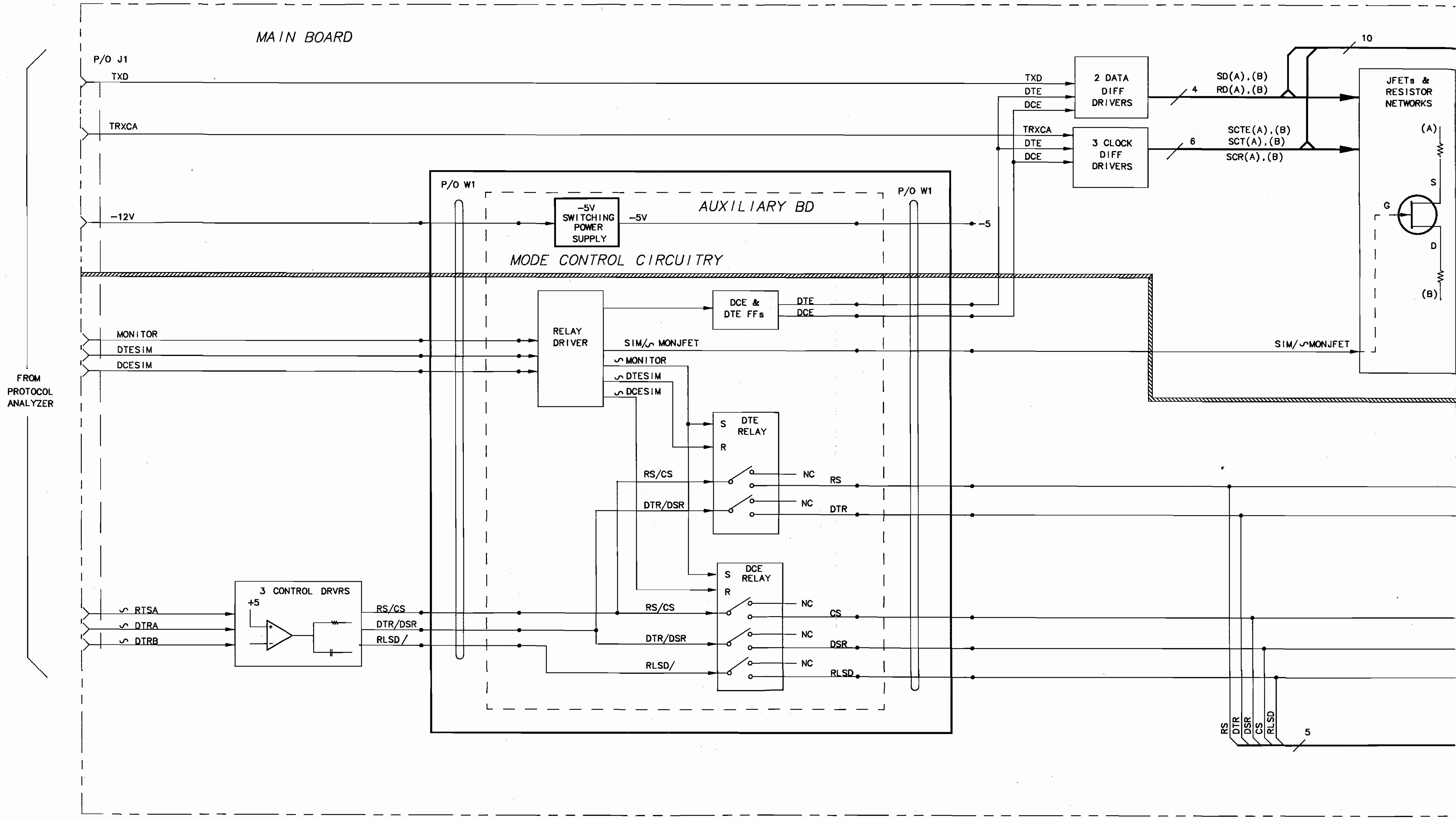
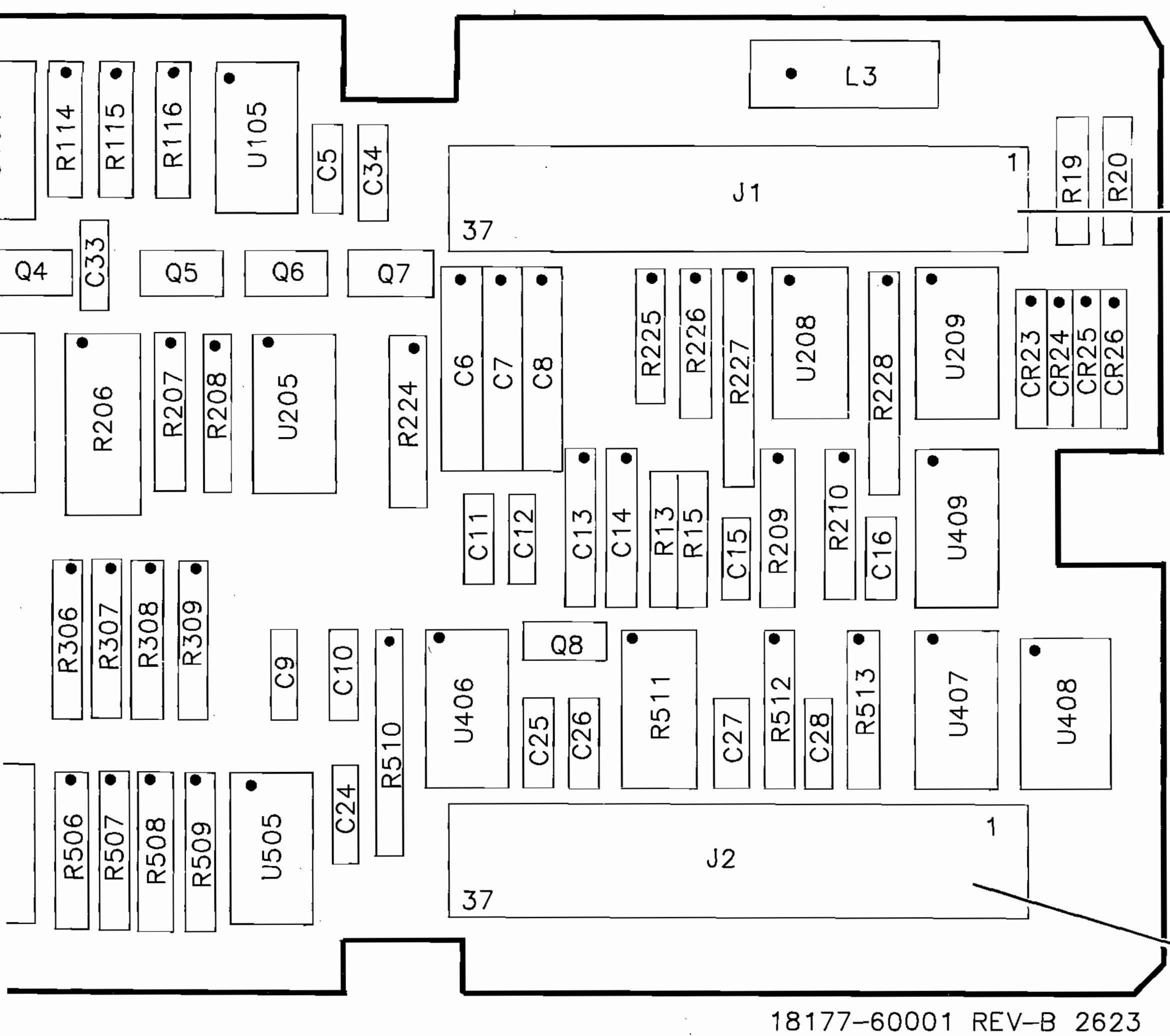


Figure C-9. HP 18177A Block Diagram


MAIN BOARD
P/O J1
TXD
TRXCA
-12V
MONITOR
DTESIM
DCESIM
FROM PROTOCOL ANALYZER
∽ RTSA
∽ DTRA
∽ DTRB
3 CONTROL DRVRS
+5
RS/CS
DTR/DSR
RLSD/
P/O W1
AUXILIARY BD
-5V SWITCHING POWER SUPPLY
-5V
-5
MODE CONTROL CIRCUITRY
RELAY DRIVER
DCE & DTE FFs
DTE
DCE
SIM/∽ MONJFET
∽ MONITOR
∽ DTESIM
∽ DCESIM
DTE RELAY
S
R
NC
RS
DTR
DCE RELAY
CS
DSR
RLSD
2 DATA DIFF DRIVERS
3 CLOCK DIFF DRIVERS
SD(A),(B)
RD(A),(B)
SCTE(A),(B)
SCT(A),(B)
SCR(A),(B)
4
6
10
5
JFETs & RESISTOR NETWORKS
(A)
(B)
S
G
D
SIM/∽MONJFET



INTERFACE POD CABLE SIGNALS (J1)

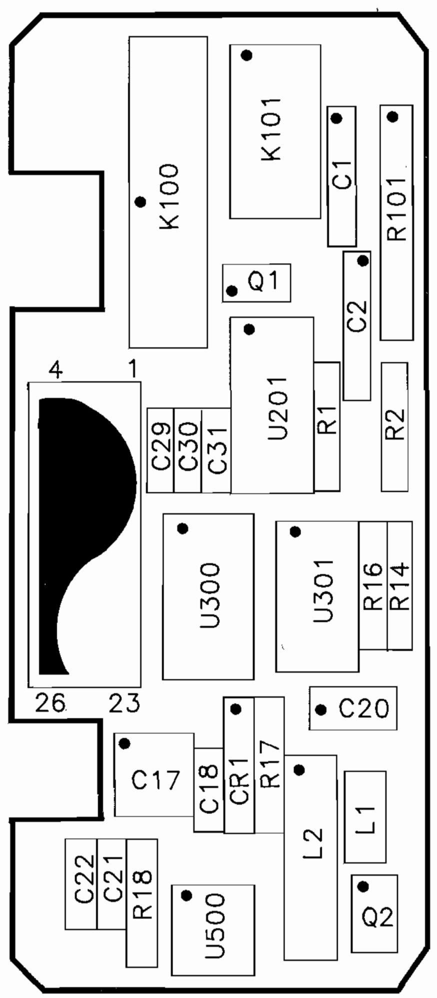
Pod End J1 Pin #	Pod Signal Name	Signal Direction HP 4951 Pod
1	SCRMARK	<--------
2	~DTRB	-------->
3	~RSON	<--------
4	GND	-------->
5	~RLSDON	<--------
6	~RSTA	-------->
7	TRXCA	-------->
8	+12V	-------->
9	-12V	-------->
10	+5V	-------->
11	unused	
12	unused	
13	ID2	<--------
14	GND	-------->
15	ID0	<--------
16	ID1	<--------
17	unused	
18	MONITOR	-------->
19	DTESIM	-------->
20	RDMARK	<--------
21	SDMARK	<--------
22	TXD	-------->
23	SCTEMARK	<--------
24	SCTMARK	<--------
25	~CSON	<--------
26	~DTRA	-------->
27	+12V	-------->
28	-12V	-------->
29	+5V	-------->
30	unused	
31	unused	
32	~DTRON	<--------
33	~DSRON	<--------
34	unused	
35	~RSON	<--------
36	GND	-------->
37	DCESIM	-------->

V.35 Y CABLE SIGNALS (J2)

Pod End J2 Pin #	Pod Signal Name	Y End Pin #
1	SD(A)	P
2	SD(B)	S
3	RD(A)	R
4	RD(B)	T
5	SCR(A)	V
6	SCR(B)	X
7	SCT(A)	Y
8	SCT(B)	AA
9	SCTE(A)	U
10	SCTE(B)	W
11	RS	C
12	DTR	H
13	CS	D
14	DSR	E
15	RLSD	F
16	GND	A
17-37	unused	

Figure C-10. HP 18177A Component Locator

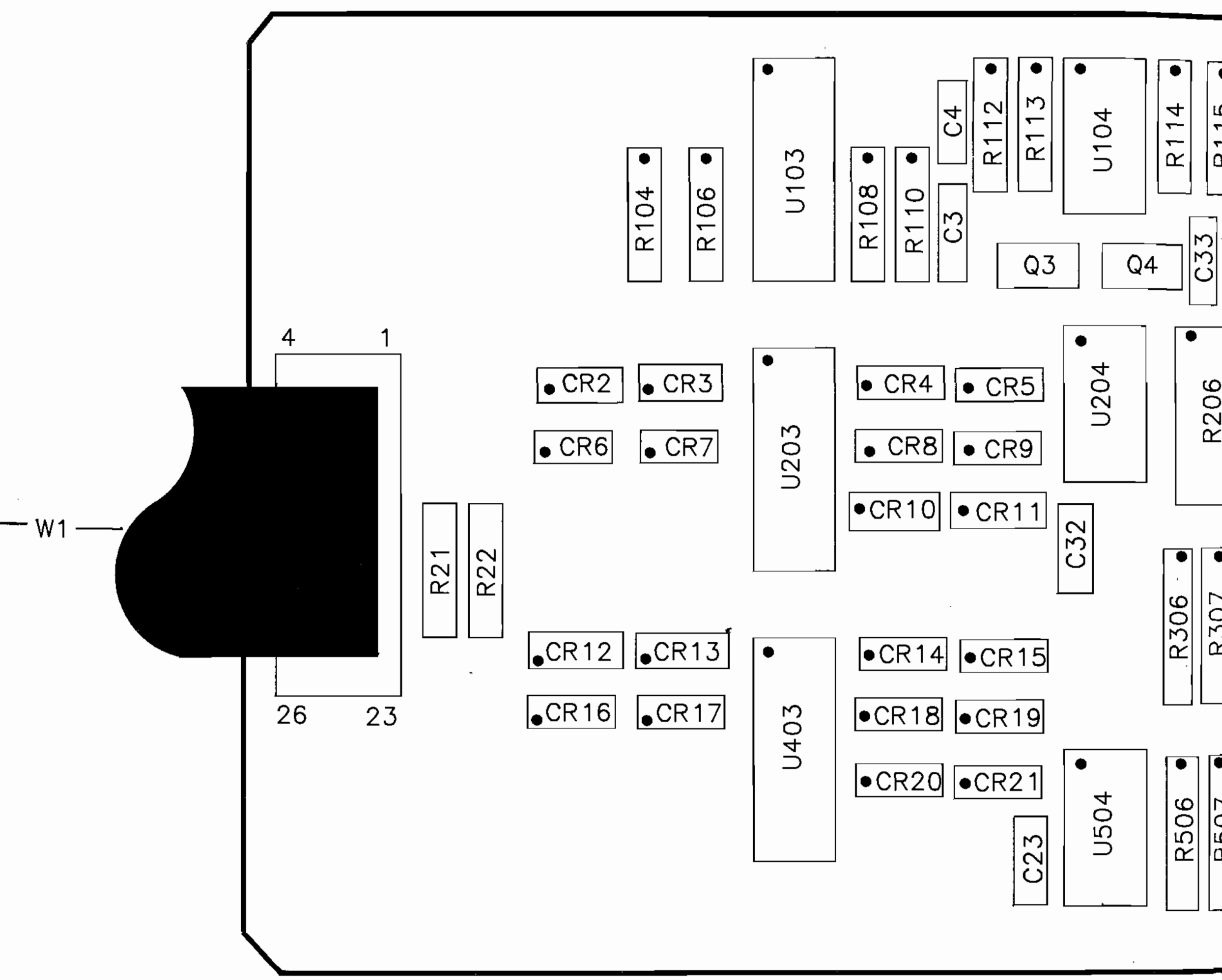
AUXILIARY BOARD

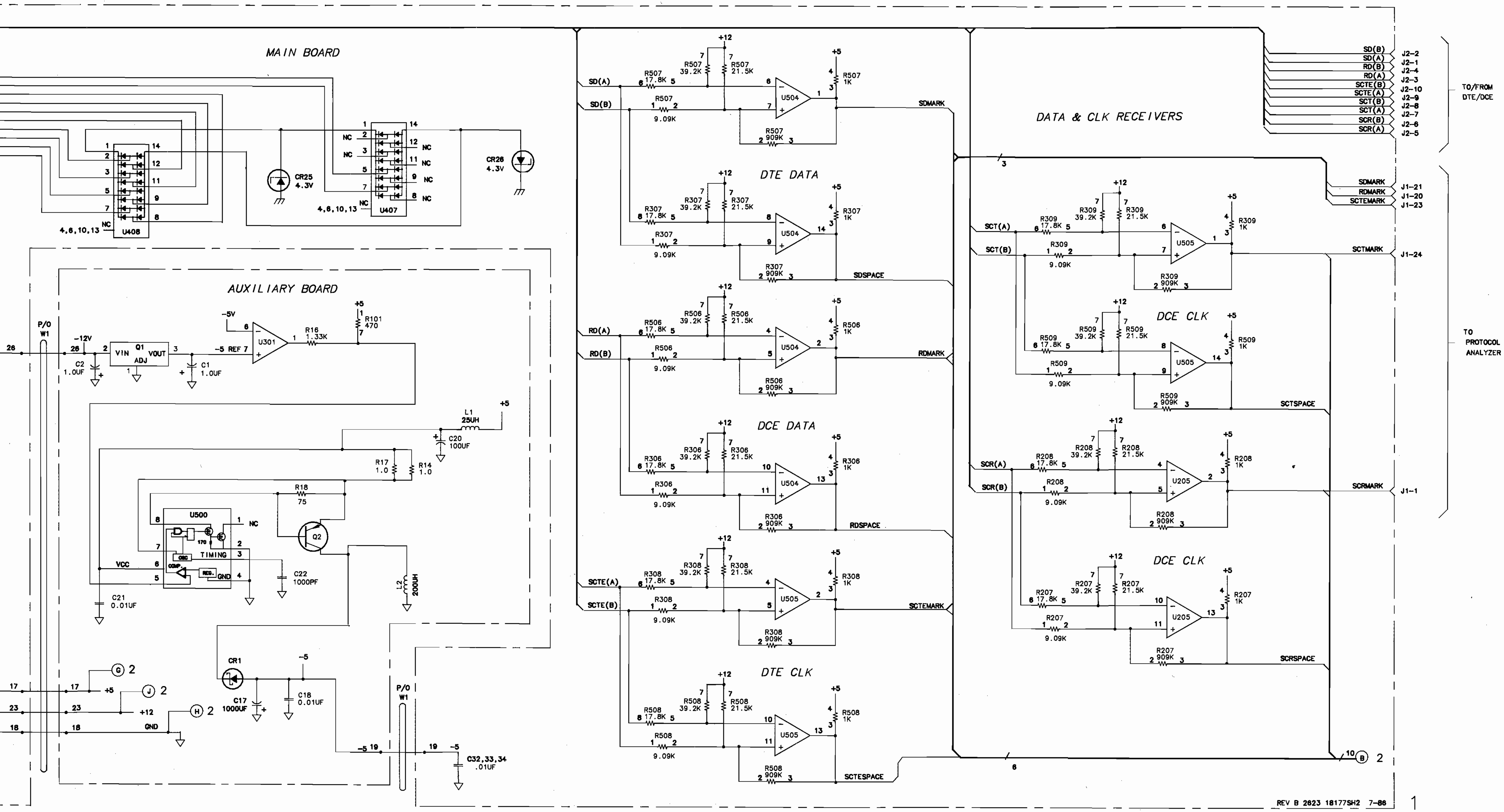


INTERCONNECT CABLE SIGNALS (W1)

W1 Interconnect Cable Pin #	Pod Signal Name	Signal Direction Main Bd. Aux. Bd.
1	RS/CS	---------->
2	DTR/DSR	---------->
3	unused	
4	unused	
5	RLSD/	---------->
6	unused	
7	RS	<----------
8	DTR	<----------
9	CS	<----------
10	DSR	<----------
11	RLSD	<----------
12	unused	
13	MONITOR	---------->
14	DTESIM	---------->
15	DCESIM	---------->
16	SIM/~MONJFET	<----------
17	+5V	---------->
18	GND	---------->
19	-5V	<----------
20	DCE	<----------
21	DTE	<----------
22	unused	
23	+12V	---------->
24	unused	
25	unused	
26	-12V	---------->

MAIN BOARD



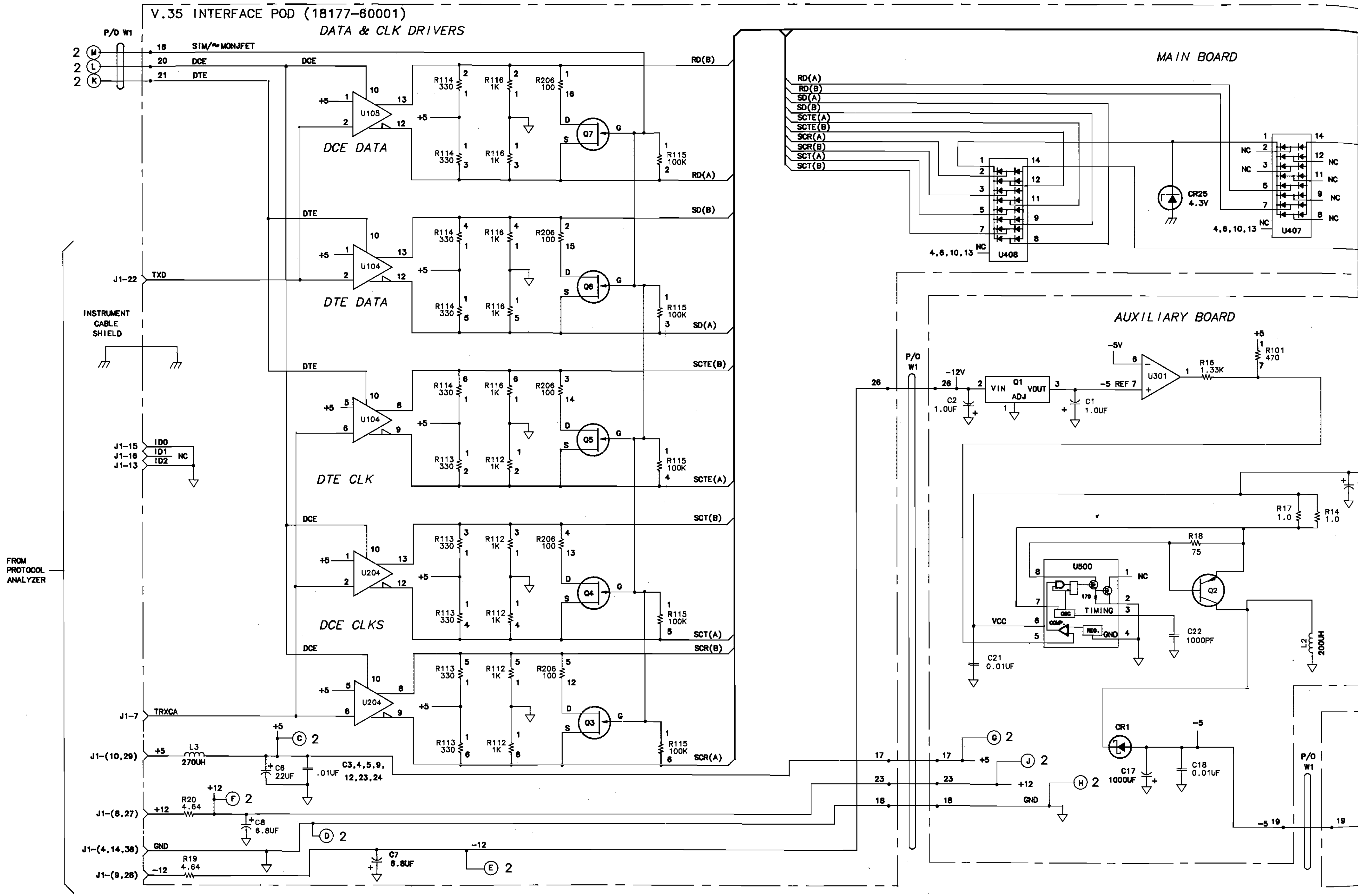


1

Figure C-11. HP 18177A Schematic 1

ower and Ground Connections

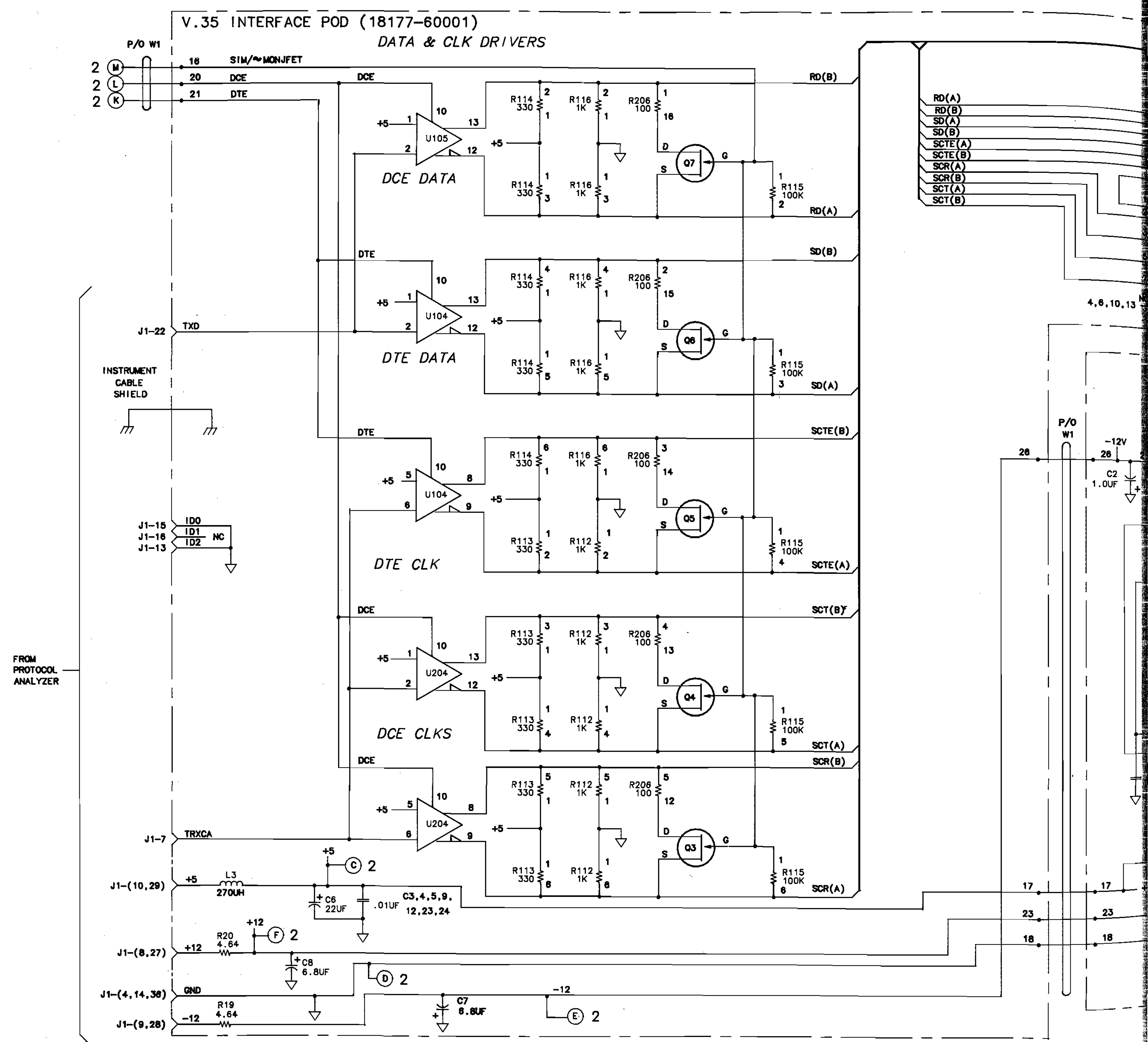
Pin	-5V Pin	-12V Pin
	11	
	11	
	11	
		12
		11



NOTE: ~ DENOTES A LOW TRUE SIGNAL.

Table C-4. HP 18177A Digital IC Power and Ground Connections

Ref. Desig.	GND Pin	+5V Pin	+12V Pin	-5V Pin	-12V Pin
U103	10	20			
U104	7	3,4,14		11	
U105	7	3,4,14		11	
U201	8	9			
U203	10	20			
U204	7	3,4,14		11	
U205	12		3		
U208	12		3		
U209	12		3		
U300	7	14			
U301			3		12
U403	10	20			
U406			4		11
U500	4				
U504	12		3		
U505	12		3		



NOTE: ~ DENOTES A LOW TRUE SIGNAL.

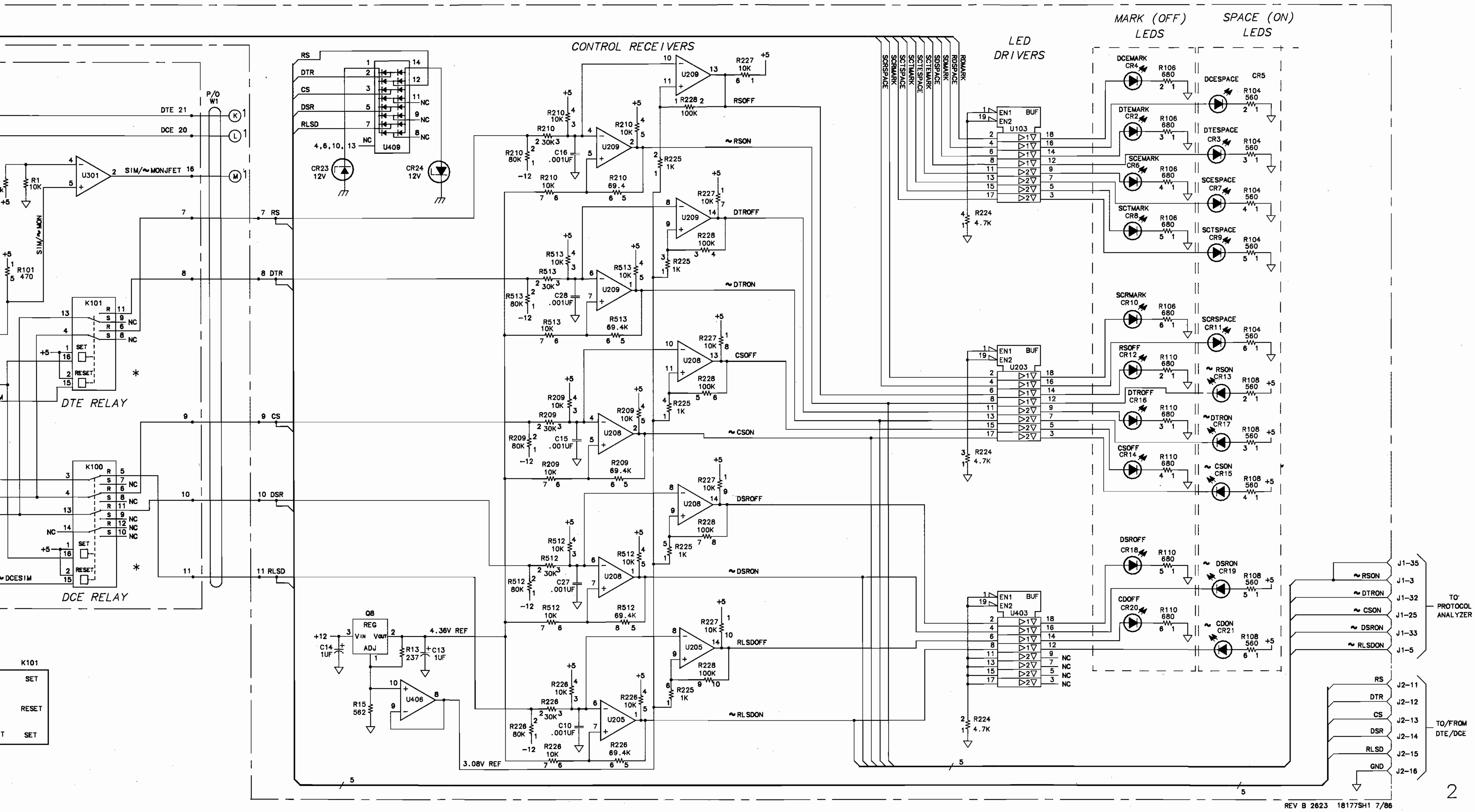
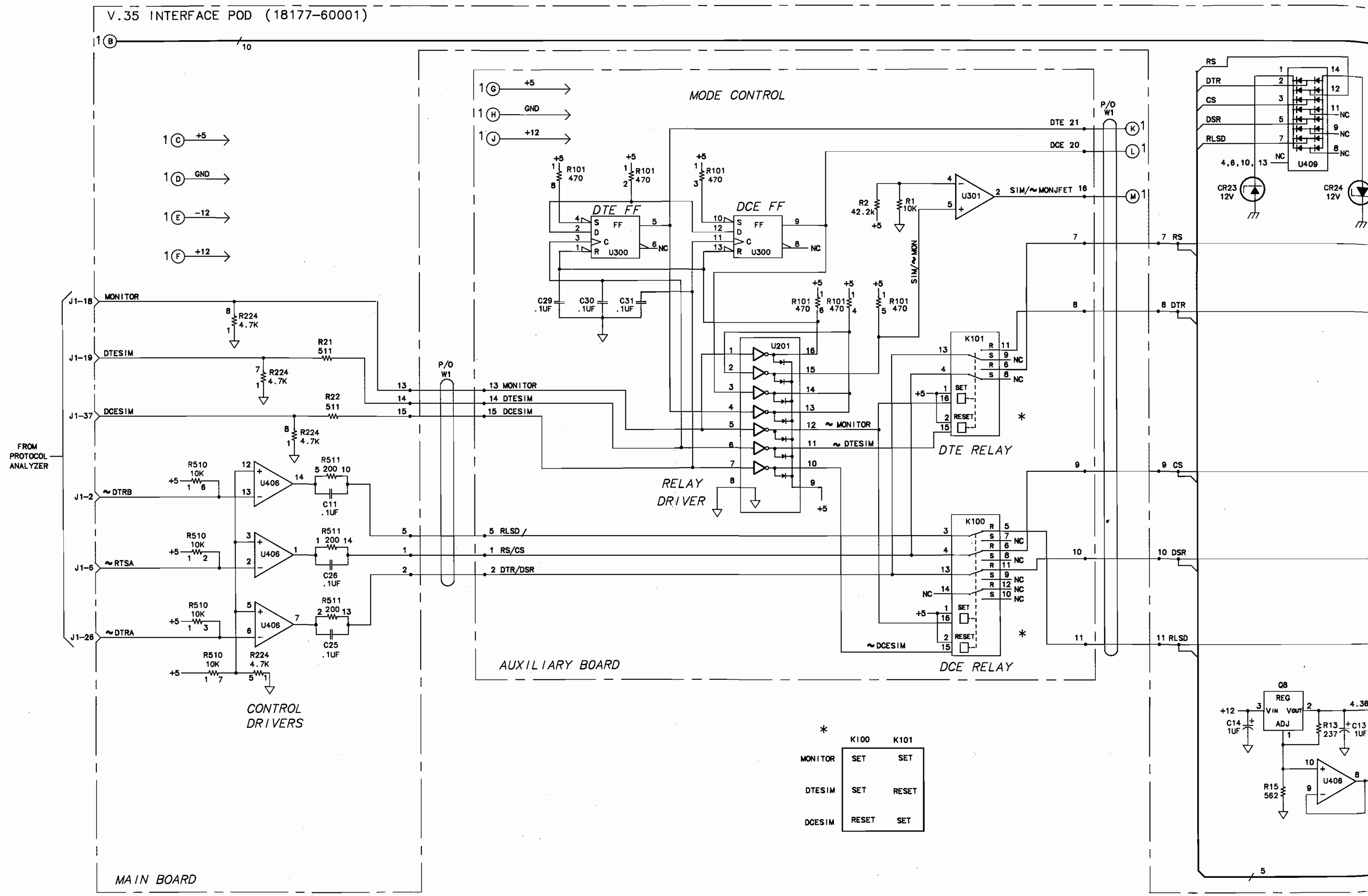


Figure C-12. HP 18177A Schematic 2



NOTE: ~ DENOTES A LOW TRUE SIGNAL.

APPENDIX D
HP 18179A
RS-232C/V.24 INTERFACE POD

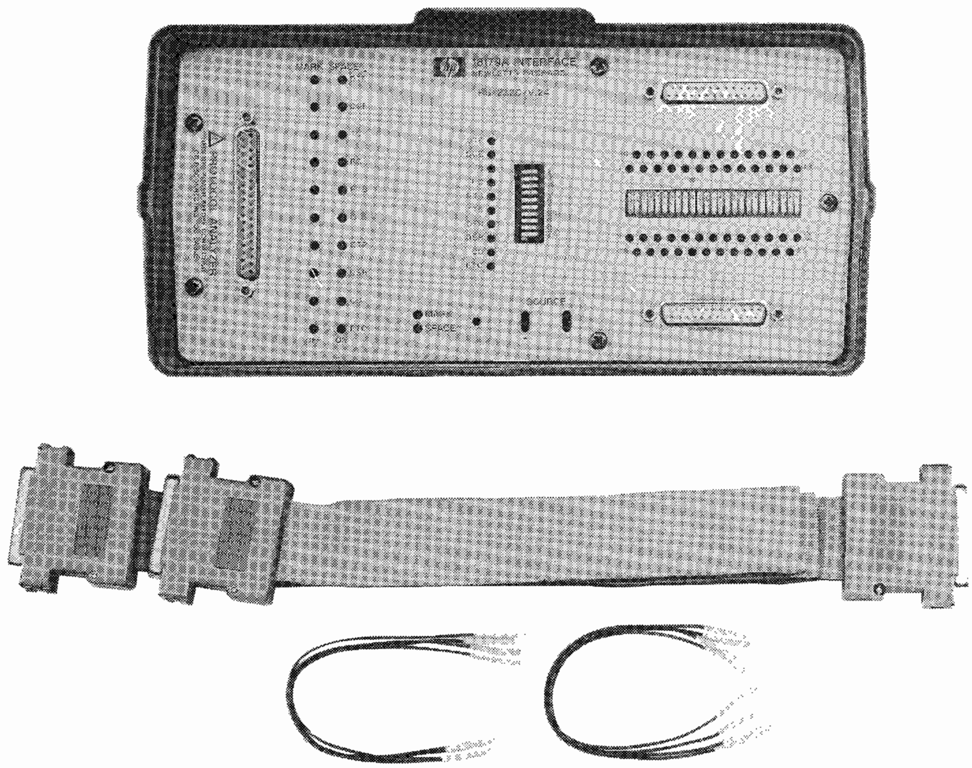


Figure D-1. HP 18179A Interface Pod

D-1. INTRODUCTION

The HP 18179A is an RS-232C/V.24 Interface Pod designed to provide the connection between the HP 4951C Protocol Analyzer and Data Terminal Equipment (DTE) and/or Data Circuit-Terminating Equipment (DCE). It supports three modes of operation: monitor, DTE simulate, and DCE simulate. The HP 18179A is compatible with CCITT V.24 and EIA RS-232C electrical, mechanical, functional, and procedural specifications.

This appendix includes information to install, operate, and service the HP 18179A.

D-2. INSTALLATION

To connect the Interface Pod to the HP 4951C Protocol Analyzer, turn off the power and attach the Interface Pod connector to the port on the back of the Protocol Analyzer. Tighten the screws to ensure that the cable will not pull off during operation.

CAUTION

Turn off the Protocol Analyzer before connecting or disconnecting any Interface Pod.

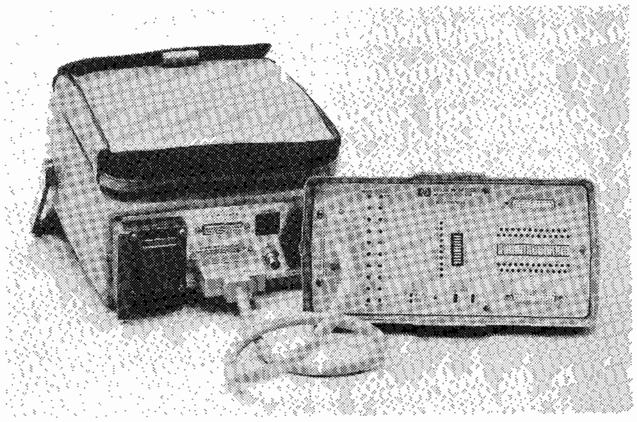


Figure D-2. Interface Pod Connection

D-3. OPERATION

This section describes the front panel controls, indicators, and connectors, as well as operation of the HP 18179A Interface Pod. Read the description of the front panel controls, indicators, and connectors before operating the instrument.

Controls, Indicators, and Connectors

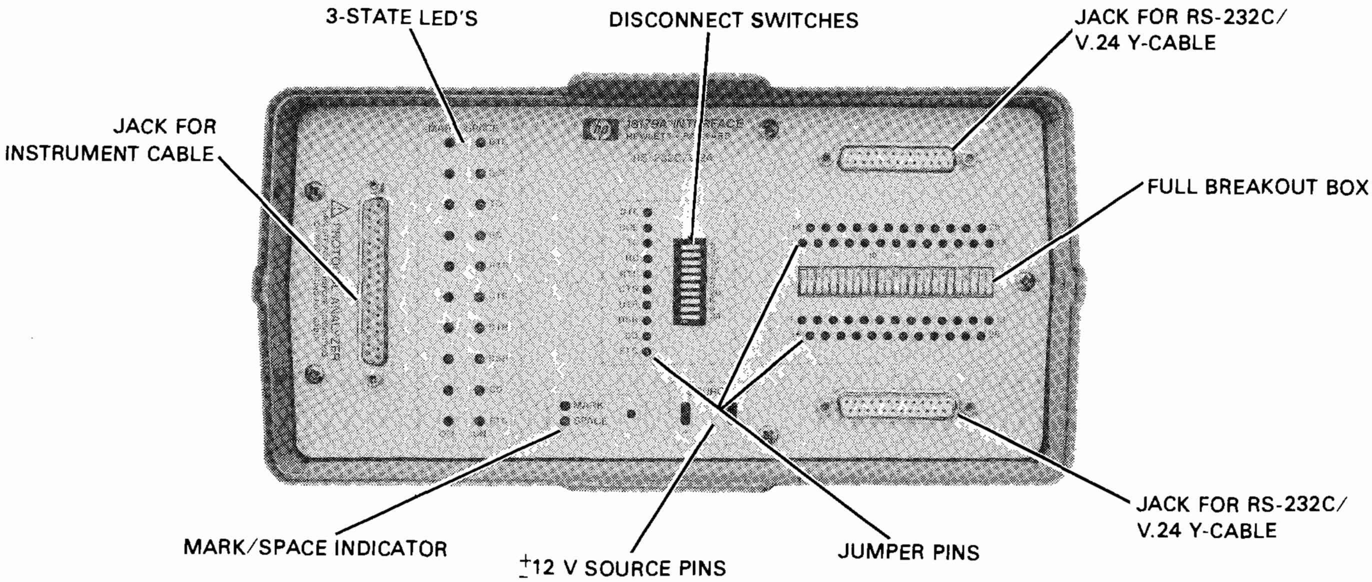


Figure D-3. HP 18179A Front Panel

3-state LEDS

The 3-state indicators indicate activity on the lines and RS-232C compliance.

green: space (logic '0', positive voltage)
turns on at >2.75 V, turns off at <0.25 V

red: mark (logic '1', negative voltage)
turns on at < -3.0 V, turns off at > -3.0 V

Disconnect Switches

Pins 2, 3, 4, 5, 6, 8, 15, 17, 20, and 24 may be individually disconnected from the data link by switches. This lets you isolate non-driven interface lines from the HP 4951C. Non-driven lines may develop cross talk noise which will be mistaken by the analyzer for transitions.

Jacks for RS-232C/V.24 Y-cable

These jacks connect the Interface Pod to the line for monitoring or simulation. The bottom jack connects directly to the line. The top jack includes the breakout box in series.

Full Breakout Box

The Breakout Box provides crosspatching, lineforcing, and monitoring capabilities for all of the RS-232C lines. The miniature switches isolate lines. Use the top RS-232/V.24 connector for the breakout box.

Jumper Pins

All 25 pins of the RS-232C jack are brought out for jumpering. If your network cable has different pin assignments from the interface standard, you can use the supplied jumper wires to connect the interface lines to the desired pin on your cable.

+-12 V Source Pins

The Source Pins supply +12 volts and - 12 volts. You may set any signal line on or off by jumpering that line to the Source Pins.

Mark/Space Indicator

The Mark/Space Indicator enables you to check the level of any signal line. Jumper the line to this pin and the appropriate indicator will light.

Jack for Instrument Cable

This jack connects the Interface Pod to the HP 4951C via the Pod-Instrument cable supplied with this instrument.

D-4. PERFORMANCE VERIFICATION

The Performance Verification test is performed by the operator. Follow the procedure described below.

HP 18179A Self Test

Description

This test checks that there is an Interface Pod connected to the Protocol Analyzer and verifies that the data lines work.

Set Up

1. Turn on the HP 4951C.
2. Press MORE.
3. Select <SELFTEST>.
4. Select <EXT DLC>.

Procedure

1. Turn off all ten disconnect switches in the switch block located in the center of the Interface Pod. When the <EXT DLC> softkey is pressed, the Interface Pod test will be automatically performed.

2. If there are no failures, DLC TEST PASSED is displayed.

   a. If there is a failure, the problem may be in the Interface Pod or in the Protocol Analyzer.

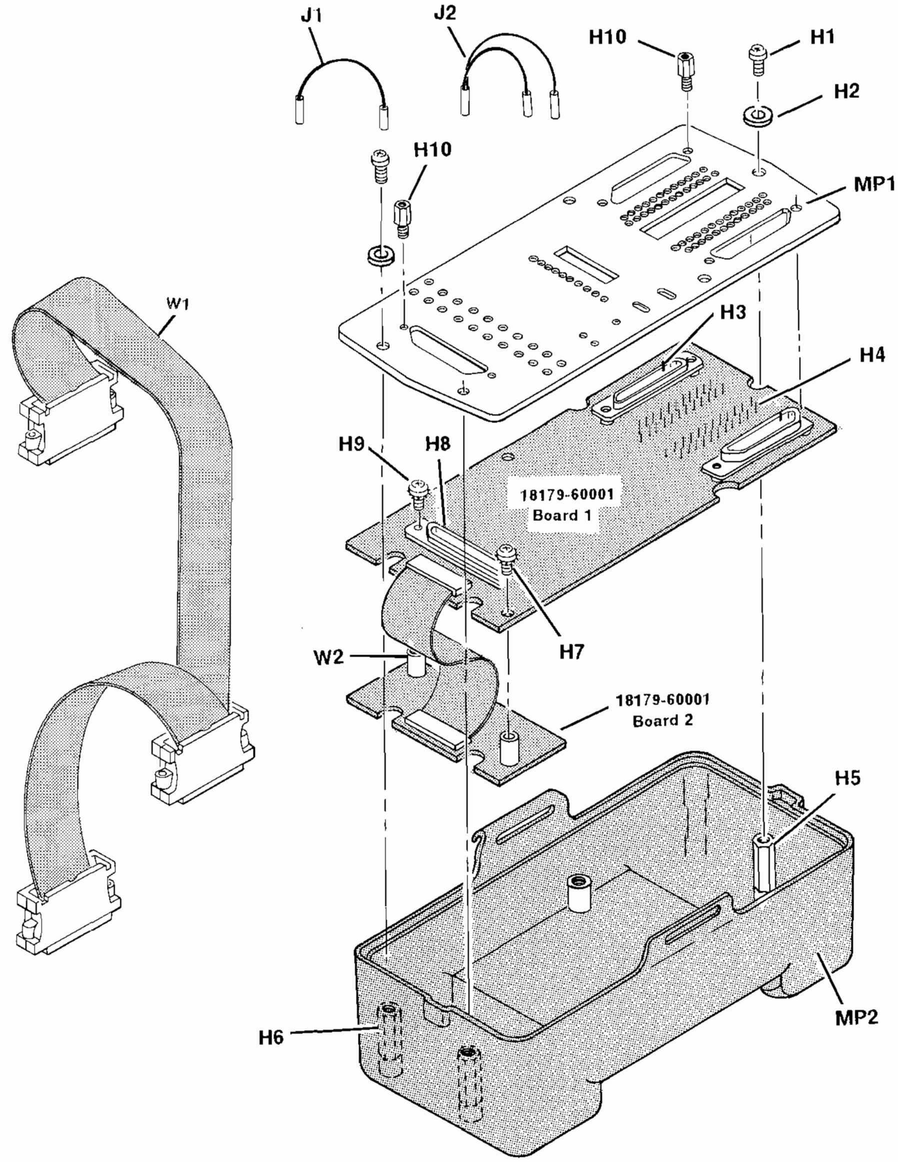
D-5. ADJUSTMENTS

There are no adjustments for the HP 18179A.

D-6. REPLACEABLE PARTS

The following tables and figure give information for ordering replacement parts. Table D-2 is the Manufacturer's Code List. Table D-1 lists the replaceable parts in reference designator order. Information is given for the Description, Quantity, HP Part Number, and Manufacturers Part Number. Chassis and mechanical parts are listed in Figure D-4. To order a listed part, include the HP Part Number, indicate the quantity needed, and send the order to the nearest Hewlett-Packard office.

When ordering a part not listed, include the instrument model number, serial number, and a physical and functional description of the part. Send the order to the nearest Hewlett-Packard office.



Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H1	2360-0195	7	5	SCREW, MACHINE 6-32-312	05610	ORDER BY DESCRIPTION
H2	2190-0876	3	5	WASHER, FLAT #6 MTLC	05313	ORDER BY DESCRIPTION
H3	1251-6074	4	2	CONNECTOR-37 PIN	04486	DC375V
H4	1251-8360	5	67	CONNECTOR POST	01380	8787-6
H5	0380-1719	6	1	STANDOFF-HEX M & F	02121	AL6981-.917-3
H6	0380-1720	9	2	STANDOFF-HEX M & F	02121	AL6981-.803-3
H7	2360-6074	4	2	SCREW, MACHINE 6-32-.312	05610	ORDER BY DESCRIPTION
H8	1251-4946	3	2	CONNECTOR 25 PIN F	04507	DB-255V
H9	2360-0115	4	2	SCREW, MACHINE 6-32-.312	05610	ORDER BY DESCRIPTION
H10	1251-2942	7	4	SCREW POST LOCK	28480	1251-2942
	0380-0162	1	2	SPACER 6-32 .750	01461	ORDER BY DESCRIPTION
J1	8120-4218	4	4	CABLE JUMPER	28480	8120-4218
J2	8120-4219	5	2	CABLE JUMPER	28480	8120-4219
MP1	18179-00001	8	1	SUPERPOD PANEL	28480	18179-00001
MP2	5041-6749	4	1	HOUSING, COATED	28480	5041-6749
W1	18173-61602	7	1	CABLE, RS-232C	28480	18173-61602
W2	18173-61601	1	1	CABLE, BOARD CONN	28480	18173-61601

Figure D-4. HP 18179A Exploded View

Table D-1. HP 18179A Replaceable Parts List

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C1	0180-3050	8	1	CAPACITOR 330UF 16VDC	08817	16TWL330RDF
A1C2	0180-0228	6	1	CAPACITOR 22 UF 15V	04200	150D226X9015BZ
A1C3	0160-0576	5	19	CAPACITOR .1UF 20% 50V	04200	1C10X7R104M050B
A1C3	0160-0576	6	1	CAPACITOR-FXD .1UF 20% 50v	04200	1C10X7R104MO50B
A1C4	0160-0576	6	1	CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C5	0160-5298	4	5	CAPACITOR-FXD 0.01UF 20% 100V	02010	MDO11C103MAA
A1C6	0160-5298	4		CAPACITOR-FXD 0.01UF 20% 100V	02010	MDO11C103MAA
A1C7	0160-5298	4		CAPACITOR-FXD 0.01UF 20% 100V	02010	MDO11C103MAA
A1C8	0160-5298	4		CAPACITOR-FXD 0.01UF 20% 100V	02010	MDO11C103MAA
A1C9	0160-5298	4		CAPACITOR-FXD 0.01UF 20% 100V	02010	MDO11C103MAA
A1C10	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C11	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C12	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C13	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C14	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C15	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C16	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C17	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C18	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C19	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C20	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C21	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C22	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C23	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C24	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C25	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C26	0160-0576	5		CAPACITOR-FXD .1UF 20% 50V	04200	1C10X7R104M050B
A1C27	0180-0116	1	2	CAPACITOR-FXD 6.8UF 35V	04200	150D685X9035B2
A1C28	0180-0116	1		CAPACITOR-FXD 6.8UF 35V	04200	150D685X9035B2
A1CR1	1990-0486	6	11	LED LAMP, RED	01542	QLMP-1347
A1CR2	1990-0485	9	11	LED LAMP, GREEN	05735	240010GB7
A1CR3	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR4	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR5	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR6	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR7	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR8	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR9	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR10	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR11	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR12	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR13	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR14	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR15	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR16	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR17	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR18	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR19	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR20	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR21	1990-0486	6		LED LAMP, RED	01542	QLMP-1347
A1CR22	1990-0485	9		LED LAMP, GREEN	05735	240010GB7
A1CR500	1906-0074	5	1	DIODE ARRAY	02237	FSA3157P
A1K100	0490-1354	8	1	RELAY-10 PIN PKG	01850	DSZE-M-12-DC5V-H36
A1K200	0490-1383	3	2	RELAY	01850	DS4E-ML2DC5V
A1K300	0490-1383	3		RELAY	01850	DS4E-ML-DC5V
A1R1	0698-8820	7	4	RESISTOR 4.64 1% .125w	05524	F-55-1
A1R2	0698-8820	7		RESISTOR 4.64 1% .125W	05524	CMF-55-1
A1R3	0698-3156	4	1	RESISTOR 14.7K 1% .125W	02995	5033R
A1R4	0757-0442	9	4	RESISTOR 10K 1% .125W	02995	5033R
A1R5	0757-0442	9		RESISTOR 10K 1% .125W	02995	5033R
A1R6	0757-0461	1	1	RESISTOR 68.1K 1% .125	02995	5033R
A1R7	0757-0442	9		RESISTOR 10K 1% .125W	02995	5033R
A1R8	0698-8820	7		RESISTOR 4.64 1% .125w	05524	CMF-55-1
A1R9	0698-8820	7		RESISTOR 4.64 1% .125W	05524	CMF-55-1
A1R10	0757-0442	9		RESISTOR 10K 1% .125W	02995	5033R
A1R11	0757-0465	9	1	RESISTOR 100K 1% .125w	02995	5033R
A1R12	0757-0280	3		RESISTOR 1KOHM 1%	02995	5033R
A1R13	0575-0280	3		RESISTOR 1K OHM 1%	02995	5033R
A1R14	0575-0280	3		RESISTOR 1K OHM 1%	02995	5033R
A1R102	1810-0747	2	2	RESISTOR-NET 330 OHM X7	28480	1810-0747
A1R103	1810-0748	3	2	RESISTOR-NET 220.0 X 7	28480	1810-0748
A1R105	1810-0679	4	11	RESISTOR-NET 10.0K X7	28480	1810-0679
A1R106	1810-0679	4		RESISTOR-NET 10.0K	28480	1810-0679
A1R205	1810-0679	9		RESISTOR-NET 10.0K	28480	1810-0679
A1R206	1810-0679	9		RESISTOR-NET 10.0K	28480	1810-0679

Table D-1. HP 18179A Replaceable Parts List (cont)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R304	1810-0746	2	3	RESISTOR-NET 100.0 X 4	28480	1810-0746
A1R400	1810-0292	0		RESISTOR-NET SIP 4	28480	1810-0292
A1R404	1810-0745	0	2	RESISTOR-NET 1K X 7	28480	1810-0745
A1R405	1810-0731	4	3	RESISTOR-NET 10.0K X 7	28480	1810-0731
A1R406	1810-0679	9		RESISTOR-NET 10.0K X 7	28480	1810-0679
A1R504	1810-0746	1		RESISTOR-NET 100.0K X 4	28480	1810-0746
A1R505	1810-0731	5		RESISTOR-NET 10.0K X 7	28480	1810-0731
A1R506	1810-0679	4		RESISTOR-NET 10.0K X 7	28480	1810-0679
A1R604	1810-0745	0		RESISTOR-NET 1K X 7	28480	1810-0745
A1R605	1810-0746	2		RESISTOR-NET 100K X 4	28480	1810-0746
A1R606	1810-0679	3		RESISTOR-NET 10.0K X 7	28480	1810-0679
A1R607	1810-0679	3		RESISTOR-NET 10.0k X 7	28480	1810-0679
A1R608	1810-0679	3		RESISTOR-NET 10.0K X 7	28480	1810-0679
A1R700	1810-0731	4		RESISTOR-NET 10.0K X 7	28480	1810-0731
A1R703	1810-0747	2		RESISTOR-NET 330.0 X 7	28480	1810-0747
A1R705	1810-0679	4		RESISTOR-NET 10.0K X 7	28480	1810-0679
A1R706	1810-0679	4		RESISTOR-NET 100.0K X 7	28480	1810-0679
A1R800	1810-0745	0	1	RESISTOR-NET 10K X 5	28480	1810-0745
A1R803	1810-0748	3		RESISTOR-NET 220.0 X 7	28480	1810-0748
A1SW1	3101-2732	8	1	DIP SWITCH	05661	DSS-10
A1SW2	3101-2618	0	1	DIP SWITCH	05735	240005GB
A1SW3	3101-2618	0		DIP SWITCH	05735	240005GB
A1SW4	3101-2619	0		DIP SWITCH	05735	240005GB
A1U105	1858-0047	1	4	TRANSISTOR ARRAY 16 P DIP	02237	FSA3157P
A1U106	1826-0759	9	6	IC - 339	02037	SL44582
A1U305	1820-2921	9	2	IC MM74HC04N	03406	MM74HC04N
A1U306	1826-0759	9		IC - 339	02037	SL44582
A1U307	1826-0753	3	3	IC 34004B	02037	MC34004BL
A1U405	1858-0047	1		TRANSISTOR ARRAY 16 P DIP	02237	FSA3157P
A1U406	1826-0759	9	6	IC - 339	02037	SL44582
A1U600	1826-0753	3		IC 34004B	02037	MC34004BL
A1U605	1820-2921	9		IC MM74HC04N	03406	MM74HC04N
A1U606	1826-0759	9	6	IC - 339	02037	SL44582
A1U700	1826-0753	3		IC 34004B	02037	MC34004BL
A1U701	1858-0047	1	4	TRANSISTOR ARRAY 16 P DIP	02237	FSA3157P
A1U705	1858-0047	1	4	TRANSISTOR ARRAY 16 P DIP	02237	FSA3157P
A1U706	1826-0759	9	6	IC - 339	02037	SL44582
A1U707	1826-0759	9	6	IC - 339	02037	SL44582

Table D-2. Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
11236	CTS OF BERNE INC	BERNE	IN	46711
13606	SPRAGUE ELECT CO SEMICONDUCTOR DIV	CONCORD	NH	03301
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

D-7. SERVICE

The following paragraphs contain service information for the HP 18179A. Included is the Theory of Operation, RS-232C/V.24 Signal Mnemonics, Troubleshooting, Component Locators, and Schematics.

D-8. THEORY OF OPERATION

The HP 18179A provides enhanced Level I protocol analysis with three state indicators on ten lines. This is implemented with two comparators per line driving MARK (red) and SPACE (green) LEDs. The HP 18179A can act as a DTE or DCE, or monitor an RS-232C data link. These modes are selected by the HP 4951C by pulsing the three mode control lines (MONITOR, DCESIM, and DTESIM). The control lines activate latching relays which connect the appropriate RS-232C drivers to the Breakout Box.

Breakout Box

The Breakout Box allows access to all 25 lines. The operator can configure the interface by opening the Breakout Box switches and patching lines with jumpers. It has one undedicated MARK/SPACE indicator. The +-12 V sources are current limited with 1 K resistors.

Specifications

The HP 18179A has the following electrical specifications.

* Steady State current, each LED on 50% of the time.

+5V	165 mA
+-12 V	30mA

* Pod ID 0,0,0

* LED thresholds

SPACE LED & data	on at 2.75 V, off at 0.25 V
MARK LED	on at -3 V, off at -2.8 V

The Interface Pod has the following features and capabilities:

It translates voltages between RS-232C and HP 4951C logic levels.

It displays the lines status of all EIA lines presented to the HP 4951C.

It has an integral Breakout Box.

In monitor mode, the HP 4951C monitors traffic on a data link.

During DTE simulate, the HP 4951C appears as a data terminal device.

During DCE simulate, the HP 4951C appears as a piece of data communication equipment.

The RS-232C drivers will operate into a worst case RS-232C load.

Simulate Mode - In the DTE and DCE simulate modes RS-232C drivers are switched into the appropriate lead by latching relays.

Monitor Mode - If monitor mode is selected all RS-232C drivers are disconnected from the line.

D-9. CIRCUIT THEORY

The MONITOR, DCESIM, and DTESIM control lines from the HP 4951C activate latching relays which connect the appropriate RS-232C line drivers to the Breakout Box. All control lines are normally at a logic 0 (0 volts).

Monitor mode	10 ms pulse on J1-18 (MONITOR)
DTE simulate mode	10 ms pulse on J1-18 (MONITOR) 10 ms pulse on J1-19 (DTESIM)
DCE simulate mode	10 ms pulse on J1-18 (MONITOR) 10 ms pulse on J1-37 (DCESIM)

Receivers

Each RS-232C line is sent to two receivers (comparators); one is a valid space indicator and the other is a valid mark indicator. The indicators drive green and red LEDs respectively. The valid space receivers have 0.5 volts of hysteresis; this window is between +0.25 V and +2.75 V. The thresholds of these receivers are set by op amp A1 U307. The valid mark receivers have hysteresis of -0.2 V at -3V to prevent oscillations. The undedicated mark/space receivers (A1 U707) have the same thresholds as the dedicated receivers.

Line Drivers

The RS-232C line drivers are implemented with op amps (A2 U600 and A2 U700). The outputs are current limited by a 200 ohm resistor in parallel with a 0.1 uf speed up capacitor to improve the rise time into large cable lengths. Diodes to the +-12 V supplies also protect the outputs of the drivers from foreign voltages.

D-10. RS-232C SIGNAL MNEMONICS

The HP 18179A is designed to accommodate two similar interface standards, the RS-232C and the V.24. Table D-3 describes RS-232C/V.24 signal mnemonics.

Table D-3. RS-232C/V.24 Signal Mnemonics

RS-232C PIN #	EIA	CCITT	CIRCUIT	DESCRIPTION
1	AA	101		Protective Ground
2	BA	103	TD*	Transmitted Data
3	BB	104	RD*	Received Data
4	CA	105	RTS*	Request To Send
5	CB	106	CTS*	Clear To Send
6	CC	107	DSR*	Data Set Ready
7	AB	102	GND	Signal Ground
8	CF	109	CD*	Carrier Detect (Received Line Signal Detector
9				unassigned
10				unassigned
11				unassigned
12	SCF	122	SCD	Secondary Carrier Detect
13	SCB	121	SCS	Secondary Clear to Send
14	SBA	118	STX	Secondary Transmitted Data
15	DB	114	TC*	Transmit Signal Elements Timing (transmit clock)
16	SBB	119	SRX(SRD)	Secondary Received Data
17	DD	115	RC*	Receiver Signal Element (Receive Clock)
18				unassigned
19	SCA	120	SRS	Secondary Request to Send
20	CD	108.2	DTR*	Data Terminal Ready
21	CG	110	SQ	Signal Quality
22	CE	125	RI	Ring Indicator
23	CH/CI	111/112	DRS	CH=Data Rate Selector, DTE CI=Data Rate Selector, DCE
24	DA	113	ETC*	EXT. Transmit Signal Element Timing (DTE source)
25				unassigned

* Monitored by the HP 18179A indicators.

D-11. TROUBLESHOOTING

Troubleshoot the portion of the pod that has failed (DTE or DCE). When entering the test programs below, "Press" indicates a hardkey and "Select" indicates a softkey.

GENERAL TROUBLESHOOTING HINTS

To check the undedicated SPACE LED (A1 CR22), connect the M/S test point to the +SOURCE.

To check the undedicated MARK LED (A1 CR21), connect the M/S test point to the -SOURCE.

The inputs to A2 U600 and A2 U700 should be at TTL levels (between 0 and +5 volts).

The outputs from A2 U600 and A2 U700 should be RS-232C levels (+-12 V).

The inputs and outputs of all other circuits should be at TTL levels.

DTE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod or jumpers.

1. Connect jumpers between the following pins on TPB (the top set of test points):

   4, 5, and 6
   8 and 20

2. Put the following switches in the on (closed) position:

   SW2 numbers 4, 5, 6, and 8
   SW3 number 0 (20th position from the left side of the switch bank).

3. Enter the following DTE test program.

Table D-4. DTE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DTE	(DTE clock)
Press	(HALT)EXIT	

The Top Level Menu will be displayed.

Table D-4. DTE Test Program (cont)

Select	Simulate
	DTE
Press	MORE
Select	Set Lead
	RTS
	Off
	and then
Press	MORE
Select	Set Lead
	DTR
	Off
	and then
	Send
Type in	CTS OFF
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	100
Press	RTN (return)
Select	Next Block
Press	MORE
Select	Set Lead
	RTS
	On
	and then
Press	MORE
Select	Set Lead
	DTR
	On
	and then
	Send
Type in	CTS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	100
Press	RTN (return)
Select	and then
	When Trig
	Lead
	RTS
	On
	then go to
Type in	1
Press	RTN (return)
	(HALT)EXIT

4. Run the program entered in Table D-4.

   Select Run Menu
   Simulate

   a. Table D-5 describes the status of the HP 18179A LED indicators while the DTE test program is running.

Table D-5. LED Indicators on HP 18179A During DTE Troubleshooting

Indicator	MARK	SPACE
DTE	on	on
DCE	off	off
TC	off	off
RC	off	off
RTS	blinking	blinking
CTS	blinking	blinking
DTR	blinking	blinking
DSR	blinking	blinking
CD	blinking	blinking
ETC	on	on

5. If any of the above conditions fail, check the following. Steps 6 and 7 show specific troubleshooting examples.

   a. Use an oscilloscope to examine the driver associated with the failed channel. The output voltage should be an RS-232C level (typically + or -12 volts, but at least + or -10 volts). If the trouble is not found, proceed to step b.

   b. Use an oscilloscope to examine the receiver associated with the failed channel. The voltage at the inverting input to the comparator should be a 6 volt peak signal with a 1 volt dc offset.

6. The following is a troubleshooting example. Assume that the RTS SPACE LED is not working. Check for the voltage levels that follow:

a. A2 U600 -	pin 8	12 volt signal
	pin 9	5 volt signal
	pin 10	2.5 Vdc reference
b. A1 U406 -	pin 8	6 volt peak signal with a 1 volt dc offset
	pin 9	4 Vdc reference
	pin 14	5 volt signal
c. A1 U305 -	pin 6	5 volt signal
d. A1 U405 -	pin 13	3 volt peak signal with a .75 Vdc offset

7. As another example, assume that the RTS MARK LED fails to light. Check for the voltage levels listed below.

a.	A1 U406 -	pin 1	2 volt signal
		pin 6	6 volt peak signal with a 1 volt dc offset
		pin 7	3 Vdc reference
b.	A1 U405 -	pin 11	3 volt peak signal with a .75 Vdc offset

DCE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod or jumpers.

1. Connect jumpers between the following pins on TPB (the top set of test points):

   2 and 3
   4, 5, and 24
   8 and 20

2. Put the following switches in the on (closed) position:

   SW2 numbers 2, 3, 4, 5, and 8
   SW3 number 0 (20th position from the left side of the switch bank).
   SW4 number 4 (24th position from the left side of the switch bank).

3. Enter the program in Table D-6.

Table D-6. DCE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DTE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed.		
Select	Simulate	
	DCE	
Press	MORE	
Select	Set Lead	
	CTS	
	Off	

Table D-6. DCE Test Program (cont)

	and then
Press	MORE
Select	Set Lead
	DSR
	Off
	and then
Press	MORE
Select	Set Lead
	CD
	Off
	and then
	Send
Type in	CTS OFF
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	100
Press	RTN (return)
Select	Next Block
Press	MORE
Select	Set Lead
	CTS
	On
	and then
Press	MORE
Select	Set Lead
	DSR
	On
	and then
Press	MORE
Select	Set Lead
	CD
	On
	and then
	Send
Type in	CTS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	100
Press	RTN (return)

Table D-6. DCE Test Program (cont)

Select	Next Block
	When Trig
	Lead
	RTS
	On
	then go to
Type in	1
Press	RTN (return)
	(HALT)EXIT

4. Run the program entered in Table D-6:

Select	Run Menu
	Simulate

a. Table D-7 describes the status of the HP 18179A LED indicators while the DCE test program is running.

Table D-7. Indicators on HP 18179A During DCE Troubleshooting

Indicator	MARK	SPACE
DTE	on	on
DCE	on	on
TC	on	on
RC	on	on
RTS	blinking	blinking
CTS	blinking	blinking
DTR	blinking	blinking
DSR	blinking	blinking
CD	blinking	blinking
ETC	blinking	blinking

5. If any of the above conditions fail, check the following. Steps 6 and 7 show specific troubleshooting examples.

   a. Use an oscilloscope to examine the driver associated with the failed channel. The output voltage should be an RS-232C level (typically + or -12 volts, but at least + or -10 volts). If the trouble is not found, proceed to step b.

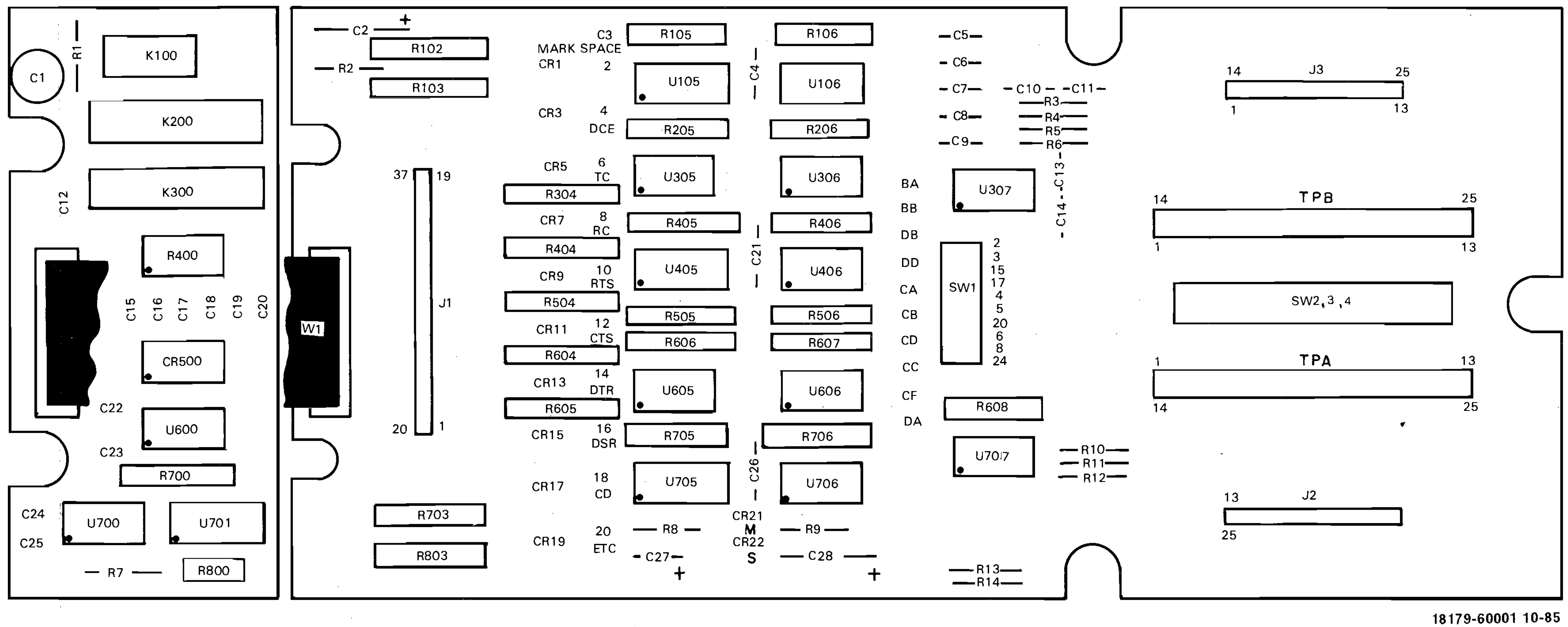
   b. Use an oscilloscope to examine the receiver associated with the failed channel. The voltage at the inverting input to the comparator should be a 6 volt peak signal with a 1 volt dc offset.

6. The following is a troubleshooting example. Assume that the DTR SPACE LED is not working. Check for the following voltage levels.

a.	A2 U600 -	pin 12	2.5 Vdc reference
		pin 13	5 volt signal
		pin 14	12 volt signal
b.	A1 U606 -	pin 10	6 volt peak signal with 1 Vdc offset
		pin 11	4 Vdc reference
		pin 13	5 volt signal
c.	A1 U605 -	pin 10	5 volt signal
d.	A1 U405 -	pin 15	3 volt peak signal with a .75 Vdc offset

7. As another example, assume that the DTR MARK LED fails to light. Check for the following voltages.

a.	A1 U606 -	pin 2	2 volt signal
		pin 4	6 volt peak signal with 1 Vdc offset
		pin 5	3 Vdc reference
b.	A1 U705 -	pin 16	3 volt peak signal with .75 Vdc offset



A2 board A1 board

Figure D-5. HP 18179A Component Locator

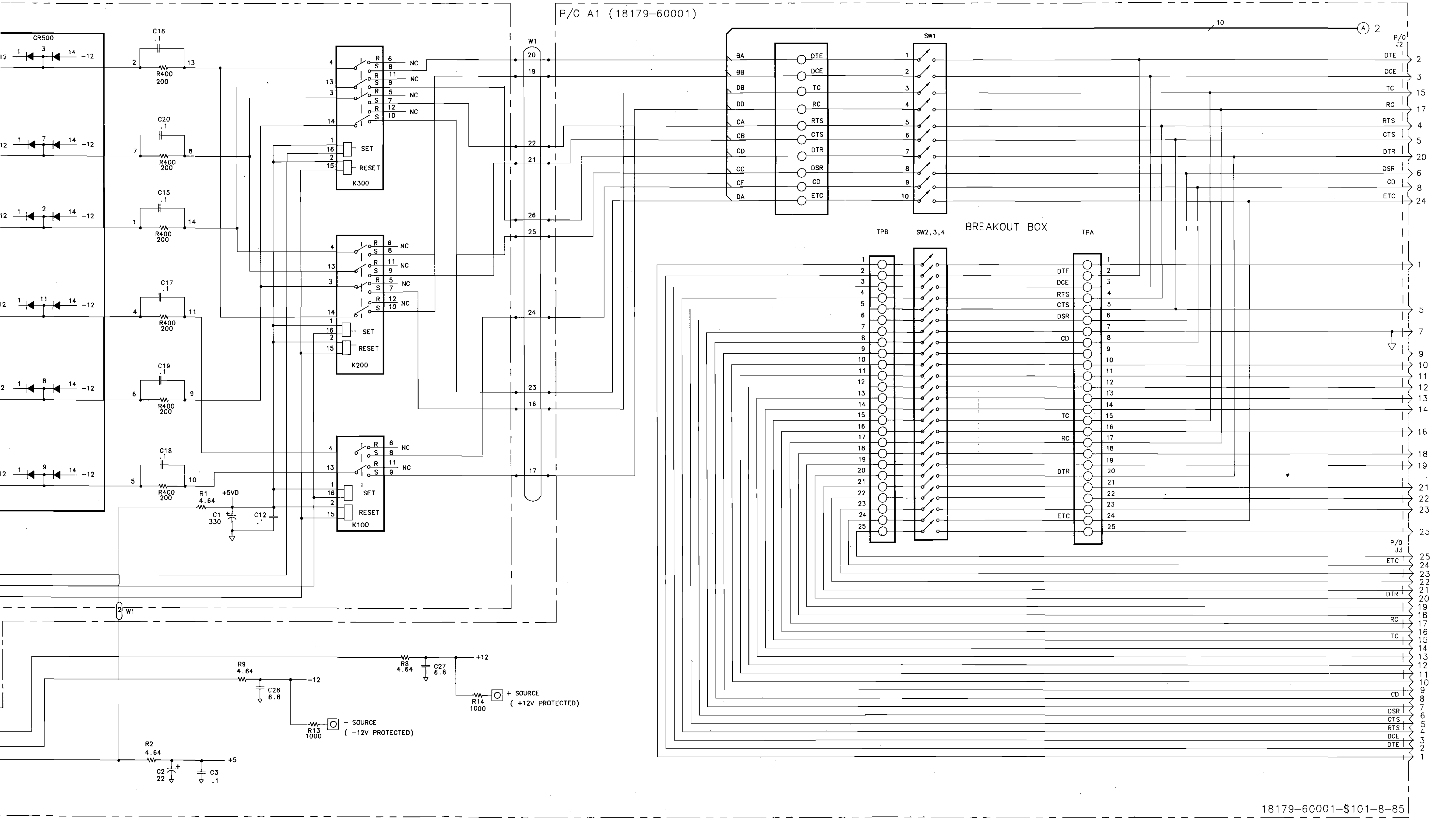
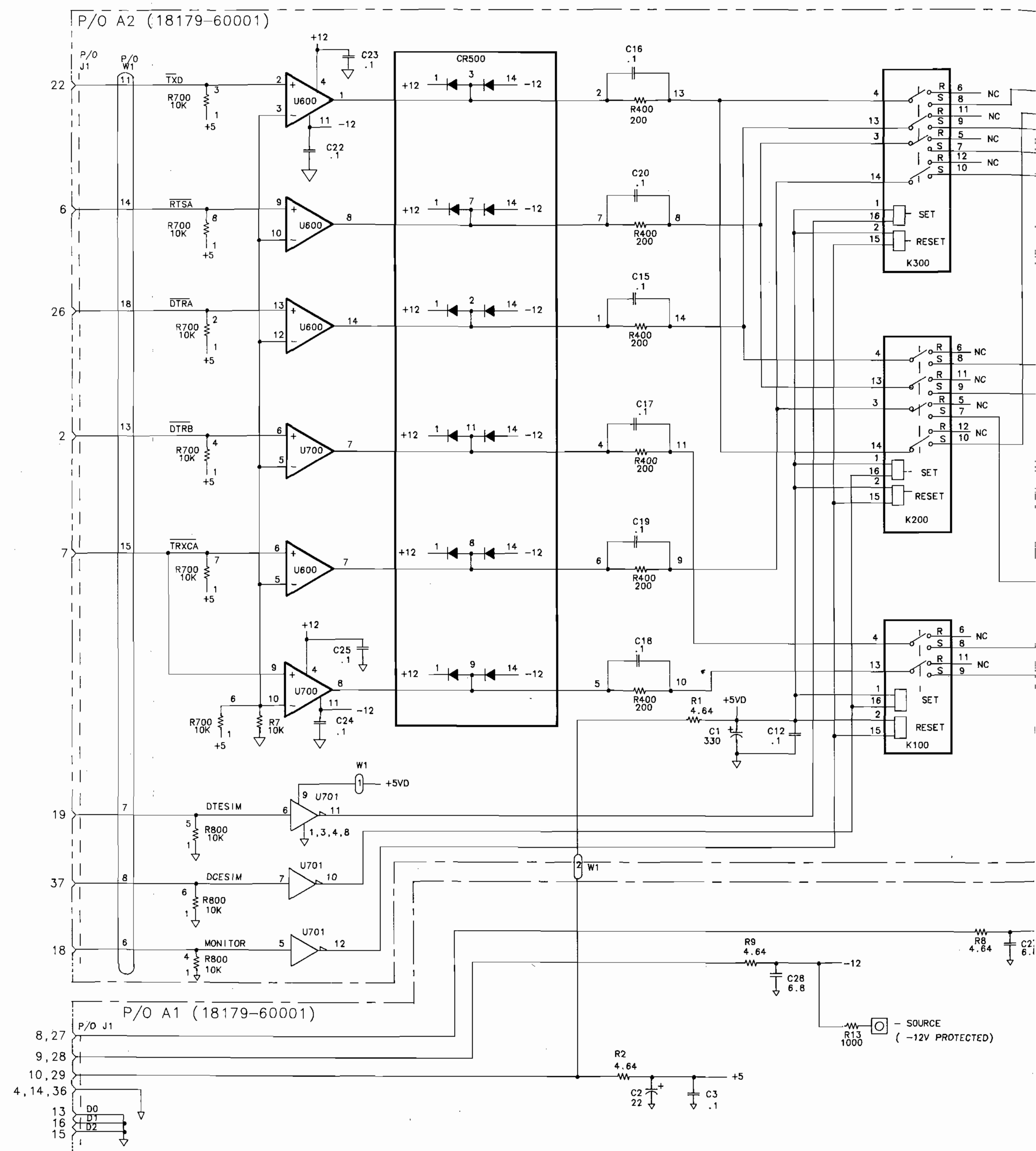


Figure D-6. HP 18179A Driver Schematic



P/O A2 (18179-60001)
P/O J1
P/O W1
TXD
RTSA
DTRA
DTRB
TRXCA
R700 10K
U600
U700
U701
CR500
C16 .1
C20 .1
C15 .1
C17 .1
C19 .1
C18 .1
C22 .1
C23 .1
C24 .1
C25 .1
R400 200
K300
K200
K100
SET
RESET
NC
DTESIM
DCESIM
MONITOR
R800 10K
R7 10K
+5VD
R1 4.64
C1 330
C12 .1
R9 4.64
C28 6.8
R8 4.64
R2 4.64
C2 22
C3 .1
R13 1000
- SOURCE
(-12V PROTECTED)
P/O A1 (18179-60001)
8,27
9,28
10,29
4,14,36
D0
D1
D2

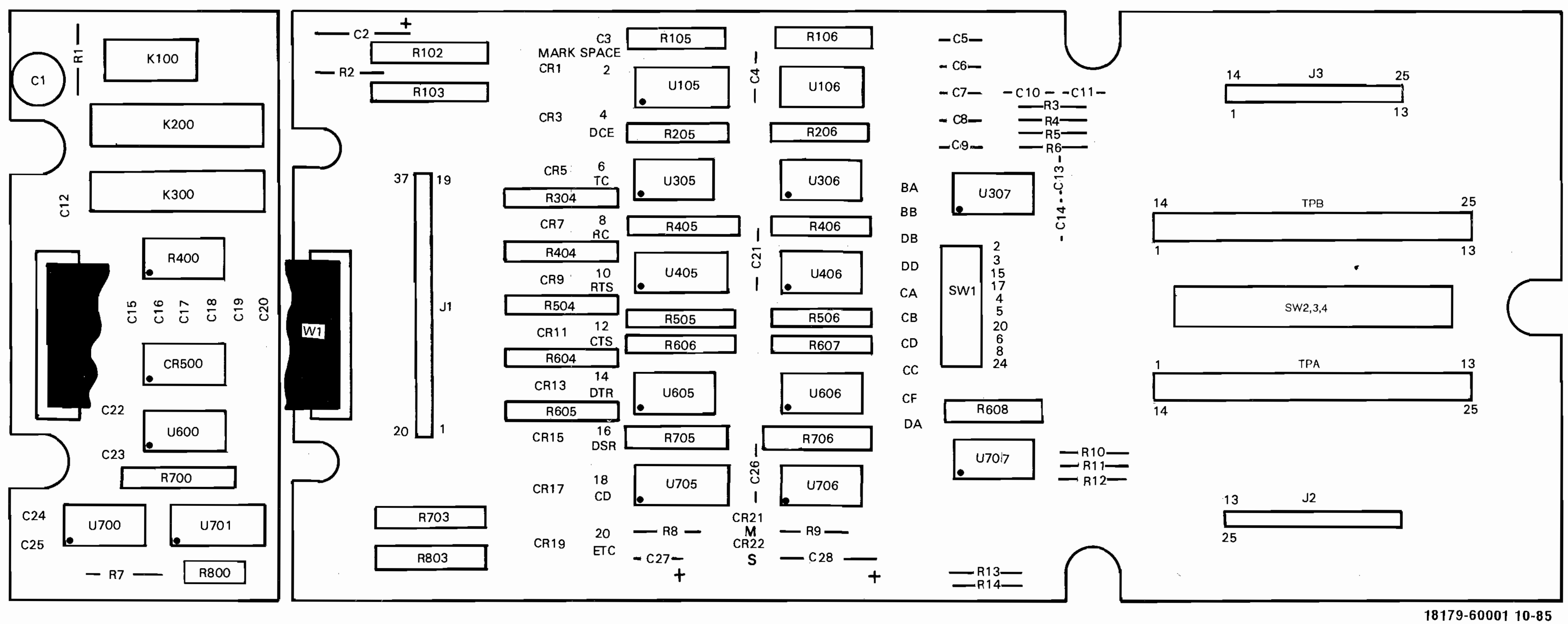


Figure D-5. HP 18179A Component Locator

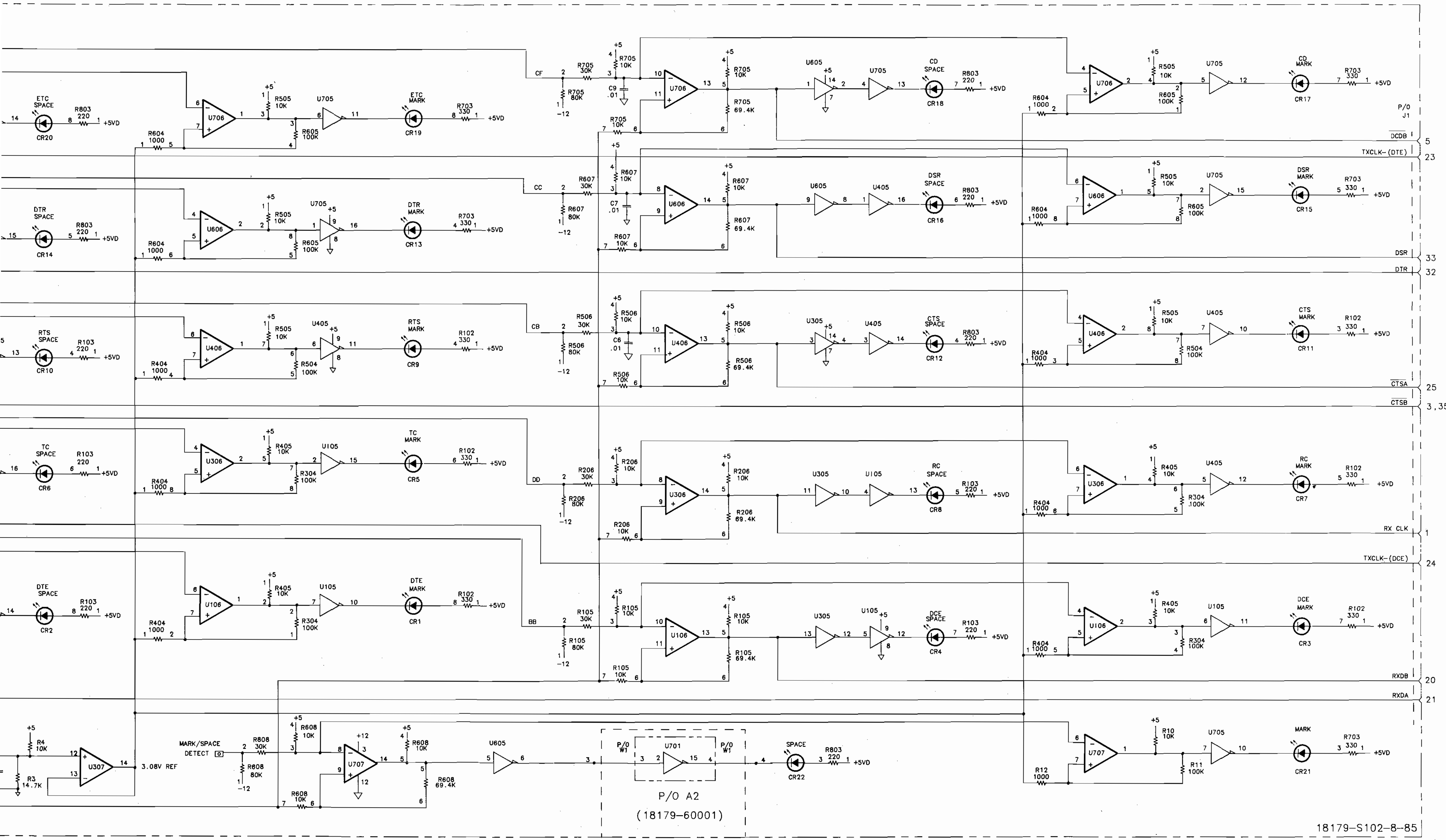
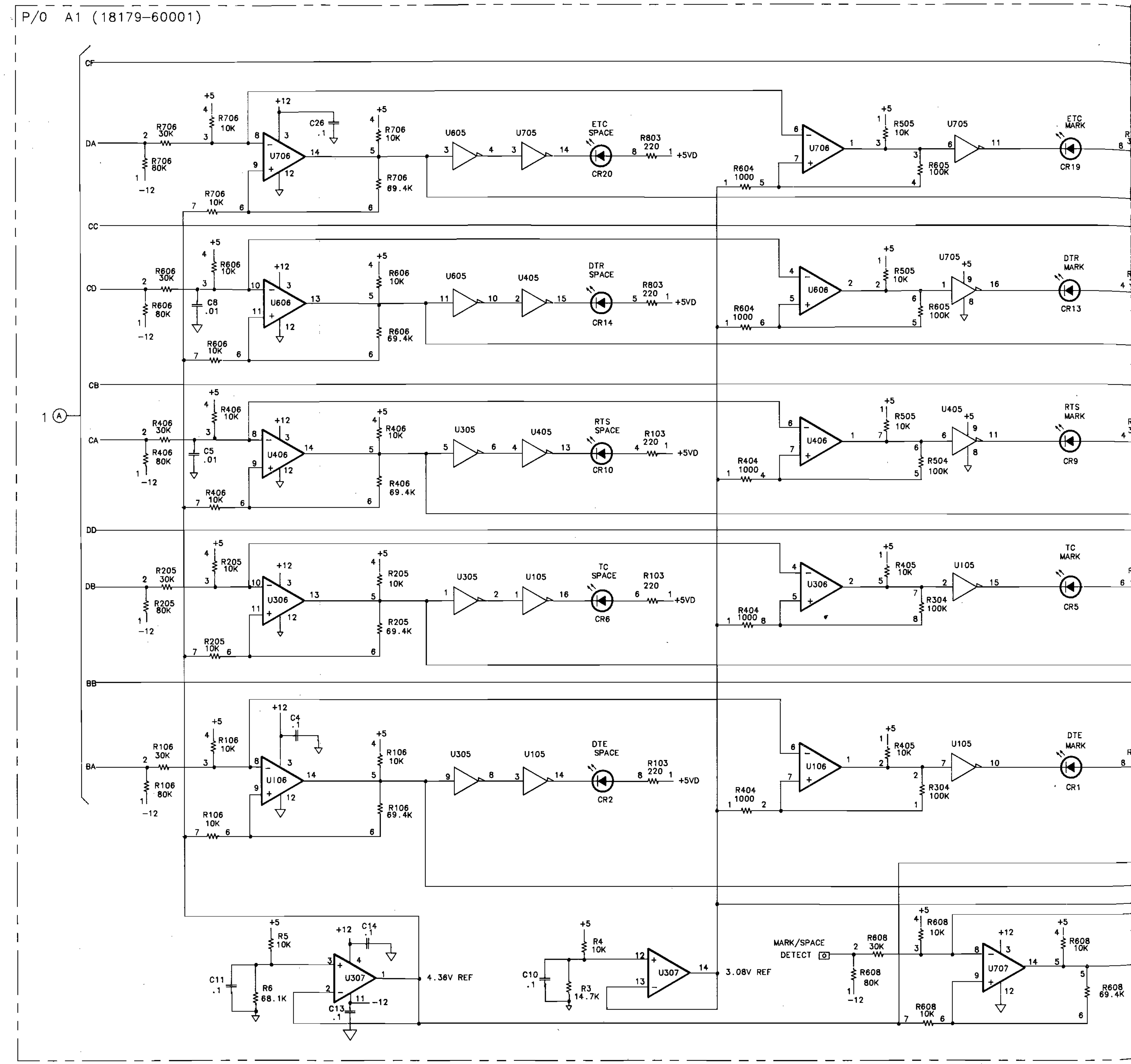


Figure D-7. HP 18179A Transmitter/Receiver Schematic



P/O A1 (18179-60001)
CF
DA
CC
CD
CB
CA
DD
DB
BB
BA
1 (A)
U706
U606
U406
U306
U106
U605
U705
U405
U305
U105
ETC SPACE
DTR SPACE
RTS SPACE
TC SPACE
DTE SPACE
ETC MARK
DTR MARK
RTS MARK
TC MARK
DTE MARK
CR20
CR14
CR10
CR6
CR2
CR19
CR13
CR9
CR5
CR1
+5VD
U307
4.38V REF
3.08V REF
MARK/SPACE DETECT
U707

APPENDIX E
HP 18180A
RS-232C/V.24/RS-449 INTERFACE POD

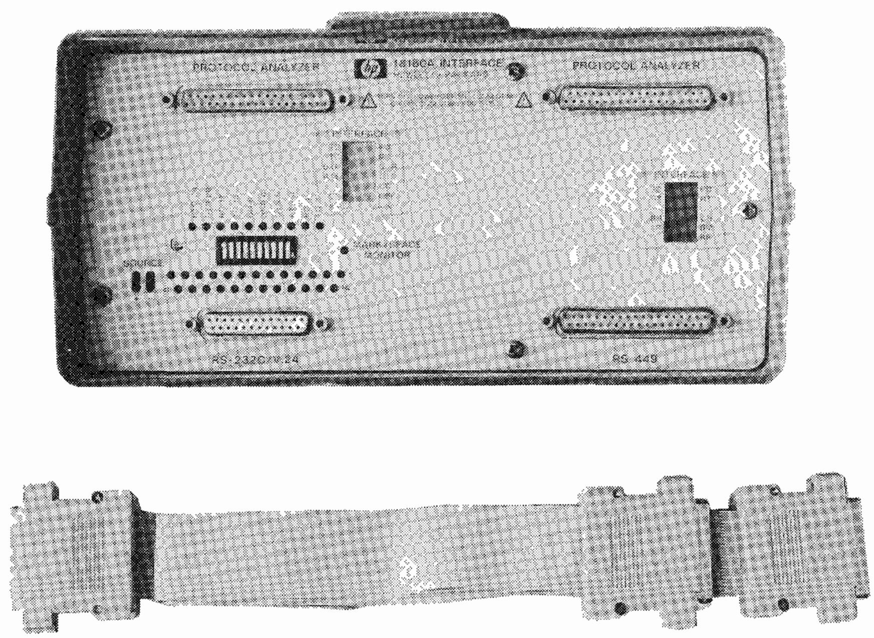


Figure E-1. HP 18180A Interface Pod and RS-232C and RS-449 Cables

E-1. INTRODUCTION

The HP 18180A is a combination RS-232C/V.24 and RS-449 Interface Pod which provides the connection between the HP 4951C Protocol Analyzer and Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The RS-232C portion of the Interface Pod is compatible with CCITT V.24 and EIA RS-232C electrical, functional, mechanical and procedural specifications. The RS-449 portion is compatible with EIA RS-449/RS-422A/423A electrical, functional, mechanical and procedural specifications.

This appendix includes information on how to install, operate, and service the HP 18180A.

E-2. INSTALLATION

WARNING

Turn the HP 4951C Protocol Analyzer off before connecting or disconnecting the Interface Pod.

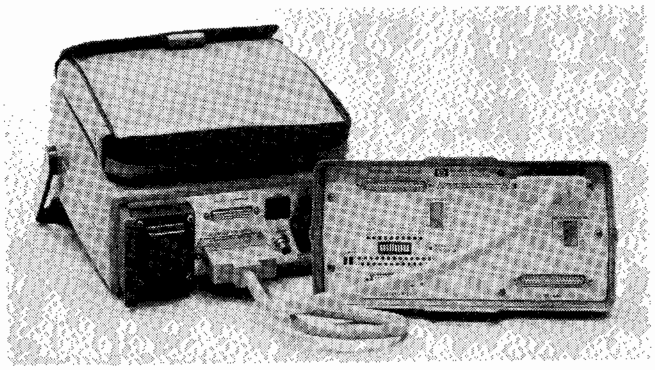


Figure E-2. Connecting the HP 18180A Interface Pod to the HP 4951C

To connect the HP 18180A Interface Pod to the HP 4951C, attach the Interface Pod Cable between the lower connector on the back of the HP 4951C and either the top right connector of the HP 18180A (if you want to use the RS-449 portion of the pod), or the top left connector of the HP 18180A (if you want to use the RS-232C/V.24 portion of the pod). The HP 4951C is shown connected to the RS-449 portion of the pod in Figure E-2. Tighten the connector screws to ensure that the cable will not pull off during operation.

E-3. OPERATION

Once the Interface Pod is connected to the HP 4951C, it effectively becomes a part of the HP 4951C. Refer to the HP 4951C Operating Manual for specific operating instructions.

The Performance Verification test in paragraph E-4 can be used to check the Interface Pod functionally before it is used.

RS-232C Portion

Connectors

The top left connector, labeled PROTOCOL ANALYZER, connects the Interface Pod to the HP 4951C via the Interface Pod cable supplied with the HP 4951C. The bottom left connector, labeled RS-232C/V.24 connects the pod to the line for monitoring or simulation.

Jumper Pins

All 25 pins of the bottom left connector are brought out for jumpering. If your network cable has different pin assignments from the interface standard, you can use the supplied jumper wires to connect the interface lines to the desired pin on your cable. Pins 2, 3, 4, 5, 6, 8, 15, 17, 20, and 24 are also brought out on the other side of the breakout switches for jumpering.

Source Pins

The six Source Pins supply +12 volts and -12 volts. You may set any signal line on or off by jumpering that line to the Source Pins.

Disconnect (breakout) Switches

Pins 2, 3, 4, 5, 6, 8, 15, 17, 20, and 24 may be individually disconnected from the data link by means of switches. This lets you isolate non-driven interface lines from the HP 4951C.

LCD Indicators

The LCD indicator for a signal line is dark when that line is On or Spacing. The LCD indicator is blank when a line is Off, Marking, or in tri-state. For the indicator to be dark the voltage on that line must be greater than +2.75 volts. Once the indicator is dark, it will not go blank until the voltage becomes less than +0.25 volts. Therefore, the LCD for individual lines do not distinguish Marking and tri-state. Use the Mark/Space Monitor to do this.

LCD Indicator	Interface Line
Dark	Logical "0" (Space, On, positive voltage)
Blank	Logical "1" (Mark, Off, negative voltage, tri-state)

Mark/Space Monitor

Use the Mark/Space Monitor Pin to check the level of any signal line. Jumper this pin to any signal pin and observe the ON/OFF LCD indicators. The On indicator is darkened for levels greater than +3 volts; the Off indicator is darkened for levels less than -3 volts. The other LCD indicators do not distinguish between Marking and tri-state conditions (they are blank below +0.25 volts). The Mark/Space Monitor lets you check these lines, or any other signal lines for mark/space levels.

E-4. PERFORMANCE VERIFICATION

This Performance Verification (PV) test is part of the HP 4951C Loop PV and can be used to check that the pod is functional once it is connected to the HP 4952A. This test should be performed twice; once with the HP 4951C connected to the RS-449 portion of the pod, and once with the HP 4951C connected to the RS-232C portion of the pod. (See paragraph E-2 for connecting the pod to the HP 4951C).

WARNING

Do not perform the pod performance verification test while the pod is connected to a network device. To do so may cause damage to the network device or the pod.

Description

This test checks if there is an Interface Pod connected to the HP 4951C, and verifies the DTE and DCE lines.

Setup

1. Turn on the HP 4951C.
2. Press MORE.
3. Select <Self Test>.
4. Select <EXT DLC>.

Procedure

1. When the <EXT DLC> softkey is pressed, the Interface Pod test is performed.

2. If there are no failures, DLC TEST PASSED is displayed.

E-5. ADJUSTMENTS

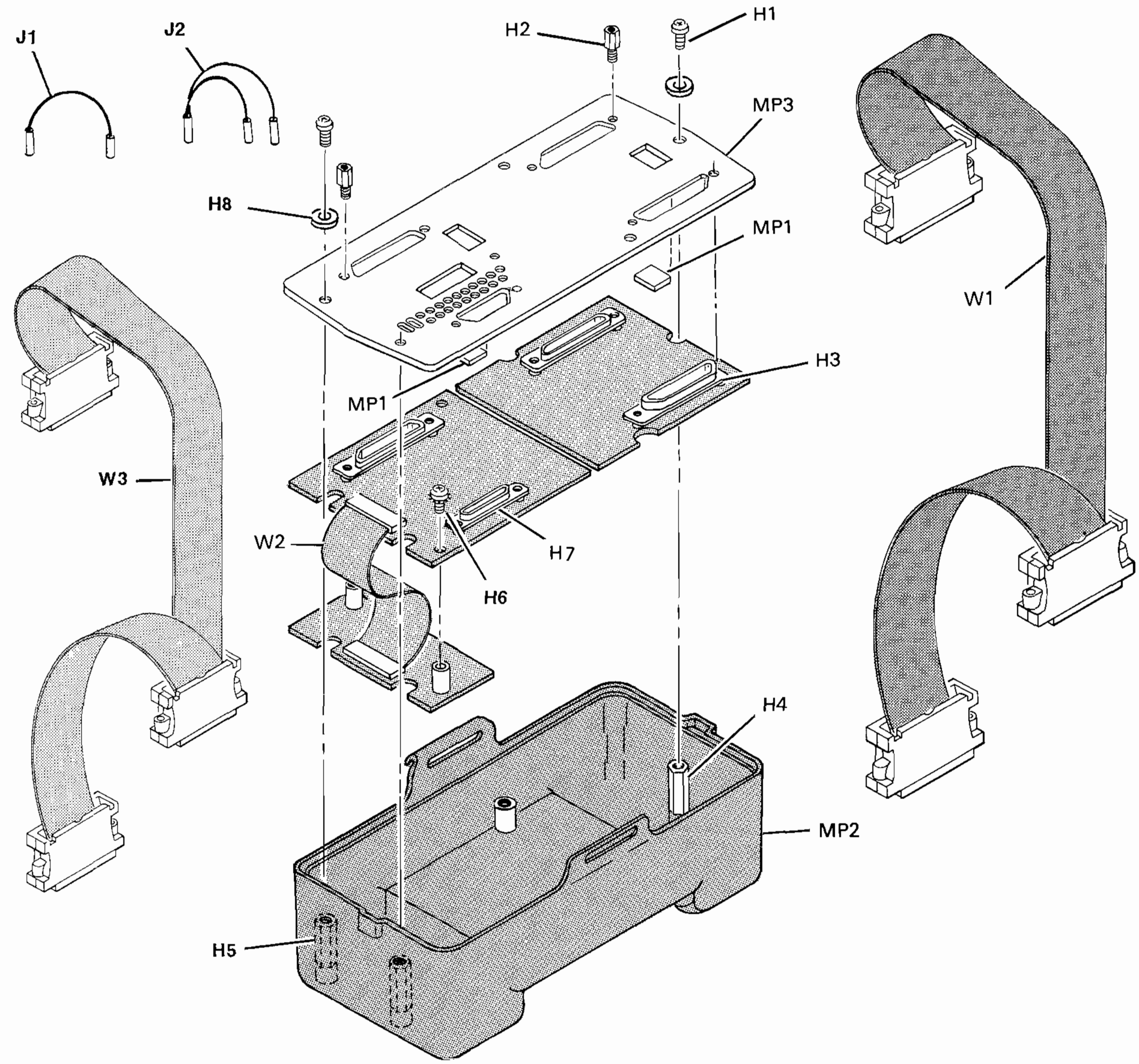
There are no adjustments for the HP 18180A.

E-6. REPLACEABLE PARTS

This section contains information for ordering parts for the HP 18180A Interface Pod. Table E-1 is a Manufacturer's Code List and Table E-2 is a list of the HP 18180A Replaceable Parts. Figure E-3 is an exploded view of the Interface Pod along with a list of the chassis and mechanical parts.

Table E-1. HP 18180A Manufacturers Code List

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
11236	CTS OF BERNE INC	BERNE	IN	46711
13606	SPRAGUE ELECT CO SEMICONDUCTOR DIV	CONCORD	NH	03301
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247



Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
H1	2360-0195	3	3	SCR, MCH, 6-32-312	04771	ORDER BY DESCRIPTION
H2	1251-2942	4	8	SCR POST LOCK	01380	206509-1
H3	1251-6074	4	2	CONNECTOR-37 PIN	04486	DC375V
H4	0380-1719	6	1	STANDOFF	28480	0380-1719
H5	0380-1720	9	2	STANDOFFS	28480	0380-1720
H6	2360-0115	8	2	SCR MCH 6-32-312	00000	ORDER BY DESCRIPTION
H7	1251-4946	5	1	CONNECTOR-25 PIN	04486	DB-255V
H8	2190-0876	3	5	WASHER, FLAT, #6	00000	ORDER BY DESCRIPTION
MP1	5040-4478	5	1	LENS	28480	5040-4478
MP2	5041-6749	4	1	HOUSING, COATED	28480	5041-6749
MP3	18180-00001	5	1	RS-232C/RS-449 PANL	28480	18180-00001
W1	18174-61601	8	1	CABLE, RS-449	28480	18174-61601
W2	18173-61601	3	1	CABLE INTERCONNECT	28480	18173-61601
W3	18173-61602	5	1	CABLE, RS-232C	28480	18173-61602
J1	8120-4218	4	4	CABLE JUMPER	28480	8120-4218
J2	8120-4219	5	2	CABLE JUMPER	28480	8120-4219

Figure E-3. HP 18180A Exploded View

Table E-2. HP 18180A Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	18173-60001	8	1	RS-232C INTERFACE POD	28480	18173-60001
A1C1	0180-1746	5	3	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C2	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C3	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A1C4	0160-5299	9		CAPACITOR-FXD .022UF+-20% 50VDC	02010	MD011C223MAA
A1C5	0160-5299	9		CAPACITOR-FXD .022UF+-20% 50VDC	02010	MD011C223MAA
A1C6	0160-5299	9		CAPACITOR-FXD .022UF+-20% 50VDC	02010	MD011C223MAA
A1C7	0160-5299	9		CAPACITOR-FXD .022UF+-20% 50VDC	02010	MD011C223MAA
A1C8	0160-5299	9		CAPACITOR-FXD .022UF+-20% 50VDC	02010	MD011C223MAA
A1C9	0180-1846	6	2	CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A1C10	0180-1846	6		CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A1C11	0160-0576	5	9	CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C12	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C13	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C14	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C15	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C16	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C17	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C18	0180-3050	8	1	CAPACITOR-FXD 330UF+50-10% 16VDC AL	28480	0180-3050
A1C19	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1C20	0160-0576	5		CAPACITOR-FXD .1UF +-20% 50VDC CER	28480	0160-0576
A1E105	1251-8360	5	2	CONNECTOR-SGL PIN	28480	1251-8360
A1E208	1251-8360	5		CONNECTOR-SGL PIN	28480	1251-8360
A1J1	1251-6074	4	1	CONNECTOR 37-PIN F D SUBMINIATURE	28480	1251-6074
A1J2	1251-4946	5	1	CONNECTOR 25-PIN F D SUBMIN	28480	1251-4946
A1K1	0490-1354	8	1	RELAY 2C 5VDC-COIL 2A 250VAC	28480	0490-1354
A1K2	0490-1383	3	2	RELAY 4C 5VDC-COIL 2A 250VAC	28480	0490-1383
A1K3	0490-1383	3		RELAY 4C 5VDC-COIL 2A 250VAC	28480	0490-1383
A1R1	0699-0556	2	3	RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A1R2	0699-0556	2		RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A1R3	0699-0556	2		RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A1R4	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A1R5	0757-0289	2	1	RESISTOR 13.3K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-1332-F
A1R6	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1R7	0698-3453	2	1	RESISTOR 196K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1963-F
A1R8	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A1R9	0698-3266	5	2	RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A1R10	0698-3266	5		RESISTOR 237K 1% .125W F TC=0+-100	24546	C4 1/8-T0-2373-F
A1R11	0757-0460	1	1	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A1R12	0757-0461	2	1	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6812-F
A1R13	0683-1025	9	2	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R14	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A1R15	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A1R16	0698-8820	7	1	RESISTOR 4.64 1% .125W F TC=0+-100	28480	0698-8820
A1R100	1810-0292	2	1	NETWORK-RES 14-DIP220.0 OHM X 7	01121	314B221
A1R200	1810-0679	9	10	RES NETWK SIP 4	28480	1810-0679
A1R201	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R202	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R300	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R301	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R302	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R400	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R401	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R402	1810-0731	9	1	NETWORK-RES SIP 10.0K OHM × 7	28480	1810-0731
A1R500	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R501	1810-0679	9		RES NETWK SIP 4	28480	1810-0679
A1R601	1810-0368	3	1	NETWORK-RES 6-SIP10.0K OHM X 5	01121	206A103
A1R602	1810-0206	8		NETWORK-RES 8-SIP10.0K OHM X 7	01121	208A103
A1U103	1820-3007	4	3	IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A1U201	1826-0759	9	3	IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U301	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U302	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A1U303	1990-0883	7	1	DISPLAY-LIQ-XTAL	28480	1990-0883
A1U400	1858-0047	5	1	TRANSISTOR ARRAY 16-PIN PLSTC DIP	13606	ULN-2003A
A1U401	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A1U402	1820-3081	4	1	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	28480	1820-3081
A1U503	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A1U600	1826-0753	3	2	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A1U603	1820-3373	7	1	IC MV CMOS/74HC MONOSTBL CLEAR DUAL	28480	1820-3373
A1U700	1826-0753	3		IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A1U703	1820-3396	4	1	IC GATE CMOS/74HC AND-OR-INV DUAL 2-INP	28480	1820-3396
	0380-0162	1	2	STANDOFF-RVT-ON .75-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
	0380-0332	7	4	STANDOFF-RVT-ON .187-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
A1XJ400	1251-8360	5	36	CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1XJ503	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1XJ504	1251-8360	5		CONNECTOR-SGL CONT PIN .025-IN-BSC-SZ SQ	28480	1251-8360
A1S501	3101-2732	8	1	DIP SWITCH	28480	3101-2732
	18173-61601	6	1	BD INTERCONN CBL	28480	18173-61601
	1251-7642	4	1	KEYING PLUG	01380	206509-1
	1260-0445	0	2	SQUARE PINS, .425 IN LONG	03206	65500-109
	1251-2942	7		SCREW LOCK POST	04507	318-15-99-011

Table E-2. HP 18180A Replaceable Parts List (cont)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	18174-60003	1	1	RS-449 POD	28480	18174-60003
A2C1	0180-1846	6	2	CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A2C2	0180-1846	6		CAPACITOR-FXD 2.2UF+-10% 35VDC TA	56289	150D225X9035B2
A2C3	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A2C4	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A2C5	0160-0576	5	3	CAPACITOR-FXD .1UF+-20% 50VDC CER	28480	0160-0576
A2C6	0160-0576	5		CAPACITOR-FXD .1UF+-20% 50VDC CER	28480	0160-0576
A2C7	0160-0576	5		CAPACITOR-FXD .1UF+-20% 50VDC CER	28480	0160-0576
A2DS1	1990-0883	7	1	DISPLAY-LQD-XTAL	28480	1990-0883
A2J1	1251-6074	4	2	CONNECTOR 37-PIN F D SUBMINIATURE	28480	1251-6074
A2J2	1251-6074	4		CONNECTOR 37-PIN F D SUBMINIATURE	28480	1251-6074
A2R1	0698-3266	5	2	RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A2R2	0698-3266	5		RESISTOR 237K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2373-F
A2R3	0699-0556	2	2	RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A2R4	0699-0556	2		RESISTOR 5.11 1% .125W F TC=0+-100	28480	0699-0556
A2R5	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R6	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A2R201	1810-0680	2	10	RESISTOR NETWK SIP 2	28480	1810-0680
A2R202	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R203	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R204	1810-0732	5	1	NETWORK-RES 10.0K OHM X 5	28480	1810-0732
A2R301	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R302	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R303	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R304	1810-0369	4	1	NETWORK-RES 6 SIP 100.0K OHM X 5	11236	750-61-R100K
A2R401	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R402	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R403	1810-0780	3	2	RESISTOR NETWK SIP 2	28480	1810-0780
A2R404	1810-0680	2		RESISTOR NETWK SIP 2	28480	1810-0680
A2R405	1810-0780	3		RESISTOR NETWK SIP 2	28480	1810-0780
A2U100	1820-3373	7	1	IC MV CMOS/74HC MONOSTBL CLEAR DUAL	28480	1820-3373
A2U101	1820-3396	4	1	IC GATE CMOS/74HC AND-OR-IN DUAL 2-INP	28480	1820-3396
A2U103	1820-3081	4	1	IC FF CMOS/74HC D-TYPE POS-EDGE-TRIG	28480	1820-3081
A2U104	1820-3007	4	3	IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A2U200	1826-0759	9	3	IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A2U202	1820-2831	0	3	ICD 75174 DRIVER	28480	1820-2831
A2U300	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A2U302	1820-2831	0		ICD 75174 DRIVER	28480	1820-2831
A2U400	1826-0759	9		IC COMPARATOR GP QUAD 14-DIP-C PKG	04713	LM339J
A2U402	1820-2831	0		ICD 75174 DRIVER	28480	1820-2831
A2U403	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
A2U404	1820-3007	4		IC GATE CMOS/74HC EXCL-OR QUAD 2-INP	28480	1820-3007
	0380-0332	7	7	STANDOFF-RVT-ON .187-IN-LG 4-40THD	00000	ORDER BY DESCRIPTION
	1251-7642	4	1	KEYING PLUG	28480	1251-7642

E-7. RS-232C/V.24 SERVICE

The HP 18180A is a combination pod containing the RS-449 and RS-232C/V.24 physical interfaces for the HP 4951C. The following information is for the RS-232 part (18173-60001 A1 board). It contains circuit theory, troubleshooting procedures, an RS-232C/V.24 mnemonic table, a component locator, and a schematic.

RS-232C/V.24 Troubleshooting

The following troubleshooting procedure contains DCE and DTE test programs to exercise the RS-232C/V.24 portion of the pod. The RS-232C/V.24 part of the pod should be connected to the HP 4951C for these tests (see paragraph E-2 for connecting the pod to the HP 4951C). When entering the test programs below, "Press" indicates a hardkey and "Select" indicates a softkey.

DCE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod or jumpers.

1. Connect jumpers between the following pins:

RD	and	TD		
DSR	and	DTR	and	CD
CTS	and	RTS		

2. Enter the following DCE test program.

Table E-3. RS-232C/V.24 DCE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DCE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed		
Select	Simulate	
	DCE	
Press	MORE	
Select	Set Lead	
	CTS	
	Off	
	and then	

Table E-3. RS-232c/V.24 DCE Test Program (cont)

Press	MORE
Select	Set Lead
	DSR
	Off
	and then
Press	MORE
Select	Set Lead
	CD
	Off
	and then
	Send
Type in	CTS OFF
Press	RTN (return)
Select	Next Block
Press	MORE
Select	Set Lead
	CTS
	On
	and then
Press	MORE
Select	Set Lead
	DSR
	On
	and then
Press	MORE
	Set Lead
	CD
	On
	and then
	Send
Type in	CTS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	CTS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

3. Run the program entered in Table E-3.

Select	Run Menu Simulate

a. All lines on the HP 4951C display should be active.

b. Check the RS-232C LCD display on the pod front panel. TD, RD, TC, and RC should be blinking. DTR, DSR, RTS, CTS, and CD should be on, and ON and OFF should be off (-- is never active).

c. If there are any segments on the LCD display that are not correct, troubleshoot that part of the RS-232C circuitry.

DTE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod or jumpers.

1. Connect jumpers between the following pins:

   RD and TD
   RTS and CTS
   DTR and DSR and CD

2. Enter the following DTE test program.

Table E-4. RS-232C/V.24 DTE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DTE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed		
Select	Simulate DTE	
Press	MORE	
Select	Set Lead	

Table E-4. RS-232C/V.24 DTE Test Program (cont)

	RTS
	Off
	and then
Press	MORE
Select	Set Lead
	DTR
	Off
	and then
	Send
Type in	RTS OFF
Press	RTN (return)
Select	Next Block
Press	MORE
Select	Set Lead
	RTS
	On
	and then
Press	MORE
Select	Set Lead
	DTR
	On
	and then
	Send
Type in	RTS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	RTS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

3. Run the program entered in Table E-4.

Select	Run Menu
	Simulate

a. All of the lines on the HP 4951C display should be active except DCE.

b. TD, RD, and TC should be blinking. DTR, DSR, RTS, CTS, and CD should be on, and OFF and ON should be off (-- is never on).

4. If any of the above conditions fail, check the following.

a. The inputs to A1 U600 and A1 U700 should be at TTL levels (between 0 and +5 volts).

b. The outputs from A1 U600 and A1 U700 should be RS-232C levels (+-12 V).

c. The inputs and outputs of all other circuits should be at TTL levels. Check for correct amplitudes and pulsing signals in all cases.

d. To check the OFF LCD, connect -12 VTP to the MARK/SPACE TP. The OFF LCD segment should turn on.

e. To check the ON LCD, connect pin 7 on the Breakout Box to pin 11, A1 U401. The ON LCD segment should turn on.

f. A1 U400 is pulsed only once to latch in the correct relay.

RS-232C/V.24 Circuit Theory

The RS-232C/V.24 part of the HP 18180A Interface Pod has the following features and capabilities:

1. It translates voltages to and from RS-232C and HP 4951C logic levels.
2. It displays EIA line signal status (of selected lines only).
3. The HP 4951C can program this part of the pod to monitor the RS-232S/V.24 interface.
4. The HP 4951C can simulate a DTE or DCE device on the RS-232C/V.24 interface by driving the appropriate lines through the pod.
5. It contains a breakout box.

The MONITOR, DTESIM and DCESIM output signals from the HP 4951C configure the Interface Pod for the correct mode of operation.

Receivers

Receivers A1 U201, A1 U301, and A1 U401 translate RS-232C voltage levels to logic levels for the HP 4951C. The mark and space thresholds are +0.25 and +2.75 volts respectively. These thresholds also provide 2.5 volts of hysteresis at the physical interface lines. The receivers operate correctly over an input voltage range of -15 volts to +25 volts and are protected against voltages between -60 and +90 volts by an input voltage divider network.

Drivers

RS-232C drivers A1 U600 and A1 U700 translate the logic voltage levels from the HP 4951C to RS-232C levels. The outputs are current limited with a series resistor to protect against driver contentions or unintentional shorts to ground in the power supply. The drivers are connected to the RS-232C interface via latching relays A1 K1, A1 K2, and A1 K3. The relays are controlled through A1 U400.

Status of the EIA lines is shown on an LCD display on the Interface Pod. Control Line bar indicators are turned on when the control line is ON. The transmit and receive clock and data indicators flash at a 2 Hz rate when edge transitions are detected.

Two of the LCD indicators provide valid mark and space threshold information. RS-232C mark and space thresholds are 3 and -3 volts respectively. A mark/space LCD detect can be connected to any incoming EIA line. When the voltage applied to this input is a valid mark or space, the appropriate indicator turns on. If the voltage is between the two thresholds, neither indicator turns on.

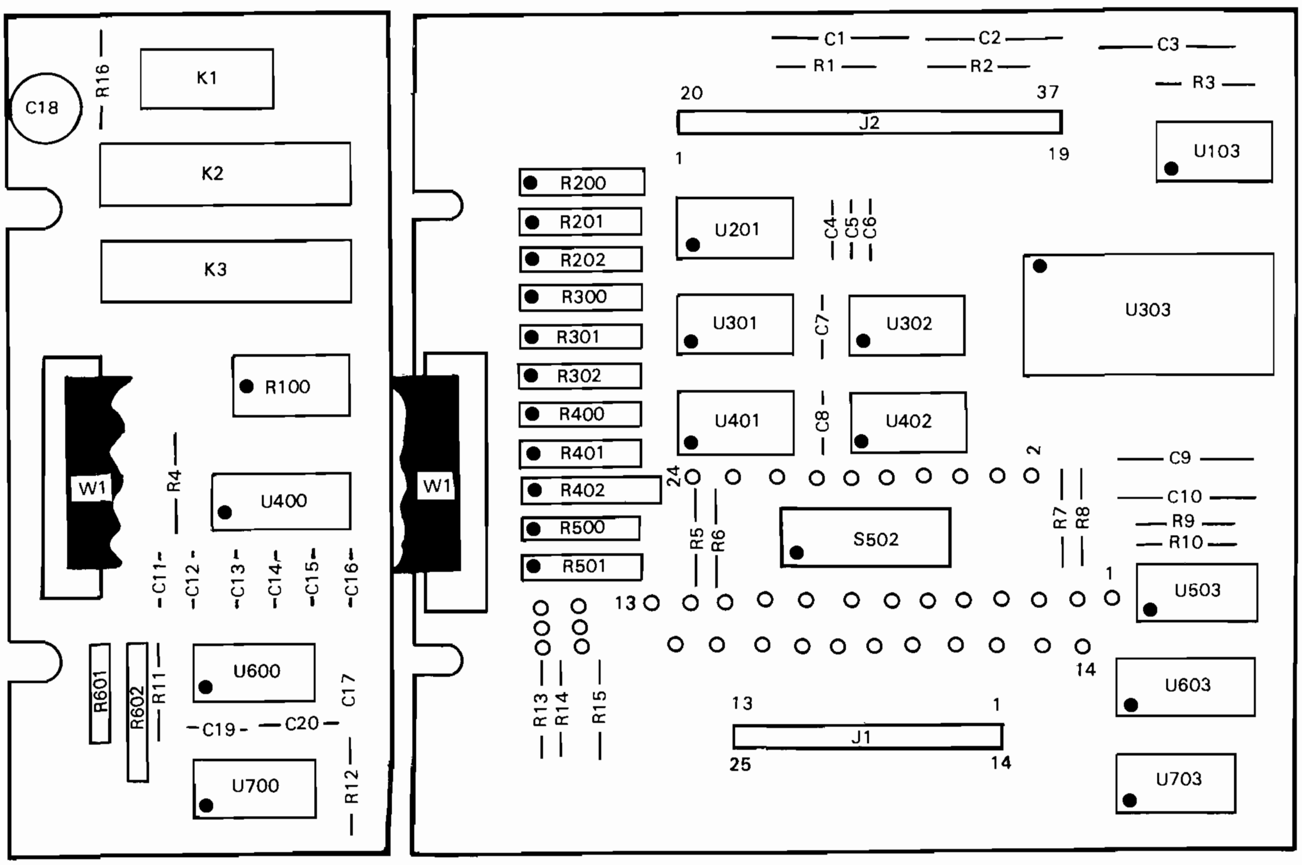
RS-232C/V.24 SIGNAL MNEMONICS

Table E-5 describes RS-232C/V.24 signal mnemonics.

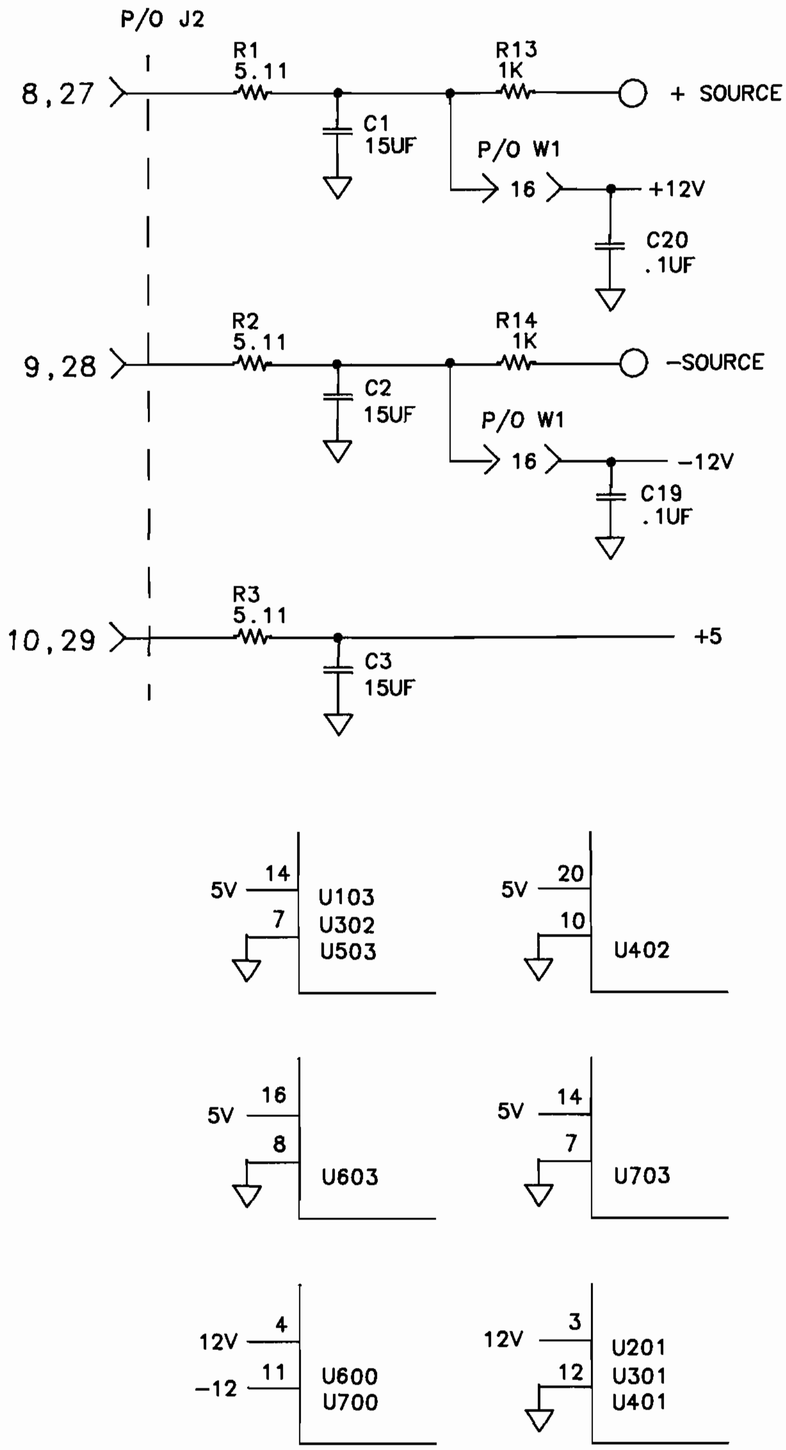
Table E-5. RS-232C/V.24 Signal Mnemonics

RS-232C PIN #	EIA	CCITT	CIRCUIT	DESCRIPTION
1	AA	101		Protective Ground
2	BA	103	TD	Transmitted Data
3	BB	104	RD	Received Data
4	CA	105	RTS	Request To Send
5	CB	106	CTS	Clear To Send
6	CC	107	DSR	Data Set Ready
7	AB	102	GND	Signal Ground
8	CF	109	CD	Carrier Detect (Received Line Signal Detector
9				unassigned
10				unassigned
11				unassigned
12	SCF	122	SCD	Secondary Carrier Detect
13	SCB	121	SCS	Secondary Clear to Send
14	SBA	118	STX	Secondary Transmitted Data
15	DB	114	TC	Transmit Signal Elements Timing (transmit clock)
16	SBB	119	SRX(SRD)	Secondary Received Data
17	DD	115	RC	Receiver Signal Element (Receive Clock)
18				unassigned
19	SCA	120	SRS	Secondary Request to Send
20	CD	108.2	DTR	Data Terminal Ready
21	CG	110	SQ	Signal Quality
22	CE	125	RI	Ring Indicator
23	CH/CI	111/112	DRS	CH=Data Rate Selector, DTE CI=Data Rate Selector, DCE
24	DA	113	ETC	EXT. Transmit Signal Element Timing (DTE source)
25				unassigned

Figure E-4. Component Locator for the RS-232C/V.24 18173-60003 A1 Board



18173-60001-0112-2-84



Power and Grounds

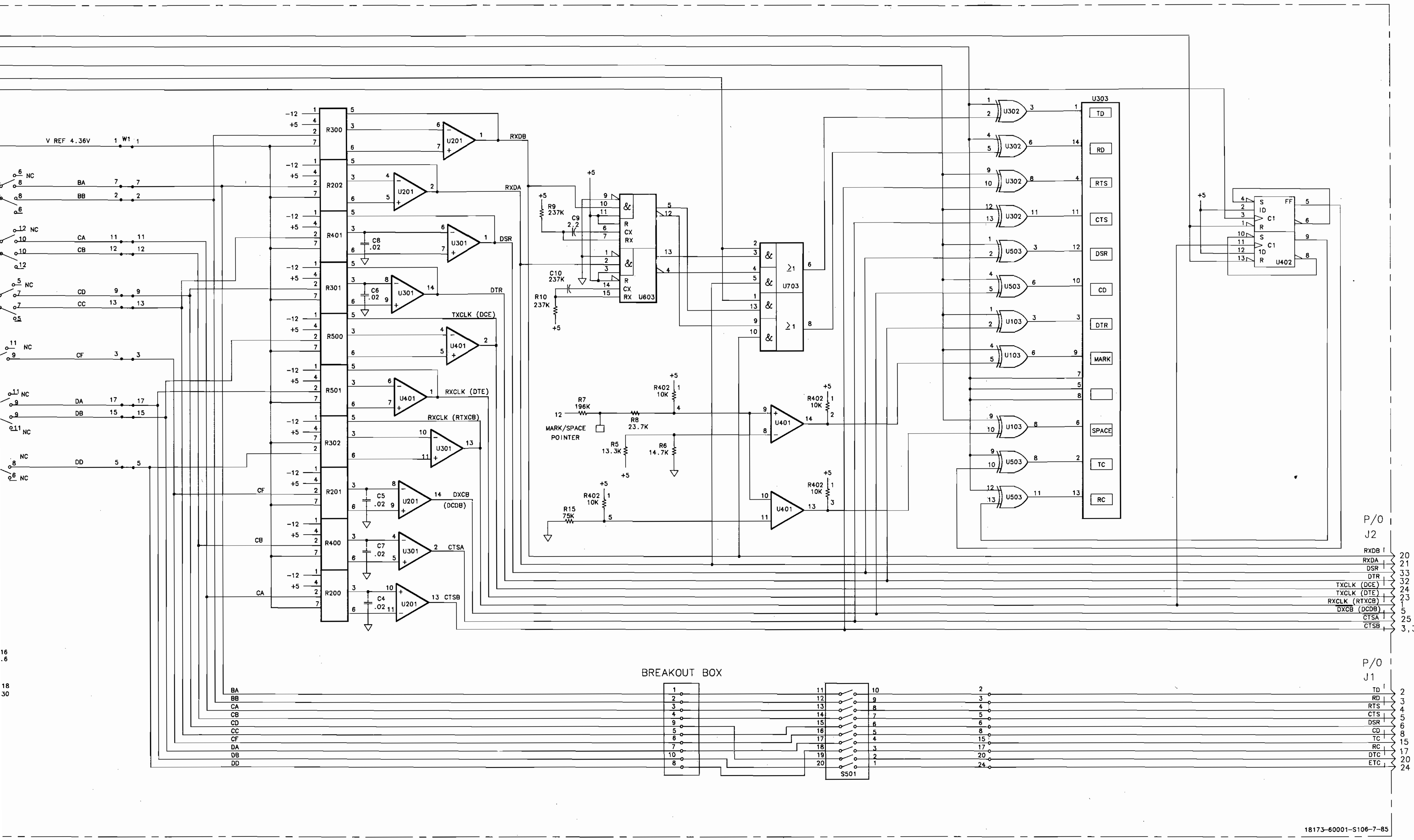
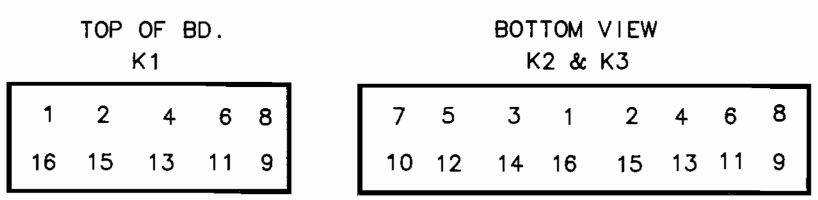
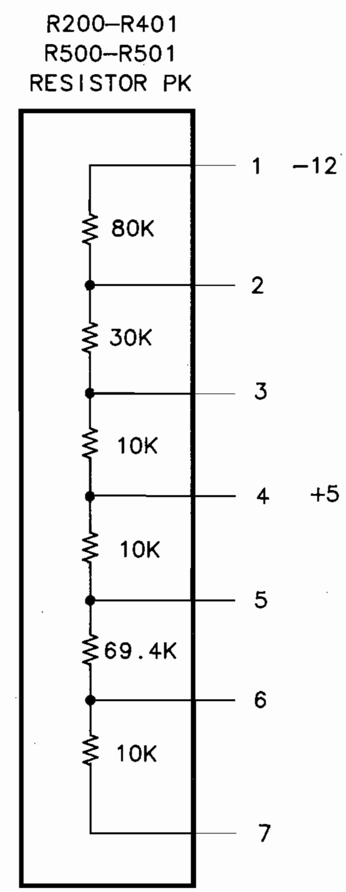
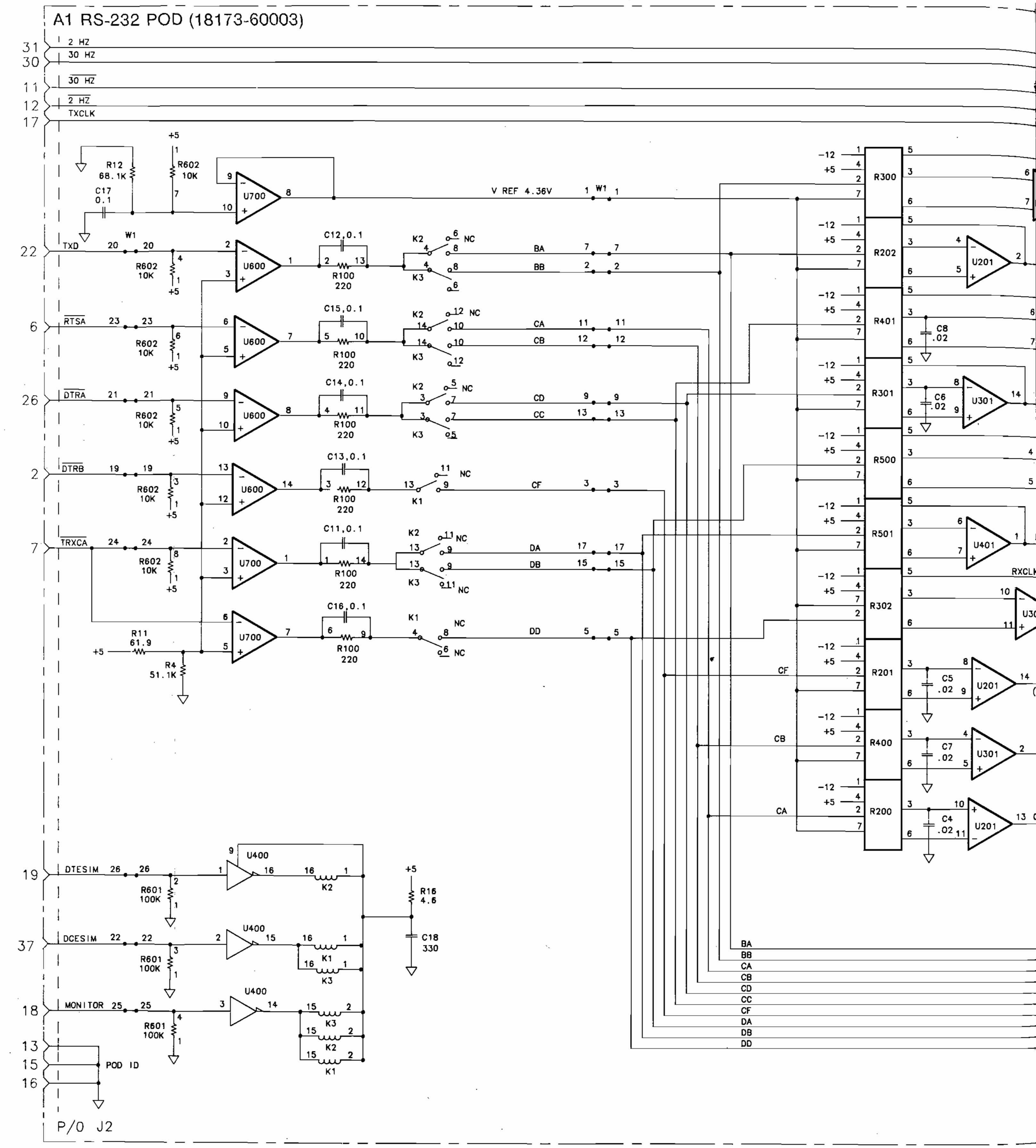


Figure E-5. Schematic for the RS-232C/V.24 18173-60003 A1 Board


TOP OF BD.
K1
1 2 4 6 8
16 15 13 11 9
BOTTOM VIEW
K2 & K3
7 5 3 1 2 4 6 8
10 12 14 16 15 13 11 9


R200–R401
R500–R501
RESISTOR PK
80K
30K
10K
10K
69.4K
10K
1 −12
2
3
4 +5
5
6
7


A1 RS-232 POD (18173-60003)
2 HZ
30 HZ
TXCLK
V REF 4.36V
TXD
RTSA
DTRA
DTRB
TRXCA
DTESIM
DCESIM
MONITOR
POD ID
P/O J2
U700
U600
U400
U201
U301
U401
R300
R202
R401
R301
R500
R501
R302
R201
R400
R200
RXCLK
BA
BB
CA
CB
CD
CC
CF
DA
DB
DD

E-8. RS-449 SERVICE

The HP 18180A is a combination pod containing the physical interfaces for either RS-232C/V.24 or RS-449 for the HP 4951C Protocol Analyzer. The following service information is for the RS-449 part (18174-60001 A2 board) of the HP 18180A pod. It contains troubleshooting procedures, circuit theory and an RS-449 mnemonic table, a component locator, and a schematic.

RS-449 Troubleshooting

The following troubleshooting procedures contain DCE and DTE test programs to exercise the RS-449 portion of the pod. The RS-449 part of the pod should be connected to the HP 4951C for these tests (see paragraph E-2 for connecting the pod to the HP 4951C). When entering the test programs below, "Press" indicates a hardkey and "Select" indicates a softkey.

DCE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod.

1. Enter the following DCE test program.

Table E-6. RS-449 DCE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DCE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed.		
Select	Simulate	
	DCE	
Press	MORE	
Select	Set Lead	
	CS	
	Off	
	and then	
Press	MORE	

Table E-6. RS-449 DCE Test Program (cont)

Select	Set Lead
	DM
	Off
	and then
Press	MORE
Select	Set Lead
	RR
	Off
	and then
	Send
Type in	CS OFF
Press	RTN (return)
Select	Next Block
Press	MORE
	Set Lead
	CS
	On
	and then
Press	MORE
Select	Set Lead
	DM
	On
	and then
Press	MORE
Select	Set Lead
	RR
	On
	and then
	Send
Type in	CS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	CS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

2. Run the program entered in Table E-6.

Select	Run Menu
	Simulate

   a. All lines on the HP 4951C display should be active except DTE and RS.

   b. Segments RD, ST, and RT should be flashing. Segments CS, DM, and RR should be on, and segments SD, RS, and TR should be off.

3. If any of the above conditions fail, troubleshoot that part of the circuit.

DTE TROUBLESHOOTING PROCEDURE

WARNING

Turn off the HP 4951C when connecting or disconnecting the Interface Pod.

1. Enter the following DTE test program.

Table E-7. RS-449 DTE Test Program

Select	Set Up	
	SDLC	(Protocol)
	ASCII 8	(Code)
	9600	(Bits/sec)
	Sync	(Mode)
	Data & State	(Display)
	DTE	(DTE clock)
Press	(HALT)EXIT	
The Top Level Menu will be displayed.		
Select	Simulate	
	DTE	
Press	MORE	
Select	Set Lead	
	RS	
	Off	
	and then	
	MORE	
	Set Lead	
	TR	
	Off	
	and then	

Table E-7. RS-449 DTE Test Program (cont)

	Send
Type in	RS OFF
Press	RTN (return)
Select	Next Block
Press	MORE
Select	Set Lead
	RS
	On
	and then
Press	MORE
Select	Set Lead
	TR
	On
	and then
	Send
Type in	RS ON
Press	RTN (return)
Select	and then
Press	MORE
Select	Wait
Type in	500
Press	RTN (return)
Select	Next Block
	When Trig
	Lead
	RS
	On
	then goto
Type in	1
Press	RTN (return)
	(HALT)EXIT

2. Run the program entered in Table E-7.

Select	Run Menu
	Simulate

3. Segments SD and ST should be flashing, RS and TR should be on, and all of the other segments should be off (-- is never active).

4. If any of the conditions in step 2 fail, check items a through c.

    a. The inputs to A2 U202, A2 U302, and A2 U402 should be at TTL levels (between 0 and 5 volts).

    b. The outputs of A2 U202, A2 U302, and A2 U402 should be RS-449 levels (+- 12V).

    c. The inputs and outputs of all other circuits should be at TTL levels. Check for correct amplitudes and pulsing signals.

RS-449 Circuit Theory

The HP 4951C operates in three modes.

1. Monitor mode: The HP 4951C monitors traffic on a communication line through the pod.
2. DTE simulate: The HP 4951C drives the DTE lines through the pod and acts as a terminal.
3. DCE simulate: The HP 4951C drives the DCE lines through the pod and acts as the digital side of a modem or another piece of Data Circuit-Terminating Equipment.

The Interface Pod is configured for the mode of operation by the DTESIM and DCESIM output signals from the Protocol Analyzer.

The RS-449 Interface Pod has the following features and capabilities.

1. Translates voltages to and from RS-449 and HP 4951C logic levels.
2. Displays EIA line signal status (of selected lines only).
3. The HP 4951C can program the pod to monitor the RS-449 interface or simulate a DTE or DCE device.
4. Supports differentially driven category I circuits.

Drivers

A2 U202, A2 U302, and A2 U402 convert the HP 4951C signals from single-ended logic levels to differential voltage waveforms. These drivers are tristate devices and are disabled when the pod is in the monitor mode to isolate them from the RS-449 interface.

Receivers

Receivers A2 U200, A2 U300, and A2 U400 operate over a common mode voltage range from -7 to +7 volts and require a minimum differential off 200 millivolts to change states. They maintain operation over a differential voltage range from 200 millivolts to 6 volts; however, the positive common mode signal voltage cannot exceed the RS-449 specification of 10 volts. The receivers are protected by divider resistors from signals up to 12 volts.

The EIA status of the selected interface lines is displayed on a bargraph LCD. Clock and data indicators are flashed at a 2Hz rate when line state transitions are detected. Table E-8 lists these RS-449 lines.

Table E-8. HP 18180A RS-449 Front Panel LCD Display

CS	Clear to Send
DM	Data Mode
RD	Receive Data
RR	Receiver Ready
RS	Request to Send
RT	Receive Timing
SD	Send Data
ST	Send Timing
TR	Terminal Ready

RS-449 SIGNAL MNEMONICS

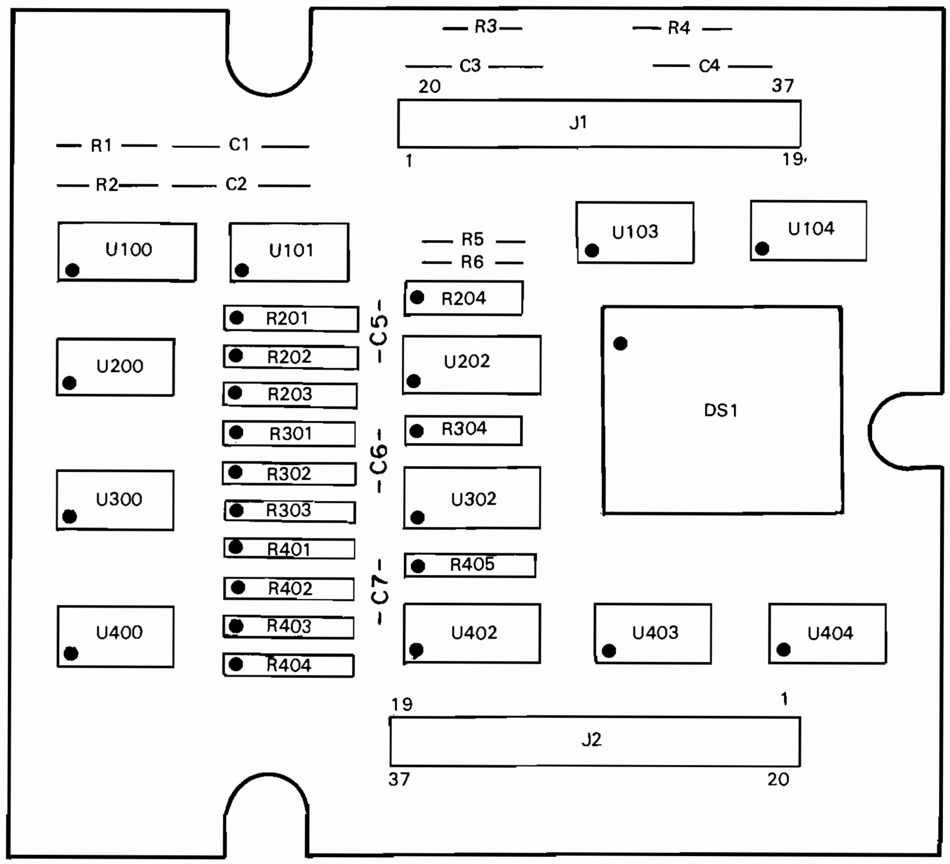
Table E-9 describes the RS-449 signal mnemonics

Table E-9. RS-449 Signal Mnemonics

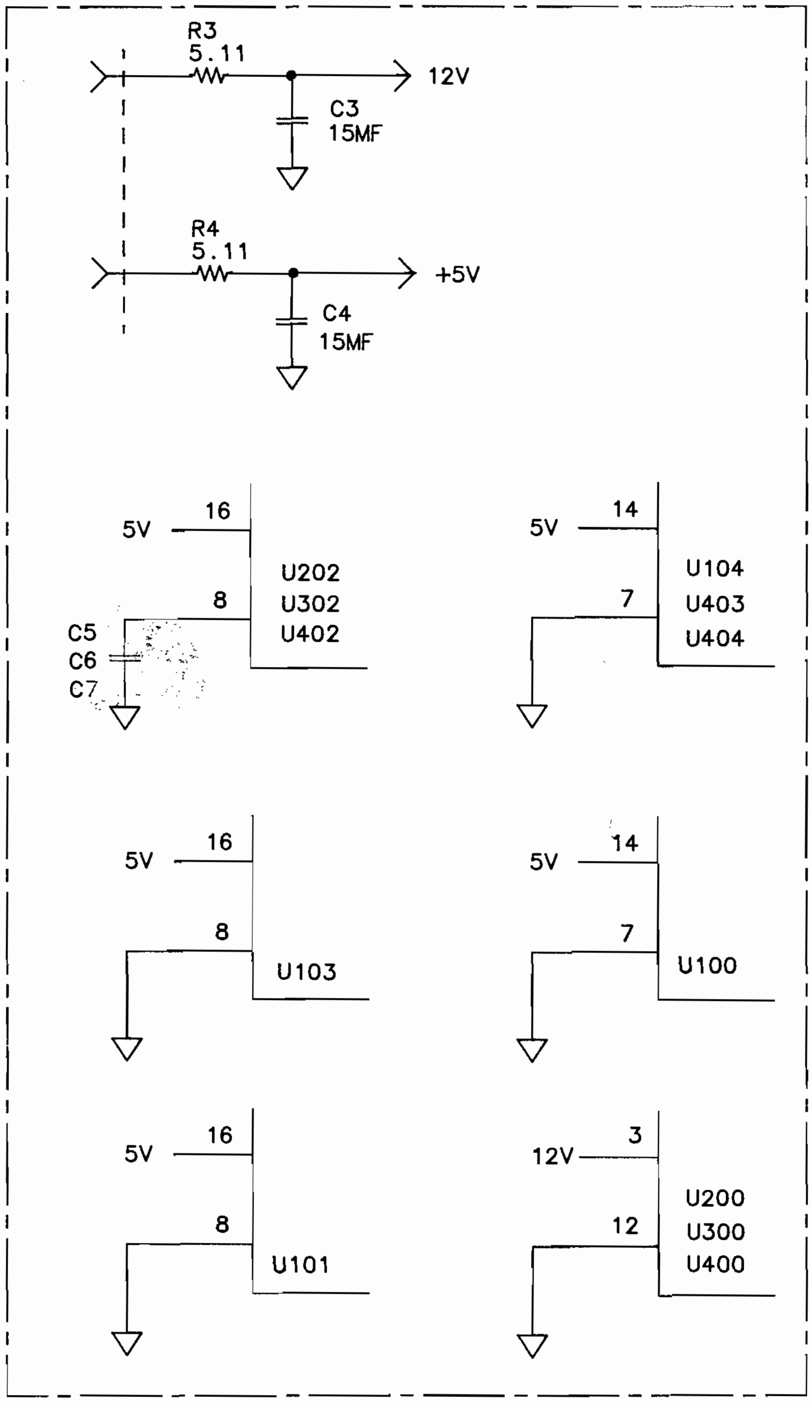
	RS449 PIN #	CIRCUIT	DESCRIPTION
	1	Shield	
	2	SI	Signaling-rate Indicator
	3	Space	
*	4	SDa	Send Data (a)
	5	STa	Send Timing (a)
*	6	RDa	Receive Data (a)
*	7	RSa	Request to Send (a)
	8	RTa	Receive Timing (a)
*	9	CSa	Clear to Send (a)
	10	LL	Local Loopback
*	11	DM	Data Mode (a)
	12	TR	Terminal Ready (a)
*	13	RR	Receiver Ready (a)
	14	RL	Remote Loopback
	15	IC	Incoming Call
	16	SF	Select Frequency/ Signaling-rate Selector
	17	TT	Terminal Timing (a)
	18	TM	Test Mode
	19		Signal Ground
	20		Receive Common
	21	Spare	
	22	DTE	Send Data (b)
	23	ST	Send Timing (b)
	24	DCE	Receive Data (b)
	25	RS	Request to Send (b)
	26	RT	Receive Timing (b)
	27	CS	Clear to Send (b)
	28	IS	Terminal in Service
	29	DM	Data Mode (b)
	30	TR	Terminal Ready (b)
	31	RR	Receiver Ready (b)
	32	SS	Select Standby
	33	SQ	Signal Quality
	34	NS	New Signal
	35	TT	Terminal Timing (b)
	36	SB	Standby Indicator
	37		Send Common

*Indicates lines for which parameters can be selected from HP 4951C display.

Figure E-6. Component Locator for the RS-449 18174-60001 A2 board



18174-60001-0113-2-84



Power and Grounds

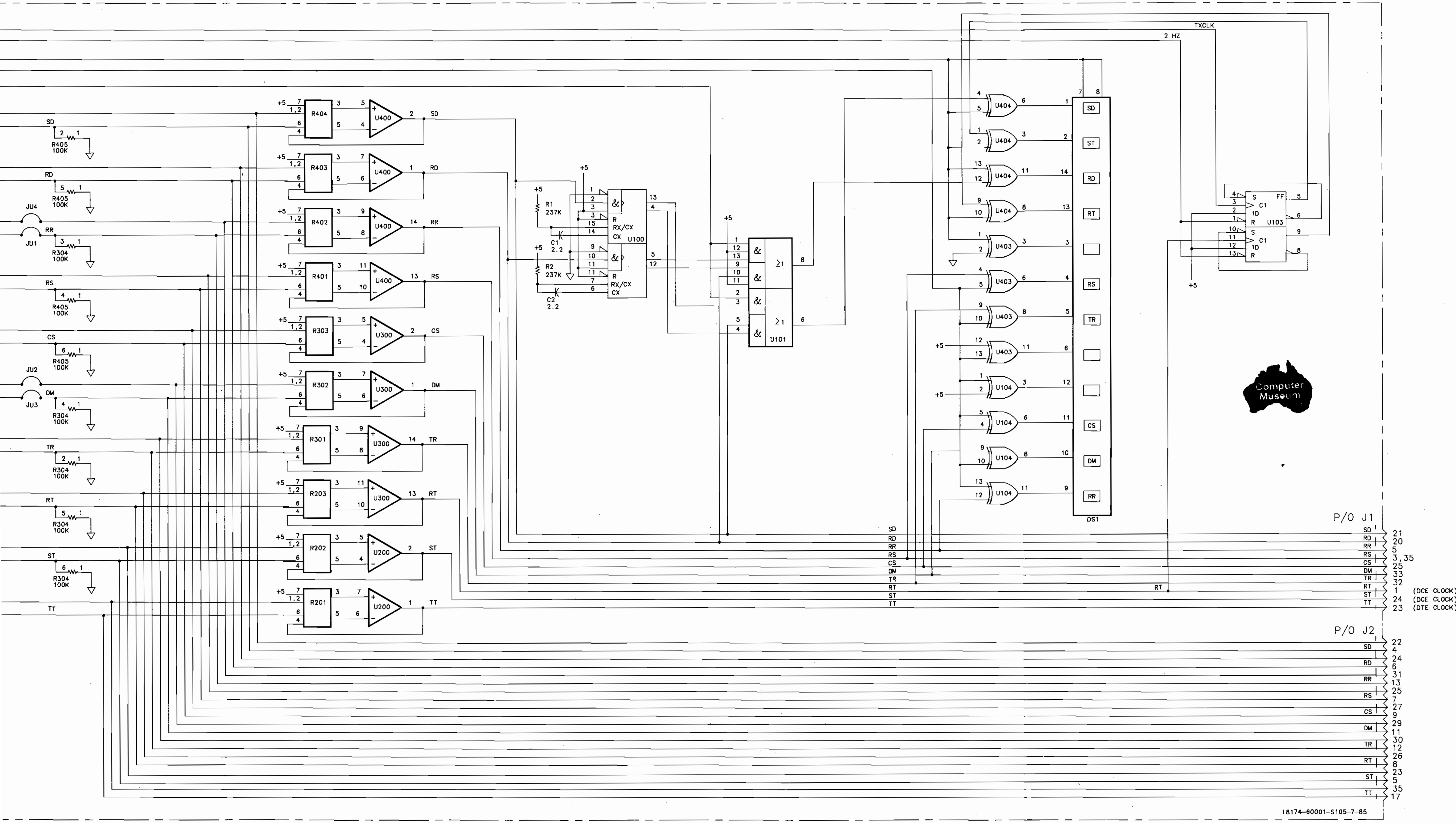
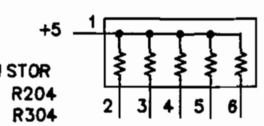
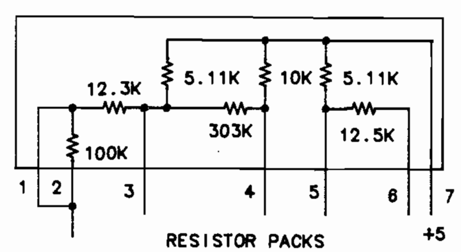


Figure E-7. Schematic for the RS-449 18174-60001 A2 board



RESISTOR PACK R204
R304
R405



RESISTOR PACKS
R201-203, R301-303, R401-404